TEXAS INSTRUMENTS

TPS28226

SLUS791A – JULY 2007 – REVISED SEPTEMBER 2015

TPS28226 High-Frequency 4-A Sink Synchronous MOSFET Drivers

1 Features

- Drives Two N-Channel MOSFETs with 14-ns Adaptive Dead Time
- Wide Gate Drive Voltage: 4.5 V Up to 8.8 V With Best Efficiency at 7 V to 8 V
- Wide Power System Train Input Voltage: 3 V Up to 27 V
- Wide Input PWM Signals: 2.0 V up to 13.2-V Amplitude
- Capable to Drive MOSFETs with ≥40-A Current per Phase
- High Frequency Operation: 14-ns Propagation Delay and 10-ns Rise/Fall Time Allow F_{SW} – 2 MHz
- Capable to Propagate <30-ns Input PWM Pulses
- Low-Side Driver Sink On-Resistance (0.4 Ω) Prevents dV/dT Related Shoot-Through Current
- 3-State PWM Input for Power Stage Shutdown
- Space Saving Enable (Input) and Power Good (Output) Signals on Same Pin
- Thermal Shutdown
- UVLO Protection
- Internal Bootstrap Diode
- Economical SOIC-8 and Thermally Enhanced 3-mm x 3-mm DFN-8 Packages
- High Performance Replacement for Popular 3-State Input Drivers

2 Applications

- Multi-Phase DC-to-DC Converters with Analog or Digital Control
- Desktop and Server VRMs and EVRDs
- Portable and Notebook Regulators
- Synchronous Rectification for Isolated Power Supplies

3 Description

The TPS28226 is a high-speed driver for N-channel complimentary driven power MOSFETs with adaptive dead-time control. This driver is optimized for use in variety of high-current one and multi-phase DC-to-DC converters. The TPS28226 is a solution that provides high efficiency, small size and low EMI emissions.

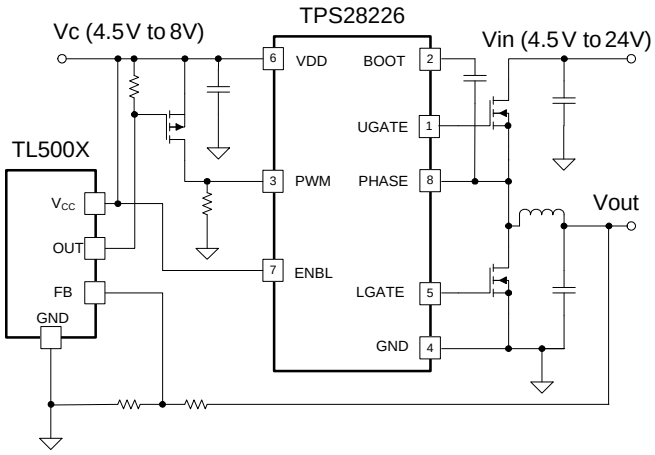
The efficiency is achieved by up to 8.8-V gate drive voltage, 14-ns adaptive dead-time control, 14-ns propagation delays and high-current 2-A source and 4-A sink drive capability. The 0.4-Ω impedance for the lower gate driver holds the gate of power MOSFET below its threshold and ensures no shoot-through current at high dV/dt phase node transitions. The bootstrap capacitor charged by an internal diode allows use of N-channel MOSFETs in a half-bridge configuration.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS28226	SOIC (8)	4.90 mm × 3.91 mm
	VSON (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

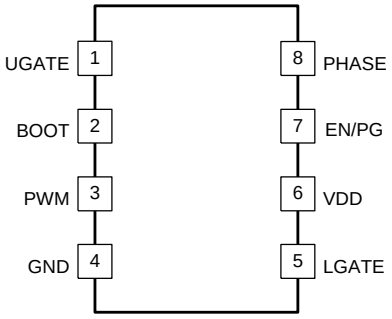
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2010) to Revision D	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

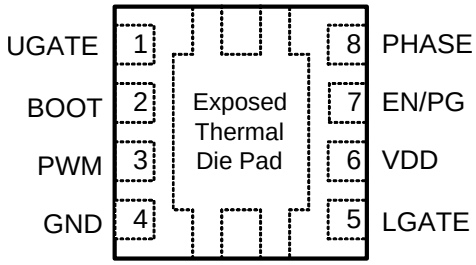
Changes from Revision B (July 2007) to Revision C	Page
• Changed FUNCTIONAL BLOCK DIAGRAM	3

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DRB Package
8-Pin VSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOIC	VSON		
BOOT	2	2	I/O	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the Phase pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
EN/PG	7	7	I/O	Enable/power good input/output pin with 1-MΩ impedance. Connect this pin to High to enable and Low to disable the device. When disabled, the device draws less than 350-µA bias current. If the V_{DD} is below UVLO threshold or over temperature shutdown occurs, this pin is internally pulled low.
GND	4	4	–	Ground pin. All signals are referenced to this node.
LGATE	5	5	O	Lower gate drive sink and source output. Connect to the gate of the low-side power N-Channel MOSFET.
PHASE	8	8	I	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.
PWM	3	3	I	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the 3-state PWM Input section under DETAILED DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
Thermal pad		Exposed die pad	–	Connect directly to the GND for better thermal performance and EMI.
UGATE	1	1	O	Upper gate drive sink/source output. Connect to gate of high-side power N-Channel MOSFET.
VDD	6	6	I	Connect this pin to a 5-V bias supply. Place a high quality bypass capacitor from this pin to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input supply voltage range, V_{DD} (3)		–0.3	8.8	V
Boot voltage, V_{BOOT}		–0.3	33	V
Phase voltage, V_{PHASE}	DC	–2	32 or V_{BOOT} + 0.3 – V_{DD} whichever is less	V
	Pulse < 400 ns, E = 20 µJ	–7	33.1 or V_{BOOT} + 0.3 – V_{DD} whichever is less	V
Input voltage range, V_{PWM}, $V_{EN/PG}$		–0.3	13.2	V
Output voltage range, V_{UGATE}		V_{PHASE} – 0.3	V_{BOOT} + 0.3, (V_{BOOT} – V_{PHASE} < 8.8)	V
	Pulse < 100 ns, E = 2 µJ	V_{PHASE} – 2	V_{BOOT} + 0.3, (V_{BOOT} – V_{PHASE} < 8.8)	V
Output voltage range, V_{LGATE}		–0.3	V_{DD} + 0.3	V
	Pulse < 100 ns, E = 2 µJ	–2	V_{DD} + 0.3	V
Continuous total power dissipation		See *Thermal Information*		
Operating virtual junction temperature range, T_J		–40	150	°C
Operating ambient temperature range, T_A		–40	125	°C
Lead temperature (soldering, 10 sec.)			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	6.8	7.2	8	V
V_{IN}	Power input voltage	3		32 V– VDD	V
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		TPS28226		UNIT
		VSON (DRB)	SOIC (D)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.2	123.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	77.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	27.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.0	63.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	N/A	°C/W

6.5 Electrical Characteristics(1)

V_{DD} = 7.2 V, EN/PG pulled up to V_{DD} by 100-kΩ resistor, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCKOUT						
	Rising threshold	V_{PWM} = 0 V		6.35	6.70	V
	Falling threshold	V_{PWM} = 0 V	4.7	5.0		V
	Hysteresis		1.00	1.35		V
BIAS CURRENTS						
$I_{DD(off)}$	Bias supply current	$V_{EN/PG}$ = low, PWM pin floating		350		µA
I_{DD}	Bias supply current	$V_{EN/PG}$ = high, PWM pin floating		500		µA
INPUT (PWM)						
I_{PWM}	Input current	V_{PWM} = 5 V		185		µA
		V_{PWM} = 0 V		–200		µA
	PWM 3-state rising threshold(2)			1.0		V
	PWM 3-state falling threshold	V_{PWM} PEAK = 5 V	3.4	3.8	4.0	V
t_{HLD_R}	3-state shutdown Hold-off time			250		ns
T_{MIN}	PWM minimum pulse to force U_{GATE} pulse	C_L = 3 nF at U_{GATE} , V_{PWM} = 5 V		30		ns
ENABLE/POWER GOOD (EN/PG)						
	Enable high rising threshold	PG FET OFF		1.7	2.1	V
	Enable low falling threshold	PG FET OFF	0.8	1.0		V
	Hysteresis		0.35	0.70		V
	Power good output	V_{DD} = 2.5 V			0.2	V
UPPER GATE DRIVER OUTPUT (UGATE)						
	Source resistance	500 mA source current		1.0	2.0	Ω
	Source current (2)	$V_{UGATE-PHASE}$ = 2.5 V		2.0		A
t_{RU}	Rise time	C_L = 3 nF		10		ns
	Sink resistance	500 mA sink current		1.0	2.0	Ω
	Sink current (2)	$V_{UGATE-PHASE}$ = 2.5 V		2.0		A
t_{FU}	Fall time	C_L = 3 nF		10		ns

(1) Typical values for T_A = 25°C
(2) Not production tested.

Electrical Characteristics(1) (continued)

V_{DD} = 7.2 V, EN/PG pulled up to V_{DD} by 100-kΩ resistor, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOWER GATE DRIVER OUTPUT (LGATE)						
	Source resistance	500 mA source current		1.0	2.0	Ω
	Source current(2)	V_{LGATE} = 2.5 V		2.0		A
t_{RL}	Rise time(2)	C_L = 3 nF		10		ns
	Sink resistance	500 mA sink current		0.4	1.0	Ω
	Sink current(2)	V_{LGATE} = 2.5 V		4.0		A
	Fall time(2)	C_L = 3 nF		5		ns
BOOTSTRAP DIODE						
V_F	Forward voltage	Forward bias current 100 mA		1.0		V
THERMAL SHUTDOWN						
	Rising threshold(2)		150	160	170	°C
	Falling threshold(2)		130	140	150	°C
	Hysteresis			20		°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIME						
t_{DLU}	UGATE turn-off propagation Delay	C_L = 3 nF		14		ns
t_{DLL}	LGATE turn-off propagation Delay	C_L = 3 nF		14		ns
t_{DTU}	Dead time LGATE turn off to UGATE turn on	C_L = 3 nF		14		ns
t_{DTL}	Dead time UGATE turn off to LGATE turn on	C_L = 3 nF		14		ns

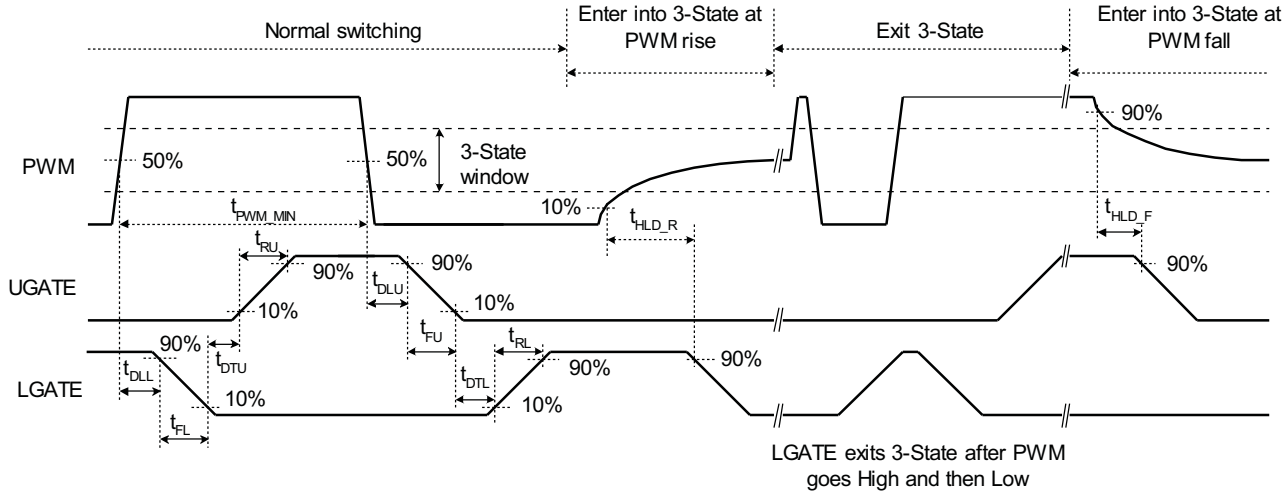
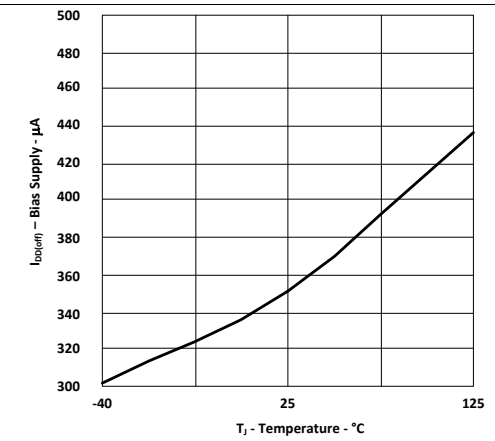


Figure 1. TPS28226 Timing Diagram

6.7 Typical Characteristics



$V_{EN/PG}$ = Low PWM Input Floating V_{DD} = 7.2 V

Figure 2. Bias Supply Current vs Temperature

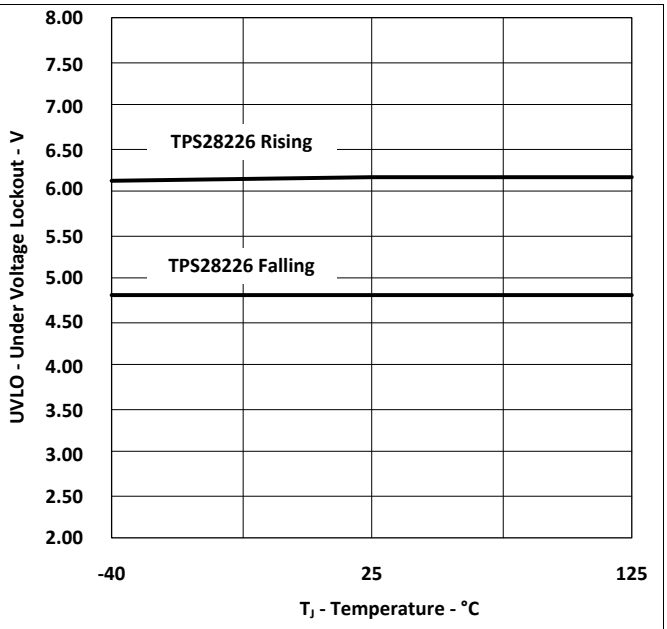
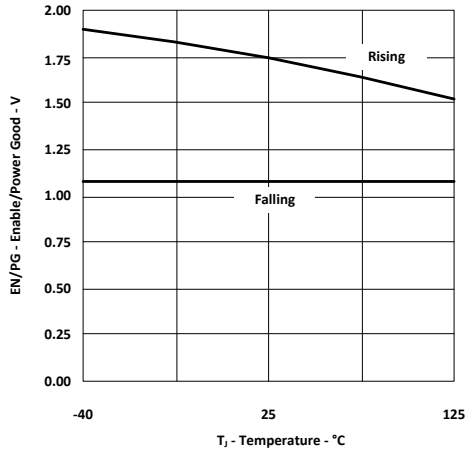
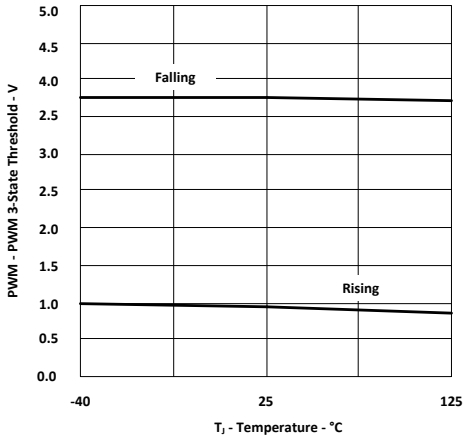


Figure 3. Undervoltage Lockout Threshold vs Temperature



V_{DD} = 7.2 V

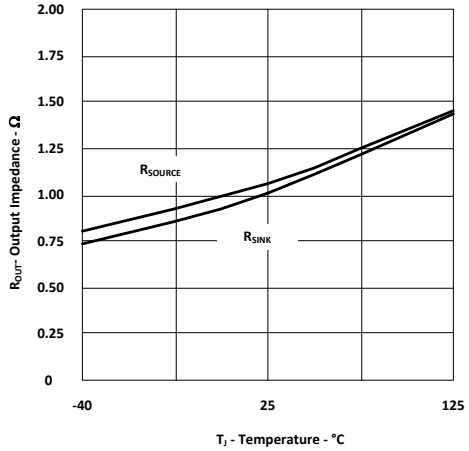
Figure 4. Enable/Power Good Threshold vs Temperature



V_{DD} = 7.2 V

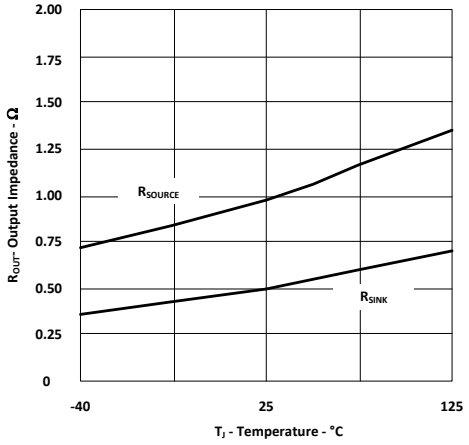
Figure 5. PWM 3-State Thresholds, (5-V Input Pulses) vs Temperature

Typical Characteristics (continued)



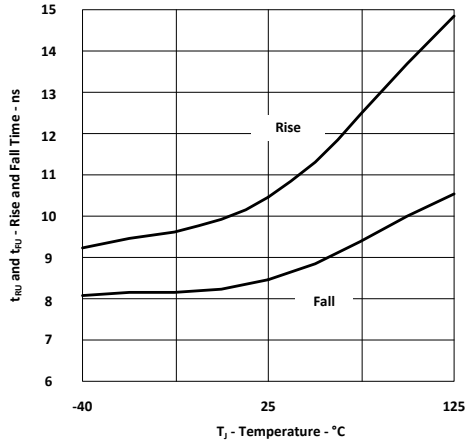
V_{DD} = 7.2 V

Figure 6. UGATE DC Output Impedance vs Temperature



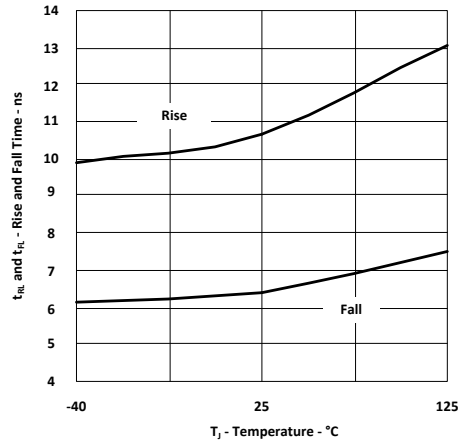
V_{DD} = 7.2 V

Figure 7. LGATE DC Output Impedance vs Temperature



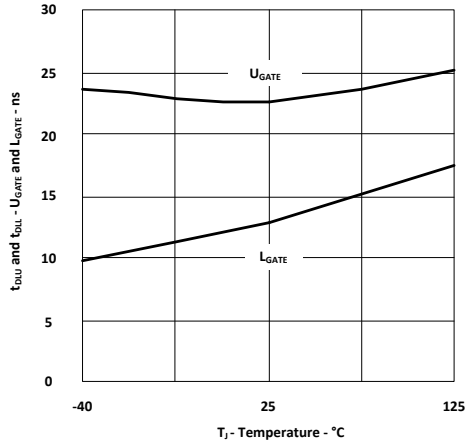
V_{DD} = 7.2 V C_{LOAD} = 3 nF

Figure 8. UGATE Rise and Fall Time vs Temperature



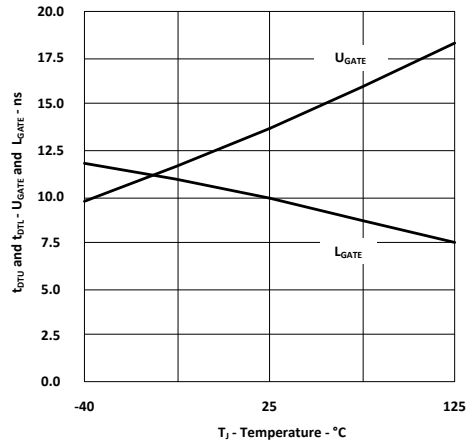
V_{DD} = 7.2 V C_{LOAD} = 3 nF

Figure 9. LGATE Rise and Fall Time vs Temperature



V_{DD} = 7.2 V C_{LOAD} = 3 nF

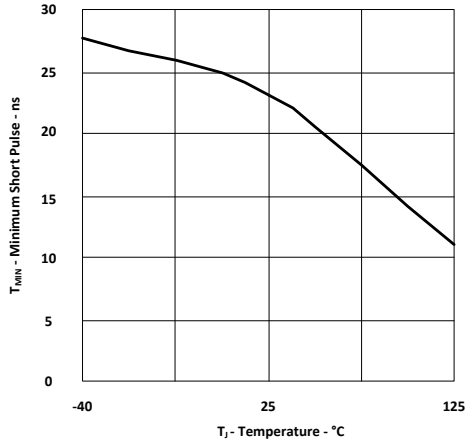
Figure 10. UGATE and LGATE (Turning OFF Propagation Delays) vs Temperture



V_{DD} = 7.2 V C_{LOAD} = 3 nF

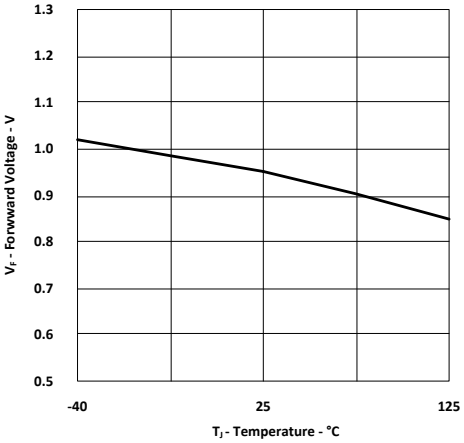
Figure 11. UGATE and LGATE (Dead Time) vs Temperture

Typical Characteristics (continued)



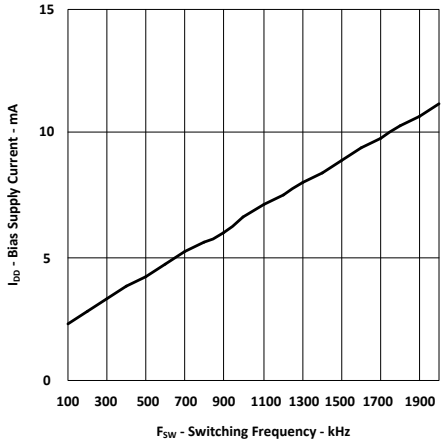
V_{DD} = 7.2 V C_{LOAD} = 3 nF

Figure 12. UGATE Minimum Short Pulse vs Temperature



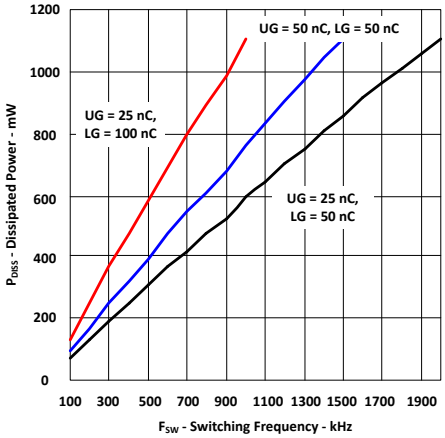
V_{DD} = 7.2 V I_F = 100 mA

Figure 13. Bootstrap Diode Forward Voltage vs Temperature



No Load V_{DD} = 7.2 V T_J = 25°C

Figure 14. Bias Supply Current vs Switching Frequency



Different Load Charge V_{DD} = 7.2 V T_J = 25°C

Figure 15. Driver Dissipated Power vs Switching Frequency

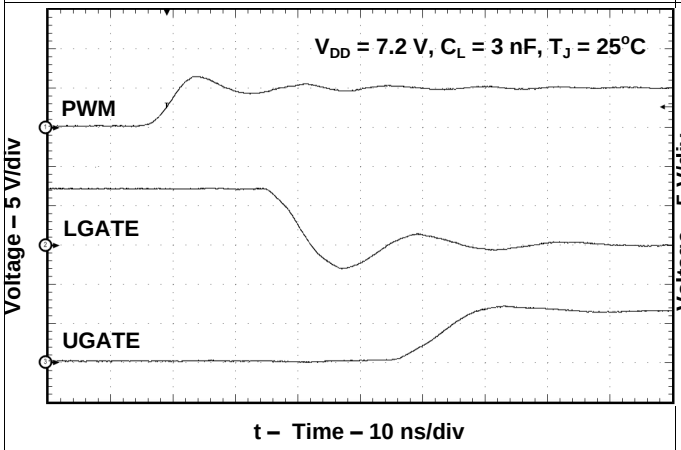


Figure 16. PWM Input Rising Switching Waveforms

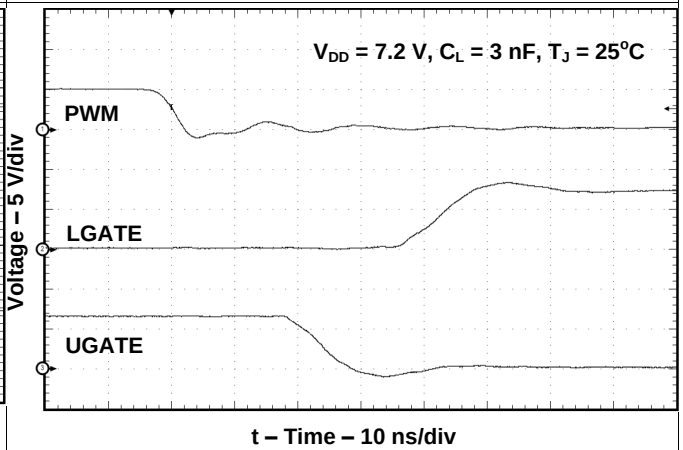


Figure 17. PWM Input Falling Switching Waveforms

Typical Characteristics (continued)

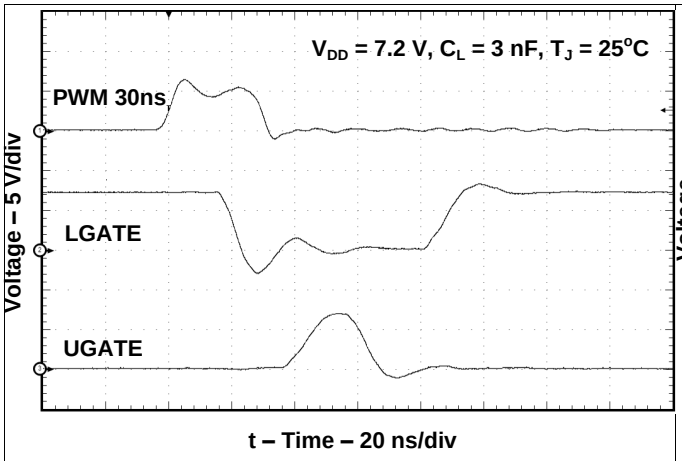


Figure 18. Minimum UGATE Pulse Switching Waveforms

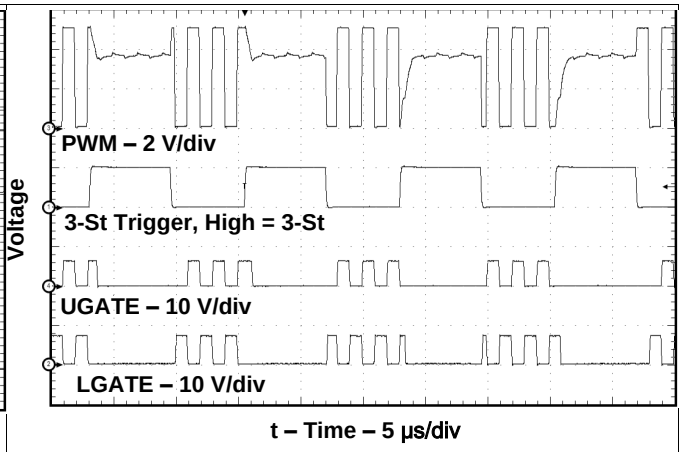


Figure 19. Normal and 3-State Operation Enter/Exit Conditions

7 Detailed Description

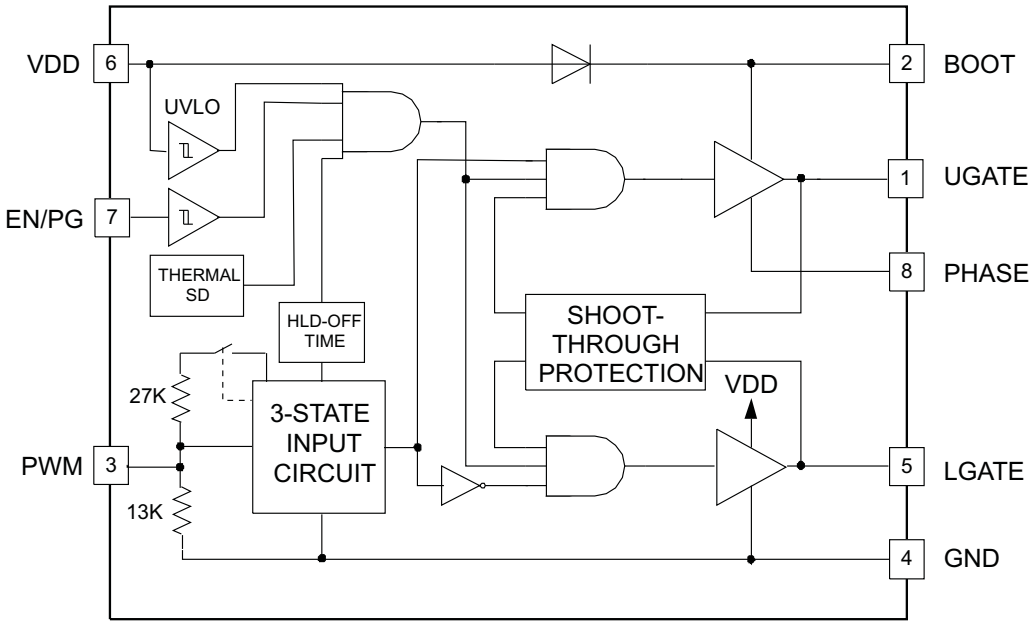
7.1 Overview

The TPS28226 features a 3-state PWM input compatible with all multi-phase controllers employing 3-state output feature. As long as the input stays within 3-state window for the 250-ns hold-off time, the driver switches both outputs low. This shutdown mode prevents a load from the reversed- output-voltage.

The other features include undervoltage lockout, thermal shutdown and two-way enable/power good signal. Systems without 3-state featured controllers can use enable/power good input/output to hold both outputs low during shutting down.

The TPS28226 is offered in an economical SOIC-8 and thermally enhanced low-size Dual Flat No-Lead (DFN-8) packages. The driver is specified in the extended temperature range of –40°C to 125°C with the absolute maximum junction temperature 150°C.

7.2 Functional Block Diagram



For the TPS28226DRB the thermal PAD on the bottom side of package must be soldered and connected to the GND pin and to the GND plane of the PCB in the shortest possible way.

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS28226 incorporates an under voltage lockout circuit that keeps the driver disabled and external power FETs in an OFF state when the input supply voltage V_{DD} is insufficient to drive external power FETs reliably. During power up, both gate drive outputs remain low until voltage V_{DD} reaches UVLO threshold, typically 6.35 V. Once the UVLO threshold is reached, the condition of the gate drive outputs is defined by the input PWM and EN/PG signals. During power down the UVLO threshold is set lower, typically 5.0 V. The 1.35 V for the TPS28226 hysteresis is selected to prevent the driver from turning ON and OFF while the input voltage crosses UVLO thresholds, especially with low slew rate. The TPS28226 has the ability to send a signal back to the system controller that the input supply voltage V_{DD} is insufficient by internally pulling down the EN/PG pin. The TPS28226 releases EN/PG pin immediately after the V_{DD} has risen above the UVLO threshold.

7.3.2 Output Active Low

The output active-low circuit effectively keeps the gate outputs low even if the driver is not powered up. This prevents open-gate conditions on the external power FETs and accidental turn on when the main power-stage supply voltage is applied before the driver is powered up. For the simplicity, the output active low circuit is shown in a block diagram as the resistor connected between LGATE and GND pins with another one connected between UGATE and PHASE pins.

Feature Description (continued)

7.3.3 Enable/Power Good

The Enable/Power Good circuit allows the TPS28226 to follow the PWM input signal when the voltage at EN/PG pin is above 2.1 V maximum. This circuit has a unique two-way communication capability. This is illustrated by Figure 20.

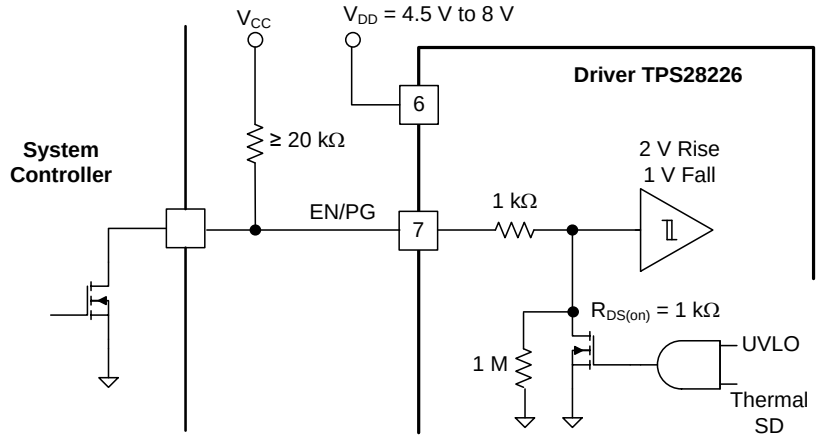


Figure 20. Enable/Power Good Circuit

The EN/PG pin has approximately 1-kΩ internal series resistor. Pulling EN/PG high by an external ≥ 20-kΩ resistor allows two-way communication between controller and driver. If the input voltage V_{DD} is below UVLO threshold or thermal shut down occurs, the internal MOSFET pulls EN/PG pin to GND through 1-kΩ resistor. The voltage across the EN/PG pin is now defined by the resistor divider comprised by the external pull up resistor, 1-kΩ internal resistor and the internal FET having 1-kΩ $R_{DS(on)}$. Even if the system controller allows the driver to start by setting its own enable output transistor OFF, the driver keeps the voltage at EN/PG low. Low EN/PG signal indicates that the driver is not ready yet because the supply voltage V_{DD} is low or that the driver is in thermal shutdown mode. The system controller can arrange the delay of PWM input signals coming to the driver until the driver releases EN/PG pin. If the input voltage V_{DD} is back to normal, or the driver is cooled down below its lower thermal shutdown threshold, then the internal MOSFET releases the EN/PG pin and normal operation resumes under the external Enable signal applied to EN/PG input. Another feature includes an internal 1-MΩ resistor that pulls EN/PG pin low and disables the driver in case the system controller accidentally loses connection with the driver. This could happen if, for example, the system controller is located on a separate PCB daughter board.

The EN/PG pin can serve as the second pulse input of the driver additionally to PWM input. The delay between EN/PG and the UGATE going high, provided that PWM input is also high, is only about 30 ns. If the PWM input pulses are synchronized with EN/PG input, then when PWM and EN/PG are high, the UGATE is high and LGATE is low. If both PWM and EN/PG are low, then UGATE and LGATE are both low as well. This means the driver allows operation of a synchronous buck regulator as a conventional buck regulator using the body diode of the low-side power MOSFET as the freewheeling diode. This feature can be useful in some specific applications to allow startup with a pre-biased output or, to improve the efficiency of buck regulator when in power saving mode with low output current.

Feature Description (continued)

7.3.4 3-State Input

As soon as the EN/PG pin is set high and input PWM pulses are initiated (see Note below). The dead-time control circuit ensures that there is no overlapping between UGATE and LGATE drive outputs to eliminate shoot through current through the external power FETs. Additionally to operate under periodical pulse sequencing, the TPS28226 has a self-adjustable PWM 3-state input circuit. The 3-state circuit sets both gate drive outputs low, and thus turns the external power FETs OFF if the input signal is in a high impedance state for at least 250 ns typical. At this condition, the PWM input voltage level is defined by the internal 27-kΩ to 13-kΩ resistor divider shown in the block diagram. This resistor divider forces the input voltage to move into the 3-state window. Initially the 3-state window is set between 1.0-V and 2.0-V thresholds. The lower threshold of the 3-state window is always fixed at about 1.0 V. The higher threshold is adjusted to about 75% of the input signal amplitude. The self-adjustable upper threshold allows shorter delay if the input signal enters the 3-state window while the input signal was high, thus keeping the high-side power FET in ON state just slightly longer than 250 ns time constant set by an internal 3-state timer. Both modes of operation, PWM input pulse sequencing and the 3-state condition, are illustrated in the timing diagrams shown in Figure 19. The self-adjustable upper threshold allows operation in wide range amplitude of input PWM pulse signals. After entering into the 3-state window and staying within the window for the hold-off time, the PWM input signal level is defined by the internal resistor divider and, depending on the input pulse amplitude, can be pulled up above the normal PWM pulse amplitude (Figure 21) or down below the normal input PWM pulse (Figure 22).

7.3.4.1 TPS28226 3-State Exit Mode

- To exit the 3-state operation mode, the PWM signal should go high and then low at least once.

This is necessary to restore the voltage across the bootstrap capacitor that could be discharged during the 3-state mode if the 3-state condition lasts long enough.

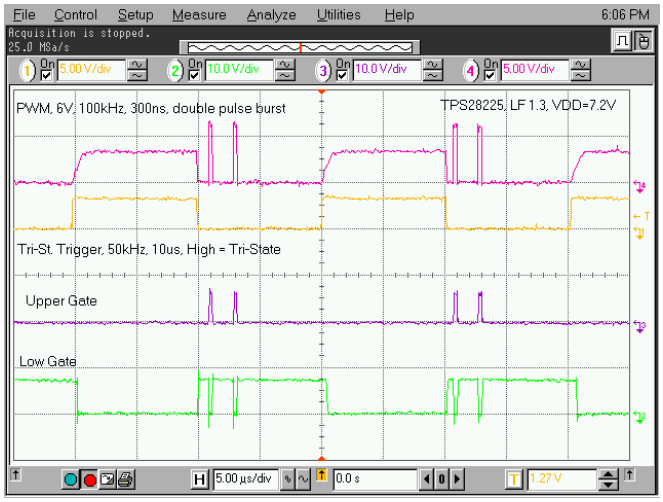


Figure 21. 6-V Amplitude PWM Pulse (TPS28225 example)

Figure 22. 2.5-V Amplitude PWM Pulse (TPS28225 example)

NOTE

The driver sets UGATE low and LGATE high when PWM is low. When the PWM goes high, UGATE goes high and LGATE goes low.

Feature Description (continued)

7.3.4.2 External Resistor Interference

Any external resistor between PWM input and GND with the value lower than 40 kΩ can interfere with the 3-state thresholds. If the driver is intended to operate in the 3-state mode, any resistor below 40 kΩ at the PWM and GND should be avoided. A resistor lower than 3.5 kΩ connected between the PWM and GND completely disables the 3-state function. In such case, the 3-state window shrinks to zero and the lower 3-state threshold becomes the boundary between the UGATE staying low and LGATE being high and vice versa depending on the PWM input signal applied. It is not necessary to use a resistor <3.5 kΩ to avoid the 3-state condition while using a controller that is 3-state capable. If the rise and fall time of the input PWM signal is shorter than 250 ns, then the driver never enters into the 3-state mode.

In the case where the low-side MOSFET of a buck converter stays on during shutdown, the 3-state feature can be fused to avoid negative resonant voltage across the output capacitor. This feature also can be used during start up with a pre-biased output in the case where pulling the output low during the startup is not allowed due to system requirements. If the system controller does not have the 3-state feature and never goes into the high-impedance state, then setting the EN/PG signal low will keep both gate drive outputs low and turn both low- and high-side MOSFETs OFF during the shut down and start up with the pre-biased output.

The self-adjustable input circuit accepts wide range of input pulse amplitudes (2 V up to 13.2 V) allowing use of a variety of controllers with different outputs including logic level. The wide PWM input voltage allows some flexibility if the driver is used in secondary side synchronous rectifier circuit. The operation of the TPS28226 with a 12-V input PWM pulse amplitude, and with V_{DD} = 7.2 V and V_{DD} = 5 V respectively is shown in Figure 23 and Figure 24.

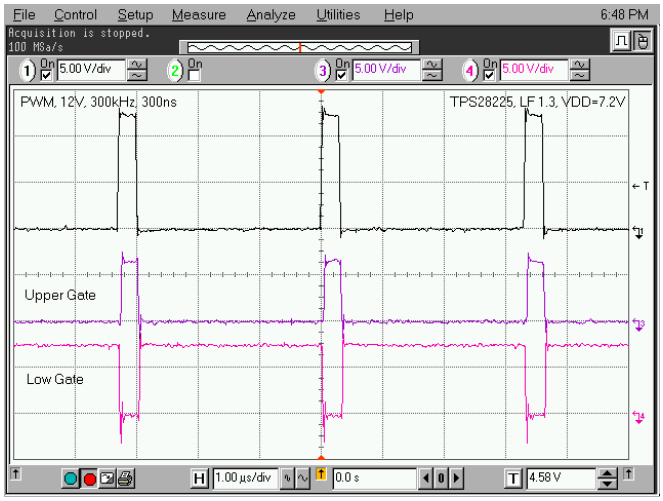


Figure 23. 12-V PWM Pulse at V_{DD} = 7.2 V

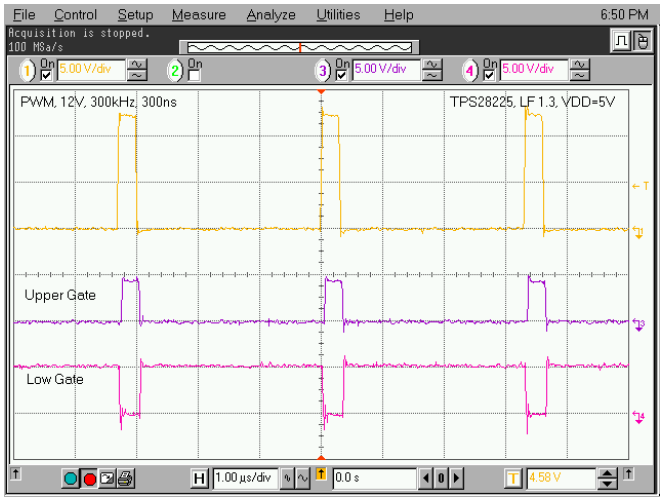


Figure 24. 12-V PWM Pulse at V_{DD} = 5 V

Feature Description (continued)

7.3.5 Bootstrap Diode

The bootstrap diode provides the supply voltage for the UGATE driver by charging the bootstrap capacitor connected between BOOT and PHASE pins from the input voltage VDD when the low-side FET is in ON state. At the very initial stage when both power FETs are OFF, the bootstrap capacitor is pre-charged through this path including the PHASE pin, output inductor and large output capacitor down to GND. The forward voltage drop across the diode is only 1.0 V at bias current 100 mA. This allows quick charge restore of the bootstrap capacitor during the high-frequency operation.

7.3.6 Upper and Lower Gate Drivers

The upper and lower gate drivers charge and discharge the input capacitance of the power MOSFETs to allow operation at switching frequencies up to 2 MHz. The output stage consists of a P-channel MOSFET providing source output current and an N-channel MOSFET providing sink current through the output stage. The ON state resistances of these MOSFETs are optimized for the synchronous buck converter configuration working with low duty cycle at the nominal steady state condition. The UGATE output driver is capable of propagating PWM input puses of less than 30-ns while still maintaining proper dead time to avoid any shoot through current conditions. The waveforms related to the narrow input PWM pulse operation are shown in Figure 18.

7.3.7 Dead-Time Control

The dead-time control circuit is critical for highest efficiency and no shoot through current operation throughout the whole duty cycle range with the different power MOSFETs. By sensing the output of driver going low, this circuit does not allow the gate drive output of another driver to go high until the first driver output falls below the specified threshold. This approach to control the dead time is called adaptive. The overall dead time also includes the fixed portion to ensure that overlapping never exists. The typical dead time is around 14 ns, although it varies over the driver internal tolerances, layout and external MOSFET parasitic inductances. The proper dead time is maintained whenever the current through the output inductor of the power stage flows in the forward or reverse direction. Reverse current could happen in a buck configuration during the transients or while dynamically changing the output voltage on the fly, as some microprocessors require. Because the dead time does not depend on inductor current direction, this driver can be used both in buck and boost regulators or in any bridge configuration where the power MOSFETs are switching in a complementary manner. Keeping the dead time at short optimal level boosts efficiency by 1% to 2% depending on the switching frequency. Measured switching waveforms in one of the practical designs show 10-ns dead time for the rising edge of PHASE node and 22 ns for the falling edge (Figure 39 and Figure 40 in the Application Section of the data sheet).

Large non-optimal dead time can cause duty cycle modulation of the DC-to-DC converter during the operation point where the output inductor current changes its direction right before the turn ON of the high-side MOSFET. This modulation can interfere with the controller operation and it impacts the power stage frequency response transfer function. As the result, some output ripple increase can be observed. The TPS28226 driver is designed with the short adaptive dead time having fixed delay portion that eliminates risk of the effective duty cycle modulation at the described boundary condition.

7.3.8 Thermal Shutdown

If the junction temperature exceeds 160°C, the thermal shutdown circuit will pull both gate driver outputs low and thus turning both, low-side and high-side power FETs OFF. When the driver cools down below 140°C after a thermal shutdown, then it resumes its normal operation and follows the PWM input and EN/PG signals from the external control circuit. While in thermal shutdown state, the internal MOSFET pulls the EN/PG pin low, thus setting a flag indicating the driver is not ready to continue normal operation. Normally the driver is located close to the MOSFETs, and this is usually the hottest spots on the PCB. Thus, the thermal shutdown feature of the TPS28226 can be used as an additional protection for the whole system from overheating.

7.4 Device Functional Modes

TPS28226 device functional mode truth table.

Table 1. Truth Table

PIN	V_{DD} RISING < 3.5 V OR T_J > 160°C	V_{DD} FALLING > 3 V AND T_J < 150°C			
		EN/PG RISING < 1.7 V	EN/PG FALLING > 1.0 V		
			PWM < 1 V	PWM > 1.5 V AND T_{RISE}/T_{FALL} < 200 ns	PWM SIGNAL SOURCE IMPEDANCE >40 kΩ FOR > 250 ns (3-State)(1)
LGATE	Low	Low	High	Low	Low
UGATE	Low	Low	Low	High	Low
EN/PG	Low	–	–	–	–

(1) To exit the 3-state condition, the PWM signal should go low. One High PWM input signal followed by one Low PWM input signal is required before re-entering the 3-state condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful MOSFET driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, MOSFET drivers are indispensable when it is impossible for the PWM controller to directly drive the MOSFETs of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. MOSFET drivers effectively combine both the level-shifting and buffer-drive functions.

MOSFET drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Typical Application

The DC-DC converter in Figure 25 displays the schematic of the TPS28226 in a multiphase high-current step-down power supply (only one phase is shown). This design uses a single high-side MOSFET Q10 and two low-side MOSFETs Q8 and Q9, the latter connected in parallel. The TPS28226 is controlled by multiphase buck DC-to-DC controller like TPS40090. As TPS28226 has internal shoot-through protection only one PWM control signal is required for each channel.

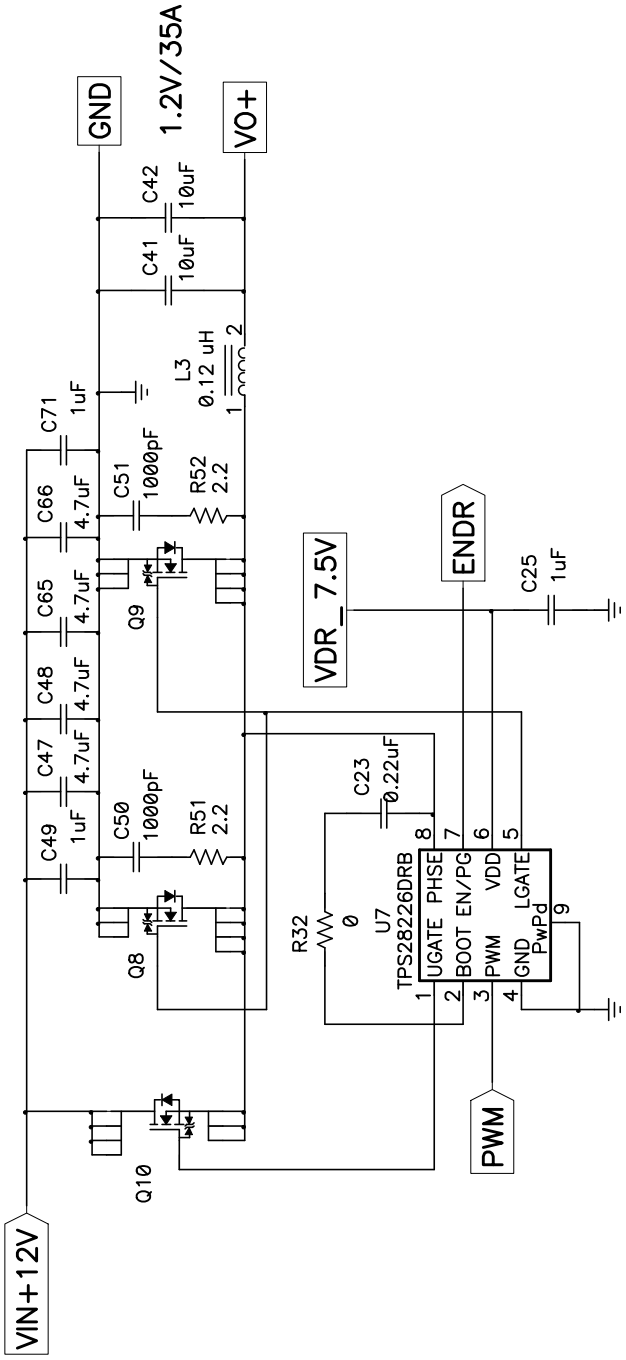


Figure 25. One of Four Phases Driven by TPS28226 Driver in 4-Phase VRM Reference Design

Typical Application (continued)

8.2.1 Design Requirements

The VRM Reference Design is capable of driving 35 A per phase. In this example it has a nominal input voltage of 12 V within a tolerance range of ±5%. The switching frequency is 500 kHz. The nominal duty cycle is 10%, therefore the low-side MOSFETs are conducting 90% of the time. By choosing lower $R_{DS(on)}$ the conduction losses of the switching elements are minimized.

Table 2. VRM Reference Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	12 V ±5%
Output voltage	0.83 V to 1.6 V
Frequency	500 kHz
Peak-to-peak output voltage variation on load current transient (0 A to 100 A) within 1 µs	<160 mV
Dynamic output voltage change slew rate	12.25 mV per 5 µs

8.2.2 Detailed Design Procedure

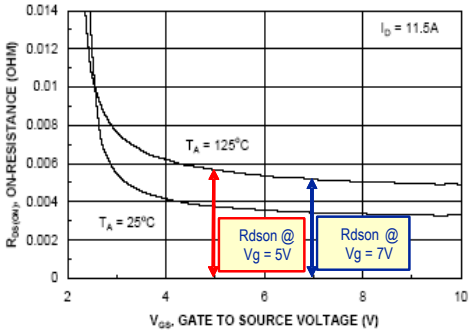
The bootstrap current can be limited by changing R32 to prevent overcharging of the bootstrap capacitor and to slow the turn-on transition of the high-side MOSFET. This reduces the peak amplitude and ringing of the switching node. Furthermore it minimizes the possibility of Cdv/dt-induced shoot-through of the low-side MOSFETs. The snubbers composed of C50 with R51 and C51 with R52 help to reduce switching noise.

The output component selection considers the requirement of a fast transient response. For output capacitors small capacitance values are chosen because of rapid changes of the output voltage. These changes also require an inductor with low inductance. Due to the small duty cycle the low-side MOSFETs conduct a long time. Two low-side MOSFETs are selected to increase both thermal performance and efficiency.

8.2.2.1 Four Phases Driven by TPS28226 Driver

When using the same power stage Figure 25, the driver with the optimal drive voltage and optimal dead time can boost efficiency up to 5%. The optimal 8-V drive voltage versus 5-V drive contributes 2% to 3% efficiency increase and the remaining 1% to 2% can be attributed to the reduced dead time. The 7-V to 8-V drive voltage is optimal for operation at switching frequency range above 400 kHz and can be illustrated by observing typical $R_{DS(on)}$ curves of modern FETs as a function of their gate-drive voltage. This is shown in Figure 26.

Figure 26 and Figure 27 show that the $R_{DS(on)}$ at 5-V drive is substantially larger than at 7 V and above that the $R_{DS(on)}$ curve is almost flat. This means that moving from 5-V drive to an 8-V drive boosts the efficiency because of lower $R_{DS(on)}$ of the MOSFETs at 8 V. Further increase of drive voltage from 8 V to 12 V only slightly decreases the conduction losses but the power dissipated inside the driver increases dramatically (by 125%). The power dissipated by the driver with 5-V, 8-V and 12-V drive as a function of switching frequency from 400 kHz to 800 kHz. It should be noted that the 12-V driver exceeds the maximum dissipated power allowed for an SOIC-8 package even at 400-kHz switching frequency.



On-Resistance Variation with Gate-to-Source Voltage.

Figure 26. $R_{DS(on)}$ of MOSFET as Function of V_{GS}

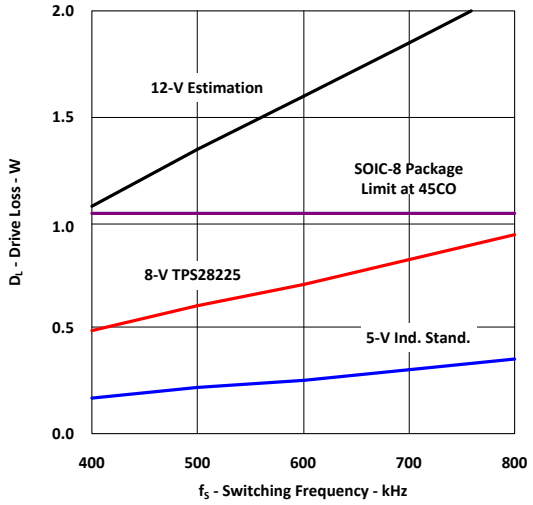


Figure 27. Drive Power as Function of V_{GS} and F_{SW}

8.2.2.2 Switching The MOSFETs

Driving the MOSFETs efficiently at high switching frequencies requires special attention to layout and the reduction of parasitic inductances. Efforts need to be done both at the driver's die and package level and at the PCB layout level to keep the parasitic inductances as low as possible. Figure 28 shows the main parasitic inductances and current flow during turning ON and OFF of the MOSFET by charging its C_{GS} gate capacitance.

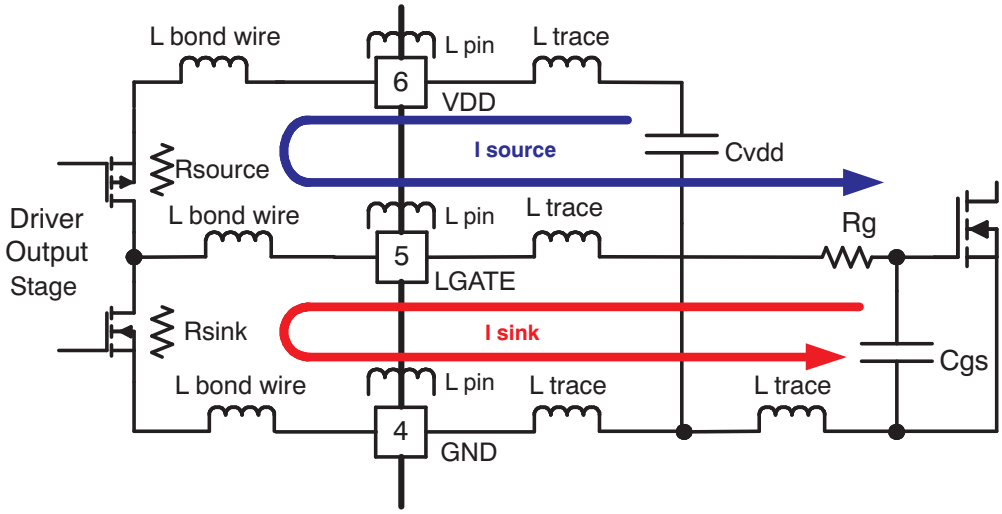


Figure 28. MOSFET Drive Paths and Main Circuit Parasitics

The I_{SOURCE} current charges the gate capacitor and the I_{SINK} current discharges it. The rise and fall time of voltage across the gate defines how quickly the MOSFET can be switched. The timing parameters specified in datasheet for both upper and lower driver are shown in Figure 16 and Figure 17 where 3-nF load capacitor has been used for the characterization data. Based on these actual measurements, the analytical curves in Figure 29 and Figure 30 show the output voltage and current of upper and low side drivers during the discharging of load capacitor. The left waveforms show the voltage and current as a function of time, while the right waveforms show the relation between the voltage and current during fast switching. These waveforms show the actual switching process and its limitations because of parasitic inductances. The static V_{OUT}/ I_{OUT} curves shown in many datasheets and specifications for the MOSFET drivers do not replicate actual switching condition and provide limited information for the user.

Turning Off of the MOSFET needs to be done as fast as possible to reduce switching losses. For this reason the TPS28226 driver has very low output impedance specified as 0.4 Ω typical for lower driver and 1 Ω typical for upper driver at DC current. Assuming 8-V drive voltage and no parasitic inductances, one can expect an initial sink current amplitude of 20 A and 8 A respectively for the lower and upper drivers. With pure R-C discharge circuit for the gate capacitor, the voltage and current waveforms are expected to be exponential. However, because of parasitic inductances, the actual waveforms have some ringing and the peak current for the lower driver is about 4 A and about 2.5 A for the upper driver (Figure 29 and Figure 30). The overall parasitic inductance for the lower drive path is estimated as 4 nH and for the upper drive path as 6 nH. The internal parasitic inductance of the driver, which includes inductances of bonded wires and package leads, can be estimated for SOIC-8 package as 2 nH for lower gate and 4 nH for the upper gate. Use of DFN-8 package reduces the internal parasitic inductances by approximately 50%.

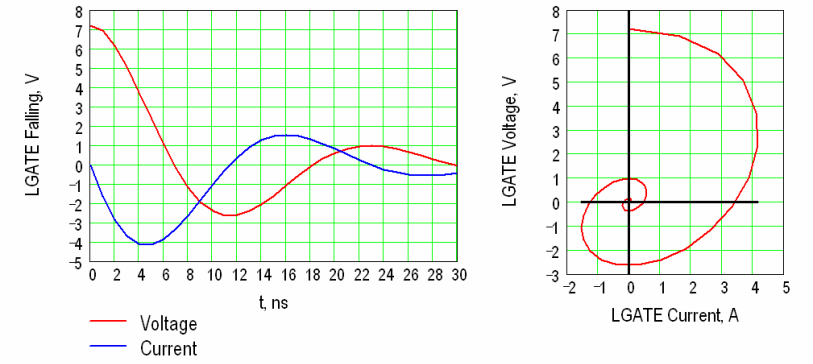


Figure 29. LGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right))

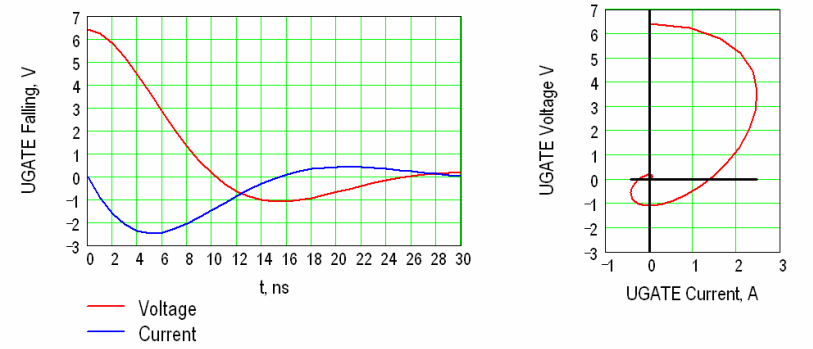


Figure 30. UGATE Turning Off Voltage and Sink Current vs Time (Related Switching Diagram (right))

8.2.2.3 List of Materials

For this specific example see Table 3. The component vendors are not limited to those shown in the table below. It should be noted that in this example, the power MOSFET packages were chosen with drains on top. The decoupling capacitors C47, C48, C65, and C66 were chosen to have low profiles. This allows the designer to meet good layout rules and place a heatsink on top of the FETs using an electrically isolated and thermally conductive pad.

Table 3. List of Materials

REF DES	COUNT	DESCRIPTION	MANUFACTURE	PART NUMBER
C47, C48, C65, C66	4	Capacitor, ceramic, 4.7 µF, 16 V, X5R 10%, low profile 0.95 mm, 1206	TDK	C3216X5R1C475K
C41, C42	2	Capacitor, ceramic, 10 µF, 16 V, X7R 10%, 1206	TDK	C3216X7R1C106K
C50, C51	2	Capacitor, ceramic, 1000 pF, 50 V, X7R, 10%, 0603	Std	Std
C23	1	Capacitor, ceramic, 0.22 µF, 16 V, X7R, 10%, 0603	Std	Std
C25, C49, C71	3	Capacitor, ceramic, 1 µF, 16 V, X7R, 10%, '0603	Std	Std
L3	1	Inductor, SMT, 0.12 µH, 31 A, 0.36 mΩ, 0.400 x 0.276	Pulse	PA0511-101
Q8, Q9	2	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 2.4 mΩ, I_D 45 A, LFPAK-i	Renesas	RJK0301DPB-I
Q10	1	Mosfet, N-channel, V_{DS} 30 V, R_{DS} 6.2 mΩ, I_D 30 A, LFPAK-i	Renesas	RJK0305DPB-I
R32	1	Resistor, chip, 0 Ω, 1/10 W, 1%, '0805	Std	Std
R51, R52	2	Resistor, chip, 2.2 Ω, 1/10 W, 1%, '0805	Std	Std
U7	1	Device, High Frequency 4-A Sink Synchronous Buck MOSFET Driver, DFN-8	Texas Instruments	TPS28226DRB

8.2.3 Application Curves

Efficiency achieved using TPS28226 driver with 8-V drive at different switching frequencies a similar industry 5-V driver using the power stage in Figure 25 is shown in Figure 31, Figure 32, Figure 33, Figure 34 and Figure 35.

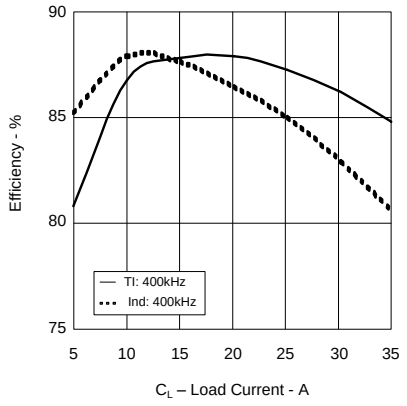


Figure 31. Efficiency vs Load Current

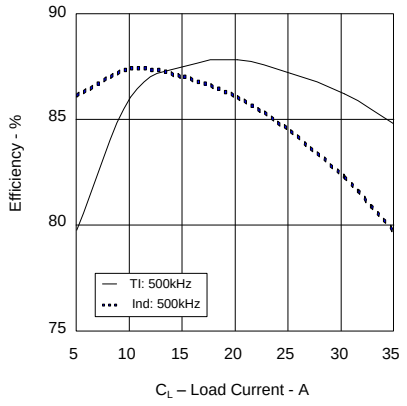


Figure 32. Efficiency vs Load Current

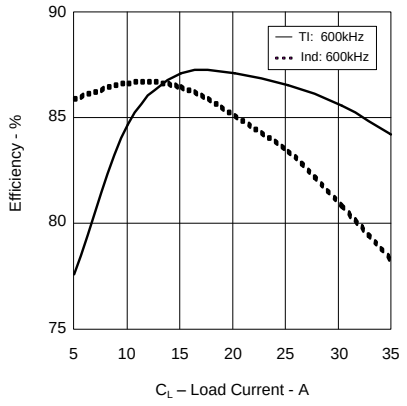


Figure 33. Efficiency vs Load Current

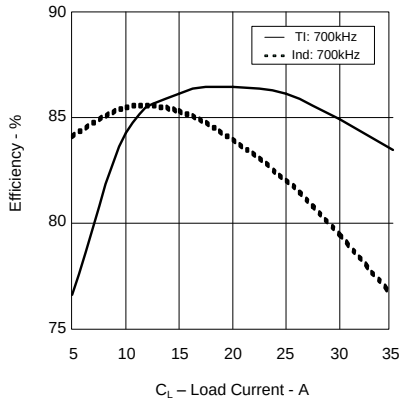


Figure 34. Efficiency vs Load Current

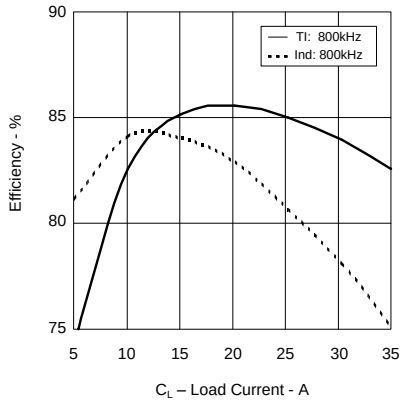


Figure 35. Efficiency vs Load Current

8.3 System Examples

Figure 36, Figure 37 and Figure 38 below illustrate typical implementations of the TPS28226 in step-down power supplies.

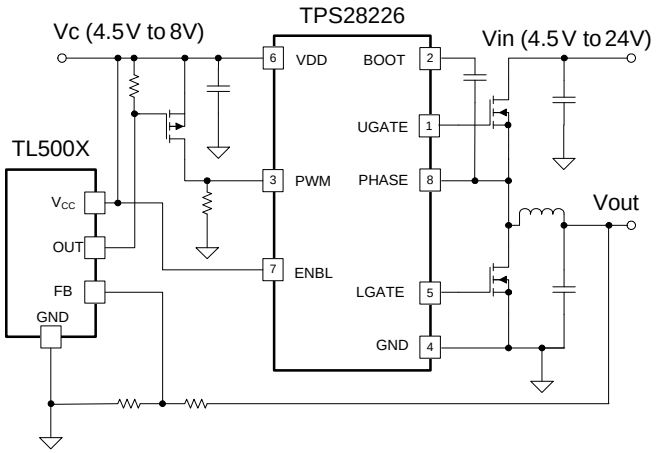


Figure 36. One-Phase POL Regulator

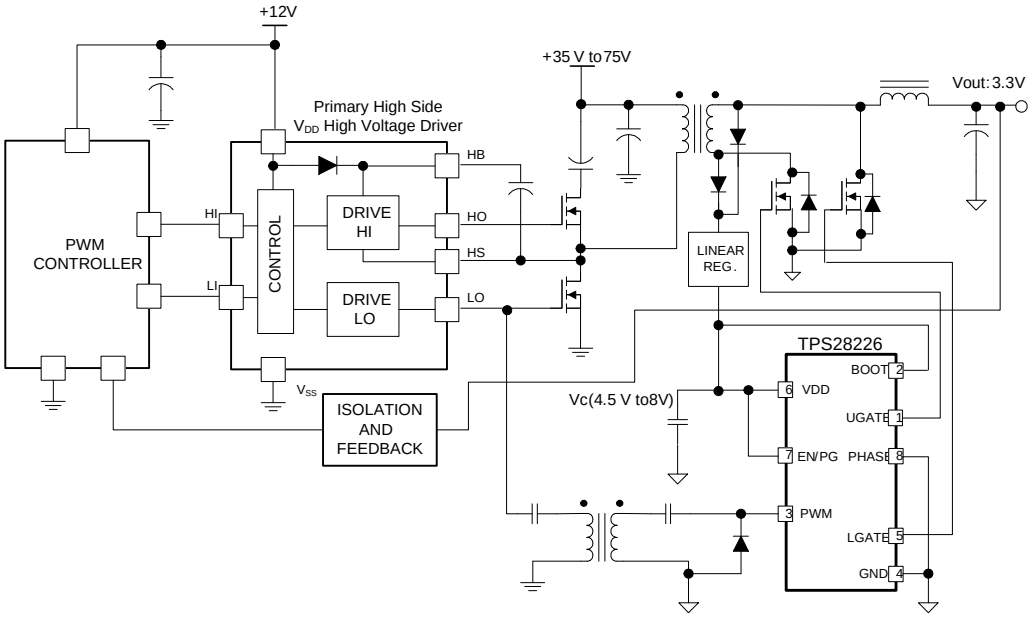


Figure 37. Driver for Synchronous Rectification with Complementary Driven MOSFETs

System Examples (continued)

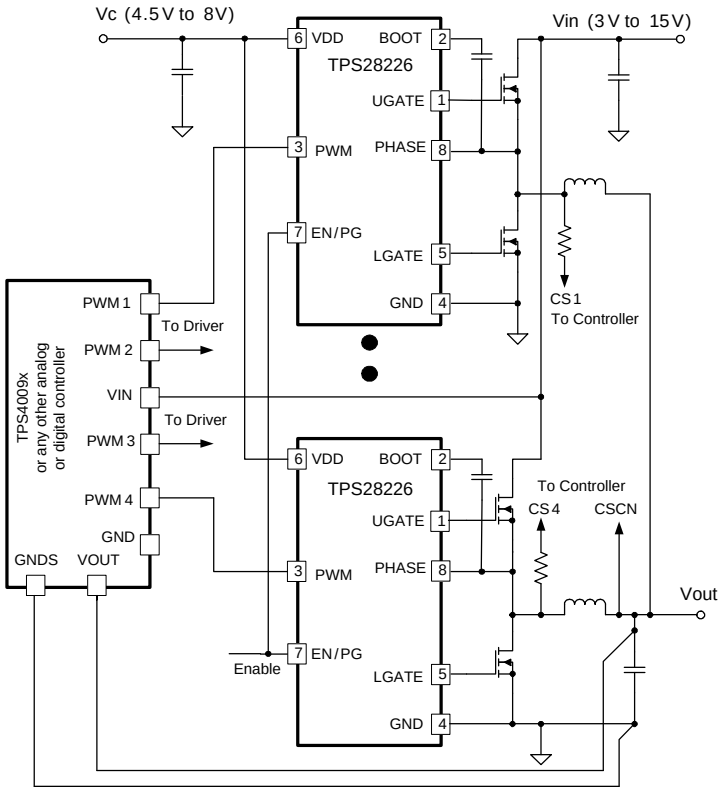


Figure 38. Multi-Phase Synchronous Buck Converter

9 Power Supply Recommendations

The supply voltage range for operation is 4.5 to 8 V. The lower end of this range is governed by the under-voltage lockout thresholds. The UVLO disables the driver and keeps the power FETs OFF when V_{DD} is too low. A lows ESR ceramic decoupling capacitor in the range of 0.22 µF to 4.7 µF between V_{DD} and GND is recommended.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules need to be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the DFN-8 package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the PHASE node as for the GND.
- Use wide traces for UGATE and LGATE closely following the related PHASE and GND traces. Eighty to 100 mils width is preferable where possible.
- Use at least 2 or more vias if the MOSFET driving trace needs to be routed from one layer to another. For the GND the number of vias are determined not only by the parasitic inductance but also by the requirements for the thermal pad.
- Avoid PWM and enable traces going close to the PHASE node and pad where high dV/dT voltage can induce significant noise into the relatively high impedance leads.

It should be taken into account that poor layout can cause 3% to 5% less efficiency versus a good layout design and can even decrease the reliability of the whole system.

The schematic of one of the phases in a multi-phase synchronous buck regulator and the related layout are shown in Figure 25 and Figure 41. These help to illustrate good design practices. The power stage includes one high-side MOSFET Q10 and two low-side MOSFETS (Q8 and Q9). The driver (U7) is located on bottom side of PCB close to the power MOSFETs. The related switching waveforms during turning ON and OFF of upper FET are shown in Figure 39 and Figure 40. The dead time during turning ON is only 10 ns (Figure 39) and 22 ns during turning OFF (Figure 40).

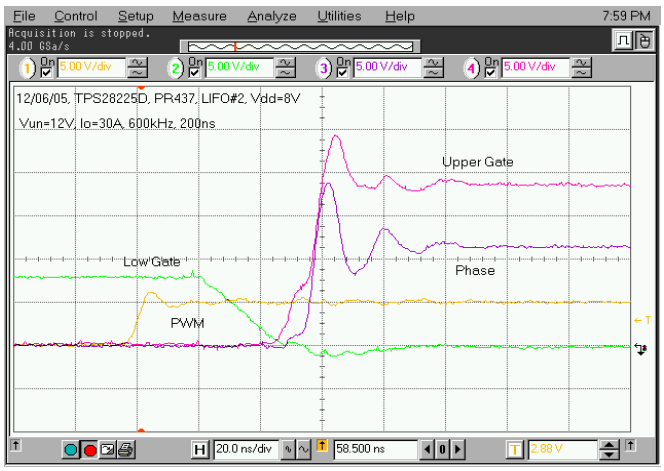


Figure 39. Phase Rising-Edge Switching Waveforms (20 ns/div) of the Power Stage in Figure 25

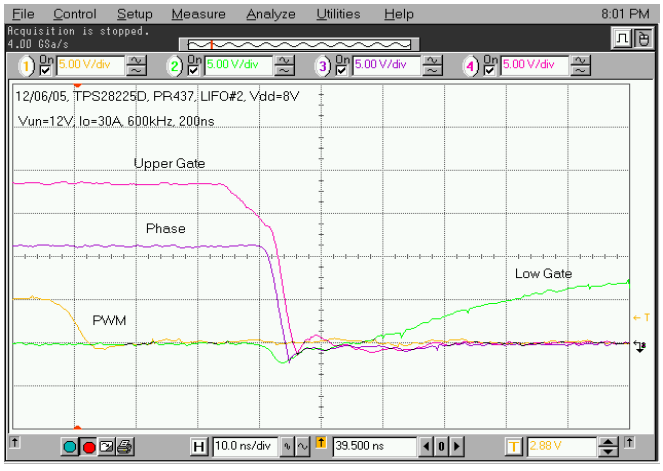


Figure 40. Phase Falling-Edge Switching Waveforms (10 ns/div) of the Power State in Figure 25

10.2 Layout Example

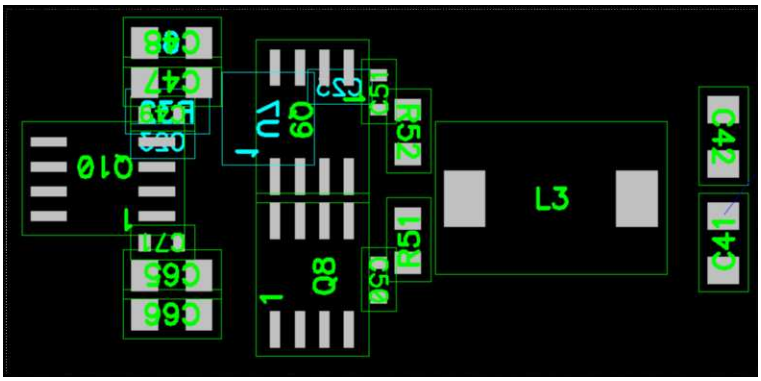


Figure 41. Component Placement Based on Schematic in Figure 25

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

- TPS40090, TPS40091 2/3/4-Phase Multi-Phase Controller, (SLUS578)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS28226D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28226	Samples
TPS28226DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28226	Samples
TPS28226DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8226	Samples
TPS28226DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8226	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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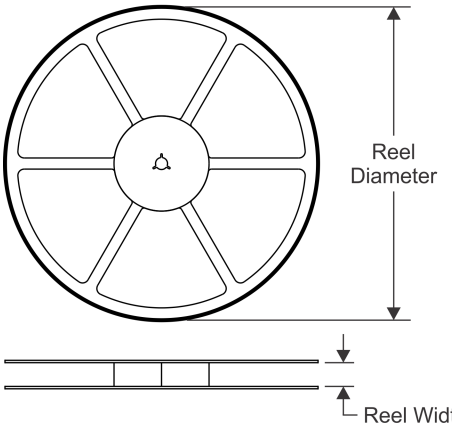
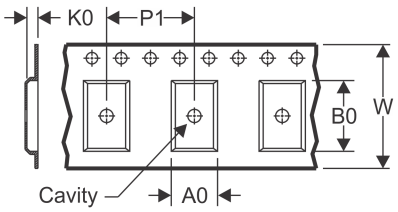
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

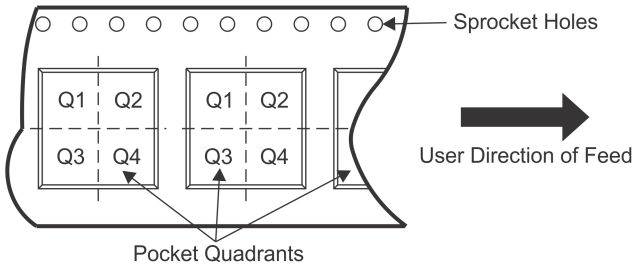


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

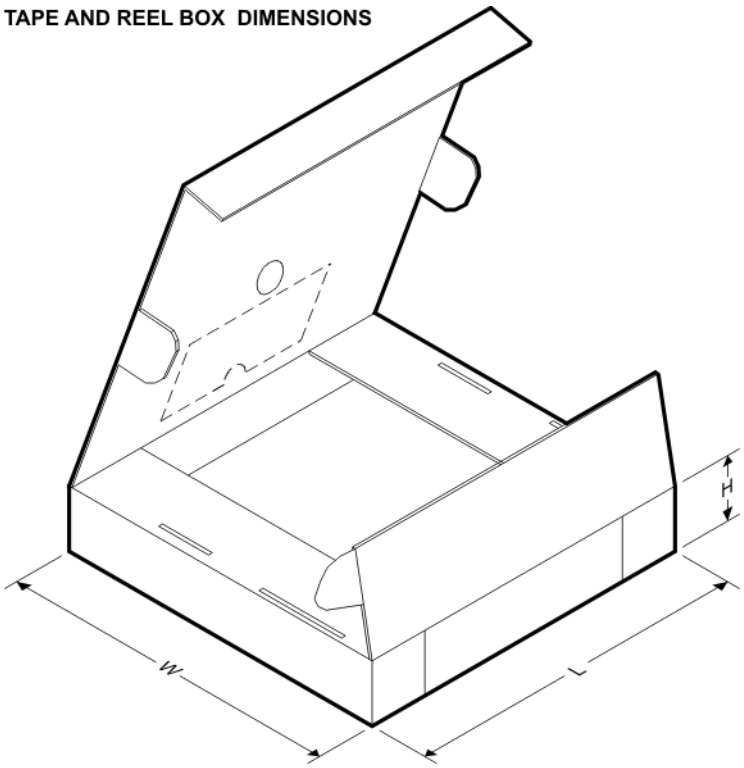
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS28226DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS28226DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS28226DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS28226DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS28226DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS28226DRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

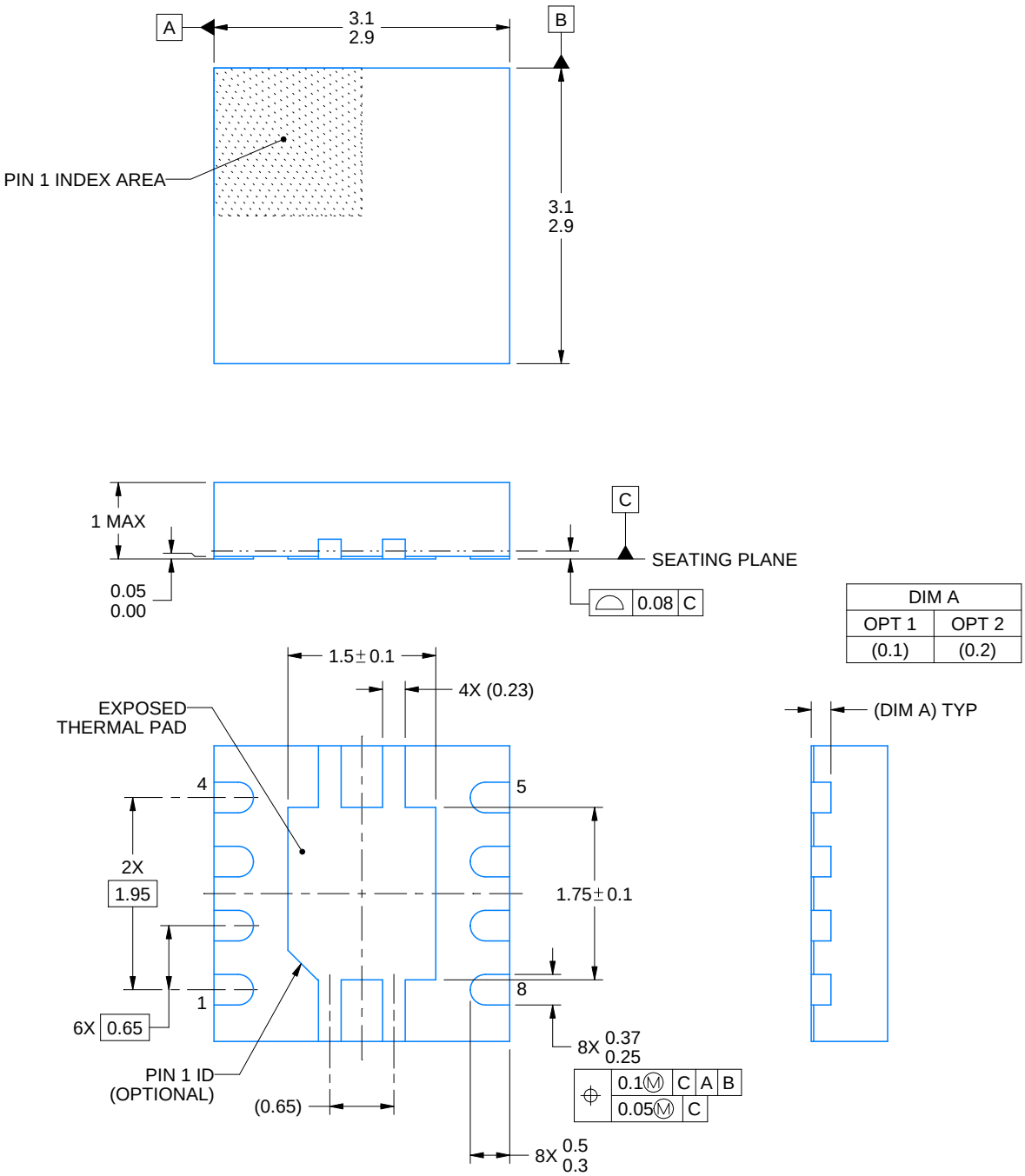
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

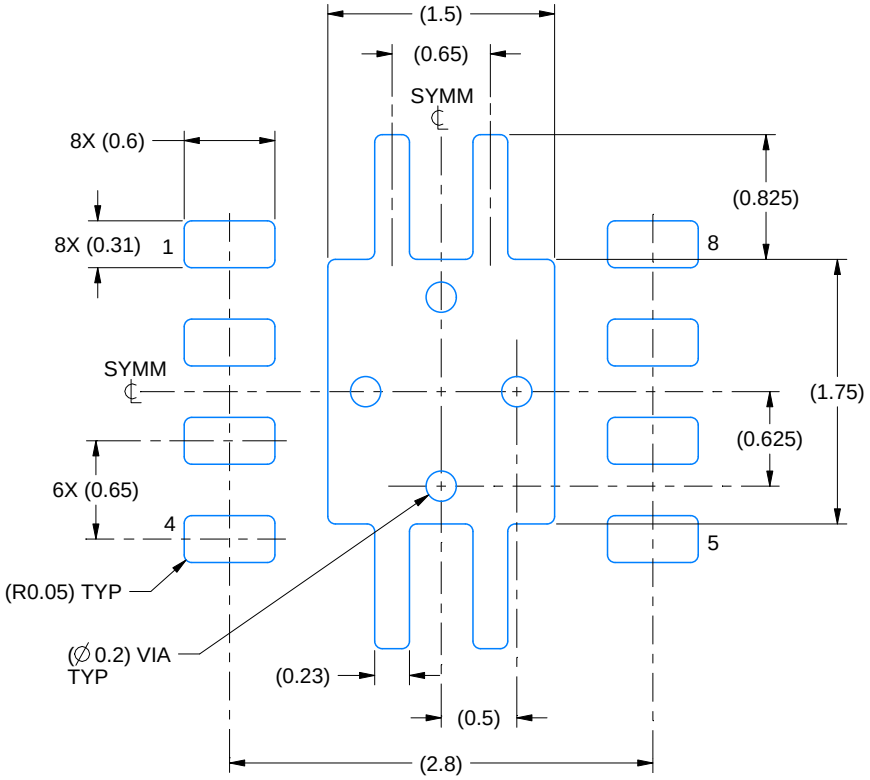
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

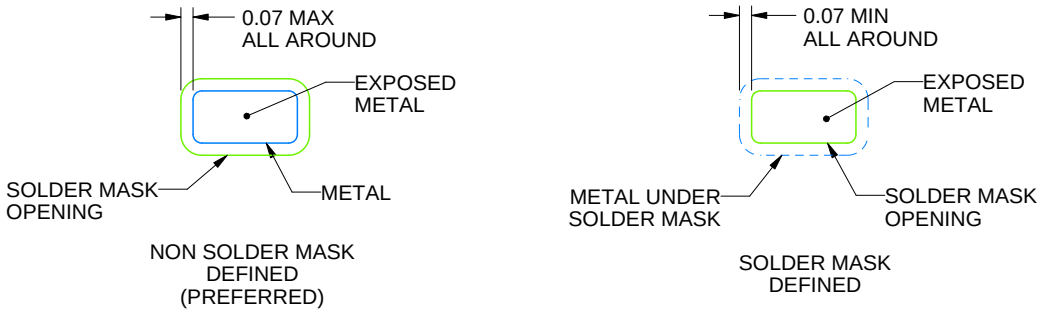
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

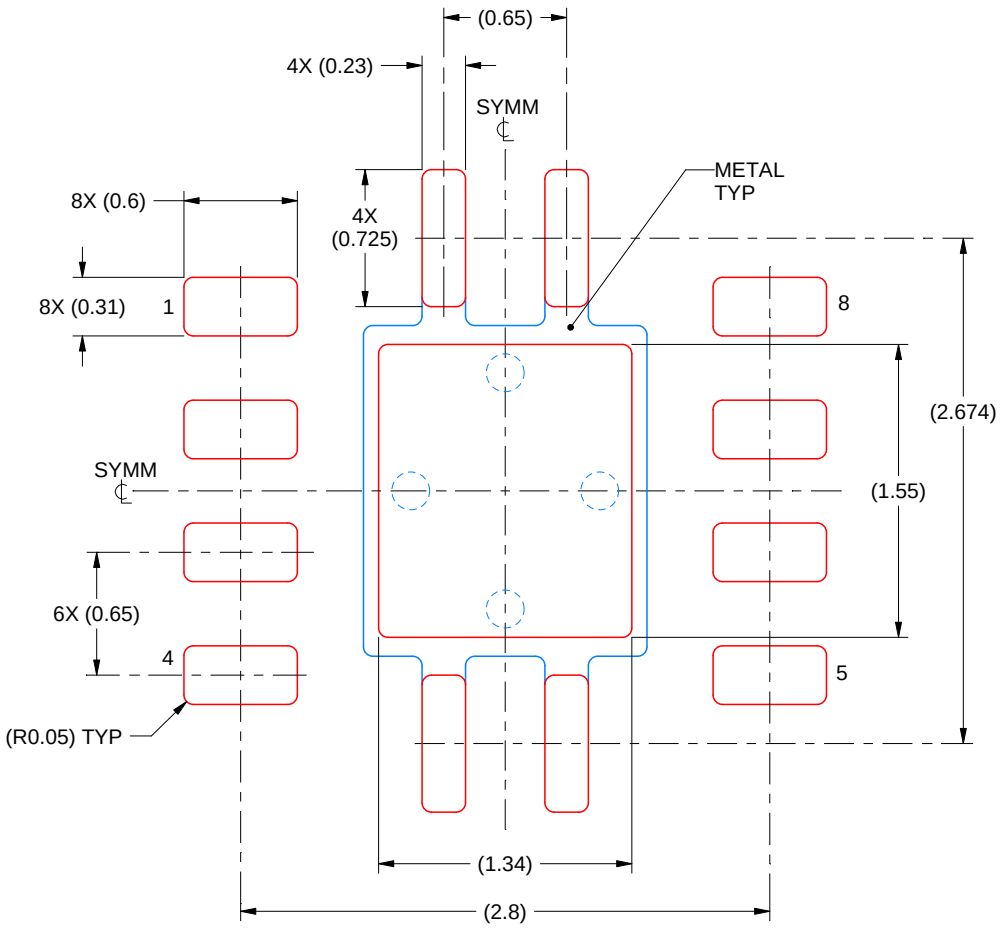


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



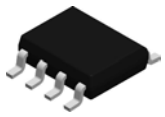
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

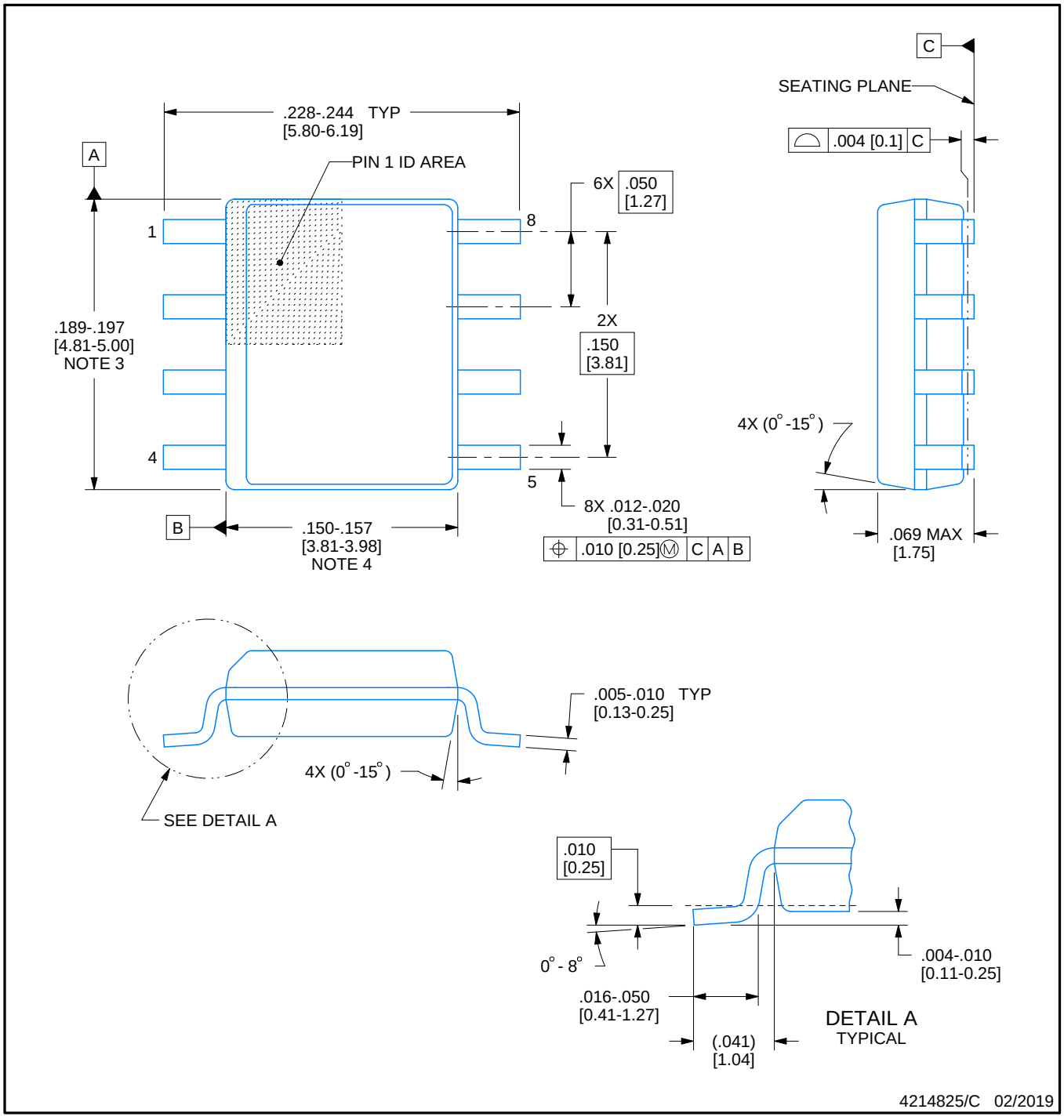


PACKAGE OUTLINE

D0008A

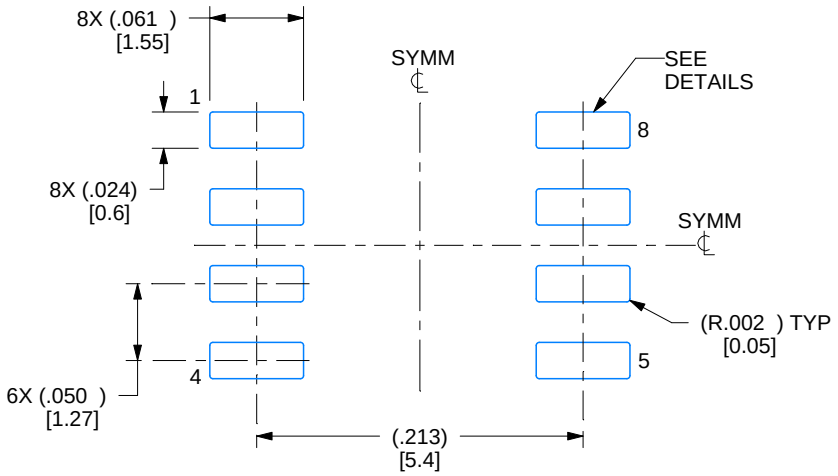
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

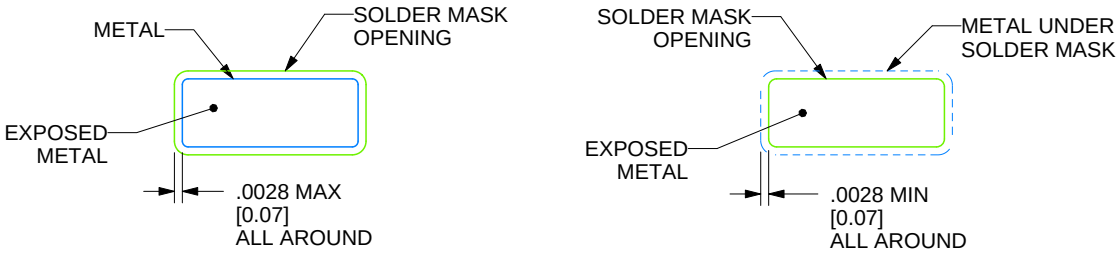


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

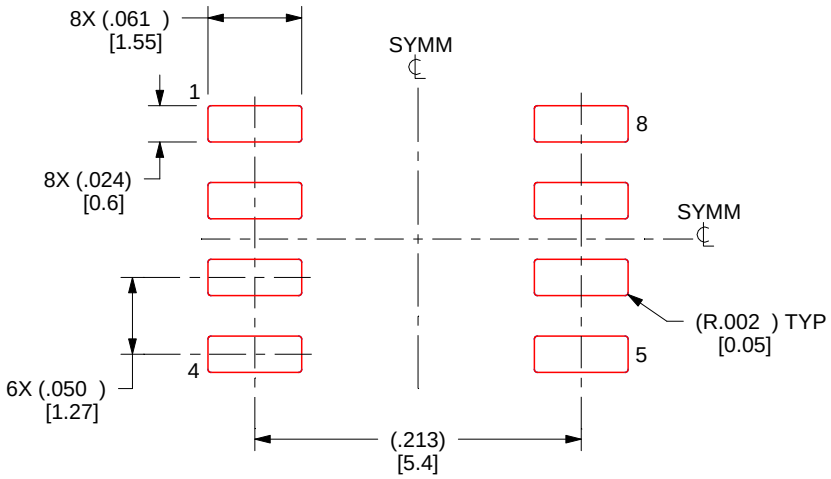
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265