



DS0026/DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the

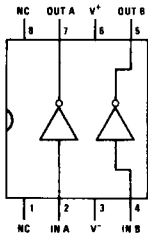
output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state. For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive— ± 1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

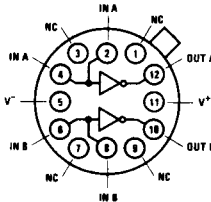
Dual-In-Line Package



TL/F/5853-2

Order Number DS0026CJ-8,
DS0026CL or DS0026CN
See NS Package Number
J08A or N08E

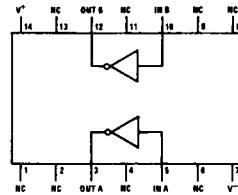
TO-8 Package



TL/F/5853-3

Order Number
DS0026G or DS0026CG
See NS Package
Number G12B

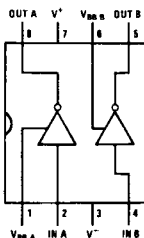
Dual-In-Line Package



TL/F/5853-4

Order Number
DS0026J or DS0026CJ
See NS Package
Number J14A

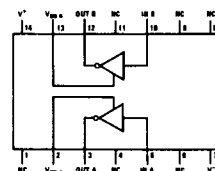
Dual-In-Line Package



TL/F/5853-6

Order Number DS0056CN
See NS Package Number N08E

Dual-In-Line Package



TL/F/5853-7

Order Number DS0056J
or DS0056CJ
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW

EIAJ SO Package	800 mW
Operating Temperature Range	
DS0026, DS0056	-55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	
	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C; derate EIAJ SO package 5.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$	2	1.5		V	
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$		10	15	mA	
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$		0.6	0.4	V	
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$		-3	-10	μA	
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V, I_{OL} = 1 mA$		$V^- + 0.7$	$V^- + 1.0$	V	
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V, V_{SS} \geq V^+ + 1.0V$ $I_{OH} = -1 mA$	DS0026	$V^+ - 1.0$	$V^+ - 0.8$	V	
			DS0056	$V^+ - 0.3$	$V^+ - 0.1$	V	
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^- = 20V, V_{IN} - V^- = 2.4V$ (Note 6)	DS0026		30	40	mA
			DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V,$ $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics ($T_A = 25^\circ C$) (Notes 5 and 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ON}	Turn-On Delay	(Figure 1)	5	7.5	12	ns
		(Figure 2)		11		ns
t_{OFF}	Turn-Off Delay	(Figure 1)		12	15	ns
		(Figure 2)		13		ns
t_r	Rise Time	(Figure 1), (Note 5)	$C_L = 500 pF$	15	18	ns
			$C_L = 1000 pF$	20	35	ns
		(Figure 2), (Note 5)	$C_L = 500 pF$	30	40	ns
			$C_L = 1000 pF$	36	50	ns
t_f	Fall Time	(Figure 1), (Note 5)	$C_L = 500 pF$	12	16	ns
			$C_L = 1000 pF$	17	25	ns
		(Figure 2), (Note 5)	$C_L = 500 pF$	28	35	ns
			$C_L = 1000 pF$	31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to $20V$, $C_L = 1000 pF$, over the temperature range of $-55^\circ C$ to $+125^\circ C$ for the DS0026, DS0056 and $0^\circ C$ to $+70^\circ C$ for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

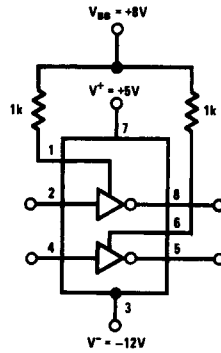
Note 4: All typical values for $T_A = 25^\circ C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1 k\Omega$ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

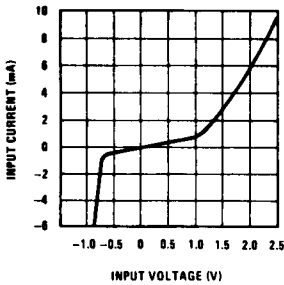
Typical V_{BB} Connection



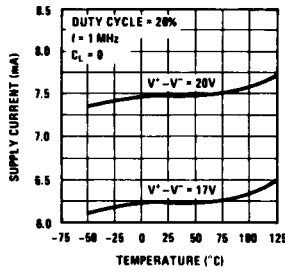
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Typical Performance Characteristics

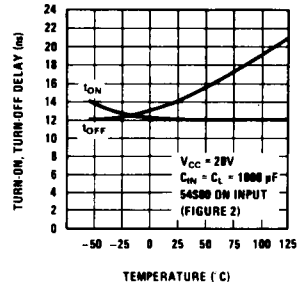
Input Current vs input Voltage



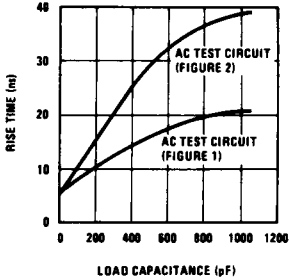
Supply Current vs Temperature



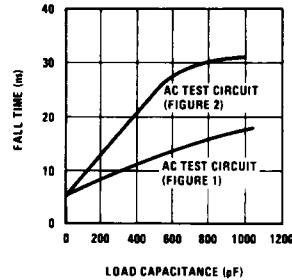
Turn-On and Turn-Off Delay vs Temperature



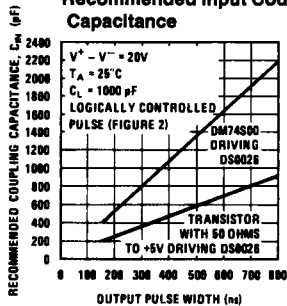
Rise Time vs Load Capacitance



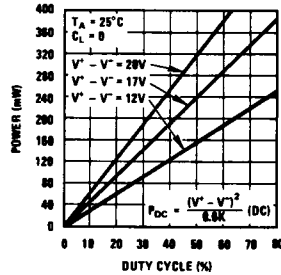
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



DC Power (P_{DC}) vs Duty Cycle

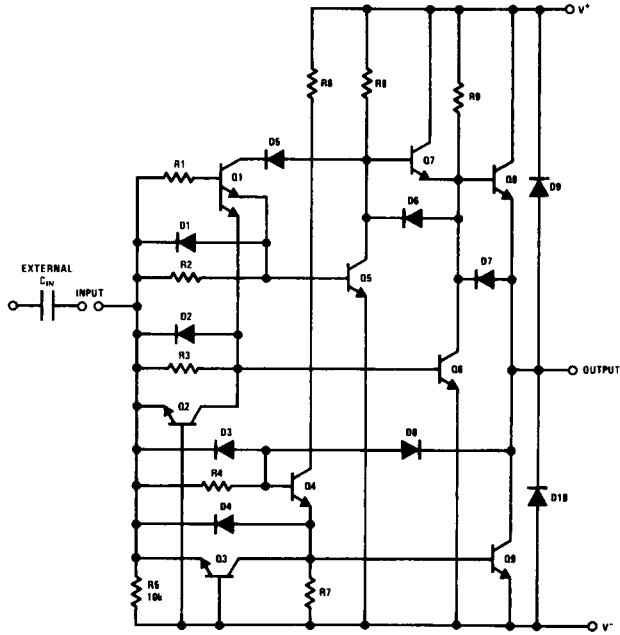


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Schematic Diagrams

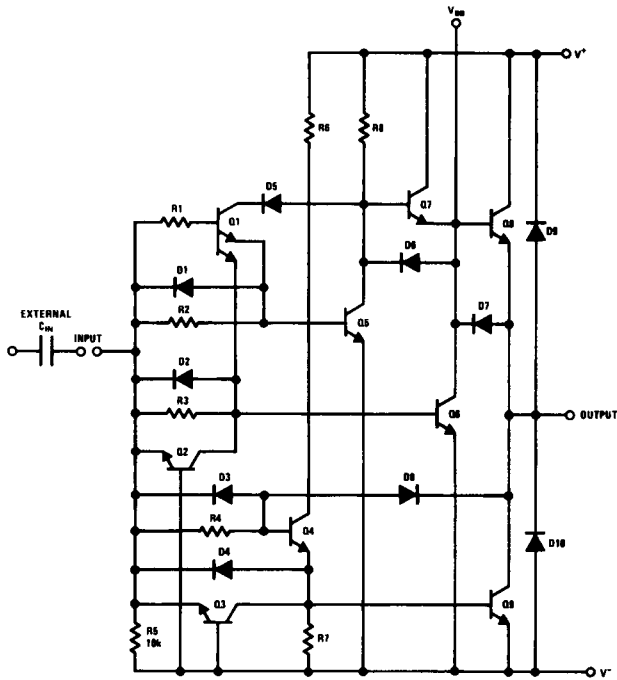
DS0026/DS0056

1/2 DS0026



TL/F/5853-10

1/2 DS0056



TL/F/5853-11

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AC Test Circuits and Switching Time Waveforms

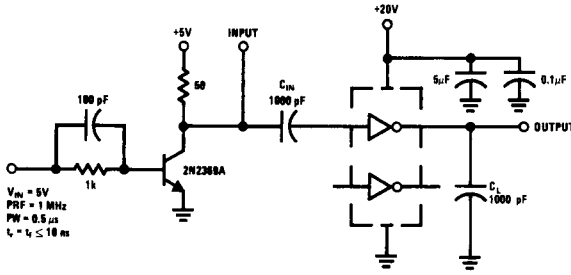
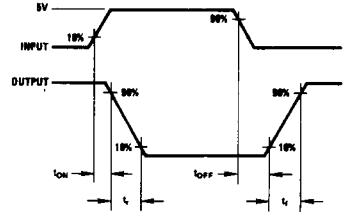


FIGURE 1

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TL/F/5853-13

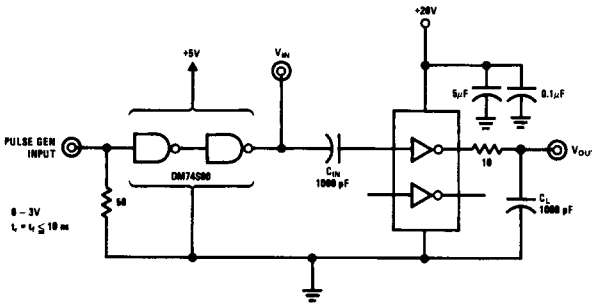
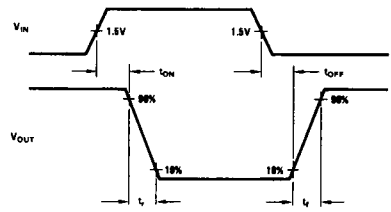


FIGURE 2

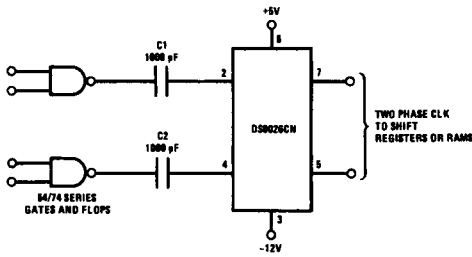
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TL/F/5853-15

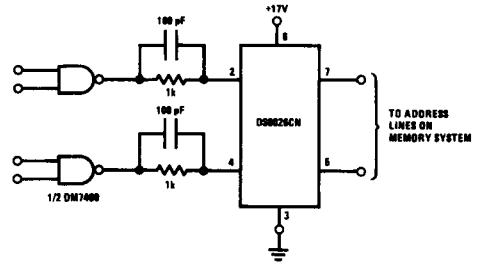
Typical Applications

AC Coupled MOS Clock Driver



TL/F/5853-16

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



TL/F/5853-17

Application Hints

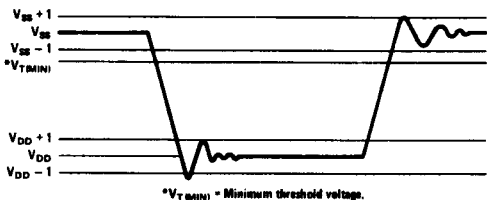
DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems

have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Application Hints (Continued)

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The



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FIGURE 6. Clock Waveform

ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1 V_{OH}$ is not maintained, at all times, the infor-

mation stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were $-1.3V$, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damp-

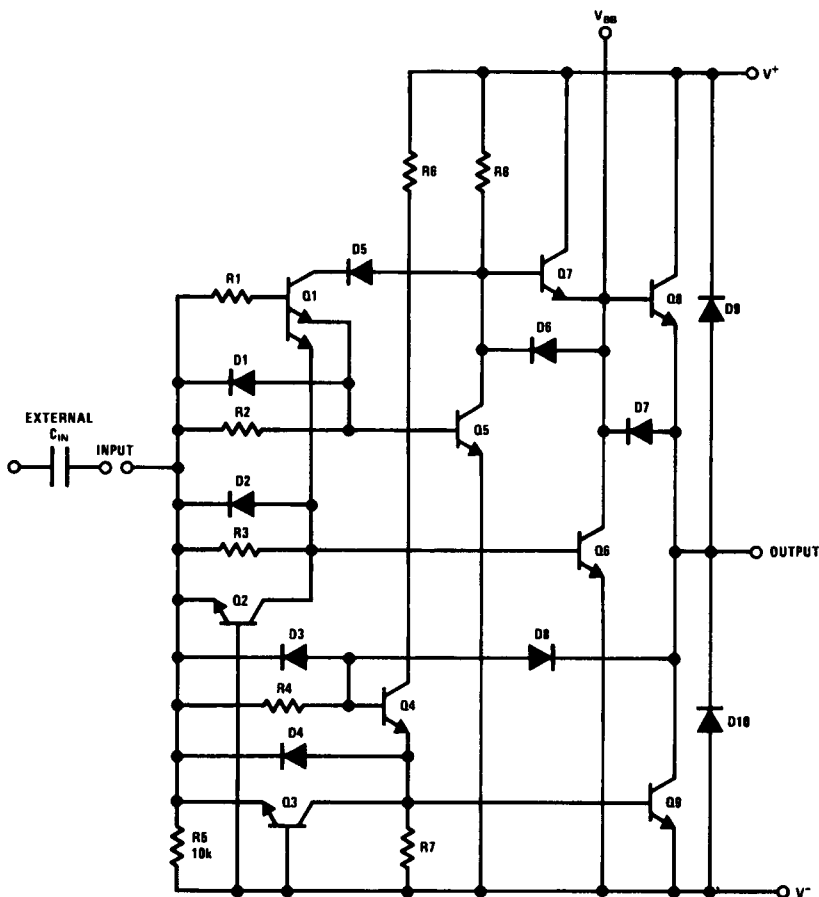


FIGURE 7. Schematic of 1/2 DS0056

TL/F/5853-11

Application Hints (Continued)

ing resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power planes minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB} , supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 k Ω resistor. This allows transistor Q8 to

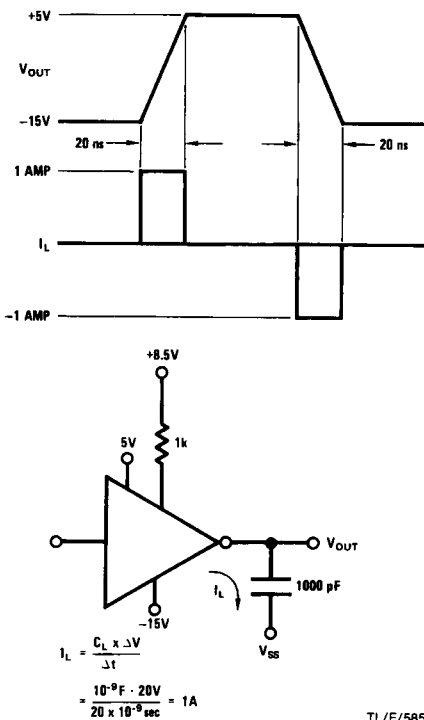


FIGURE 8. Clock Waveforms (Voltage and Current)

saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0\text{V}$ clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q8 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin on this line to zero.

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C , to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L , is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L .

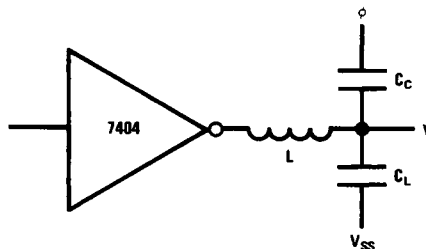


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20 \text{V} \times \frac{C_C}{C_L + C_C} = 20 \text{V} \times \left(\frac{1}{56 + 1} \right) = 0.35 \text{V}$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of

Application Hints (Continued)

noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

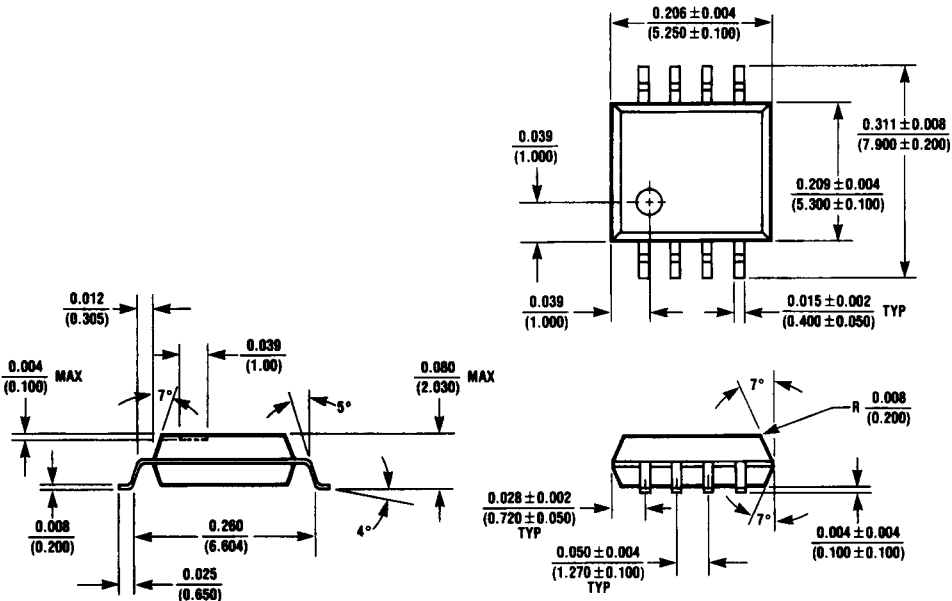
$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1 \text{ mA}$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Packaging Information



8-Lead Surface Mount Package
Order Number DS0026CL

TL/F/5853-21