NCP1927

Combination Power Factor Correction Controller and Flyback Controller for Flat Panel TVs

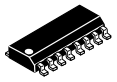
ON Semiconductor®

http://onsemi.com

This combination IC integrates the primary side control blocks – power factor correction (PFC) and flyback controllers with sequencing circuitry – necessary to implement a compact highly efficient Flat Panel TV Switched Mode Power Supply.

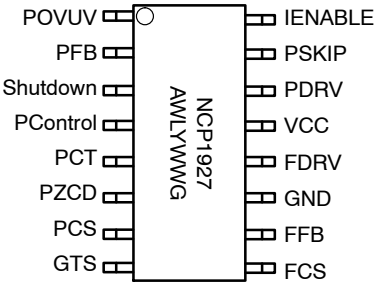
The PFC controller exhibits near–unity power factor while operating in Critical Conduction Mode (CrM) with an internal frequency clamp. The circuit incorporates all the features necessary for building a robust and compact PFC stage while minimizing the number of external components.

The fixed–frequency current–mode flyback controller features a proprietary Soft–Skip™ mode combined with frequency foldback enabling excellent efficiency during light load conditions while achieving very low standby power consumption. Soft–Skip dramatically reduces the risk of acoustic noise, therefore enabling the use of inexpensive transformers and capacitors in the clamping network. Frequency jittering and ramp compensation make this controller an excellent fit for converters where ruggedness and component cost are the key constraints.



SOIC–16
CASE 751B

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP1927DR2G	SOIC–16 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Common General Features

- Wide V_{CC} Range from 10 V to 30 V
- Very Low Startup Current Consumption ($\leq$ 20 μA MAX)
- Inverter Enable Output
- Shutdown Pin to Disable IC
- Go To Standby Input
- This is a Pb–Free Device

PFC Controller Features

- Critical Conduction Mode (CrM) with Constant On Time Control
- Internal Frequency Clamp
- Skip Mode Operation During Light Load Conditions
- Fast Line / Load Transient Compensation
- Accurate and Programmable Maximum On Time Control
- Negative Current Sensing
- Programmable Overvoltage/Undervoltage Protection
- 800 mA Source / 1200 mA Sink Gate Drive

Flyback Controller Features

- 65 kHz Fixed–Frequency Operation with Built–In Ramp Compensation
- Frequency Jittering for Softened EMI Signature
- Frequency Foldback then Soft–Skip for Improved Performance in Standby
- Timer–Based Overload Protection with Auto–Recovery
- Protection Against Winding Short–Circuit
- 4 ms Soft–Start Timer
- 800 mA Source / 1200 mA Sink Gate Drive

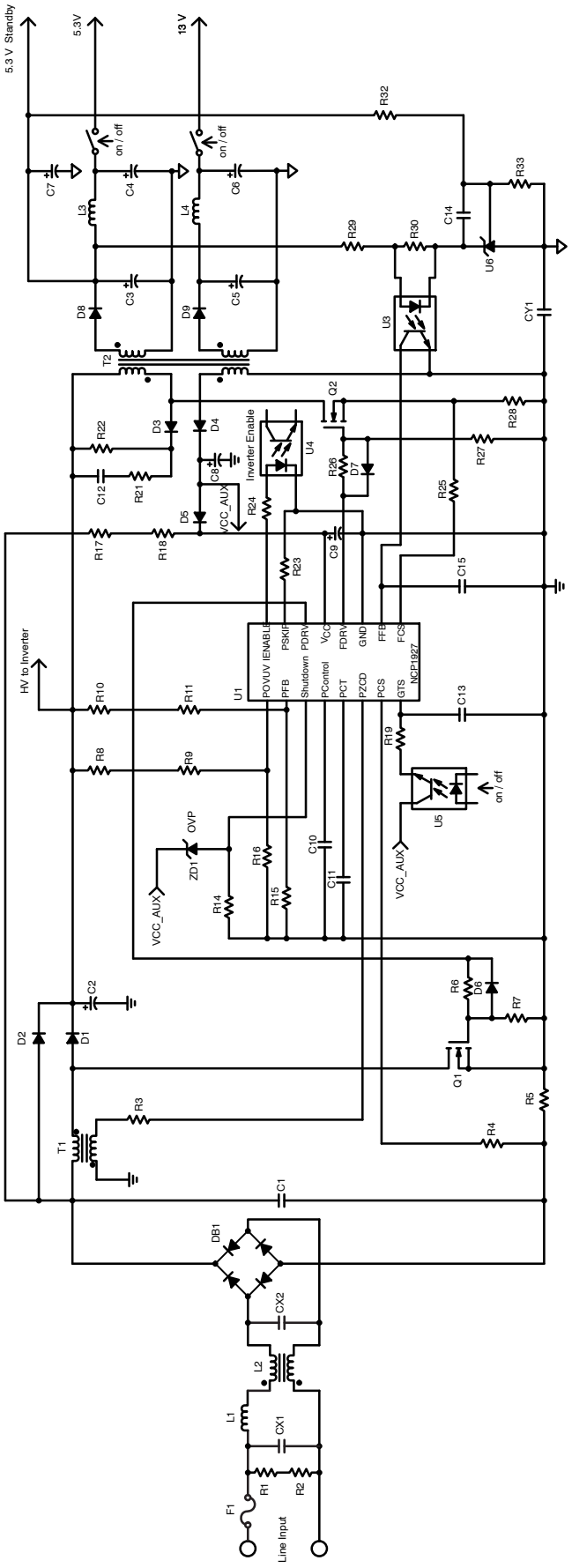
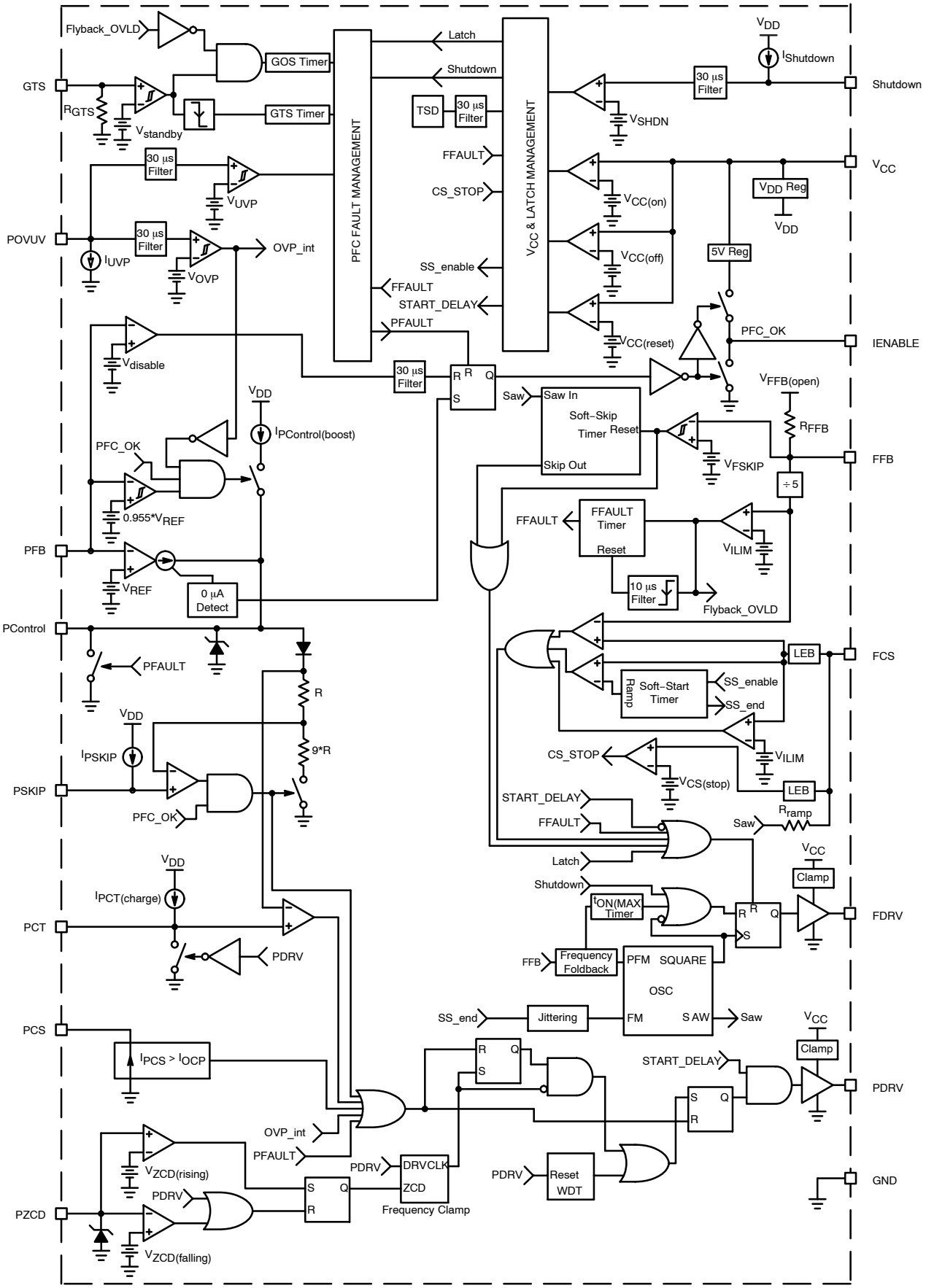


Figure 1. Typical Application Example



* Values are typical values

* All latches are Reset Dominant

Figure 2. Internal Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Description
1	POVUV	The gate drive is disabled while V_{POVUV} is below V_{UVP} (300 mV typ) or above V_{OVP} (2.5 V typ).
2	PFB	This pin receives a portion of the pre−converter output voltage. This information is used for the regulation and the “output low” detection that speeds up the loop response when the output voltage drops below 95.5% (typ) of the programmed level.
3	Shutdown	Pull this pin above 1.0 V (typ) to disable the part. Ground this pin when not in use.
4	PControl	The error amplifier output is available on this pin. The capacitor connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve a high power factor. This pin is internally grounded when the circuit is off so that when it starts operation, the power increases gradually (soft−start).
5	PCT	The PCT pin sources a 210 μA (typ) current to charge an external timing capacitor. The circuit controls the power switch on time by comparing the PCT voltage to an internal voltage derived from the regulation block.
6	PZCD	The voltage of an auxiliary winding is applied to this pin to detect when the inductor is demagnetized for operation in critical conduction mode.
7	PCS	This pin monitors a negative voltage proportional to the coil current. This signal is sensed to limit the maximum coil current and protect the PFC stage during overload conditions.
8	GTS	Pull this pin low to disable the PFC controller during standby mode. Standby mode can also be entered by monitoring the feedback voltage of the flyback stage with an external resistor divider.
9	FCS	This pin senses the primary current for current−mode operation of the flyback stage. Ramp compensation can be added with an external resistor.
10	FFB	Connecting this pin to ground through an optocoupler allows regulation of the flyback stage.
11	GND	This is the the controller ground.
12	FDRV	This is the driver’s output to an external MOSFET gate of the flyback power stage.
13	V_{CC}	This pin is connected to an external auxiliary voltage.
14	PDRV	This is the driver’s output to an external MOSFET gate of the PFC power stage.
15	PSKIP	To adjust the power level below which the PFC stage will enter skip mode, connect a resistor between this pin and ground. To disable skip mode, connect this pin directly to ground.
16	IENABLE	This pin voltage is high (5 V) when the output of the PFC stage is in steady state regulation and low at all other times. This signal serves to “inform” the backlight inverter that the PFC output is ready and that it can start operation. It can also be used as a stable 5 V reference.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Pin (pin 13) (Note 2) Voltage Range Current Range	 $V_{CC(MAX)}$ $I_{CC(MAX)}$	 −0.3 to 30 ±30	 V mA
PFC Drive Pin (pin 14) (Note 2) Voltage Range Current Range	 $V_{PDRV(MAX)}$ $I_{PDRV(MAX)}$	 −0.3 to 20 −800, +1200	 V mA
Flyback Drive Pin (pin 12) (Note 2) Voltage Range Current Range	 $V_{FDRV(MAX)}$ $I_{FDRV(MAX)}$	 −0.3 to 20 −800, +1200	 V mA
Inverter Enable Pin (pin 16) (Note 2) Voltage Range Current Range	 $V_{IENABLE(MAX)}$ $I_{IENABLE(MAX)}$	 −0.3 to 6 ±20	 V mA
Control Pin (pin 4) (Note 2) Voltage Range Current Range	 $V_{PControl(MAX)}$ $I_{PControl(MAX)}$	 −0.3 to 6 ±10	 V mA
PFC Current Sense Pin (pin 7) (Note 2) Voltage Range Current Range	 $V_{PCS(MAX)}$ $I_{PCS(MAX)}$	 −0.3 to 3 ±10	 V mA
ZCD Pin (pin 6) (Note 2) Voltage Range Current Range	 $V_{PZCD(MAX)}$ $I_{PZCD(MAX)}$	 −0.9 to 12 ±10	 V mA
All Other Pins (Note 2) Voltage Range Current Range	 V_{MAX} I_{MAX}	 −0.3 to 10 ±10	 V mA
Thermal Resistance Junction−to−Air, 100 mm^2 Single Layer of 1 oz Copper	$R_{\theta JA}$	140	°C/W
Temperature Range Storage Temperature Operating Junction Temperature	 $T_{JSTRG(MAX)}$ $T_{J(MAX)}$	 −60 to 150 −25 to 125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Charged Device Model 2000 V per JEDEC Standard JESD22-C101D
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model 200 V per JEDEC Standard JESD22−A115A
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{PFB} = 2.4 V, V_{POVUV} = 2.3 V, $V_{PControl}$ = 4 V, V_{PZCD} = 0 V, V_{PCS} = 0 V, V_{GTS} = 1 V, V_{PSKIP} = 0 V, V_{FFB} = 2.4 V, V_{FCS} = 0 V, $V_{Shutdown}$ = 0 V, $V_{IENABLE}$ = open, C_{PCT} = 1 nF, C_{PDRV} = 1 nF, C_{FDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 25°C to 125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
SUPPLY CIRCUIT						
Supply Voltage						V
Startup Threshold	V_{CC} increasing, dV/dt = 1.25 mV/μs	$V_{CC(on)}$	16	17	18	
Minimum Operating Voltage	V_{CC} decreasing, dV/dt = 125 μV/μs	$V_{CC(off)}$	8	9	10	
Internal latch reset level	V_{CC} decreasing	$V_{CC(reset)}$	5.0	6.5	8.0	
Supply Current						
PFC is switching at 70kHz	C_{FDRV} = open, C_{PDRV} = open	I_{CC1}	2.4	3.3	4.2	mA
PFC is switching at 70kHz		I_{CC2}	3.8	5.1	6.4	mA
Flyback Switching, PFC is in GTS	V_{FFB} = V_{fold} – 0.2 V, C_{FDRV} = open, V_{FCS} = 0.8 V	I_{CC3}	1.0	1.5	2.0	mA
During Faults		I_{CC4}	1.0	1.5	2.5	mA
Startup	V_{CC} = $V_{CC(on)}$ – 0.2 V	I_{CC5}	–	–	20	μA
FLYBACK FEEDBACK						
Equivalent Internal Pull–Up Resistor		R_{FFB}	14	20	31	kΩ
V_{FFB} to Internal Current Setpoint Division Ratio		K_{FFB}	4.8	5.0	5.2	
Overload Detection Filter		$t_{delay(FOVLD)}$	–	10	–	μs
Flyback Fault Timer	V_{FFB} = 4.5 V to FDRV turn–off	t_{FOVLD}	60	80	100	ms
FFB Pin Voltage	V_{FFB} = open	$V_{FFB(open)}$	4.5	5.0	5.5	V
FLYBACK CURRENT SENSE						
Current Sense Voltage Threshold	V_{FFB} = 4.5 V	V_{ILIM}	0.655	0.700	0.725	V
Leading Edge Blanking Duration		t_{LEB}	190	250	310	ns
Propagation Delay	Step V_{FCS} 0 V to 2 V, to FDRV falling edge					
Current Sense Voltage Threshold		$t_{delay(ILIM)}$	–	80	110	ns
Immediate Fault Protection		$t_{CS(stop)}$	–	80	110	ns
Immediate Fault Protection Threshold	V_{FFB} = 3 V, V_{FCS} dV/dt = 500 μV/μs	$V_{CS(stop)}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $I_{CS(stop)}$		$t_{LEB(stop)}$	90	120	150	ns
Input Bias Current	V_{FCS} = V_{ILIM}	$I_{FCS(bias)}$	–1	–	+1	μA
Current Sourced by the FCS Pin	V_{FCS} = 0 V, 80% Duty Ratio	$I_{ramp(MAX)}$	100	150	200	μA
FLYBACK SOFT–START						
Soft–Start Period	1st FDRV pulse to V_{FCS} = V_{ILIM}	t_{SSTART}	2.8	4.0	5.2	ms
OSCILLATOR						
Base Oscillator Frequency		f_{OSC}	60	65	70	kHz
Maximum Duty Ratio		D_{MAX}	76	80	84	%
Frequency Modulation in Percentage of f_{OSC}		f_{MOD}	–	±6	–	%
Frequency Modulation Frequency		f_{jitter}	–	125	–	Hz
Oscillator Frequency Voltage Stability	$V_{CC(MIN)}$ < V_{CC} < $V_{CC(MAX)}$	$f_{OSC(VSTAB)}$	–1	–	+1	%

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{PFB} = 2.4 V, V_{POVUV} = 2.3 V, $V_{PControl}$ = 4 V, V_{PZCD} = 0 V, V_{PCS} = 0 V, V_{GTS} = 1 V, V_{PSKIP} = 0 V, V_{FFB} = 2.4 V, V_{FCS} = 0 V, $V_{Shutdown}$ = 0 V, $V_{IENABLE}$ = open, C_{PCT} = 1 nF, C_{PDRV} = 1 nF, C_{FDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 25°C to 125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
FLYBACK GATE DRIVE						
FDRV Impedance Sink Source	 V_{FDRV} = 10 V V_{FDRV} = 2 V	 $R_{FDRV(SNK)}$ $R_{FDRV(SRC)}$	 – –	 12.5 14	 – –	 Ω Ω
FDRV Rise Time (10% to 90%)		$t_{FDRV(r)}$	15	30	80	ns
FDRV Fall Time (90% to 10%)		$t_{FDRV(f)}$	12	25	70	ns
FDRV Low Voltage	I_{FDRV} = 0 mA	$V_{FDRV(low)}$	–	0.06	0.5	V
FDRV Voltage Drop	$V_{CC} = V_{CC(off)}$ + 0.2 V, R_{FDRV} = 33 kΩ	$V_{FDRV(drop)}$	–	–	1	V
FDRV Clamp Voltage	V_{CC} = 30 V, I_{FDRV} = 0 mA	$V_{FDRV(clamp)}$	11	13.5	16	V
FLYBACK SKIP MODE/FREQ FOLDBACK						
Skip Threshold	V_{FFB} Decreasing	V_{FSKIP}	630	700	770	mV
Skip Comparator Hysteresis		$V_{FSKIP(HYS)}$	65	100	135	mV
Soft−Skip Duration	1st Pulse to $V_{FCS} = V_{fold}/K_{FFB}$	t_{SSKIP}	50	100	140	μs
Frequency Foldback Threshold	V_{FFB} Decreasing, dV/dt = 500 μV/μs	V_{fold}	1.26	1.40	1.54	V
Minimum Switching Frequency	$V_{FFB} = V_{FSKIP}$ + 150 mV	$f_{OSC(MIN)}$	21	26	31	kHz
Maximum On Time	Frequency Foldback or Skip Mode	$t_{on(MAX)}$	10.0	13.0	16.0	μs
PFC CURRENT SENSE						
PCS Pin Voltage	R_{PCS} = 2.5 kΩ, I_{PCS} = 265 μA	V_{PCS}	−20	0	20	mV
Overcurrent Protection Threshold	R_{PCS} = 2.5 kΩ	I_{OCP}	230	250	265	μA
Propagation Delay	step I_{PCS} 0 μA to 400 μA I_{OCP} to PDRV falling edge R_{PCS} = 1 kΩ	t_{OCP}	–	100	210	ns
PFC RAMP CONTROL						
PCT Charge Current	V_{PCT} = 1.5 V	$I_{PCT(charge)}$	189	210	231	μA
C_{PCT} Discharge Time	$V_{PControl}$ = open, $C_{PControl}$ = 10 nF $V_{PCT} = V_{PCT(MAX)}$ −100 mV to 600 mV	$t_{CPCT(discharge)}$	–	–	500	ns
Maximum PCT Level Before PDRV Switches Off	$V_{PControl}$ = open, $C_{PControl}$ = 10 nF	$V_{PCT(MAX)}$	4.7	5.0	5.3	V
Propagation Delay of the PWM Comparator	step V_{PCT} from 3.5 V to 5.0 V	t_{PWM}	–	150	200	ns
PFC Frequency Clamp		f_{clamp}	330	385	440	kHz
PFC GATE DRIVE						
PDRV Impedance Sink Source	 V_{PDRV} = 10 V V_{PDRV} = 2 V	 $R_{PDRV(SNK)}$ $R_{PDRV(SRC)}$	 – –	 12.5 14	 – –	 Ω Ω
PDRV Rise Time (10 % to 90 %)		$t_{PDRV(r)}$	15	30	80	ns
PDRV Fall Time (90 % to 10 %)		$t_{PDRV(f)}$	12	25	70	ns
PDRV Low Voltage	I_{PDRV} = 0 mA	$V_{PDRV(low)}$	–	0.06	0.5	V
PDRV Voltage Drop	$V_{CC} = V_{CC(off)}$ + 0.2 V, R_{PDRV} = 33 kΩ	$V_{PDRV(drop)}$	–	–	1	V
PDRV Clamp Voltage	V_{CC} = 30 V, I_{PDRV} = 0 mA	$V_{PDRV(clamp)}$	11	13.5	16	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{PFB} = 2.4 V, V_{POVUV} = 2.3 V, $V_{PControl}$ = 4 V, V_{PZCD} = 0 V, V_{PCS} = 0 V, V_{GTS} = 1 V, V_{PSKIP} = 0 V, V_{FFB} = 2.4 V, V_{FCS} = 0 V, $V_{Shutdown}$ = 0 V, $V_{IENABLE}$ = open, C_{PCT} = 1 nF, C_{PDRV} = 1 nF, C_{FDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 25°C to 125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
PFC ZERO CURRENT DETECTION						
Zero Current Detection Threshold Rising Falling		 $V_{ZCD(rising)}$ $V_{ZCD(falling)}$	 1.12 0.56	 1.40 0.70	 1.68 0.84	V
Hysteresis on Voltage Threshold	$V_{ZCD(rising)} - V_{ZCD(falling)}$	$V_{ZCD(HYS)}$	560	700	840	mV
Propagation Delay	Step V_{PZCD} from 2 V to 0 V	t_{ZCD}	–	100	170	ns
Clamp Voltage Upper Clamp Negative Clamp	 I_{PZCD} = 3 mA I_{PZCD} = –2 mA	 $V_{CL(POS)}$ $V_{CL(NEG)}$	 8 –0.9	 10 –0.7	 12 0	V
Minimum detectable ZCD pulse width		t_{SYNC}	–	70	100	ns
Maximum Off Time	PDRV off = 10% to PDRV on = 90%	t_{start}	75	180	300	μs
Input Bias Current	V_{PZCD} = 5 V V_{PZCD} = –0.2 V	$I_{PZCD(bias)}$ $I_{PZCD(bias)}$	–2 –2	– –	2 2	μA μA
PFC SKIP MODE						
Skip Pin Internal Current Source		I_{PSKIP}	27	30	33	μA
Hysteresis of the skip cycle detection level	V_{PSKIP} = 1 V	$V_{PSKIP(HYS)}$	10	12	16	%
PFC REGULATION BLOCK						
Voltage Reference		V_{REF}	2.463	2.500	2.537	V
Error Amplifier Current Capability Maximum Source Current Maximum Sink Current	 V_{PFB} = 2.4 V, V_{POVUV} = 3 V V_{PFB} = 2.6 V, V_{POVUV} = 3 V	 $I_{EA(SRC)}$ $I_{EA(SNK)}$	 16 16	 20 20	 24 24	 μA μA
Error Amplifier Transconductance	V_{PFB} = V_{REF} ± 100 mV, V_{POVUV} = 3 V	gm	100	200	300	μS
PFB Bias Current	V_{PFB} = 2.5 V	$I_{PFB(bias)}$	–0.5	–	0.5	μA
Maximum EA Output Voltage	V_{PFB} = 2 V $V_{PControl}$ = open, $C_{PControl}$ = 10 nF	$V_{PControl(MAX)}$	5.05	5.6	6.1	V
Minimum EA Output Voltage	V_{PFB} = 3 V $V_{PControl}$ = open, $C_{PControl}$ = 10 nF	$V_{PControl(MIN)}$	0.35	0.6	0.8	V
EA Output Regulation Voltage Swing	$V_{PControl(MAX)} - V_{PControl(MIN)}$	$\Delta V_{PControl}$	4.7	5.0	5.3	V
Ratio (V_{out} Low Detect Threshold / V_{REF})		V_{OLOW}/V_{REF}	95.0	95.5	96.0	%
V_{out} Low Detect / V_{REF} Hysteresis		$V_{OLOW(HYS)}/V_{REF}$	–	–	1.0	%
Source Current During V_{OUT} Low Detect		$I_{PControl(boost)}$	190	240	290	μA
GO TO STANDBY (GTS)						
Internal Pull–Down Resistor		R_{GTS}	80	200	320	kΩ
Standby Threshold	V_{GTS} Decreasing	$V_{standby}$	270	300	330	mV
Standby Hysteresis		$V_{standby(HYS)}$	85	100	125	mV
Go To Standby Timer	Step V_{GTS} from 1 V to 0 V Step V_{GTS} from 0 V to 1 V	$t_{GTS(off)}$ $t_{GTS(on)}$	37.5 30	50.0 50	62.5 70	ms μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{PFB} = 2.4 V, V_{POVUV} = 2.3 V, $V_{PControl}$ = 4 V, V_{PZCD} = 0 V, V_{PCS} = 0 V, V_{GTS} = 1 V, V_{PSKIP} = 0 V, V_{FFB} = 2.4 V, V_{FCS} = 0 V, $V_{Shutdown}$ = 0 V, $V_{IENABLE}$ = open, C_{PCT} = 1 nF, C_{PDRV} = 1 nF, C_{FDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 25°C to 125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
PFC FAULT PROTECTION						
Overvoltage Protection Threshold		V_{OVP}	2.450	2.500	2.550	V
Overvoltage Protection Hysteresis		$V_{OVP(HYS)}$	20	40	60	mV
Overvoltage Protection Filter Delay		$t_{delay(OVP)}$	–	30	–	μs
Undervoltage Protection Threshold		V_{UVP}	285	300	315	mV
Undervoltage Protection Hysteresis		$V_{UVP(HYS)}$	20	40	60	mV
Undervoltage Protection Filter Delay		$t_{delay(UVP)}$	–	30	–	μs
UVP Pull Down Current Source		I_{UVP}	0.7	1.0	1.3	μA
Ratio Between V_{OVP} and V_{REF} (Note 3)		V_{OVP}/V_{REF}	99.5	100.0	100.5	%
INVERTER ENABLE/REFERENCE						
Disable Threshold		$V_{disable}$	1.809	1.865	1.921	V
Disable Filter Delay		$t_{delay(disable)}$	–	30	–	μs
Voltage Reference	$I_{IENABLE(SRC)}$ = 8 mA $I_{IENABLE(SRC)}$ = 1 mA $I_{IENABLE(SNK)}$ = 250 μA	$V_{IENABLE(high)}$ $V_{IENABLE(high)}$ $V_{IENABLE(low)}$	4.5 4.7 –	5.0 5.0 60	5.4 5.4 120	V V mV
Reference Pin Decoupling Capacitor		C_{REF}	0	–	1	μF
THERMAL PROTECTION						
Thermal Shutdown		T_{TSHDN}	–	150	–	°C
Thermal Shutdown Delay		$t_{delay(TSHDN)}$	–	30	–	μs
SHUTDOWN PIN						
Shutdown Threshold	$V_{Shutdown}$ Increasing	V_{SHDN}	0.90	1.00	1.10	V
Shutdown Filter Delay	$V_{Shutdown}$ Increasing	$t_{delay(SHDN)}$	–	30	–	μs
Pull Up Current Source		$I_{Shutdown}$	2.3	3.3	4.3	μA

3. Guaranteed by design

DETAILED OPERATING DESCRIPTION

INTRODUCTION

The NCP1927 is a combination power factor correction (PFC) and flyback controller optimized for use in Flat Panel TVs. This device includes all the features needed to implement a highly efficient and compact power supply. It integrates a critical conduction mode (CrM) PFC controller and a fixed−frequency current mode flyback controller with proper sequencing for simplified system design.

This device includes frequency jittering, a shutdown input, an inverter enable output, a go to standby input, and a dedicated pin for under/overvoltage protection.

SUPPLY SEQUENCING

The flyback controller of the NCP1927 is enabled once V_{CC} reaches $V_{CC(on)}$, provided it is not in thermal shutdown and has not been latched off or shutdown. Once the flyback controller is enabled, a soft−start timer is activated, and it begins switching. The soft−start timer provides a ramp signal that increases over t_{SSTART} (typically 4.0 ms). This ensures that the peak current gradually increases to minimize power component stress and limit output voltage overshoot. Frequency jittering is disabled while the soft−start timer is running.

Once the flyback controller detects regulation on the output (it is no longer in overload), the PFC controller can be enabled. As soon as the PFC controller is enabled, the error amplifier begins to source its maximum output current, $I_{EA(MAX)}$, (typically 20 μA) to linearly charge the PControl pin capacitor ($C_{PControl}$). Soft−start is achieved as $C_{PControl}$ charges. An internal grounding switch on the PControl pin is turned on each time the PFC controller is disabled, and turned off when it is enabled. This ensures that $C_{PControl}$ is always fully discharged at the beginning of soft−start.

As the PFC stage approaches regulation on the output, the error amplifier output current, I_{EA}, gradually reduces to 0 μA. Once the output is in regulation and I_{EA} reaches 0 μA, the IENABLE pin is set to $V_{IENABLE(high)}$ (typically 5 V).

V_{CC} MANAGEMENT

When power is initially applied to the application, the V_{CC} capacitor (C_{VCC}) begins charging through a resistor connected to the high voltage line (V_{in}). The resistor value must be chosen so that the charging current is greater than the IC bias current during startup. The maximum value for the startup resistor is calculated using Equation 1.

$$R_{start} = \frac{V_{in}}{I_{CC5}} \qquad \text{(eq. 1)}$$

where V_{in} is the rectified dc input voltage and I_{CC5} is the IC bias current during startup (20 μA maximum).

When V_{CC} reaches $V_{CC(reset)}$ (typically 6.5 V), a Power On Reset occurs. This resets all logic states on the device. As V_{CC} continues to rise, the IC bias current remains at I_{CC5} until V_{CC} reaches $V_{CC(on)}$ (typically 17 V). Once V_{CC} reaches $V_{CC(on)}$, the flyback controller is enabled and the IC bias current increases to I_{CC3} (1.5 mA typical). However, the total I_{CC} current is greater than this due to the gate charge load at the flyback drive output (FDRV). Once the flyback is in regulation, the PFC controller can be enabled. When the PFC is enabled, the I_{CC} current increases further due to the gate charge load at the PFC drive output (PDRV). The increase in I_{CC} per MOSFET is calculated using Equation 2.

$$I_{CC(x)} = f_{OSC} \cdot Q_{G(x)} \qquad \text{(eq. 2)}$$

where, f_{OSC} is the switching frequency and $Q_{G(X)}$ is the gate charge of the external MOSFET *X*.

C_{VCC} must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ (9 V typical) is maintained while the auxiliary supply voltage increases during startup. If C_{VCC} is too small, V_{CC} falls below $V_{CC(off)}$ and the controller turns off before the auxiliary winding powers up the controller. The total I_{CC} current after the flyback controller is enabled (I_{CC3} plus $I_{CC(FDRV)}$) must be considered to correctly size C_{VCC}. It is often useful to connect a small V_{CC} capacitor (C1) directly to the V_{CC} pin, while a larger capacitor (C2) is connected to the V_{CC} pin through a diode and charged by the aux winding. This allows minimum startup time while providing enough V_{CC} capacitance to operate during light load conditions. This implementation is shown in Figure 3 and the startup sequence is shown in Figure 4.

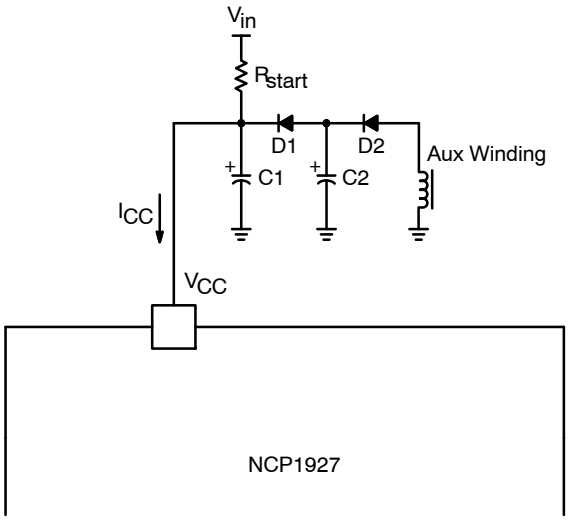


Figure 3. Operation with Dual V_{CC} Capacitors

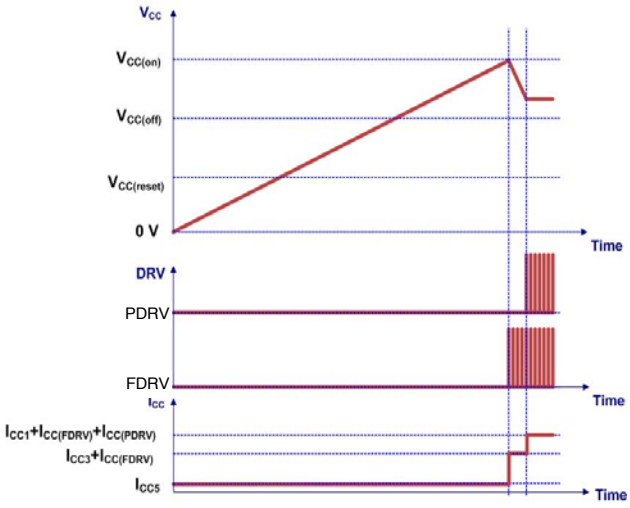


Figure 4. Startup Sequence of the NCP1927

FAULT MANAGEMENT

When the NCP1927 detects a non−latching fault (Shutdown Mode, TSD, and Flyback Overload), the drivers are disabled, and V_{CC} falls towards $V_{CC(off)}$ due to the IC internal current consumption. Once V_{CC} falls below $V_{CC(off)}$, the fault is reset and the IC internal current consumption is reduced to the startup current, I_{CC5}. V_{CC} begins to rise as if power was initially applied and the device resumes normal operation once V_{CC} reaches $V_{CC(on)}$. This cycle between $V_{CC(on)}$ and $V_{CC(off)}$ is commonly referred to as a V_{CC} hiccup and is shown in Figure 5.

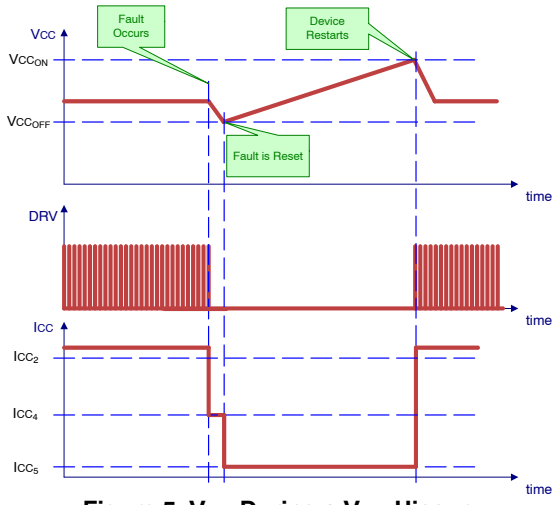


Figure 5. V_{CC} During a V_{CC} Hiccup

SHUTDOWN PIN

The Shutdown pin allows for external disabling of the NCP1927. When $V_{Shutdown}$ is pulled above the shutdown threshold, V_{SHDN} (typically 1.0 V), both the flyback and PFC drive outputs are immediately turned off, and a V_{CC} hiccup occurs (see Figure 5). When V_{CC} reaches $V_{CC(on)}$, the cycle repeats unless the NCP1927 is taken out of shutdown. This is achieved when $V_{Shutdown}$ becomes less than V_{SHDN}. The NCP1927 leaves shutdown mode and will start when V_{CC} reaches $V_{CC(on)}$ according to the initial power−on sequence. The V_{CC} behavior during shutdown mode is shown in Figure 6.

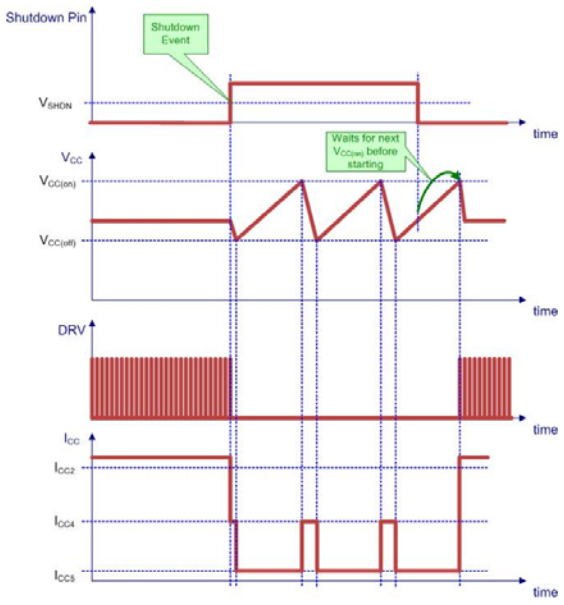


Figure 6. V_{CC} Behavior During Shutdown Mode

THERMAL SHUTDOWN

When the junction temperature exceeds T_{TSHDN} (140°C minimum), a temperature sensing circuit disables the gate drives and a V_{CC} hiccup occurs (see Figure 5). When V_{CC} reaches $V_{CC(on)}$, the cycle repeats unless the junction temperature drops below T_{TSHDN}.

CLAMPED DRIVERS

The NCP1927 includes two powerful MOSFET drivers capable of sourcing 800 mA and sinking 1200 mA each. Since V_{CC} is rated at 30 V (maximum), each driver output is internally clamped to 16 V (maximum) to allow the use of 20 V MOSFETs.

FLYBACK CONTROLLER

The NCP1927 flyback stage implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint.

Oscillator with Maximum Duty Ratio and Frequency Jittering

The NCP1927 flyback controller includes an oscillator that sets the switching frequency with an accuracy of ±7.7%. The maximum duty ratio of the FDRV pin is 80% (typical).

In order to improve the EMI signature, the switching frequency jitters at f_{MOD} (±6% typical) around its nominal value, with a triangle−wave shape and at a frequency of f_{jitter} (125 Hz typical). The frequency jittering is fully disabled during soft−start and frequency foldback. Figure 7 depicts the jittering operation.

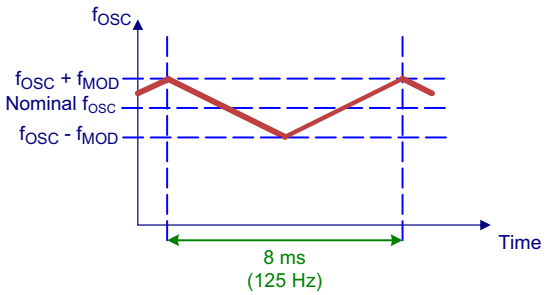


Figure 7. Frequency Jittering

Current Sensing

NCP1927 is a current−mode controller, which means that the feedback voltage sets the peak current flowing in the transformer and the MOSFET. This is done through the PWM comparator. The switch current is sensed across a resistor and the resulting voltage is applied to the FCS pin. It is then applied to one input of the PWM comparator through a 250 ns leading edge blanking (LEB) block. On the other input, the feedback voltage divided by K_{FFB} (typically 5) sets the current limit threshold. When the current reaches this threshold, the output driver is turned off. A dedicated comparator monitors the current sense voltage, and if it reaches the maximum value, V_{ILIM} (typically 0.7 V), the output driver is turned off immediately. This occurs even if the limit imposed by the feedback voltage is higher than V_{ILIM}. Figure 8 shows the schematic of the current sense circuit.

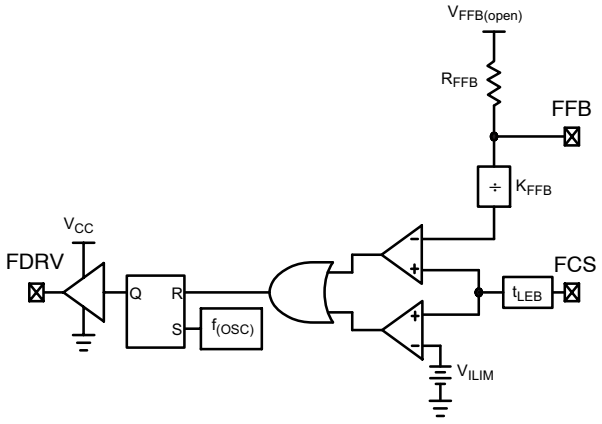


Figure 8. Current Sense Block Schematic

Short−Winding Protection

Under some conditions, like a transformer winding or output diode short−circuit, the primary current increases above V_{ILIM} before the LEB timer expires. To prevent dangerously high current from flowing, an additional comparator senses when V_{FCS} reaches $V_{CS(stop)}$. Once this comparator toggles, the controller immediately latches off.

The effect of latching off the IC is identical to shutdown mode, however, the V_{CC} cycle repeats indefinitely until the input power is removed and C_{VCC} is allowed to discharge below $V_{CC(reset)}$. When input power is reapplied, the NCP1927 operates according to the initial power−on sequence. The V_{CC} behavior during short winding protection is shown in Figure 9.

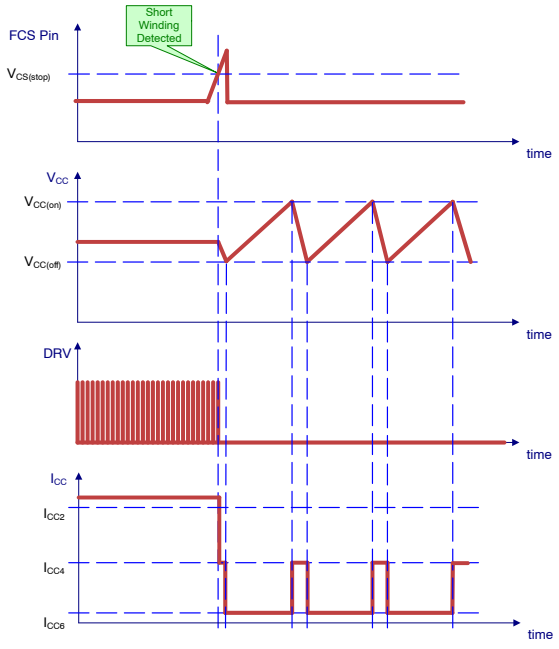


Figure 9. V_{CC} Behavior During Short Winding Protection

Feedback

The ratio from the feedback voltage to the current limit threshold, K_{FFB} (typically 5), determines the peak current limit threshold. This means that the feedback voltage when the current limit threshold equals V_{ILIM} is 3.5 V (typical).

The FFB pin is connected to the internal V_{DD} rail through a resistor divider. To ease system design, the FFB pin is represented by a Thevenin equivalent circuit containing a voltage source and series resistor, $V_{FFB(open)}$ (typically 5 V) and R_{FFB} (typically 20 kΩ).

Soft−Start

The NCP1927 flyback controller features an internal soft−start circuit. Every time the controller starts (i.e. the controller was off and starts, or restarts due to a fault), a soft−start is applied when V_{CC} reaches $V_{CC(on)}$. The current limit threshold is linearly increased from 0 until it reaches V_{ILIM} (in 4.0 ms), or until the feedback loop imposes a setpoint lower than the one imposed by the soft−start (the 2 comparator outputs are OR'ed together). Figure 10 shows a typical startup sequence.

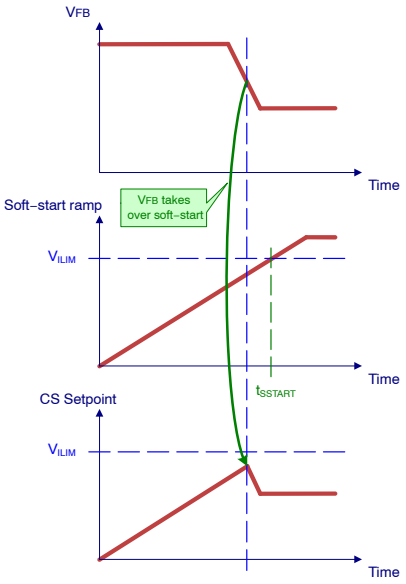


Figure 10. Soft−Start Timing

Ramp Compensation

Ramp compensation is a known method for preventing subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during continuous conduction mode (CCM) when the duty ratio is greater than 50%. To prevent these oscillations, one typically lowers the current loop gain by injecting between 50% and 75% of the inductor downslope. This is done by inserting a resistor (R_{SCOMP}) between the FCS pin and the current sense resistor. Figure 11 shows an example of this. The ramp signal is disconnected from the FCS pin during the off time.

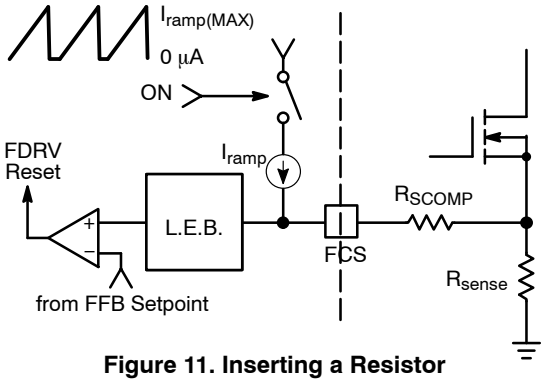


Figure 11. Inserting a Resistor

When calculating the proper value for R_{SCOMP}, it is necessary to express the internal ramp signal in terms of its slope (dI_{OSC}/dt). This is done using Equation 3.

$$\frac{dI_{OSC}}{dt} = \frac{I_{ramp(MAX)} \cdot f_{OSC}}{D_{MAX}} \quad \text{(eq. 3)}$$

The inductor downslope ($dV_{P(off)}/dt$) projected across the current sense resistor (R_{sense}) is then calculated using Equation 4.

$$\frac{dV_{P(off)}}{dt} = R_{sense} \cdot \frac{(V_{out} + V_D) \cdot \frac{N_S}{N_P}}{L_P} \quad \text{(eq. 4)}$$

where V_D is the forward drop of the output rectifier, N_S/N_P is the turns ratio, and L_P is the primary inductance.

Using the results from Equations 3 and 4, R_{SCOMP} can be calculated using Equation 5.

$$R_{SCOMP} = \frac{\alpha \cdot \frac{dV_{P(off)}}{dt}}{\frac{dI_{OSC}}{dt}} \quad \text{(eq. 5)}$$

where α is the percentage of $dV_{P(off)}/dt$ to be injected.

Overload Protection with Fault Timer

When an overload occurs on the output of the power supply, the feedback loop asks for more power than the controller can deliver, and the current limit threshold reaches V_{ILIM}. When this event occurs, a fault timer (t_{FOVLD}) is enabled.

When the timer expires, FDRV pulses are stopped, the PFC is disabled, and a V_{CC} hiccup occurs. When V_{CC} reaches $V_{CC(on)}$, the controller starts according to the initial power−on sequence. If the overload is still present, the fault timer continues to run and the cycle repeats when it expires. The fault timer is reset if the current limit threshold goes back below V_{ILIM}. A short delay, $t_{delay(FOVLD)}$, is added to prevent the fault timer from resetting due to noise. This autorecovery operation is depicted in Figure 12.

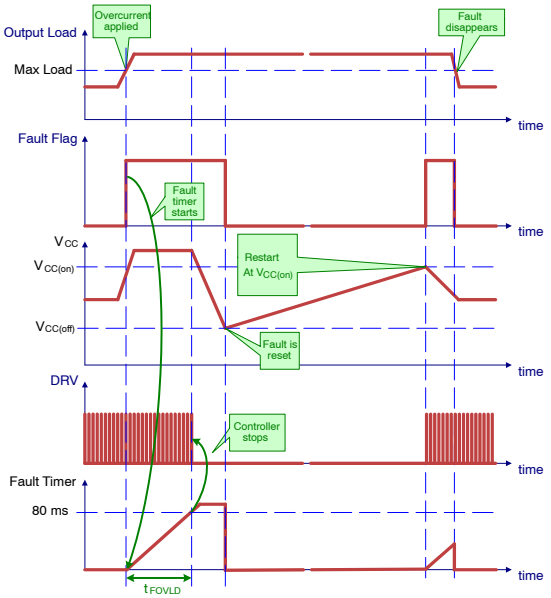


Figure 12. Operation During Overload

Frequency Foldback

In order to improve the efficiency at light load conditions, the frequency of the internal oscillator is linearly reduced from its nominal value down to $f_{OSC(MIN)}$ (typically 26 kHz). The frequency foldback starts when the voltage on the FFB pin goes below V_{fold}, and is completed before V_{FFB} reaches V_{FSKIP}. The current−mode control remains active while the oscillator frequency decreases. This is shown in Figure 13.

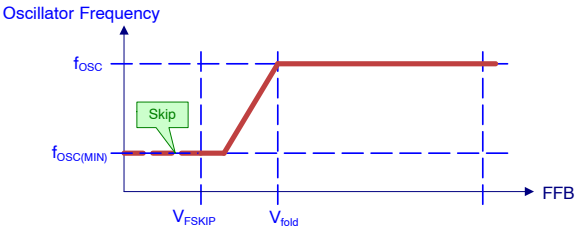


Figure 13. Switching Frequency as V_{FFB} Decreases

Skip Cycle Mode with Soft−Skip

When the feedback voltage reaches V_{FSKIP} while decreasing, skip mode is activated and the driver stops switching. While the driver is disabled, V_{FFB} begins to rise. As soon as V_{FFB} rises above V_{FSKIP} + $V_{FSKIP(HYS)}$, the driver starts to switch again, but the duty ratio is gradually increased from nearly 0% over a short Soft−Skip duration (t_{SSKIP}). This is accomplished by comparing the current

sense signal to an internal ramp generated by the Soft−Skip timer instead of the feedback voltage. Since the LEB of the FCS Pin prevents operation at nearly 0% duty ratio, the controller instead compares the soft−skip ramp to an internal sawtooth signal generated by the oscillator (not subjected to LEB). This causes the controller to operate briefly in voltage mode instead of current mode. Once the CS signal reaches the feedback voltage, the controller resumes normal operation in current mode. The skip mode block diagram is shown in Figure 14. The ramp timing and overall timing diagrams are shown in Figures 15 and 16.

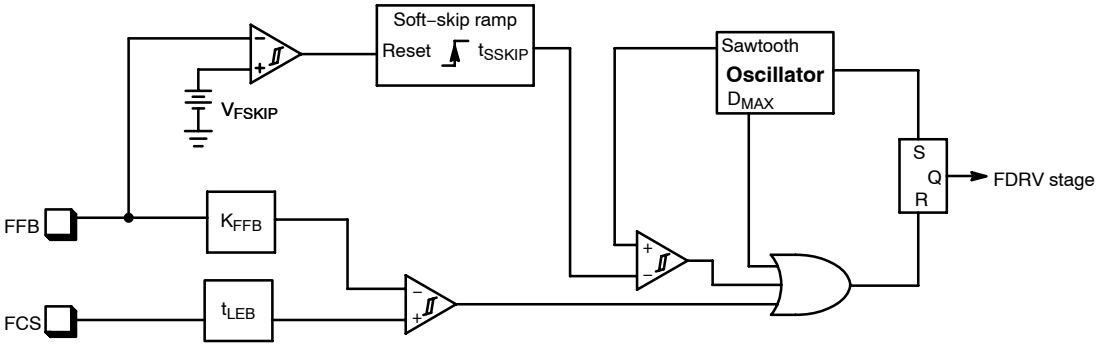


Figure 14. Skip Cycle with Soft−Skip Architecture

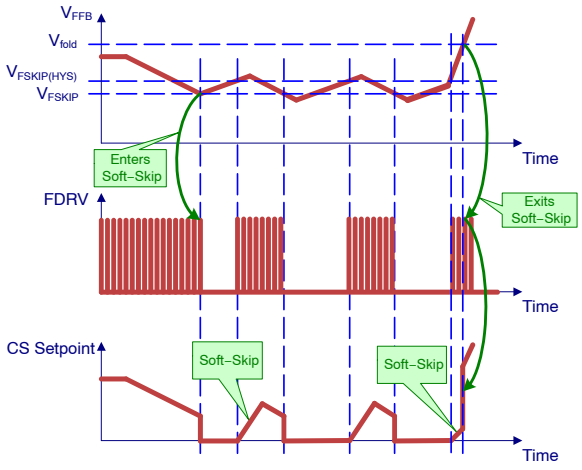


Figure 15. Skip Cycle with Soft−Skip Timing Diagram

During the Soft−Skip duration if the feedback voltage goes above V_{fold}, the Soft−Skip ends instantaneously allowing the controller to operate in current mode.

This transient load detection feature avoids large output drops if a load transient occurs while the controller is in skip mode.

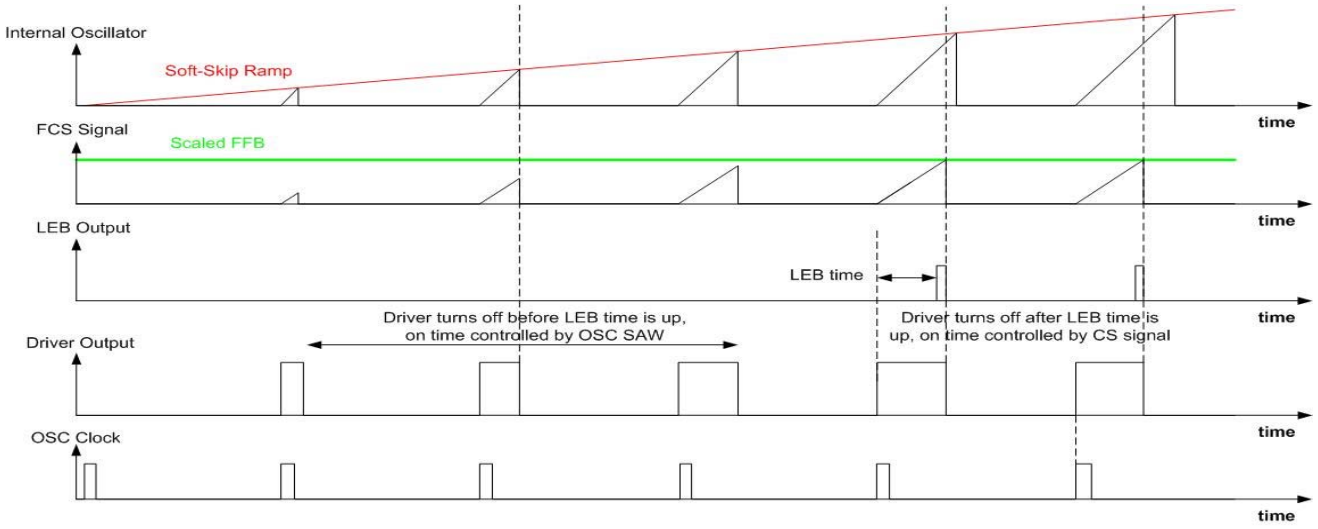


Figure 16. Soft−Skip Timing Diagram

PFC CONTROLLER

The PFC stage operates in critical conduction mode (CrM). CrM occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CrM, the driver on time is initiated when the boost inductor current reaches zero. CrM operation is an ideal choice for medium power PFC boost stages because it combines the lower peak currents of CCM operation with the zero current switching of DCM operation. The operation and waveforms in a PFC boost converter are illustrated in Figure 17.

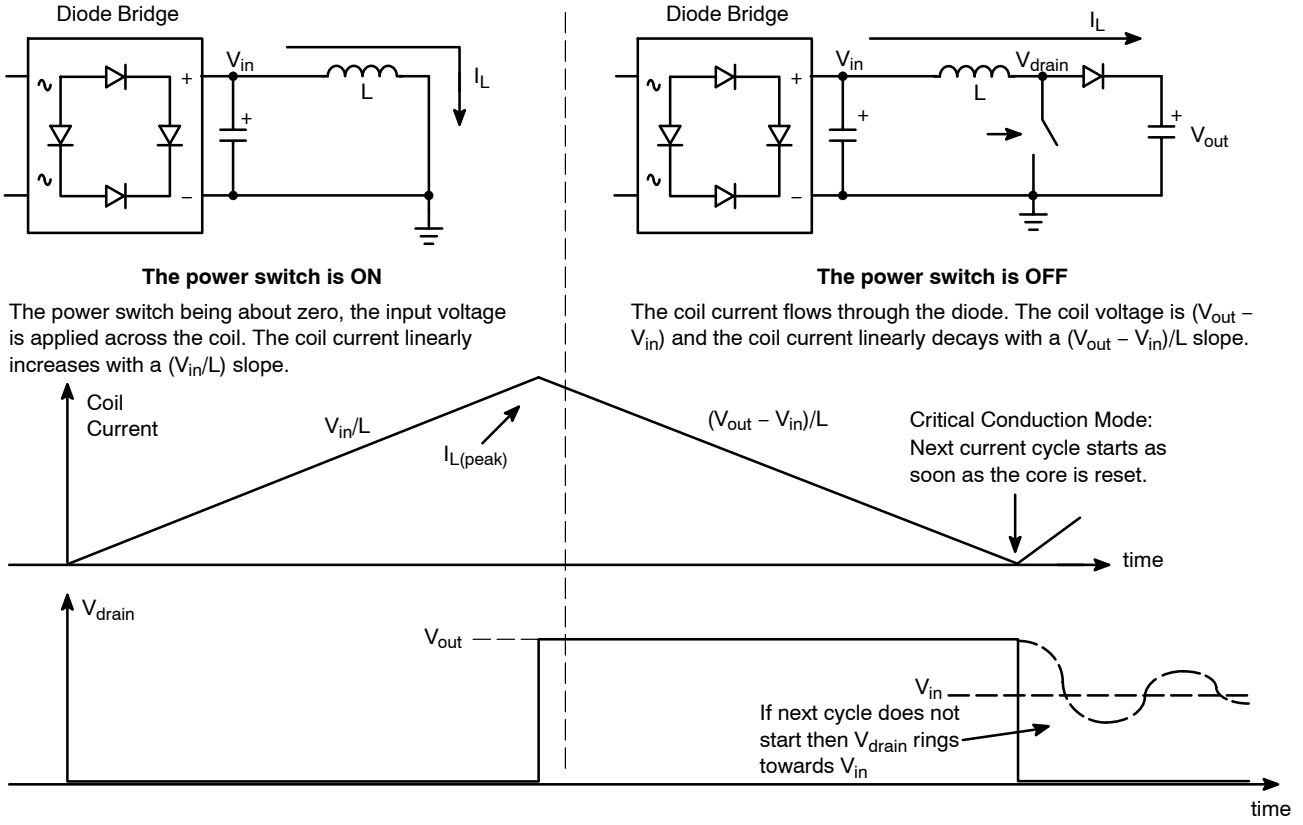


Figure 17. Schematic and Waveforms of an Ideal CrM Boost Converter

When the switch is closed, the inductor current increases linearly to its peak value. When the switch opens, the inductor current linearly decreases to zero. At this point, the drain voltage of the switch (V_{drain}) begins to drop. If the next switching cycle does not start, the voltage rings with a dampened frequency around Vin. A simple derivation of equations (such as those found in AND8123) leads to the result that good power factor correction in CrM operation is achieved when the on time is constant across a single ac cycle. Equation 6 shows the relationship between on time and system operating conditions.

$$t_{on} = \frac{2 \cdot P_{out} \cdot L}{\eta \cdot Vac^2} \qquad \text{(eq. 6)}$$

where P_{out} is the output power, L is the boost inductor inductance and η is the system efficiency.

A plot of the MOSFET on/off time over an ac line cycle is illustrated in Figure 18. The MOSFET off time varies based on the instantaneous line voltage, but the on time is constant. This causes the peak inductor current ($I_{L(peak)}$) to follow the ac line voltage. The NCP1927 implements constant on time CrM control in a cost−effective and robust manner.

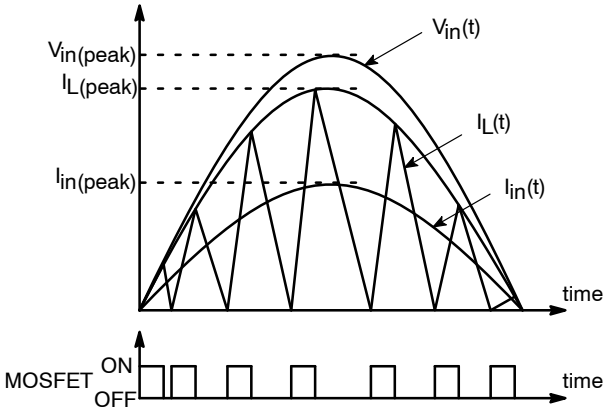


Figure 18. Inductor Waveform During CrM Operation

Output Regulation

The NCP1927 error amplifier (EA) consists of an operational transconductance amplifier (OTA) with the inverting input connected to the PFB pin and the output connected to the PControl pin to regulate the output voltage. It features a typical transconductance (gm) of 200 μS and a maximum output ($I_{EA(SRC)}$ and $I_{EA(SNK)}$) of ±20 μA (typical). The non−inverting input is connected internally to a voltage reference (V_{REF}) with a typical value of 2.5 V ±1.5% over process and temperature. During normal operation, the voltage on the PControl pin varies between $V_{PControl(MIN)}$ (typically 0.6 V) and $V_{PControl(MAX)}$ (typically 5.6 V). A simplified diagram of the OTA circuit is shown in Figure 19.

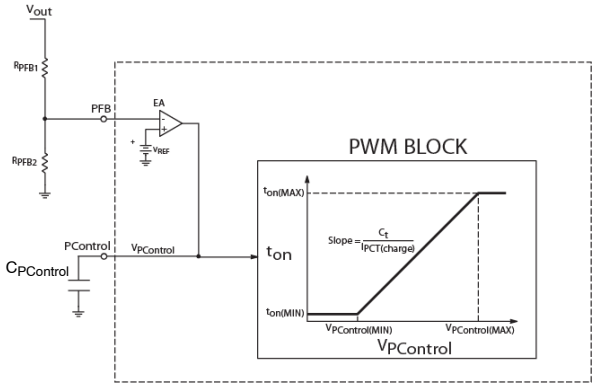


Figure 19. Error Amplifier and On Time Regulation Circuits

A resistor divider from the boost output to the PFB pin provides a scaled−down representation of the output voltage (V_{out}) to the EA. When V_{out} is in regulation, V_{PFB} equals V_{REF}. If V_{out} drops below regulation, the feedback voltage (V_{PFB}) drops and the EA sources current until V_{PFB} returns towards V_{REF}. This increases the control voltage ($V_{PControl}$) and the on time of the driver (t_{on}), which in turn increases the power delivered to the load and brings V_{out} back into regulation. Alternatively, if V_{out} (and also V_{PFB}) is too high, the EA sinks current and $V_{PControl}$ decreases, thus shortening t_{on} until V_{out} returns to regulation. The output voltage is calculated using Equation 7.

$$V_{out} = V_{REF} \cdot \frac{R_{PFB1} + R_{PFB2}}{R_{PFB2}} \qquad \text{(eq. 7)}$$

where R_{PFB1} is the upper resistor of the resistor divider, and R_{PFB2} is the lower resistor.

The impedance of the feedback network determines its noise immunity and power dissipation. While a lower impedance provides better noise immunity, it also increases power dissipation. Once the divider current is chosen, R_{PFB1} is determined using Equation 8.

$$R_{PFB1} = \frac{V_{out}}{I_{divider}} \qquad \text{(eq. 8)}$$

where $I_{divider}$ is the resistor divider current.

Using R_{PFB1}, R_{PFB2} is calculated with Equation 9.

$$R_{PFB2} = \frac{R_{PFB1} \cdot V_{REF}}{V_{out} - V_{REF}} \qquad \text{(eq. 9)}$$

Compensation

A compensation network must be connected between the PControl pin and ground due to the nature of an active PFC circuit. The PFC stage generates a sinusoidal current from the ac line voltage and provides the load with a power that matches the average demand. When the input voltage is at its peak, the PFC stage delivers more power than the load requires, and the output capacitor charges. Conversely, when the input voltage is at a valley, the load requires more power than the PFC stage can deliver, and the output capacitor discharges. The situation is depicted in Figure 20.

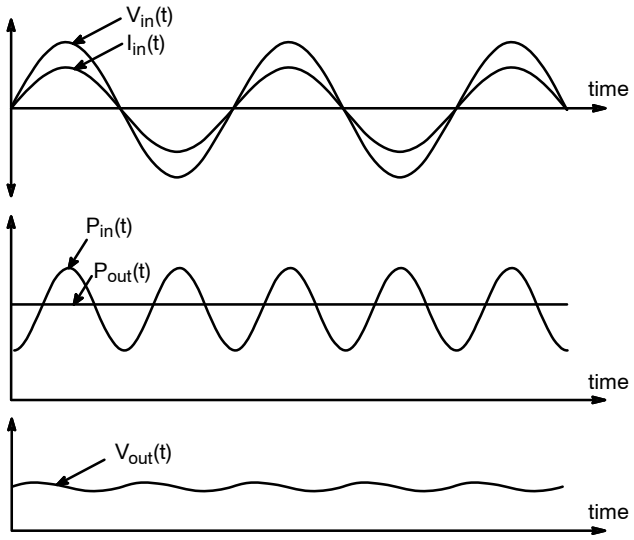


Figure 20. Output Voltage Ripple for a Constant Output Power

This creates a ripple on the output with frequency equal to twice the line frequency (f_{line}). Since the on time must remain constant during each ac line cycle to maintain good power factor correction, the EA must reject the output ripple. This is commonly achieved by setting the regulation bandwidth below 20 Hz. A type 1 compensation network is typically used for simplicity, as it only requires a single capacitor ($C_{PControl}$) connected between the PControl pin and ground (see Figure 19). For a type 1 network, $C_{PControl}$ is calculated using Equation 10.

$$C_{PControl} = \frac{gm}{2\pi \cdot f_c} \qquad \text{(eq. 10)}$$

where gm is the transconductance of the EA (typically 200 μS), and f_c is the desired crossover frequency (typically less than 20 Hz).

Transient Load Detection

Due to the low bandwidth of the regulation loop, fast load transients may result in output voltage over and undershoots. Overshoots are limited by the overvoltage protection (see OVP section). To control the undershoots, an internal comparator monitors the ratio between V_{PFB} and V_{REF}. When it is lower than V_{OLOW}/V_{REF} (95.5% typical), $I_{PControl(boost)}$ (240 μA typical) is connected to the PControl pin to speed up the charging of $C_{PControl}$. This has the effect of increasing the EA gain by a factor of approximately 13.

The transient load detection circuit is disabled during the startup sequence of the PFC stage to prevent it from interfering with the operation of the soft−start circuit.

On Time Control

Since the NCP1927 is designed to control a CrM boost converter, the switching pattern consists of constant on times and variable off times. The on time is set via an external capacitor (C_t) connected to the PCT pin. At the beginning of each switching cycle, C_t is charged linearly by $I_{PCT(charge)}$ (210 μA typical). An internal comparator monitors the voltage on the PCT pin (V_{PCT}) and compares it to an internal regulation limit set by $V_{PControl}$. The internal limit is determined by shifting $V_{PControl}$ down by a voltage equal to one diode drop (0.6 V typical) to account for the offset of the control voltage range. Once this level is exceeded, the drive is turned off. C_t is then discharged within $t_{CPCT(discharge)}$ (maximum 500 ns) and held low until the beginning of the next switching cycle. This sequence is shown in Figure 21.

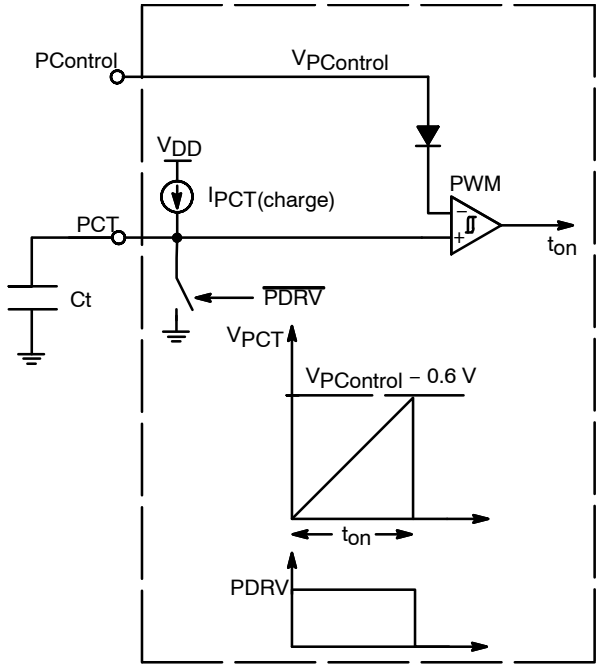


Figure 21. On Time Generation

Since $V_{PControl}$ varies with the RMS line voltage and output load, this naturally satisfies Equation 6. If the values of compensation components are sufficient to filter out the bulk capacitor voltage ripple, the on time remains constant over the entire ac line cycle.

The maximum on time of the controller occurs when $V_{PControl}$ is at its maximum value. Therefore, C_t must be sized to ensure that the required on time can be achieved at maximum output power and minimum input voltage. The maximum on time is calculated using Equation 11.

$$t_{on(MAX)} = \frac{C_t \cdot V_{PCT(MAX)}}{I_{PCT(charge)}} \qquad \text{(eq. 11)}$$

where $V_{PCT(MAX)}$ = 5 V (typical) and $I_{PCT(charge)}$ = 210 μA (typical).

Combining Equation 11 with Equation 6, results in Equation 12.

$$C_t = \frac{2 \cdot P_{out} \cdot L \cdot I_{PCT(charge)}}{\eta \cdot Vac_{LL}^{\,2} \cdot V_{PCT(MAX)}} \qquad \text{(eq. 12)}$$

Where, Vac_{LL} is the minimum ac rms input voltage.

Off Time Control

The off time varies with the instantaneous line voltage and is adjusted every cycle so that the inductor is demagnetized before the next switching cycle begins. The inductor is demagnetized once its current reaches zero. When this happens, the drain voltage begins to drop. This is detected by sensing the voltage across an inductor auxiliary winding. This winding, commonly known as a zero crossing detection (ZCD) winding, provides the NCP1927 with a scaled version of the inductor voltage. Figure 22 shows a typical ZCD winding arrangement.

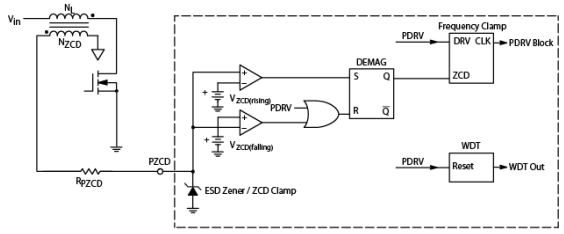


Figure 22. ZCD Winding Implementation

While the switch is on, a negative voltage appears at the PZCD pin. When the switch turns off, the ZCD voltage swings positive, arming the ZCD detector. The ZCD voltage remains positive until the inductor current falls to zero and the inductor is demagnetized. The voltage then drops to 0 V and triggers the ZCD detector to begin the next switch cycle. The arming threshold of the ZCD detector is typically 1.4 V ($V_{ZCD(rising)}$) and the triggering threshold is typically 0.7 V ($V_{ZCD(falling)}$).

The PZCD pin is internally clamped to $V_{CL(POS)}$ (typically 10 V) and $V_{CL(NEG)}$ (typically −0.7 V). A resistor in series with the PZCD pin is required to limit the current into the pin and prevent it from exceeding 3 mA at $V_{CL(POS)}$ or −2 mA at $V_{CL(NEG)}$. Figure 23 shows typical ZCD waveforms.

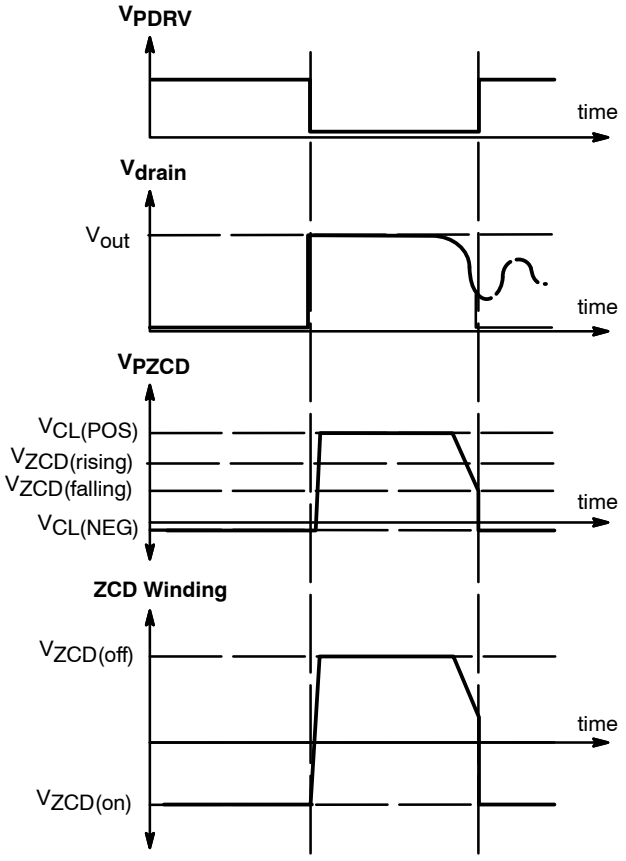


Figure 23. Voltage Waveforms for Zero Current Detection

During startup, there are no ZCD transitions to enable the PFC switch. A watchdog timer, t_{start}, enables the PFC driver when no switch pulses are detected before it times out (180 μs typical). The watchdog timer is also useful while operating at light load because the amplitude of the ZCD signal may be too small to cross the ZCD thresholds.

Frequency Clamp

Since the NCP1927 operates in CrM mode over the ac line half cycle, the switching frequency naturally increases as the line voltage approaches zero. In order to minimize the PFC inductor size, the NCP1927 features an internal oscillator that clamps the maximum switching frequency to f_{clamp} (typically 385 kHz).

Overvoltage/Undervoltage Protection

The low bandwidth of the PFC stage feedback network causes it to have a slow transient response. This increases the risk of overshoots during transient conditions (startup, load steps, etc.). For safe operation, overvoltage protection (OVP) is utilized to prevent the output voltage from rising too high and overstressing the power stage components. The NCP1927 detects high V_{out} levels and disables the driver until the output voltage returns to nominal levels. This protection keeps the output voltage within an acceptable range.

While traditional PFC controllers often use one single pin for both under/overvoltage protections and feedback, the NCP1927 uses a dedicated pin for undervoltage protection (UVP) and OVP. This configuration allows the implementation of two separate feedback networks as shown in Figure 24.

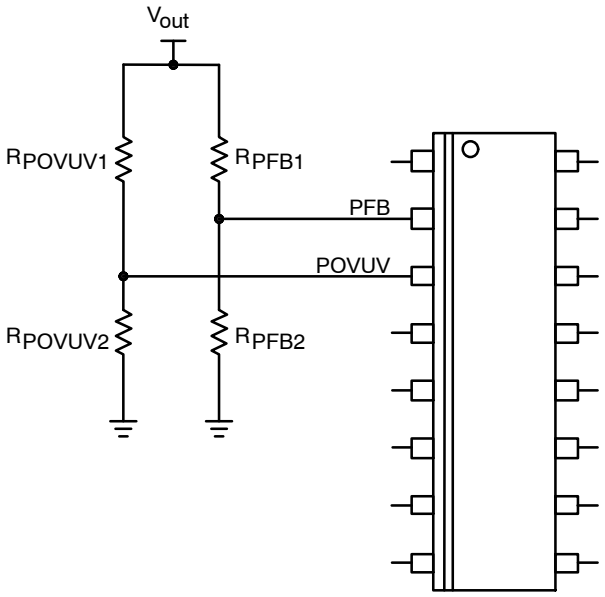


Figure 24. Configuration with Two Separate Feedback Networks

The double feedback configuration provides an increased level of safety, as it protects the PFC stage even if there is a failure of one of the two feedback arrangements.

A 1 μA (typical) current source, I_{UVP}, pulls the POVUV pin voltage below the UVP threshold if the pin is left floating to ensure the PFC stage will be protected.

A comparator connected to the POVUV pin provides the OVP protection. The output voltage that activates the OVP fault detection is calculated using Equation 13.

$$V_{out(OVP)} = V_{OVP} \cdot \frac{R_{POVUV1} + R_{POVUV2}}{R_{POVUV2}} + I_{UVP} \cdot R_{POVUV1} \quad \text{(eq. 13)}$$

where $V_{out(OVP)}$ is the peak value of the output voltage including ripple and V_{OVP} is the OVP threshold (2.5 V typical).

When the OVP comparator is activated, the PFC driver is immediately turned off. Once the feedback voltage drops below the hysteresis of V_{OVP} ($V_{OVP(HYS)}$), the PFC driver is re−enabled. This helps to limit overshoots on the output during startup and transient loads. Figure 25 depicts the operation of the OVP circuitry, while Figure 26 shows the internal block diagram.

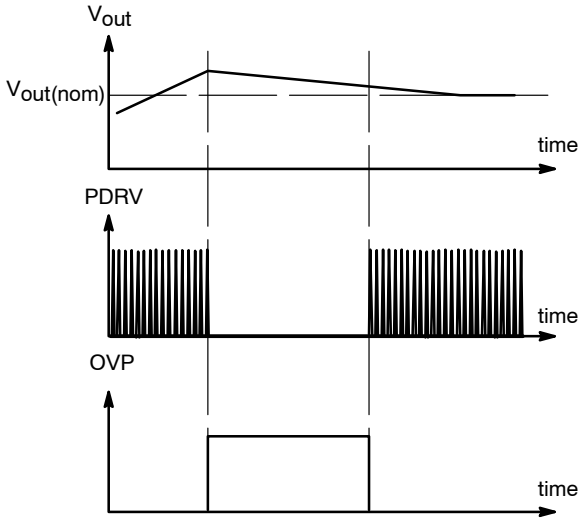


Figure 25. OVP Timing Diagram

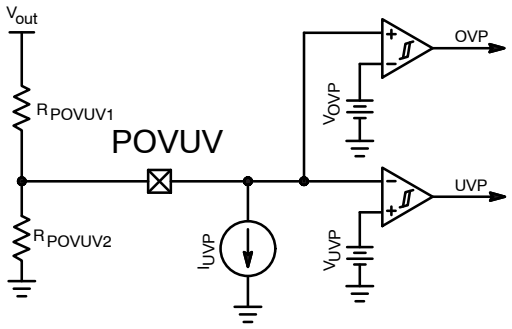


Figure 26. POVUV Pin Block

The NCP1927 detects a UVP fault when the output voltage falls below the UVP limit. During a UVP fault, the drive output and error amplifier (EA) are disabled, and $C_{PControl}$ is discharged. It is important to note that the PFC stage does not start if V_{POVUV} is lower than V_{UVP}. This protects the application when there is a problem with the power path to the bulk capacitor (i.e. the capacitor is unable to charge up) or if the controller is unable to sense the output voltage (i.e. the POVUV Pin is floating). The output voltage that causes a UVP fault is calculated using Equation 14.

$$V_{out(UVP)} = V_{UVP} \cdot \frac{R_{POVUV1} + R_{POVUV2}}{R_{POVUV2}} + I_{UVP} \cdot R_{POVUV1} \quad \text{(eq. 14)}$$

Overcurrent Protection (OCP)

The NCP1927 contains an OCP circuit to protect the PFC stage by limiting the coil current. A current sense resistor (R_{sense}) is inserted in the return path to generate a negative voltage proportional to the coil current (V_{Rsense}) as portrayed by Figure 27. The circuit uses V_{Rsense} to detect when the coil current exceeds its maximum permissible level. To do so, the circuit incorporates an operational amplifier that sources the current necessary to maintain the PCS pin at zero volts. A resistor (R_{PCS}) inserted between the PCS pin and R_{sense} allows the current sourced by the PCS pin (I_{PCS}) to be adjusted via Equation 15.

$$-\left(R_{sense} \cdot I_L\right) + \left(R_{PCS} \cdot I_{PCS}\right) = 0 \quad \text{(eq. 15)}$$

where I_L is the current flowing through the boost inductor.

Rearranging Equation 15 allows I_{PCS} to be calculated using Equation 16.

$$I_{PCS} = \frac{R_{sense}}{R_{PCS}} \cdot I_L \quad \text{(eq. 16)}$$

If I_{PCS} exceeds I_{OCP} (typically 250 μA), an OCP condition is detected and the driver is turned off. The driver remains off until I_{PCS} falls below I_{OCP}, and the next ZCD transition occurs or the watchdog timer expires. The maximum coil current ($I_{L(MAX)}$) is calculated with Equation 17.

$$I_{L(MAX)} = \frac{R_{PCS}}{R_{sense}} \cdot I_{OCP} \quad \text{(eq. 17)}$$

where I_{OCP} is the OCP threshold current.

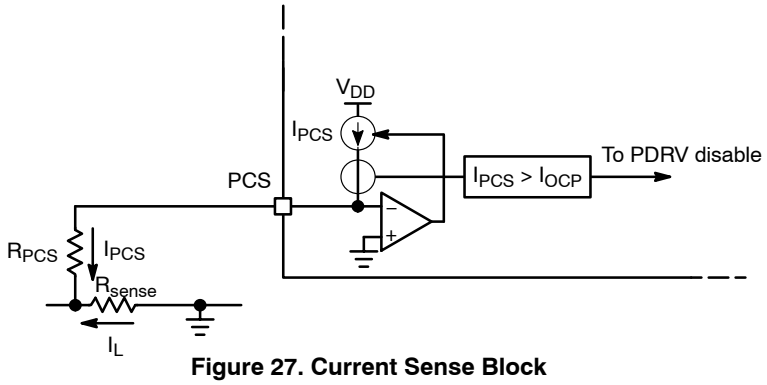


Figure 27. Current Sense Block

Skip Mode Operation

The NCP1927 automatically skips switching cycles when the power demand drops below a given level. This is accomplished by monitoring the internal offset PControl voltage. This voltage is compared to the PCT ramp to control the power level in a particular design. During normal operation, the circuit generates the input line current necessary for matching the load power demand. If the need for power decreases, the regulation loop lowers the regulation voltage to reduce the power delivery accordingly. When the regulation voltage goes below a programmable pre−set level, the PFC stage stops switching. This causes the output voltage to decrease, and the regulation voltage to increase. When the regulation voltage exceeds the skip threshold, switching resumes.

This operation allows the PFC stage to deliver 10% power for 10% of the time, as opposed to 1% power for 100% of the time. This skip cycle mode, also called controlled burst operation, is much more efficient than a continuous power flow since it drastically reduces the number of switching pulses and their associated switching losses. To ensure stability, hysteresis is added.

The PSKIP pin provides the possibility to adjust these levels by connecting it through a single resistor to ground. Since the skip threshold power levels can vary with line voltage, they are calculated using Equations 18 and 19.

$$P_{skip(lower)} = \frac{V_{PSKIP}}{5\ V \cdot \left(\frac{Vac_{LL}}{Vac}\right)^2} \cdot P_{out(MAX)} \quad \text{(eq. 18)}$$

$$P_{skip(upper)} = \frac{V_{PSKIP}}{4.5\ V \cdot \left(\frac{Vac_{LL}}{Vac}\right)^2} \cdot P_{out(MAX)} \quad \text{(eq. 19)}$$

where V_{PSKIP} is the voltage applied to the PSKIP pin, Vac_{LL} is the minimum ac line voltage, Vac is the operating line voltage, and $P_{out(MAX)}$ is the maximum output power.

The skip pin voltage is adjusted through a resistor to ground using Equation 20.

$$V_{PSKIP} = I_{PSKIP} \cdot R_{PSKIP} \quad \text{(eq. 20)}$$

where I_{PSKIP} is the value of the internal current source (30 μA typical) and R_{PSKIP} is the external resistor connected to ground.

If desired, skip mode can be easily disabled by connecting the PSKIP pin directly to ground. If the PSKIP pin is left floating, V_{PSKIP} will rise towards the internal voltage rail and disable the drive. Since the PControl Pin is low during startup, the PFC skip mode is disabled until the PFC output reaches regulation and the IENABLE Pin is high. A simplified schematic of the PSKIP pin is shown in Figure 28.

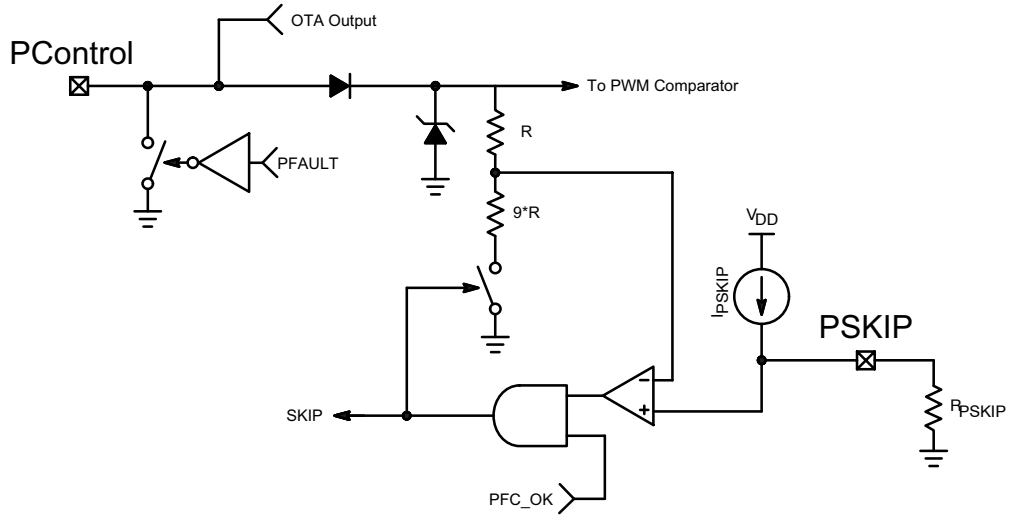


Figure 28. Schematic for PSKIP Pin

Go To Standby Pin

The Go To Standby (GTS) pin is used to disable the PFC stage during system standby based on the flyback stage load condition. This can be done by connecting it to the flyback stage feedback pin (FFB) through a resistor divider or by directly driving the pin with an optocoupler. These implementations are shown in Figures 29 and 30.

The GTS pin contains an internal pull down resistor, R_{GTS} (typically 200 kΩ), for use with an optocoupler and to ensure the PFC is disabled if the pin is floating.

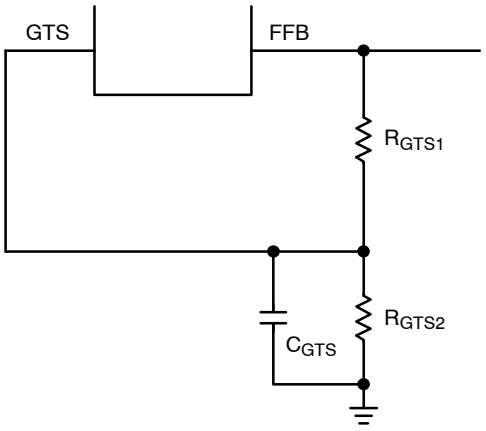


Figure 29. GTS Implementation with Feedback Pin

The resistor divider from the FFB pin is used to setup the GTS power level threshold. When V_{GTS} is brought below the GTS threshold, $V_{standby}$, the PFC controller stops switching and enter standby mode. It remains in standby until V_{GTS} is brought above the hysteresis of $V_{standby}$ ($V_{standby(HYS)}$). A timer is included on the GTS pin to ensure transients on the flyback converter do not trigger GTS. However, the PFC must come out of standby as soon as possible if there is a request to turn on the TV. Therefore, the timer is bypassed when coming out of standby. The FFB voltage at which the PFC enters GTS is expressed using Equation 21.

$$V_{FFB(GTS)} = V_{GTS} \cdot \frac{R_{GTS1} + R_{equiv}}{R_{equiv}} \qquad \text{(eq. 21)}$$

where R_{equiv} is the parallel resistor combination of R_{GTS} and R_{GTS2} and is calculated using Equation 22.

$$R_{equiv} = \frac{R_{GTS} \cdot R_{GTS2}}{R_{GTS} + R_{GTS2}} \qquad \text{(eq. 22)}$$

If direct control of the PFC standby mode is desired, the GTS pin can instead be driven with an optocoupler from the secondary side to force the PFC stage in and out of standby mode. A resistor (R_{limit}) is placed in series with the optocoupler to limit the current into the GTS pin.

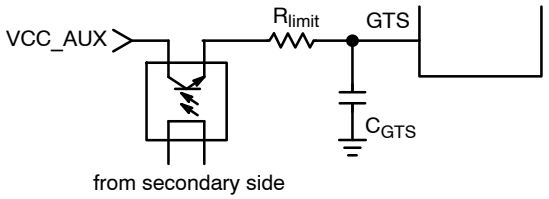


Figure 30. GTS Implementation with Optocoupler

IENABLE Pin

The IENABLE pin is designed to drive an optocoupler that enables the Flat Panel TV backlight inverter once the PFC stage reaches regulation. The NCP1927 achieves this by monitoring the current sourced by the EA. Once this current drops to 0 μA, the IENABLE pin voltage switches to $V_{IENABLE(high)}$ (typically 5.0 V). This operation is shown in Figure 31.

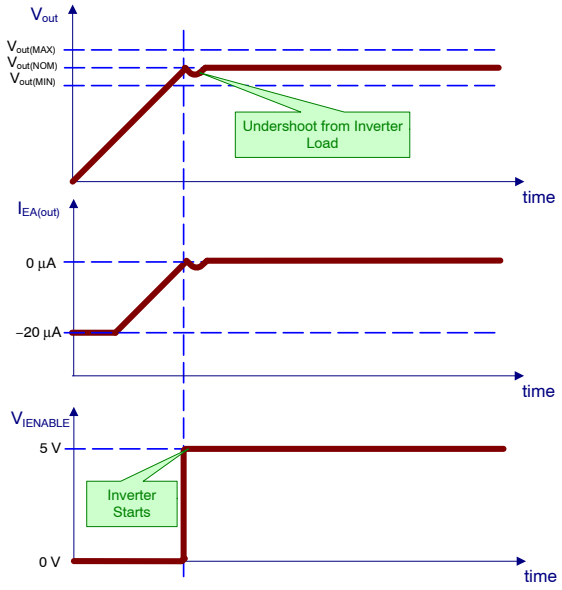


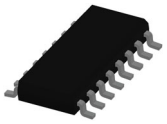
Figure 31. IENABLE Pin Timing

A separate comparator on the PFB pin is used to protect the inverter from undervoltage conditions by detecting when the PFB voltage falls below $V_{disable}$. When this occurs, the IENABLE pin voltage switches to $V_{IENABLE(low)}$. Using the result from Equation 7, the output threshold that sets the IENABLE pin low can be calculated with Equation 23.

$$V_{out(disable)} = \frac{V_{out} \cdot V_{disable}}{V_{REF}} \qquad \text{(eq. 23)}$$

where $V_{disable}$ is the disable threshold (1.865 V typical).

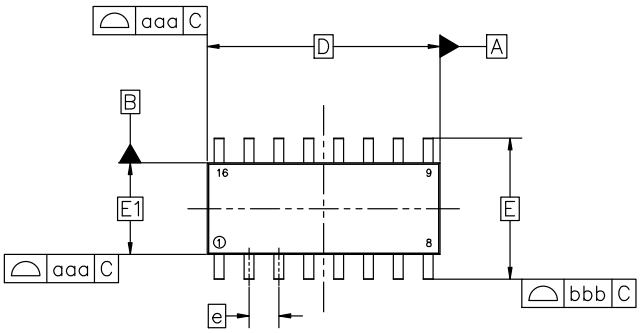
The IENABLE pin can also be used as a voltage reference. To filter noise, a decoupling capacitor (C_{REF}) may be connected to the pin.



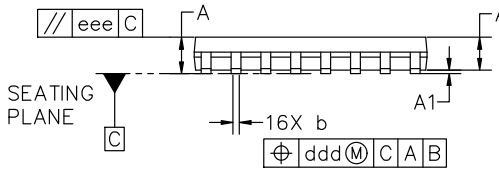
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

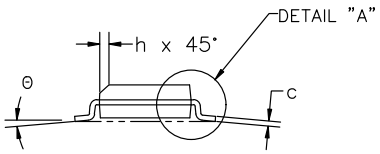
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

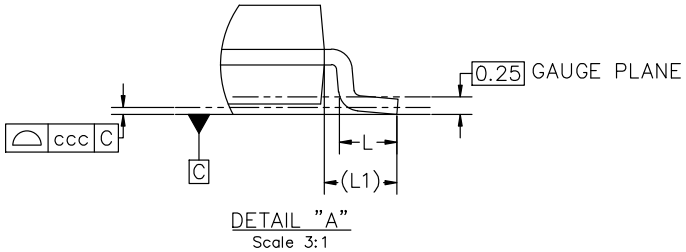


SIDE VIEW

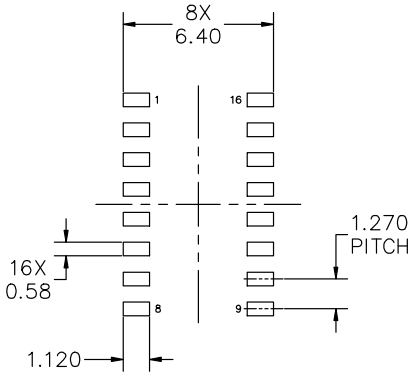


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

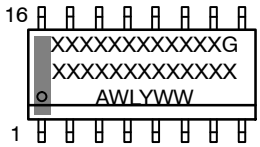
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales