

Description

The IRF7413PBF uses advanced trench technology

to provide excellent R_{DS(ON)}, low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a

Battery protection or in other Switching application.

General Features

 $V_{DS} = 30V I_{D} = 15A$

 $R_{DS(ON)}$ < 10m Ω @ V_{GS} =10V

Application

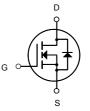
Battery protection

Load switch

Uninterruptible power supply



SOP-8 (SO-8)



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7413PBF	SOP-8(SO-8)	HXY MOSFET	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Symbol	Parameter Rating		Units
V _{DS}	Drain-Source Voltage	30	V
Vgs	Gate-Source Voltage	±20	V
I _D @T _A =25°C	Continuous Drain Current ¹	Continuous Drain Current ¹ 15	
I _D @T _A =70°C	Continuous Drain Current ¹	Continuous Drain Current ¹ 8	
IDM	Pulsed Drain Current ²	Pulsed Drain Current ² 45	
EAS	Single Pulse Avalanche Energy ³	Single Pulse Avalanche Energy ³ 12	
P _D @T _A =25°C	Total Power Dissipation ⁴	Total Power Dissipation⁴ 15	
Тѕтс	Storage Temperature Range	perature Range -55 to 150	
TJ	Operating Junction Temperature Range	-55 to 150	°C
_	Thermal Resistance Junction-ambient¹(t≤10s)	85	°C/W
R _θ JA	Thermal Resistance Junction-ambient ¹	25	°C/W



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	30			V	
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25°C , I _D =1mA		0.034		V/°C	
	Static Drain-Source On-Resistance ²	V_{GS} =10V , I_D =7A	1	8	10	mΩ	
$R_{DS(ON)}$	Static Dialii-Source Off-Resistance	V _{GS} =4.5V , I _D =4A	, I _D =4A 12 15		15	1112.2	
$V_{GS(th)}$	Gate Threshold Voltage	\/aa=\/aa a=250uA	1.2	1.4	2.5	٧	
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=250uA$		-3.84		mV/°C	
lana	Drain-Source Leakage Current	V _{DS} =24V , V _{GS} =0V , T _J =25°C			1	- uA	
IDSS		V _{DS} =24V , V _{GS} =0V , T _J =55°C			5		
Igss	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$			±100	nA	
gfs	Forward Transconductance	V _{DS} =5V , I _D =7A		6.2		S	
R_g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz		1.04	2.1	Ω	
Qg	Total Gate Charge (4.5V)			6	8.4		
Q _{gs}	Gate-Source Charge	V _{DS} =15V , V _{GS} =4.5V , I _D =7A		2.2	3.1	nC	
Q _{gd}	Gate-Drain Charge			2	2.8		
T _{d(on)}	Turn-On Delay Time			1.2	2.4		
Tr	Rise Time	V_{DD} =15V , V_{GS} =10V , R_{G} =3.3 Ω		40	72.0	ns	
$T_{d(off)}$	Turn-Off Delay Time	I _D =7A		18	36.0		
Tf	Fall Time			7.2	14.4		
Ciss	Input Capacitance			983	1616		
Coss	Output Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz		147	207.8	pF	
C _{rss}	Reverse Transfer Capacitance			109	162.6		
Is	Continuous Source Current ^{1,5}	V-=V-=0V Force Current			7	Α	
Ism	Pulsed Source Current ^{2,5}	──V _G =V _D =0V , Force Current			35	Α	
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =1A , T _J =25°C			1.2	V	
t _{rr}	Reverse Recovery Time			7.2		nS	
Qrr	Reverse Recovery Charge	IF=7A , dI/dt=100A/µs , T _J =25°C		2.9		nC	

Note:

^{1.} The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

^{2.}The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%

^{3.} The EAS data shows Max. rating . The test condition is V_{DD} =25V, V_{GS} =10V, L=0.1mH, I_{AS} =20A

^{4.} The power dissipation is limited by 150°C junction temperature

^{5.} The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

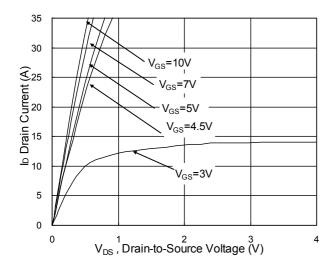


Fig.1 Typical Output Characteristics

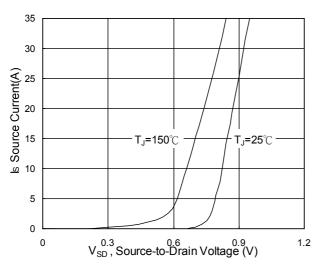


Fig.3 Forward Characteristics Of Reverse

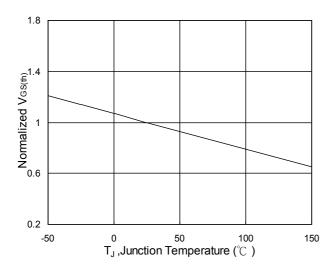


Fig.5 Normalized $V_{\text{GS(th)}}$ vs. T_{J}

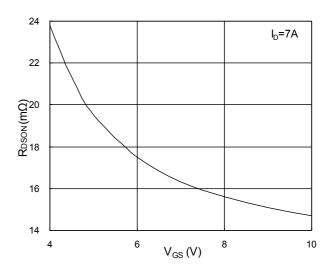


Fig.2 On-Resistance vs. Gate-Source

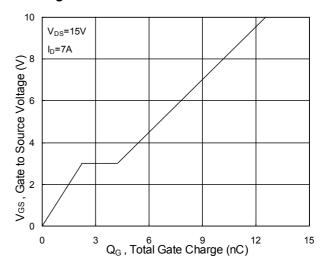


Fig.4 Gate-Charge Characteristics

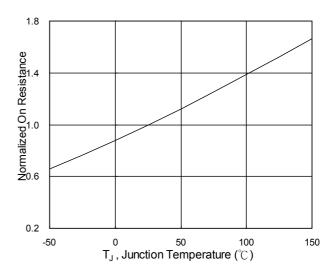
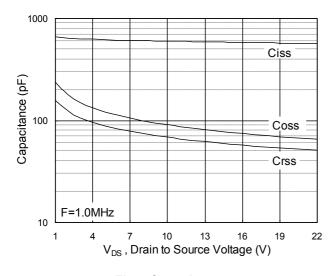


Fig.6 Normalized R_{DSON} vs. T_J





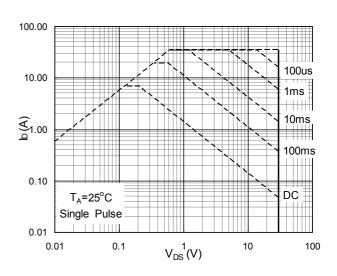


Fig.7 Capacitance

Fig.8 Safe Operating Area

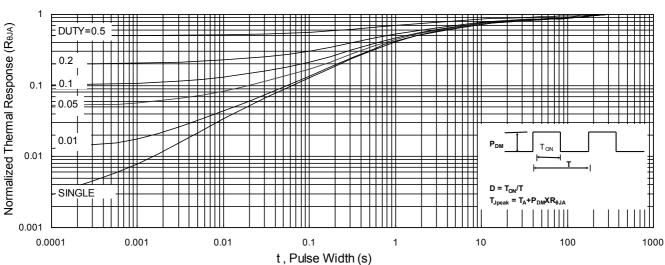


Fig.9 Normalized Maximum Transient Thermal Impedance

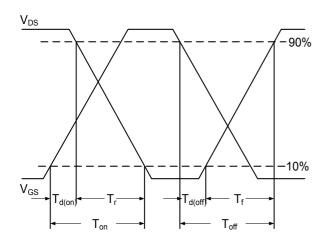


Fig.10 Switching Time Waveform

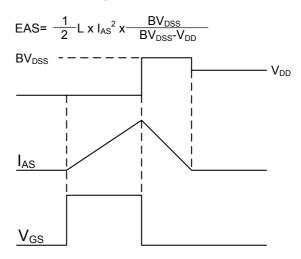
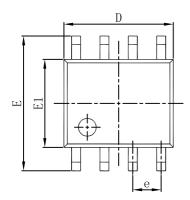
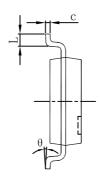


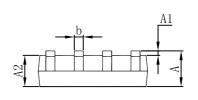
Fig.11 Unclamped Inductive Switching Waveform



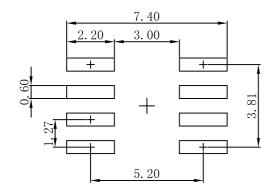
SOP-8(SO-8) Package Outline Dimensions







Symbol	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min	Max	Min	Max	
A	1. 350	1.750	0.053	0.069	
A1	0.100	0. 250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
c	0.170	0. 250	0.007	0.010	
D	4.800	5.000	0.189	0.197	
e	1. 270 (BSC)		0.050 (BSC)		
E	5.800	6. 200	0. 228	0. 244	
E1	3.800	4.000	0.150	0. 157	
L	0.400	1. 270	0.016	0.050	
θ	0°	8°	0°	8°	



- Note: 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
 3.The pad layout is for reference purposes only.

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