ISL59885

Auto-Adjusting Sync Separator for HD and SD Video

FN7442
Rev 8.00
October 31, 2011

The ISL59885 video sync separator extracts sync timing information from both standard and non-standard video inputs in the presence of Macrovision pulses. The ISL59885 provides horizontal, vertical, and composite sync outputs as well as SD/HDTV detection. An auto input frequency detect feature automatically adapts to a wide range of video standards (it does not need a different RSET resistor for different frequencies). The vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The horizontal output gives horizontal timing with pre/post equalizing pulses. Fixed 70mV sync tip slicing provides sync edge detection when the video input level is between $0.5V_{P-P}$ and $2V_{P-P}$.

The ISL59885 is available in an 8 Ld SOIC package and is specified for operation over the full -40°C to +85°C temperature range.

Features

- NTSC, PAL, SECAM, HDTV, Non-standard Video Sync Separation
- Fixed 70mV Slicing of Video Input Levels from $0.5V_{P-P}$ to $2V_{P-P}$
- Single 3V to 5V Supply
- Composite Sync Output
- Vertical Output
- Horizontal Output
- HDTV Detection
- Macrovision Compatible
- Available in 8 Ld SOIC Package
- Pb-free (RoHS Compliant)

Applications

- High-definition Video Equipment

Related Literature

- AN1269, “One Transistor Enables Clean HDTV and NTSC Video Sync Separation”
- AN1316, “One Transistor Enables Clean HDTV and NTSC Video Sync Separation”
- TB476, “Regenerating H_{SYNC} from Corrupted SOG or C_{SYNC} during V_{SYNC}”

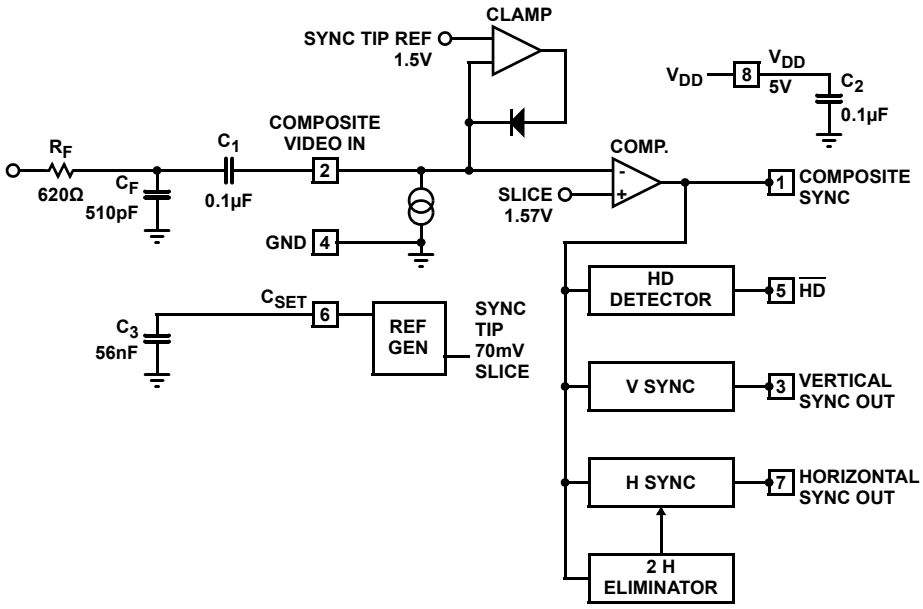
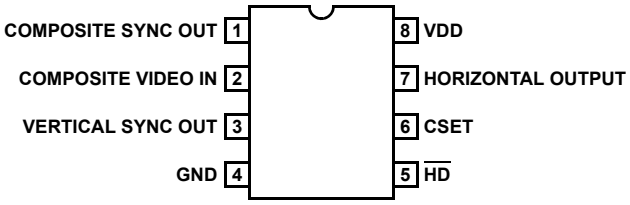


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

Pin Configuration

ISL59885
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	Composite Sync Out	Composite sync pulse output; sync pulses start on a falling edge and end on a rising edge.
2	Composite Video In	AC-coupled composite video input; sync tip must be at the lowest potential (positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output; the falling edge of vertical sync is the start of the vertical period.
4	GND	Supply ground
5	$\overline{HD}$	Low when input horizontal frequency is greater than 25kHz.
6	CSET	(An external capacitor to ground); bypass pin for internal bias generator.
7	Horizontal Output	Horizontal output; falling edge active
8	VDD	Positive supply

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL59885ISZ	59885 ISZ	-40 to +85	8 Ld SOIC	M8.15E
ISL59885ISZ-EVAL	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL59885. For more information on MSL, please see Tech Brief TB363.

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply 7V
Pin Voltages. . . . . -0.5V to V_{CC} +0.5V

Recommended Operating Conditions

Operating Ambient Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5)	120	66

Operating Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation. 400mW
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

DC Electrical Specifications

V_{DD} = 3.3V, T_A = +25°C, C_{SET} = 56nF, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{DD}, Quiescent	V_{DD} = 3.3V	**1**	2.2	**4**	mA
Clamp Voltage	Pin 2, I_{LOAD} = -100µA	**1.35**	1.5	**1.65**	V
Clamp Discharge Current	Pin 2 = 2V	**6**	15	**30**	µA
Clamp Charge Current	Pin 2 = 1V	**-9**	-7.2	**-5.2**	mA
V_{OL} Output Low Voltage	I_{OL} = 1.6mA		0.24	**0.5**	V
V_{OH} Output High Voltage	I_{OH} = -40µA	**3**	3.2		V
	I_{OH} = -1.6mA	**2.5**	3.0		V

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Dynamic Characteristics

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	DESCRIPTION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Comp Sync Prop Delay, t_{CS}	(See Figure 8)		35	**75**	ns
Horizontal Sync Delay, t_{HS}	(See Figure 8)		40	**80**	ns
Horizontal Sync Width, t_{HS-PW}	(See Figure 8)	**3.8**	5.2	**6.2**	µs
Vertical Sync Width, t_{VS}	Normal or default trigger, 50% to 50% (see Figure 7)	**230**	280	**350**	µs
Vertical Sync Default Delay, t_{VSD}	(See Figure 9)	**28**	50	**68**	µs
Hsync Blanking Window		**70**	80	**90**	%
Input Dynamic Range	Video input amplitude to maintain slice level spec, V_{DD} = 3.3V	**0.5**		**2**	V_{P-P}
Slice Level	V_{SLICE} above V_{CLAMP}	**50**	70	**90**	mV
$\overline{HD}$ Pin Level	720p, 1080i, 1080p		0		V

Typical Performance Curves

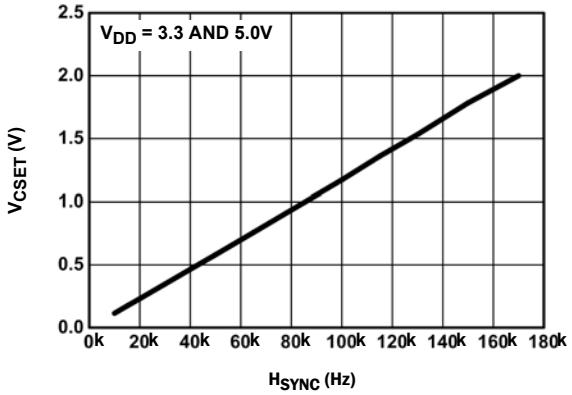


FIGURE 2. H_{SYNC} vs V_{CSET} (R_{SET} = OPEN)

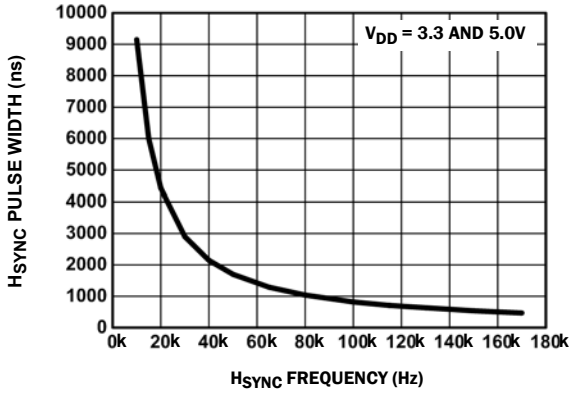


FIGURE 3. H_{SYNC} PULSE WIDTH vs H_{SYNC} FREQUENCY (R_{SET} = OPEN)

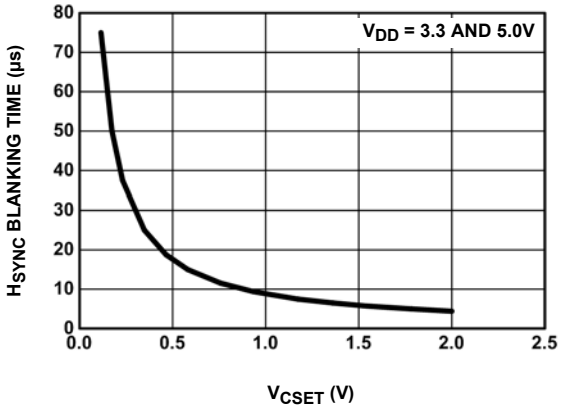


FIGURE 4. H_{SYNC} vs V_{CSET} (R_{SET} = OPEN)

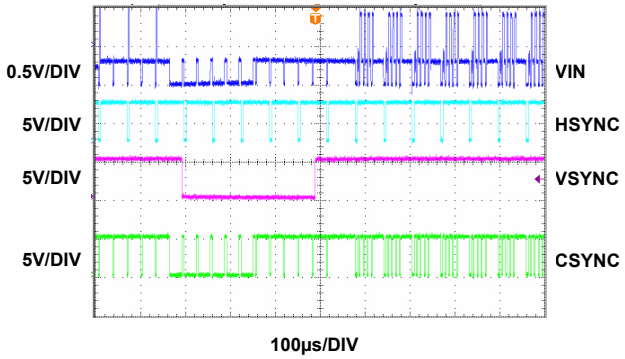


FIGURE 5. MACROVISION COMPATIBILITY (NTSC)

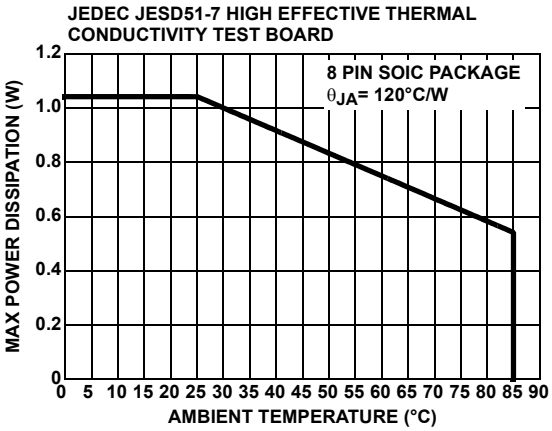
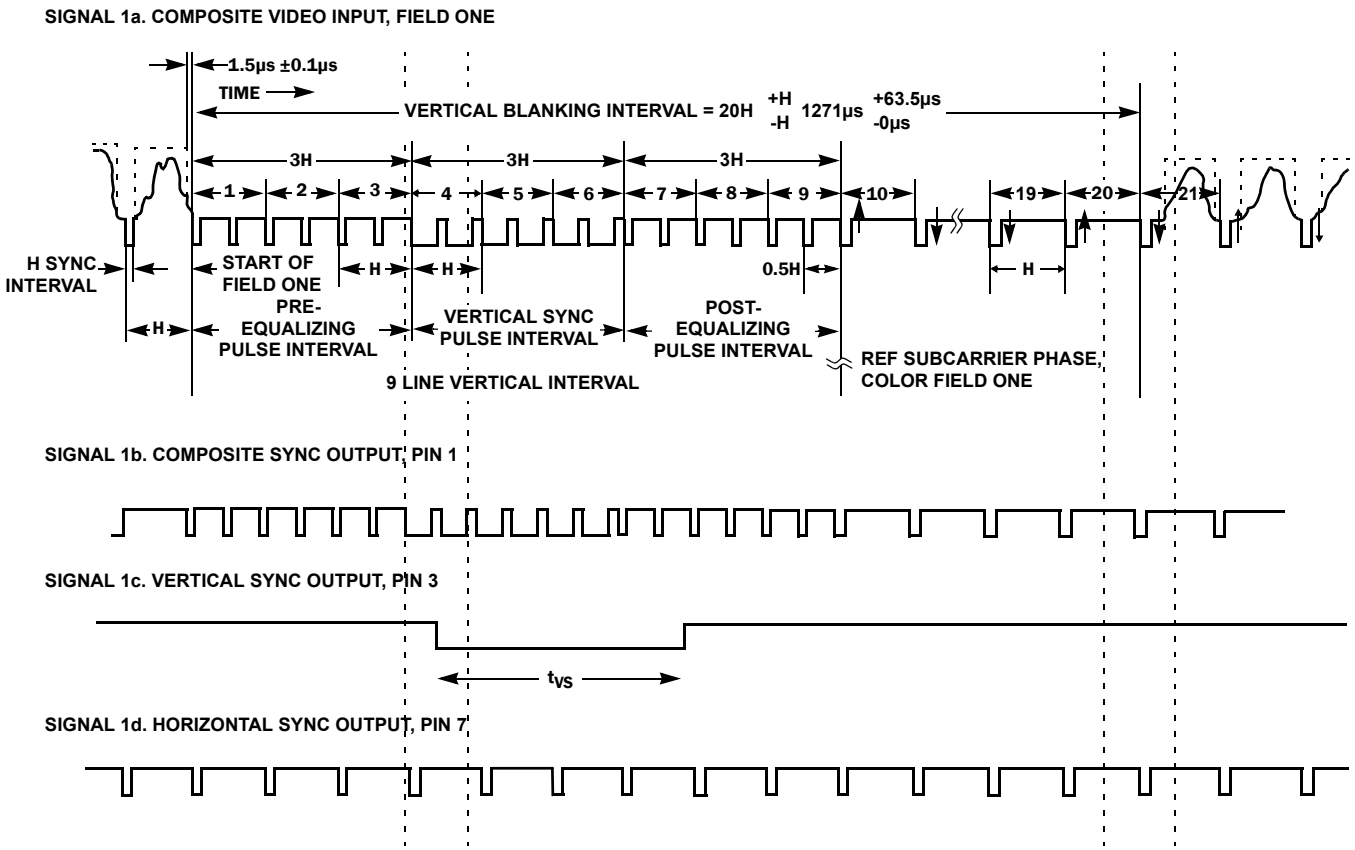


FIGURE 6. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE



NOTES:

7. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
8. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.
9. Horizontal sync output produces the “H” pulses of nominal width of 5µs. It has the same delay as the composite sync.

FIGURE 7. TIMING DIAGRAM

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

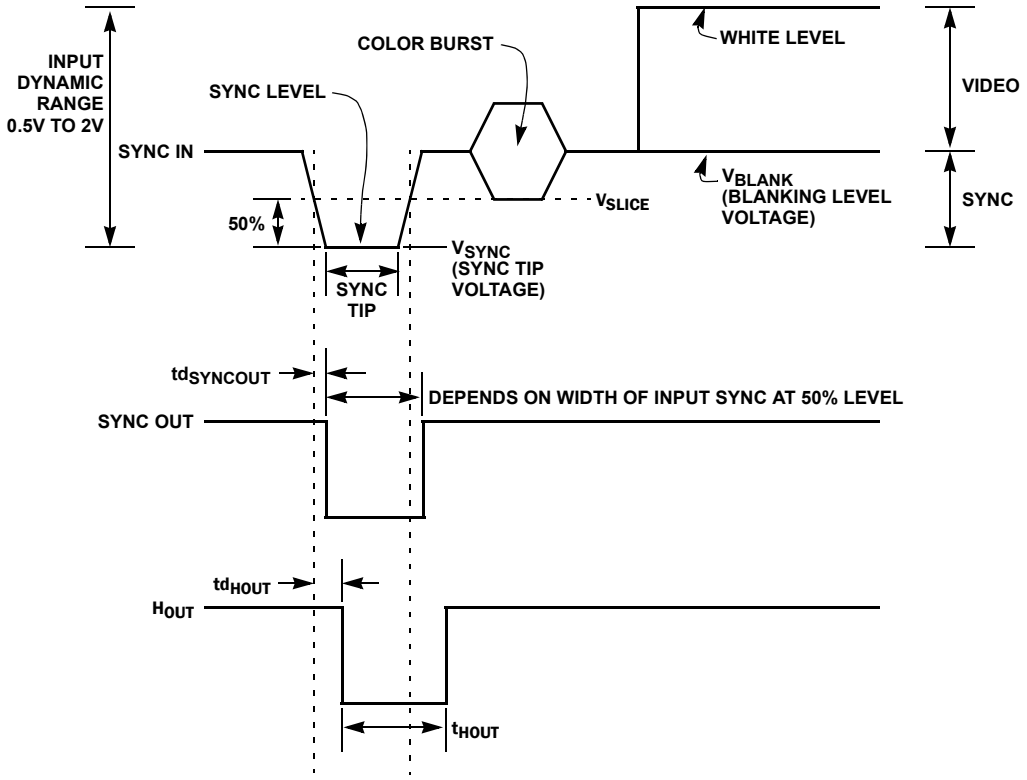


FIGURE 7. HORIZONTAL INTERVAL 525/625 LINE COMPOSITE

PARAMETER	DESCRIPTION	CONDITIONS	TYP (Note 10)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 7)	65	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 7)	470	ns
t_{HOUT}	Horizontal Output Width	(See Figure 7)	5.2	µs

NOTES:

10. Delay variation is less than 2.5ns over-temperature range.

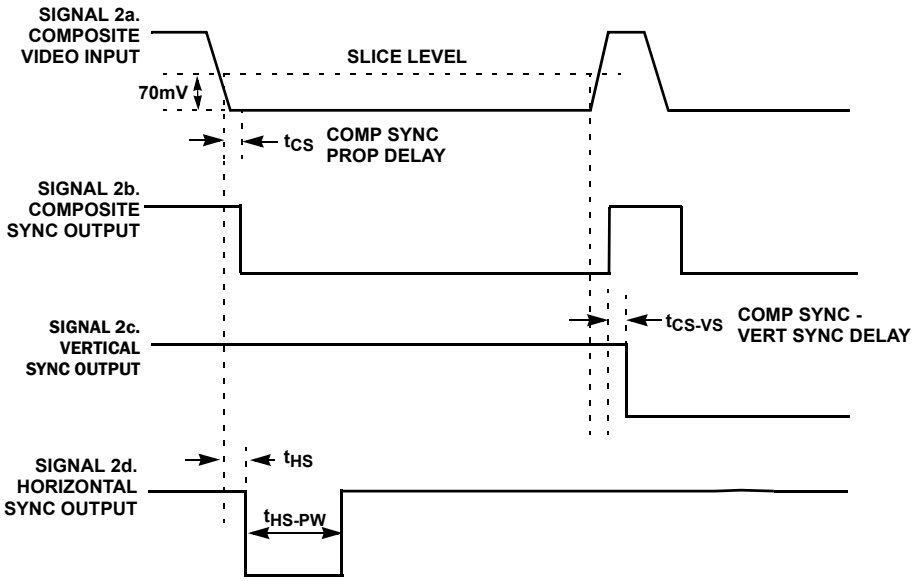


FIGURE 8. STANDARD VERTICAL TIMING

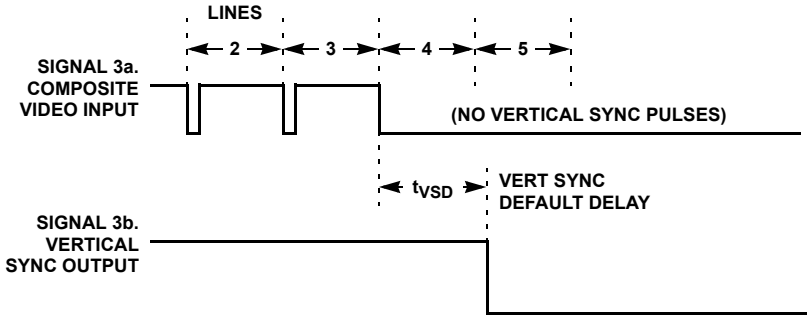
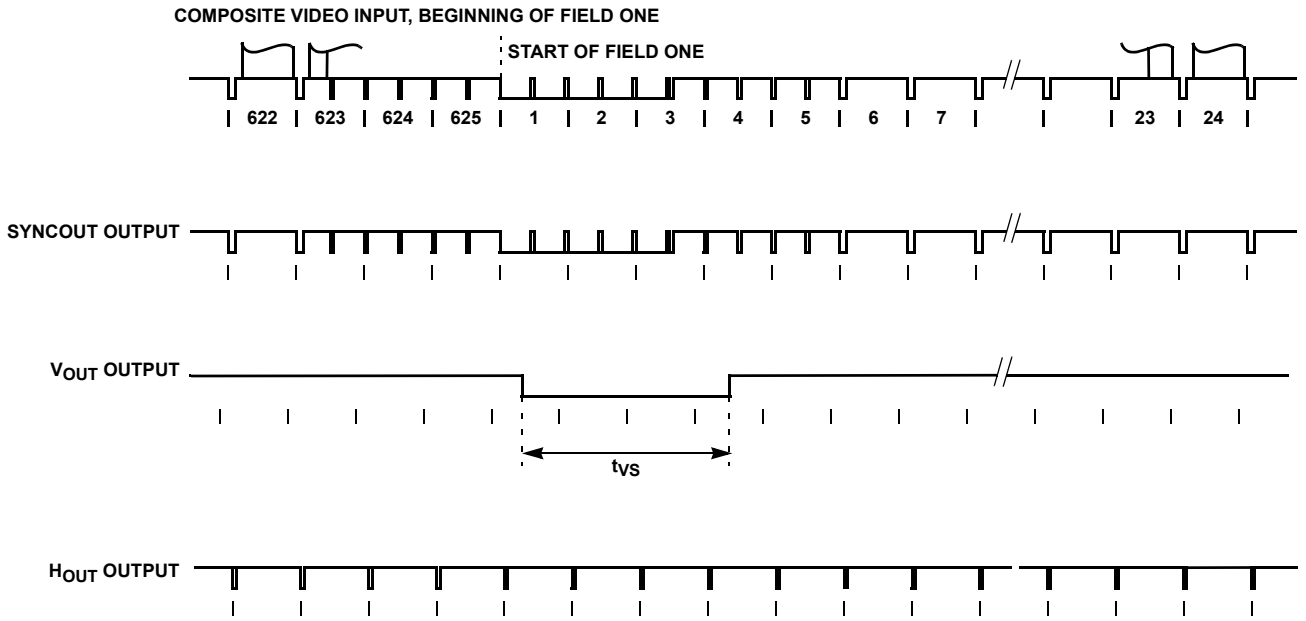


FIGURE 9. NON-STANDARD VERTICAL TIMING



NOTES:

11. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
12. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

FIGURE 11. EXAMPLE OF VERTICAL INTERVAL (625)

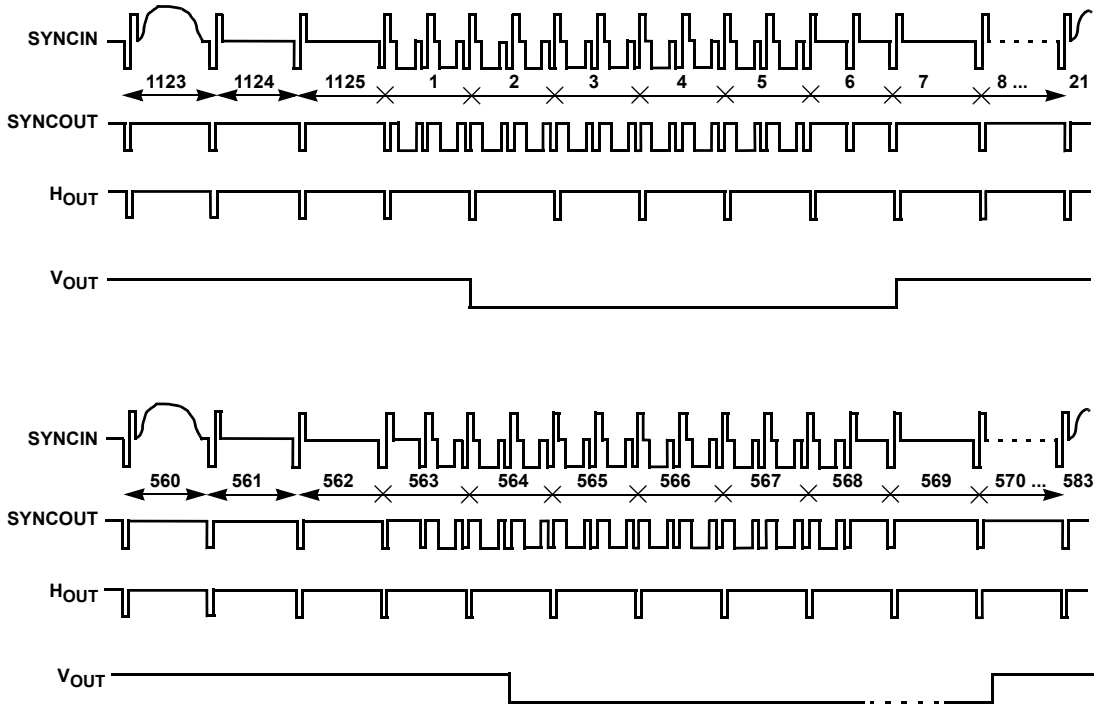


FIGURE 10. EXAMPLE OF HDTV 1080I/30 LINE COMPOSITE VIDEO: INTERLACED

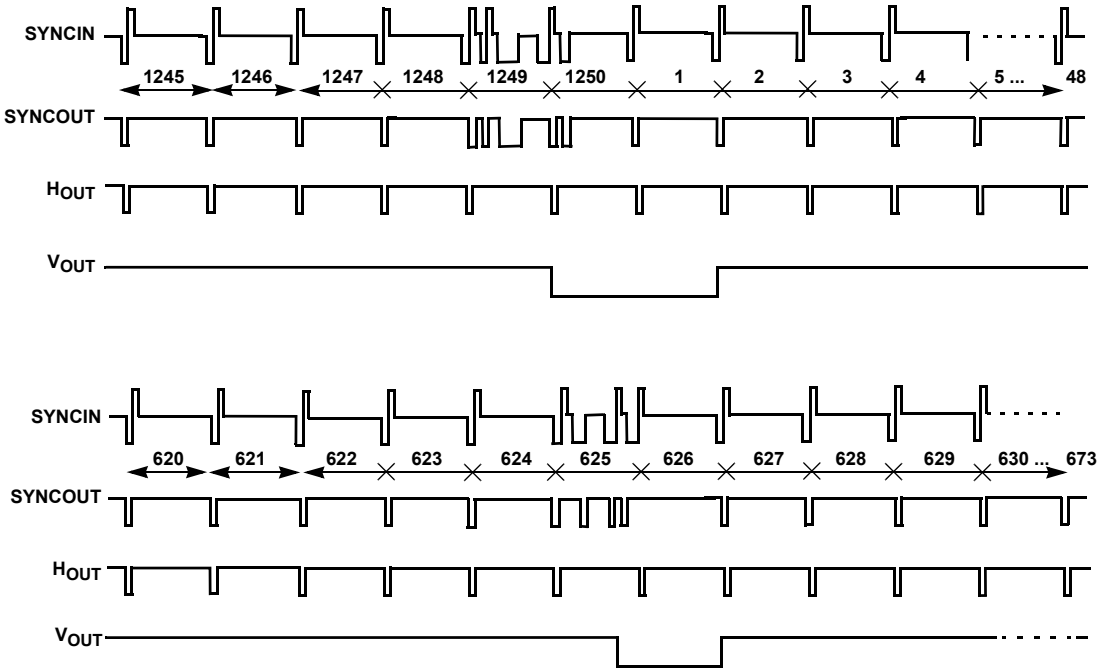


FIGURE 11. HDTV 1080I/25 LINE COMPOSITE VIDEO: INTERLACED (1250 LINES)

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

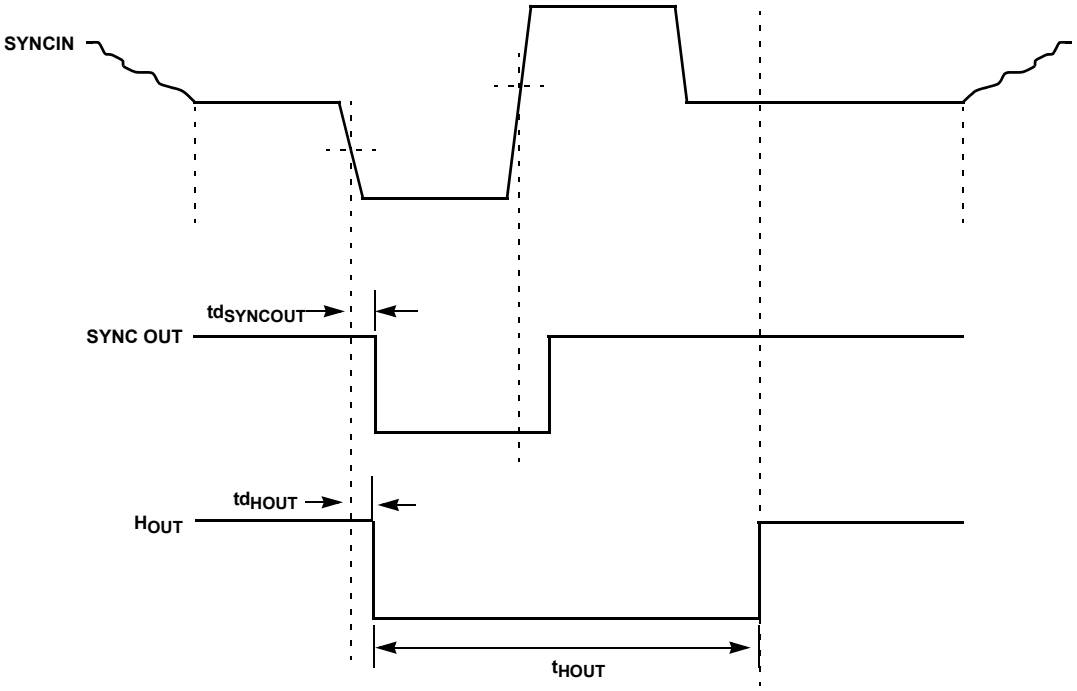


FIGURE 12. HORIZONTAL INTERVAL (HDTV) (720p)

H TIMING FOR HDTV, NO FILTER (USING 720P INPUT SIGNAL)

PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 13)	TYP @ 5V (Note 13)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 12)	56	50	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 12)	48	36	ns
t_{HOUT}	Horizontal Output Width	(See Figure 12)	1.90	1.90	µs

NOTES:

13. Delay variation is less than 2.5ns over-temperature range.

CONDITIONS: V_{DD} = 3.3V/5V, T_A = +25°C

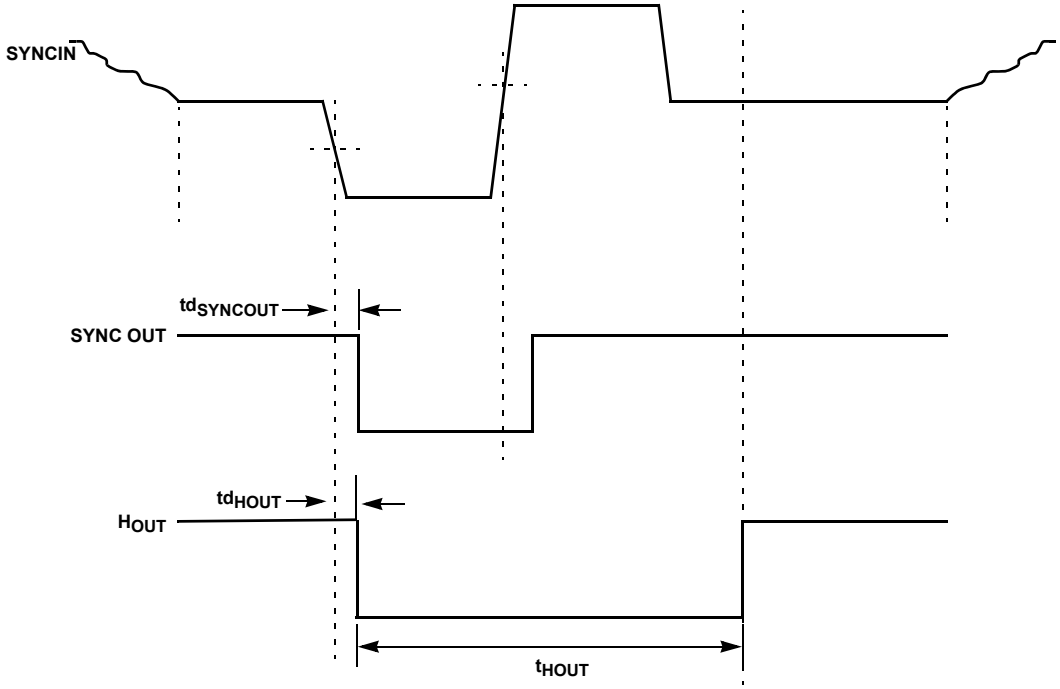


FIGURE 13. HORIZONTAL INTERVAL (HDTV) (720p)

H TIMING FOR HDTV, WITH FILTER (USING 720P INPUT)

PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V (Note 14)	TYP @ 5V (Note 14)	UNIT
$td_{SYNCOUT}$	SYNCOUT Timing Relative to Input	(See Figure 13)	120	110	ns
td_{HOUT}	HOUT Timing Relative to Input	(See Figure 13)	112	100	ns
t_{HOUT}	Horizontal Output Width	(See Figure 13)	200	200	ns

NOTES:

14. Delay variation is less than 2.5ns over-temperature range.

Applications Information

Video In

See the “Simplified Block Diagram” on page 13.

An AC-coupled video signal is input to Video In pin 2 via C_1, nominally 0.1µF. Clamp charge current prevents the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1mA. A clamp discharge current of about 10µA is always attempting to discharge C_1 to Sync Tip Ref; thus, charge is lost between sync pulses that must be replaced during sync pulses. Droop voltage can be calculated from It = CV, where V is the droop voltage, I is the discharge current, t is the time between sync pulses (sync period-sync tip width), and C is C_1.

An NTSC video signal has a horizontal frequency of 15.73kHz and a sync tip width of 4.7µs. This gives a period of 63.6µs and a time of t = 58.9µs. The droop voltage will then be V = 5.9mV. This is less than 2% of a nominal sync tip amplitude of 286mV. The charge represented by this droop is replaced in a time given by t = CV/I, where I = clamp charge current = 5.3mA. Here, t = 590ns, about 12% of the sync pulse width of 4.7µs. It is important that C_1 be large enough that droop voltage does not approach the switching threshold of the internal comparator.

Composite Sync

The composite sync output is simply a reproduction of the input signal with the active video removed. The sync tip of the composite video signal is clamped to 1.5V at pin 2 and then slices at 70mV above the sync tip reference. The output signal is buffered out to pin 1. When there is loss of sync, the composite sync output is held low.

Vertical Sync

A low-going vertical sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical sync is clocked out of the ISL59885 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse is forced out after the vertical sync default delay time, which is approximately 60µs after the last falling edge of the vertical equalizing phase.

Horizontal Sync

The horizontal block senses the leading edges of the composite sync signal and generates horizontal pulses of nominal width 5.2µs. Any half line pulses present in the input signal during vertical blanking are removed with an internal 2H line eliminator function that inhibits retriggering of horizontal output pulses until 70% of the line time is reached. Then, the horizontal output operation is enabled again. Any signals present on the I/P signal after the real H sync are ignored; thus, the horizontal output is not affected by MacroVision copy protection. When there is a loss of incoming composite sync, the horizontal sync output is held high.

C_{SET}

An external C_{SET} capacitor is connected from C_{SET} pin 6 to ground. The C_{SET} capacitor should be a X7R grade or better because the Y5U general use capacitors may be too leaky and cause faulty operation. The C_{SET} capacitor should be very close to the CSET pin to reduce possible board leakage. A setting of 56nF is recommended (see “CSET Bias Block Diagram” on page 13). The C_{SET} capacitor rectifies a 5µs pulse current and creates a voltage on C_{SET}. The C_{SET} voltage is converted to bias current for H_{SYNC} and V_{SYNC} timing.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure 14. It can be implemented very simply and inexpensively with a series resistor of 100Ω and a capacitor of 570pF, which gives a single pole roll-off frequency of about 2.79MHz during NTSC or PAL. This sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal, yet passes the approximately 15kHz sync signals without appreciable attenuation. During HDTV, the transistor turns off and a 100pF capacitor is left to filter any noise present at the input. A chroma filter will increase the propagation delay from the composite input to the outputs.

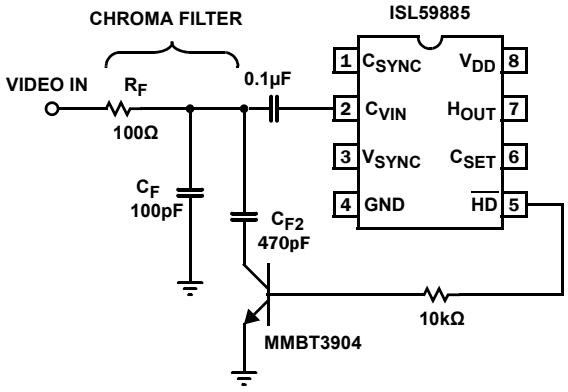
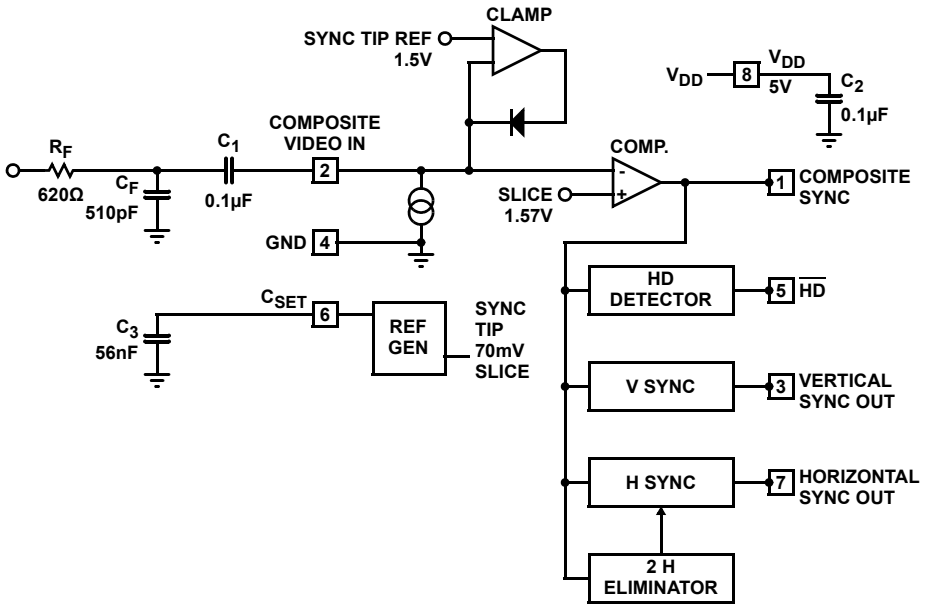


FIGURE 14. OPTIONAL CHROMA FILTER

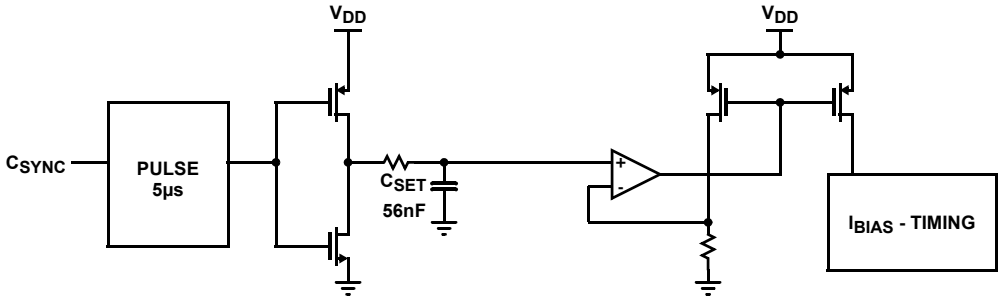
HD-Detect

High definition video is flagged by $\overline{HD}$ going low when the input horizontal frequency is greater than 25kHz.

Simplified Block Diagram



C_{SET} Bias Block Diagram



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
5/25/2011	FN7442.8	• On page 1, removed “Demo Board” section and included ISL59885ISZ-EVAL evaluation board in Ordering Information on page 2. • On page 2, Pin Descriptions table: changed $\overline{HD}$ pin function from “Low when input horizontal frequency is greater than 20kHz." to "Low when input horizontal frequency is greater than 25kHz." • On page 2, Ordering Information table: removed ISL59885IS; obsolete. Changed Package Drawing Number for ISL59885ISZ from MDP0027 (obsolete) to M8.15E. Added ISL59885ISZ-EVAL evaluation board. • On page 3, Thermal Information: added Θ_{JA} value of 120°C. • On page 4, modified Figure 6, “PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE” to reflect Θ_{JA} value of 120°C instead of 110°C. Removed Figure 7, which showed Θ_{JA} of 160°C measured on low effective thermal conductivity board, as it is not relevant. • On page 12, under HD-Detect: text changed from "High definition video is flagged by $\overline{HD}$ going low when the input horizontal frequency is greater than 20kHz." to "High definition video is flagged by $\overline{HD}$ going low when the input horizontal frequency is greater than 25kHz."
5/12/2009	FN7442.7	• Pg 2, DC Electrical Specifications: Changed MIN spec for IDD, Quiescent from 1.5mA to 1mA • Added Hsync Blanking Window spec to Dynamic Characteristics Table • Pg 5, Figure 8: Timing Diagram. Revised Note 4 re: Horizontal Sync Output. • Pg 11, Horizontal Sync: updated text in this section. • Pg 12: renamed CSET Bias Circuit to CSET Bias Block
8/15/2007	FN7442.6	• Pg 1, revised first paragraph. • Updated Ordering Information table (removed all custom parts). • Updated Package Outline Drawing to most recent revision.
8/9/2006	FN7442.5	• Added ISL59885ISZR5260 and ISL598851SZ-T7R5260 to Ordering Information. • Updated Features on pg 1 and Dynamic Characteristics table.
1/23/2006	FN7442.4	• Changed VCC to VDD. • Changed Vs to VDD.
9/8/2005	FN7442.3	• Pg 1, Ordering Information: added “ISL59885ISR5218” “ISL59885IS-T7R5218” “ISL59885IS-T13R5218” “ISL59885ISZR5218” “ISL59885ISZ-T7R5218” and “ISL59885ISZ-T13R5218”. • Pg 2, Pin Descriptions, CSET, removed “and resistor” in the sentence “(An external capacitor and resistor to ground).
7/7/2005	FN7442.2	• Replaced microvision scope photo. • Corrected Csync output waveform. • Removed Rset resistor.
5/20/2005	FN7442.1	• Updated Ordering information with latest parts.
5/11/2005	FN7442.0	• Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL59885

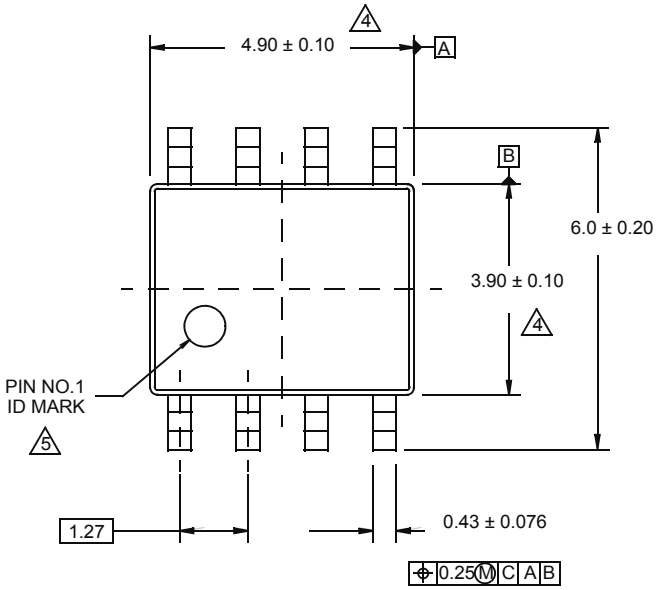
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

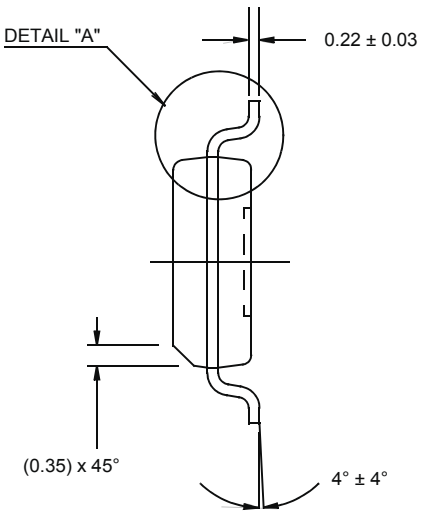
Package Outline Drawing

M8.15E

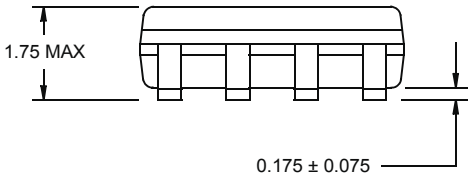
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



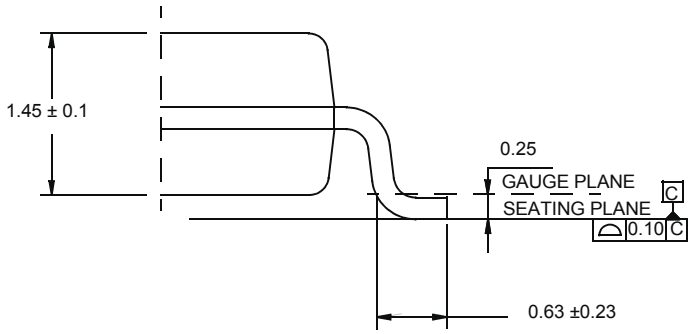
TOP VIEW



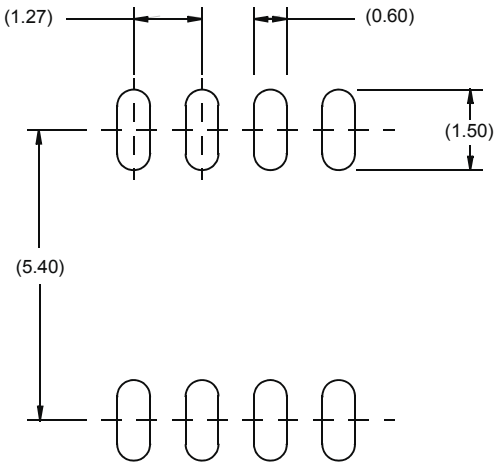
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.