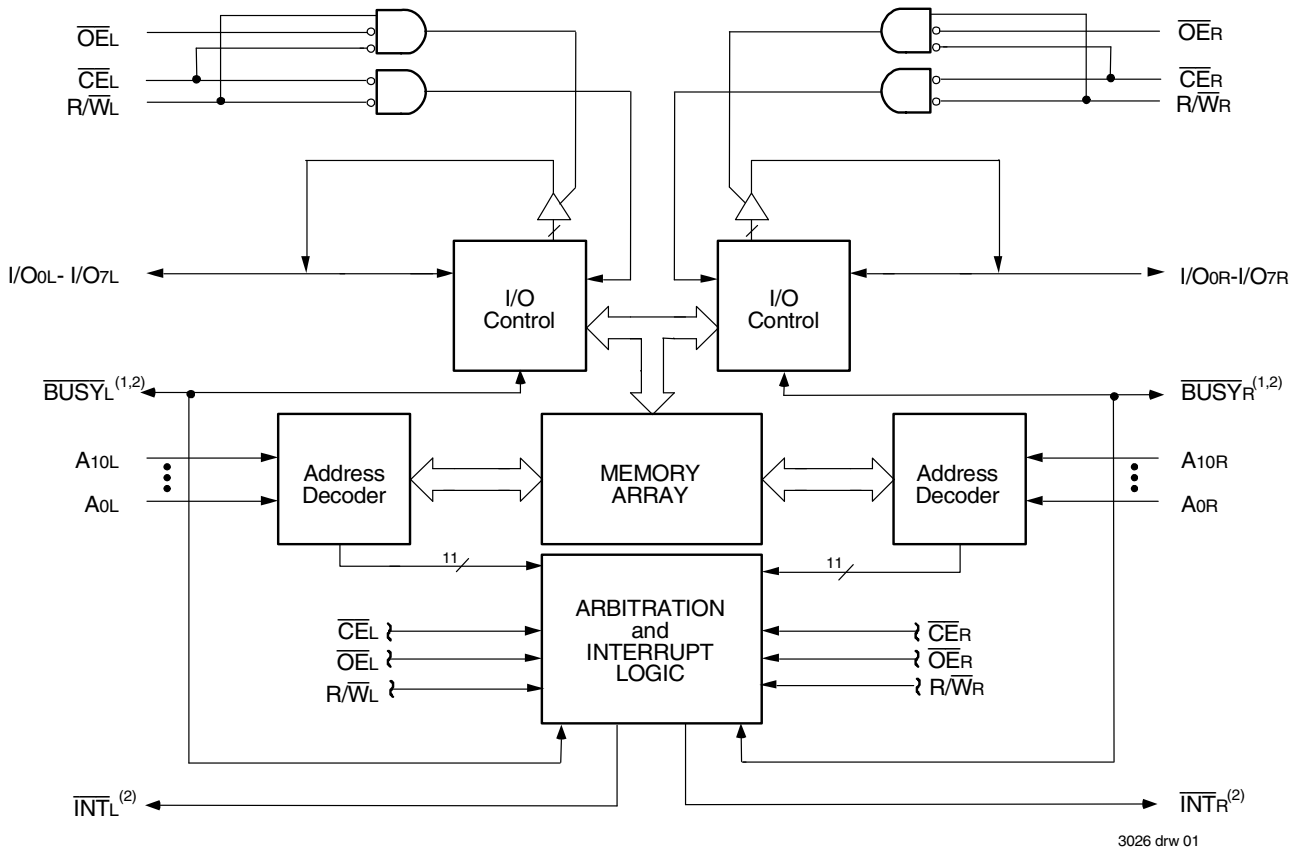
HIGH SPEED 3.3V 2K X 8 DUAL-PORT STATIC RAM WITH INTERRUPTS

71V321L

Features

- **High-speed access**
  - *Commercial & Industrial: 25/35ns (max.)*
- **Low-power operation**
  - *IDT71V321L*
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- **Two $\overline{INT}$ flags for port-to-port communications**
- **On-chip port arbitration logic (IDT71V321 only)**
- **$\overline{BUSY}$ output flag**
- **Fully asynchronous operation from either port**
- **Battery backup operation—2V data retention (L only)**
- **TTL-compatible, single 3.3V power supply**
- **Available in 52-pin PLCC, 64-pin TQFP and STQFP packages**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



3026 drw 01

NOTES:
1. IDT71V321 (MASTER): $\overline{BUSY}$ is an output
2. $\overline{BUSY}$ and $\overline{INT}$ are totem-pole outputs.

JULY 2019

Description

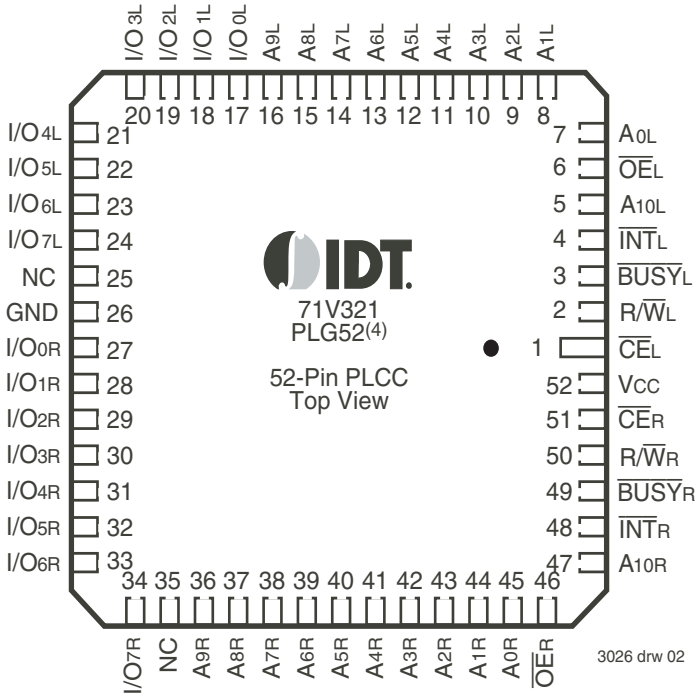
The IDT71V321 is a high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71V321 is designed to be used as a stand-alone 8-bit Dual-Port RAM.

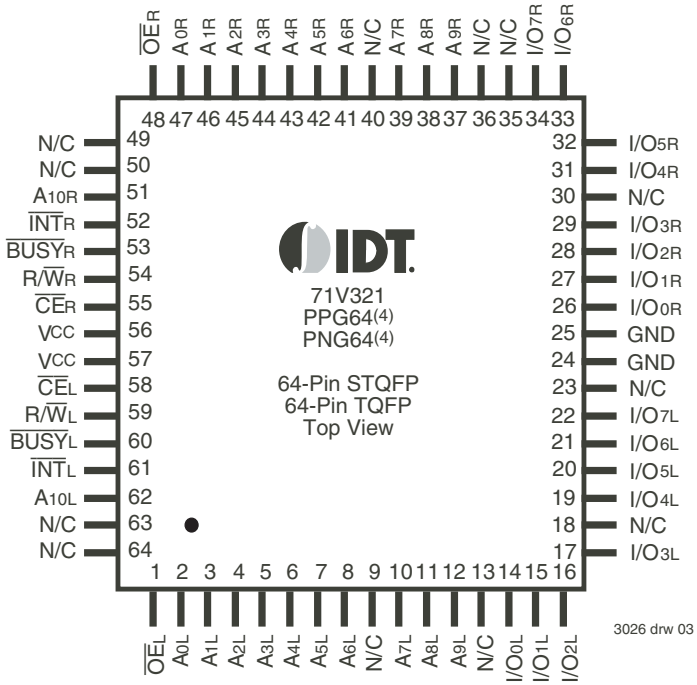
The device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 325mW of power. Low-power (L) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71V321 devices are packaged in a 52-pin PLCC, a 64-pin TQFP (thin quad flatpack), and a 64-pin STQFP (super thin quad flatpack).

Pin Configurations[1,2,3]





NOTES:

1. All VCC pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. J52-1 package body is approximately .75 in x .75 in x .17 in.
   PP64-1 package body is approximately 10mm x 10mm x 1.4mm.
   PN64-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

3026 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Capacitance(1)

(TA = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

3026 tbl 04

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Recommended Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3026 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

3026 tbl 03

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	71V321S		71V321L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = 3.6V	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3026 tbl 05

NOTE:
1. At $V_{CC} \leq$ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,2] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		71V321X25 Com'l & Ind Typ.	71V321X25 Com'l & Ind Max.	71V321X35 Com'l & Ind Typ.	71V321X35 Com'l & Ind Max.	71V321X55 Com'l & Ind Typ.	71V321X55 Com'l & Ind Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	55	130	55	125	55	115	mA
				L	55	100	55	95	55	85	
			IND	L	55	130	55	125	55	115	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	15	35	15	35	15	35	mA
				L	15	20	15	20	15	20	
			IND	L	15	35	15	35	15	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	25	75	25	70	25	60	mA
				L	25	55	25	50	25	40	
			IND	L	25	75	25	70	25	60	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	3	0.2	3	0.2	3	
			IND	L	0.2	6	1.0	5	1.0	5	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	S	25	70	25	65	25	55	mA
				L	25	55	25	50	25	40	
			IND	L	25	70	25	65	25	55	

3026 tbl 06

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 70mA (Typ.).
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC} and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

Data Retention Characteristics (L Version Only)

Symbol	Parameter	Test Condition		Min.	Typ. [1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2v, $\overline{CE}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		COM'L.	—	100	500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		IND.	—	100	1000	µA
				0	—	—	V
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	V

3026 tbl 07

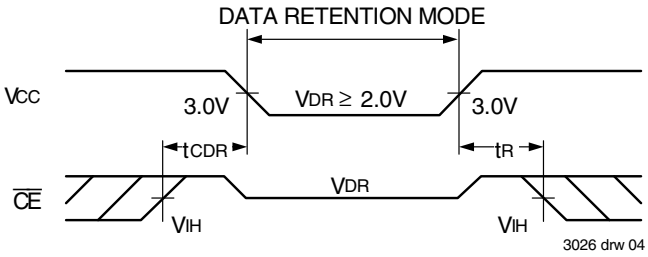
NOTES:
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3026 tbl 08

Data Retention Waveform



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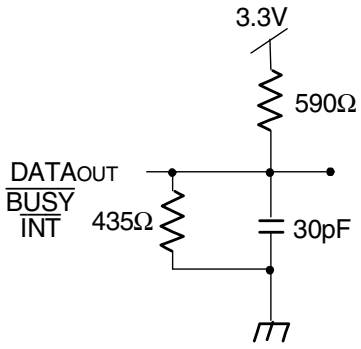


Figure 1. AC Output Test Load

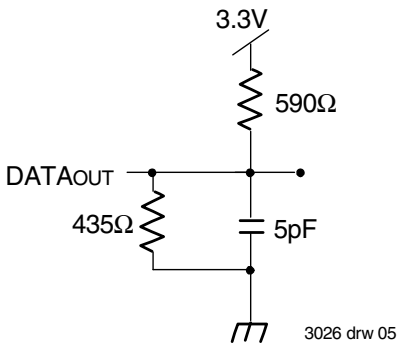


Figure 2. Output Test Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})
* Including scope and jig.

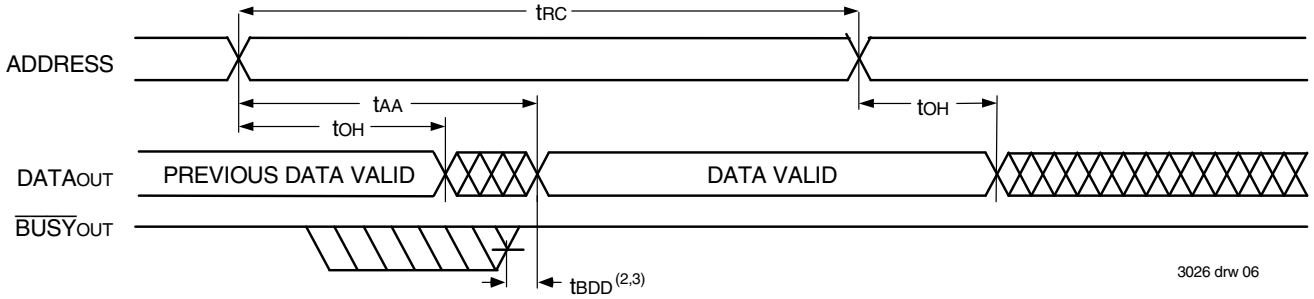
AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[2]

Symbol	Parameter	71V321X25 Com'l & Ind		71V321X35 Com'l & Ind		71V321X55 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	35	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	12	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns

3026 tbl 09

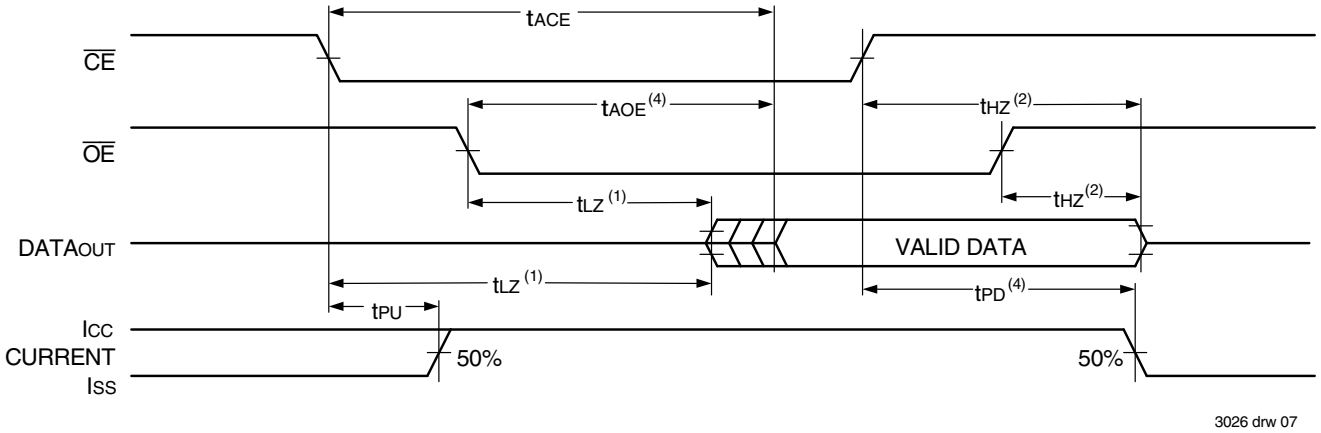
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Read Cycle No. 1, Either Side(1)



NOTES:
1. R/$\overline{W}$ = V_{IH}, $\overline{CE}$ = V_{IL}, and is $\overline{OE}$ = V_{IL}. Address is valid prior to the coincidental with $\overline{CE}$ transition LOW.
2. t_{BDD} delay is required only in the case where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA}, and t_{BDD}.

Timing Waveform of Read Cycle No. 2, Either Side (3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH} and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA}, and t_{BDD}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4]

Symbol	Parameter	71V321X25 Com'l & Ind		71V321X35 Com'l & Ind		71V321X55 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	30	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2]	0	—	0	—	0	—	ns

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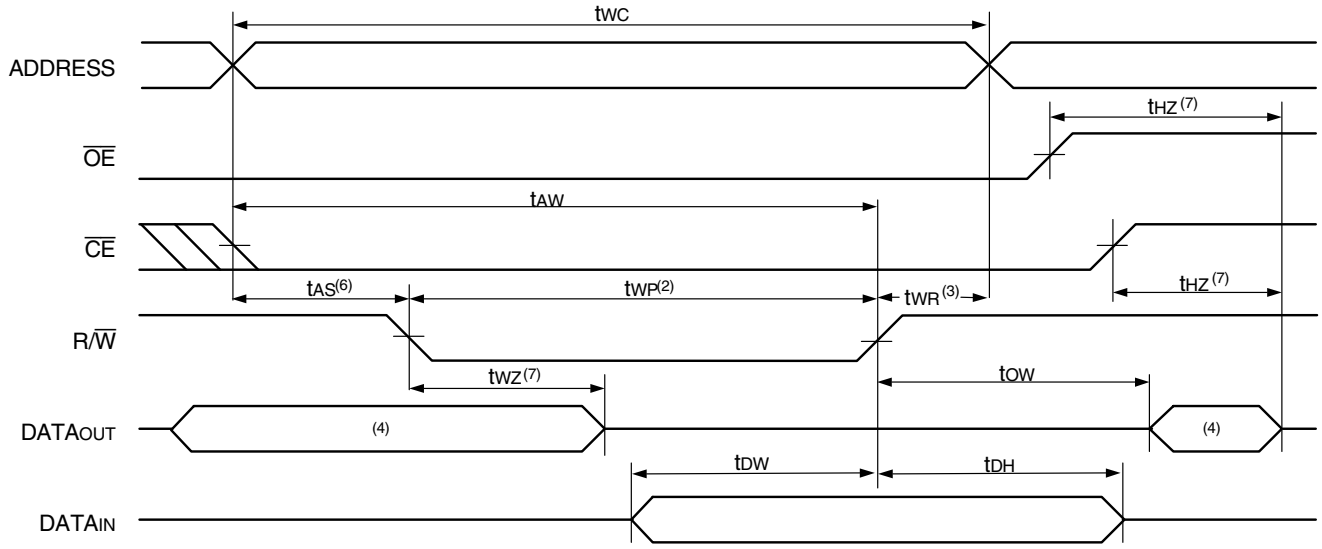
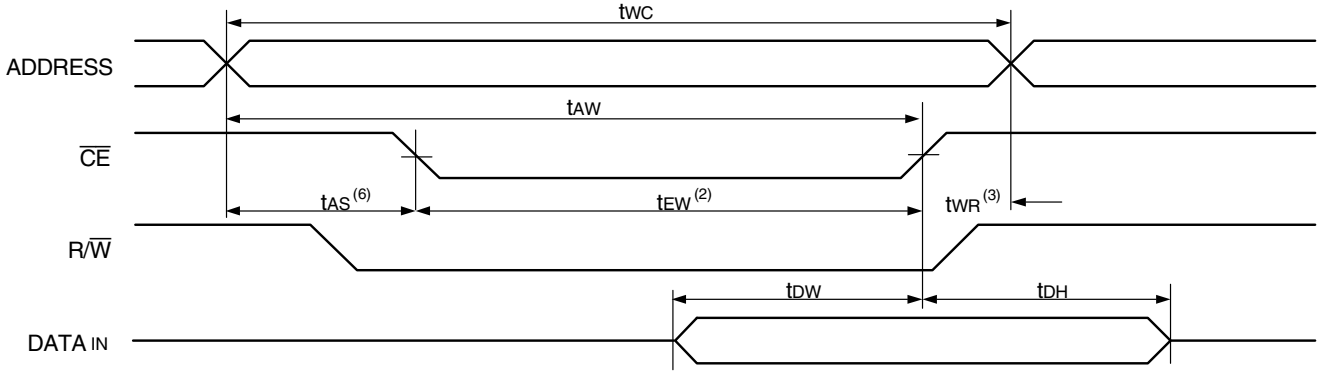
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, (R/$\overline{W}$ Controlled Timing)(1,5,8)



3026 drw 08

Timing Waveform of Write Cycle No. 2, ($\overline{CE}$ Controlled Timing)(1,5)



3026 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of $\overline{CE}$ = VIL and R/W= VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined to be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

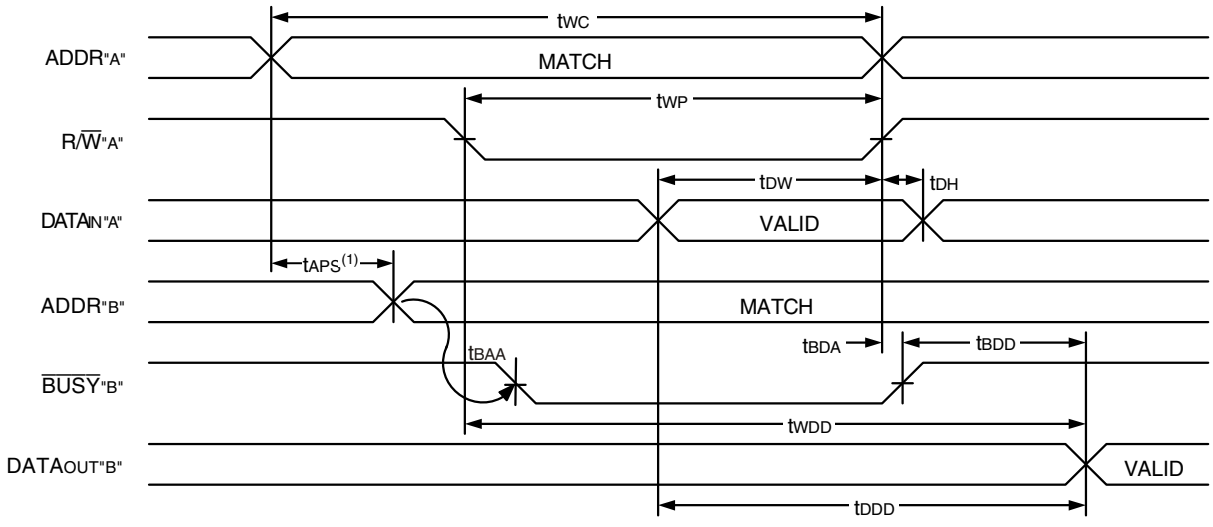
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6)

		71V321X25 Com'l & Ind		71V321X35 Com'l & Ind		71V321X55 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
$\overline{BUSY}$ Timing								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	30	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	45	—	65	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
t_{BDD}	BUSY Disable to Valid Data(3)	—	30	—	30	—	45	ns

3026 tbl 11

NOTES:
1. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$."
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that a write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (S or L).

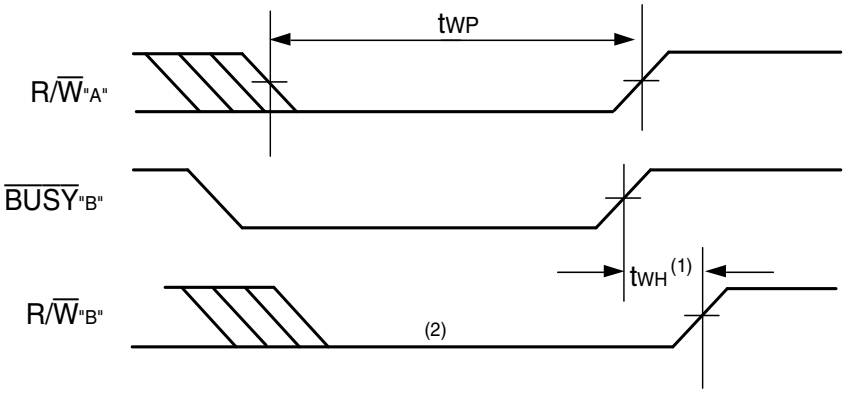
Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$(2,3,4)



3026 drw 10

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE}$ = V_{IL} for the reading port.
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

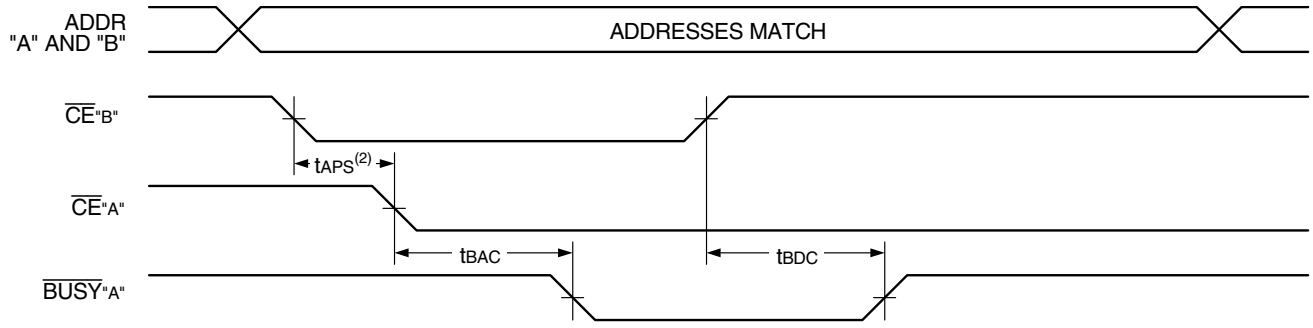
Timing Waveform of Write with $\overline{BUSY}$(3)



3026 drw 11

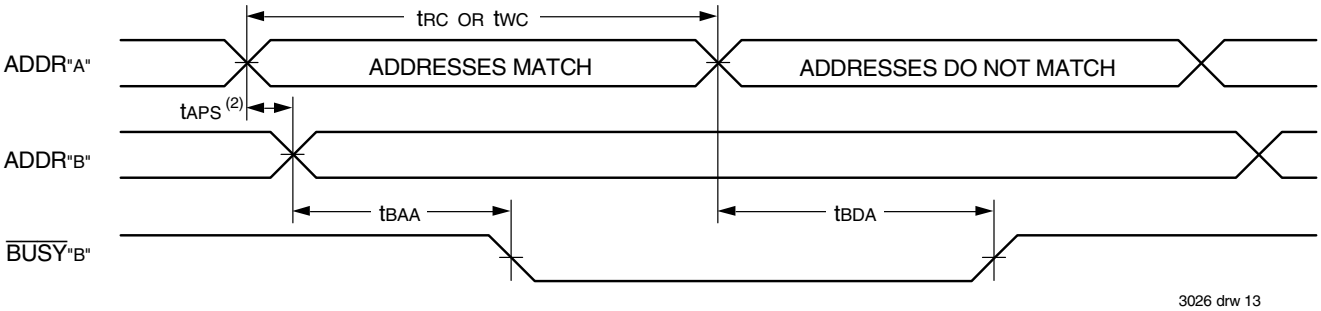
NOTES:
1. t_{WH} must be met for $\overline{BUSY}$ output 71V321.
2. $\overline{BUSY}$ is asserted on port 'B' blocking $R/\overline{W}_{'B'}$, until $\overline{BUSY}_{'B'}$ goes HIGH.
3. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing(1)



3026 drw 12

Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by Address Match Timing(1)



3026 drw 13

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

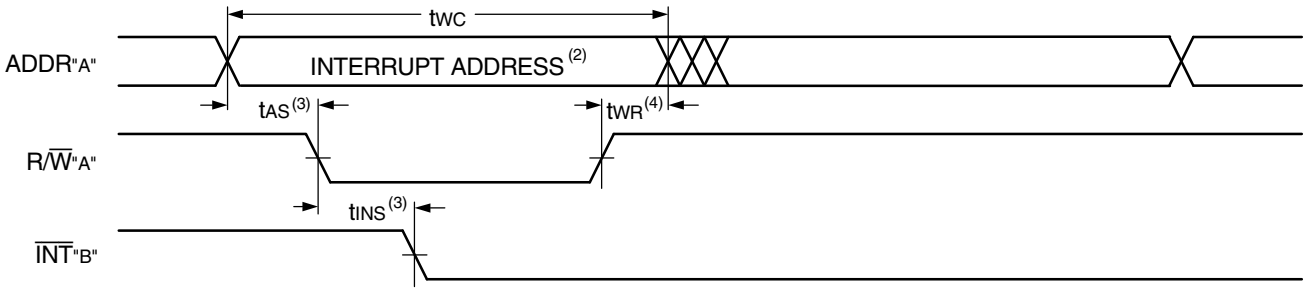
		71V321X25 Com'l & Ind		71V321X35 Com'l & Ind		71V321X55 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	25	—	45	ns
t_{INR}	Interrupt Reset Time	—	25	—	25	—	45	ns

3026 tbl 12

NOTES:
1. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Interrupt Mode(1)

SET $\overline{INT}$



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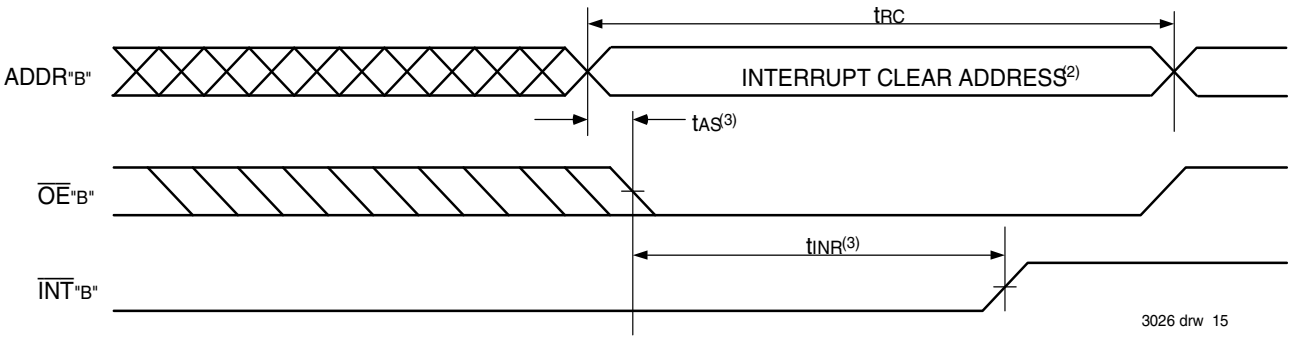
CLEAR $\overline{INT}$



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NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Tables

Table I — Non-Contention Read/Write Control(4)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Deselected and in Power-Down Mode. I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High-impedance Outputs

3026 tbl 13

NOTES:
1. $A_{0L} - A_{10L} \neq A0R - A10R$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = High-impedance.

Table II — Interrupt Flag(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{10L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{10R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

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NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH, 'L' = LOW, 'X' = DON'T CARE

Table III — Address **$\overline{BUSY}$** Arbitration

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{OL}-A_{10L} A_{OR}-A_{10R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3026 tbl 15

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs. $\overline{BUSY}_X$ outputs on the IDT71V321 are totem-pole.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Functional Description

The IDT7V1321 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V321 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per Truth Table II. The left port clears the interrupt by accessing address location 7FE when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/W is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ Logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation.

Depth Expansion

The $\overline{BUSY}$ arbitration, is based on the chip enable and address signals only. It ignores whether an access is a read or write.

The $\overline{BUSY}$ outputs on the IDT71V321 are totem-pole type outputs and do not require pull-up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate

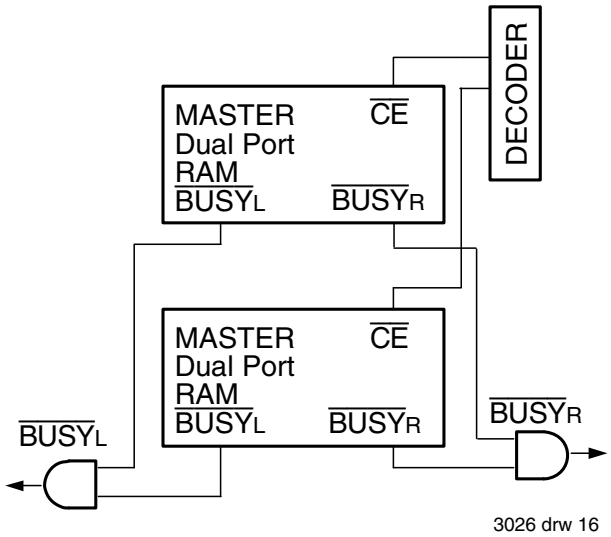
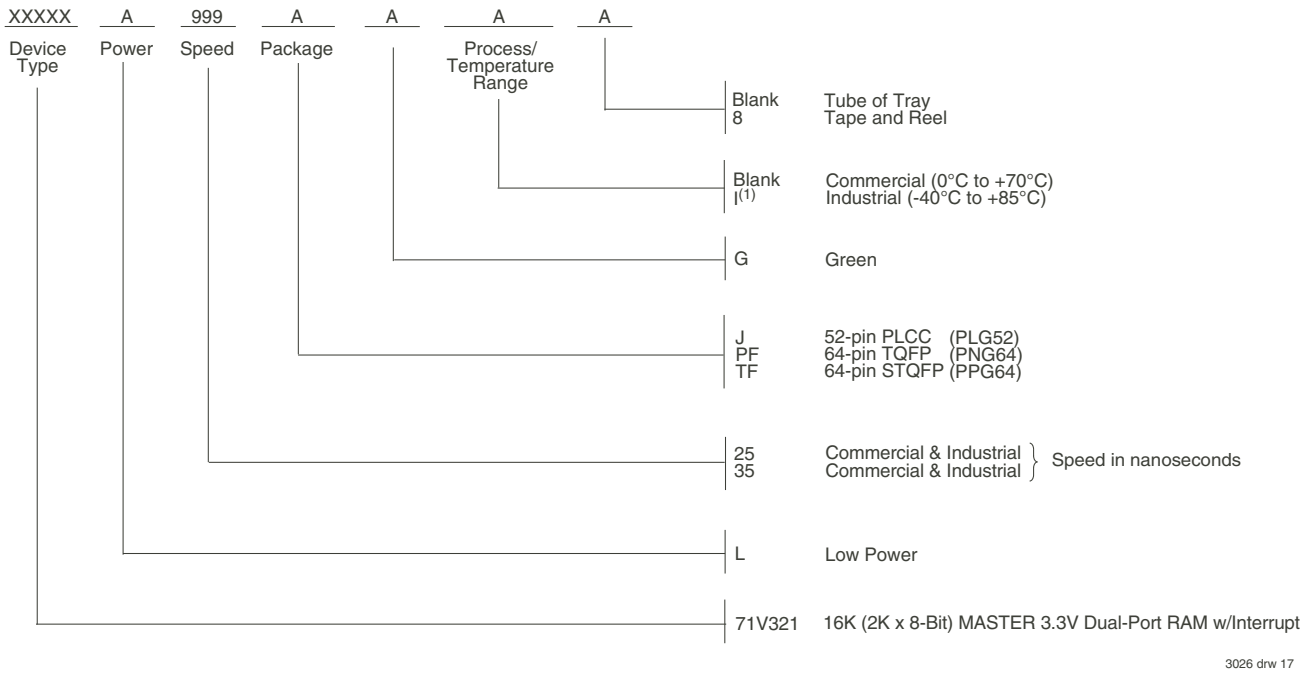


Figure 3. Busy and chip enable routing for depth expansion with IDT71V321.

Ordering Information



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NOTES:

1. Contact your sales office Industrial temperature range is available for selected speeds, packages and powers.

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	71V321L25JG	PLG52	PLCC	C
	71V321L25JG8	PLG52	PLCC	C
	71V321L25PFG	PNG64	TQFP	C
	71V321L25PFG8	PNG64	TQFP	C
	71V321L25PFGI	PNG64	TQFP	I
	71V321L25PFGI8	PNG64	TQFP	I
	71V321L25TFG	PPG64	TQFP	C
	71V321L25TFG8	PPG64	TQFP	C
	71V321L25TFGI	PPG64	TQFP	I
35	71V321L35JG	PLG52	PLCC	C
	71V321L35JG8	PLG52	PLCC	C
	71V321L35JGI	PLG52	PLCC	I
	71V321L35JGI8	PLG52	PLCC	I
	71V321L35PFGI	PNG64	TQFP	I
	71V321L35PFGI8	PNG64	TQFP	I

Datasheet Document History

03/24/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Page 2 Added additional notes to pin configurations
06/15/99:	Changed drawing format
10/15/99:	Page 12 Changed open drain to totem-pole in Table III, note 1
10/21/99:	Page 13 Deleted 'does not' in copy from Busy Logic
11/12/99:	Replaced IDT logo
01/12/01:	Page 1 & 2 Moved full "Description" to page 2 and adjusted page layouts
	Page 3 Increased storage temperature parameters
	Clarified T_A parameter
	Page 4 DC Electrical parameters–changed wording from "open" to "disabled"
	Changed ±200mV to 0mV in notes
08/22/01:	Page 4, 5, 7, 9 &11 Industrial temp range offering removed from DC & AC Electrical Chars for 35 and 55ns
01/17/06:	Page 1 Added green availability to features
	Page 14 Added green indicator to ordering information
	Page 1 & 14 Replaced old IDT™ with new IDT™ logo
08/25/06:	Page 11 Changed $\overline{INT}$"A" to $\overline{INT}$"B" in the CLEAR $\overline{INT}$ drawing in the Timing Waveform of Interrupt Mode
10/23/08:	Page 14 Removed "IDT" from orderable part number
01/25/10:	Page 4 In order to correct the DC Chars table for the 71V321/71V421L35 speed grade and the Data Retention Chars table, I Temp values have been added to each table respectively. In addition, all of the AC Chars tables and the ordering information also now reflect this I temp correction
06/25/15:	Page 2 Removed IDT in reference to fabrication
	Page 2 & 14 The package codes J52-1, PN64-1 & PP64-1 changed to J52, PN64 & PP64 respectively to match standard package codes
	Page 14 Added Tape and Reel indicator to Ordering Information
10/14/15:	Page 1 -15 Removed 71V421S/L from the part number, in the pin configurations and throughout the datasheet
	Page 1 - 15 Removed all references to Master/Slave throughout the datasheet
	Page 1 -15 Updated the Com'l and Ind speeds for the 25/35/55ns offerings in Features , in the DC & AC Chars tables, in the Ordering Information and throughout the datasheet
	Page 13 Removed Width Expansion with Busy Logic Master/Slave Arrays diagram for part numbers 71V321/71V421S/ L and updated with a Depth Expansion diagram for the single part number 71V321S/L
	Updated the corresponding Depth Expansion descriptive text in the Depth Expansion section of the datasheet
01/12/18:	Product Discontinuation Notice - PDN# SP-17-02
	Last time buy expires June 15, 2018
07/23/19:	Page 2 Updated package codes J52 to PLG52, PP64 to PPG64 and PN64 to PNG64
	Page 14 Added Orderable Part Information table

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