CURRENT MODE PWM CONTROLLER

DESCRIPTION

The UC3842B/43B/44B/45B are fixed frequency current mode PWM controller. They are specially designed for OFF–Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Protection circuitry includes built under voltage lockout and current limiting.

The UC3842B, UC3844B have UVLO thresholds of 16 V (on) and 10 V (off).

The corresponding thresholds for the UC3843B, UC3845B are 8.4V (on) and 7.6V (off).

The UC3842B, UC3843B can operate within 100% duty cycle.

The UC3844B, UC3845B can operate within 50% duty cycle.

The UC3842B/43B/44B/45B is characterized for operation from TA = -40°C to 85°C.

ORDERING INFORMATION

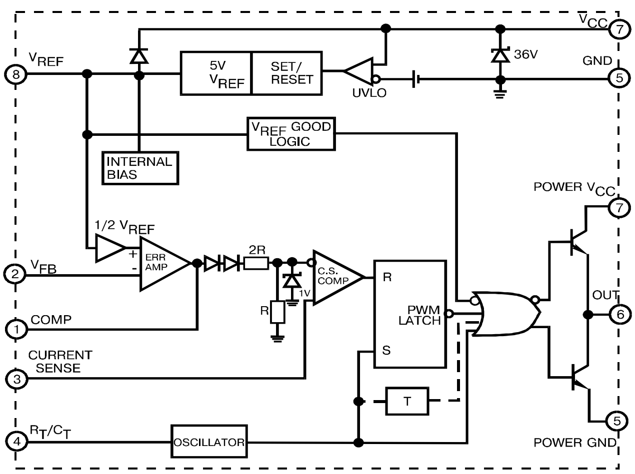
DEVICE	Package Type	MARKING	Packing	Packing Qty
UC3842BN	DIP8	UC3842B	TUBE	2000/box
UC3843BN	DIP8	UC3843B	TUBE	2000/box
UC3844BN	DIP8	UC3844B	TUBE	2000/box
UC3845BN	DIP8	UC3845B	TUBE	2000/box
UC3842BM/TR	SOP8	UC3842B	REEL	2500/reel
UC3843BM/TR	SOP8	UC3843B	REEL	2500/reel
UC3844BM/TR	SOP8	UC3844B	REEL	2500/reel
UC3845BM/TR	SOP8	UC3845B	REEL	2500/reel

FEATURES

- Low Start-Up and Operating Current
- High Current Totem Pole Output
- Under voltage Lockout With Hysteresis
- Operating Frequency Up To 500KHz

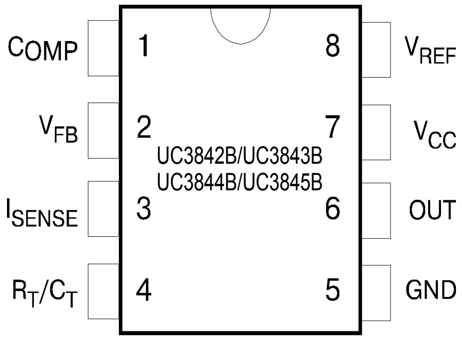
BLOCK DIAGRAM

(toggle flip flop used only in UC3844B, UC3845B)



PIN CONNECTION

(TOP VIEW)



DIP8/SOP8

PIN FUNCTION

N	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	V_{CC}	This pin is the positive supply of the integrated circuit.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T .

Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage (low impedance source)	V_{CC}	30	V
Output Current	I_O	± 1	A
Input Voltage (Analog Inputs pins 2,3)	V_I	−0.3 to 5.5	V
Error Amp Output Sink Current	$I_{SINK\ (E.A)}$	10	mA
Power Dissipation (T_A=25°C)	P_O	1	W
Storage Temperature Range	Tstg	-65 to150	°C
Lead Temperature (soldering 5 sec.)	T_L	260	°C

Electrical characteristics (*V_{CC}=15V, R_T=10kΩ, C_T=3.3nF, T_A=0°C to +70°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	V_{REF}	T_J = 25°C, I_{REF} = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	12V ≤ V_{CC} ≤ 25 V		6.0	20	mV
Load Regulation	ΔV_{REF}	1 mA ≤ I_{REF} ≤ 20mA		6.0	25	
Short Circuit Output Current	I_{SC}	T_A = 25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T_J = 25°C	47	52	57	KHz
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	12V ≤ V_{CC} ≤ 25 V		0.05	1.0	%
Oscillator Amplitude	$V_{(OSC)}$	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I_{BIAS}	V_{FB}=3V		-0.1	-2	µA
Input Voltage	$V_{I(E.A)}$	V_{pin1} = 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V ≤ V_0 ≤ 4V	65	90		dB
Unity Gain Bandwidth	UGBW	T_j=25°C, Note 3	0.5	0.6		MHz
Power Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		dB
Output Sink Current	I_{SINK}	V_{pin2} = 2.7V, V_{pin1} = 1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_{pin2} = 2.3V, V_{pin1} = 5V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{pin2} = 2.3V, R_L = 15KΩ to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{pin2} = 2.7V, R_L = 15KΩ to PIN 8		0.8	1.1	
Current Sense Section						
Gain	G_V	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{pin1} = 5V (Note1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V_{CC} ≤ 25 V (Note 1)		70		dB
Input Bias Current	I_{BIAS}	V_{pin3} = 3V		-3.0	-10	µA
Output Section						
Low Output Voltage	V_{OL}	I_{SINK} = 20 mA		0.08	0.4	V
		I_{SINK} = 200 mA		1.4	2.2	
High Output Voltage	V_{OH}	I_{SINK} = 20 mA	13	13.5		
		I_{SINK} = 200 mA	12	13.0		
Rise Time	t_R	T_J = 25°C, C_L = 1nF (Note 3)		45	150	nS
Fall Time	t_F	T_J = 25°C, C_L = 1nF (Note 3)		35	150	
Undervoltage Lockout Section						
Start Theshold	$V_{TH(ST)}$	UC3842B,UC3844B	14.5	16.0	17.5	V
		UC3843B,UC3845B	7.8	8.4	9.0	
Min. Operating Voltage (After Turn On)	$V_{OPR(min)}$	UC3842B,UC3844B	8.5	10	11.5	V
		UC3843B,UC3845B	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	$D_{(MAX)}$	UC3842B,UC3843B	95	97	100	%
		UC3844B,UC3845B	47	48	50	
Min. Duty Cycle	$D_{(MAX)}$				0	
Total Standby Current						
Start–Up Current	I_{ST}	UC3842B/43B/44B/45B		0.17	0.3	mA
Operating Supply Current	$I_{CC\ (OPR)}$	V_{pin3} = V_{pin2} = 0V		13	17	
Zener Voltage	V_Z	I_{CC}=25 mA	30	38		V

* Adjust V_{CC} above the start threshold before setting it to 15V.
Note 1: Parameter measured at trip point of latch with V_{pin2}=0.
Note 2: Gain defined as $A=\Delta V_{pin1}/\Delta V_{pin3}$; $0 \le V_{pin3} \le 0.8V$.
Note 3: These parameters, although guaranteed, are not 100% tested in production.

APPLICATION INFORMATION

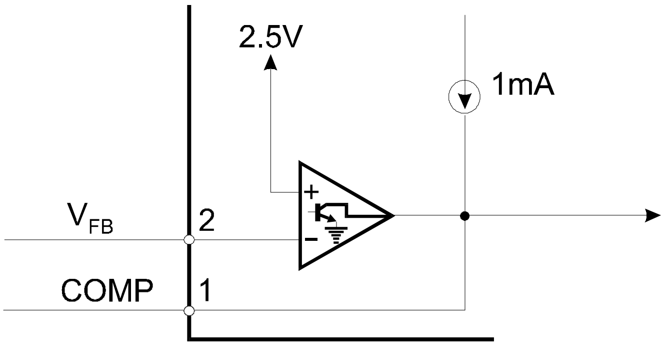
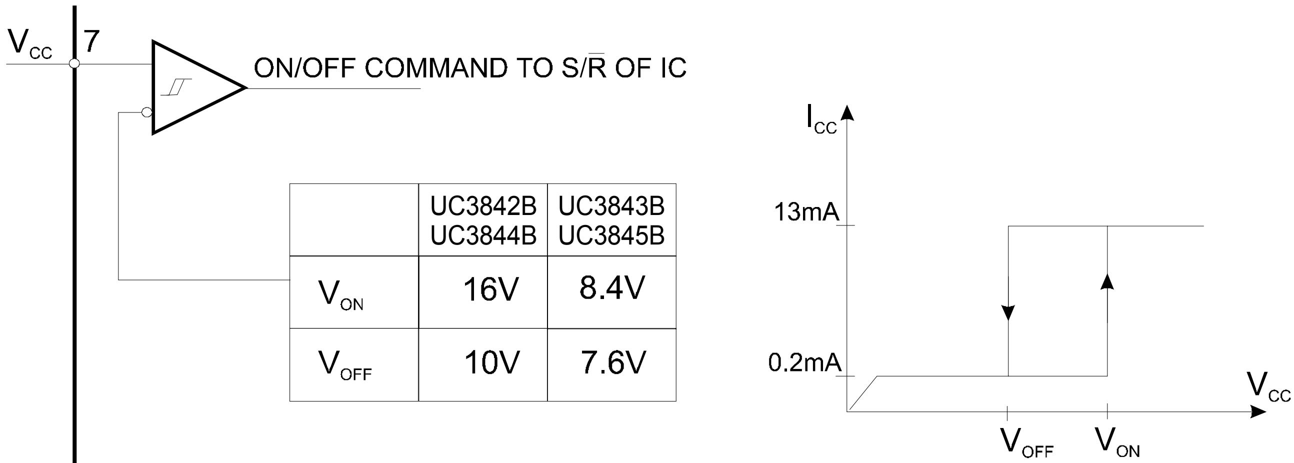


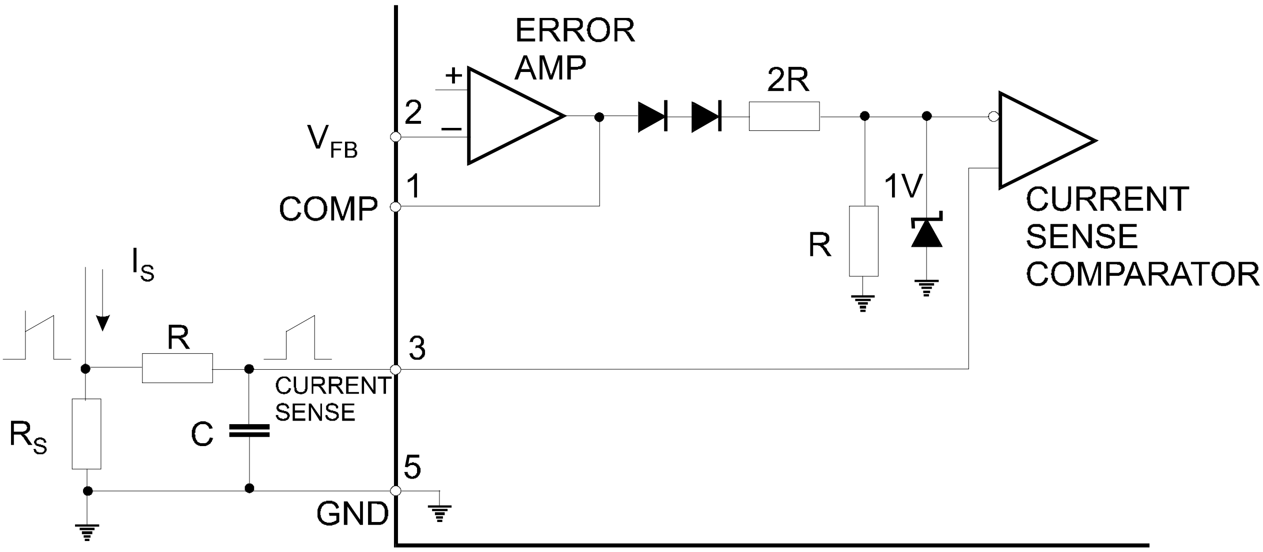
Figure 1. Error Amp Configuration



	UC3842B UC3844B	UC3843B UC3845B
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

During UVLO, the Output is low

Figure 2. Under voltage Lockout



Peak current is determined by $I_{S\ max} \approx \frac{1.0V}{R_S}$

Figure 3. Current Sense Circuit

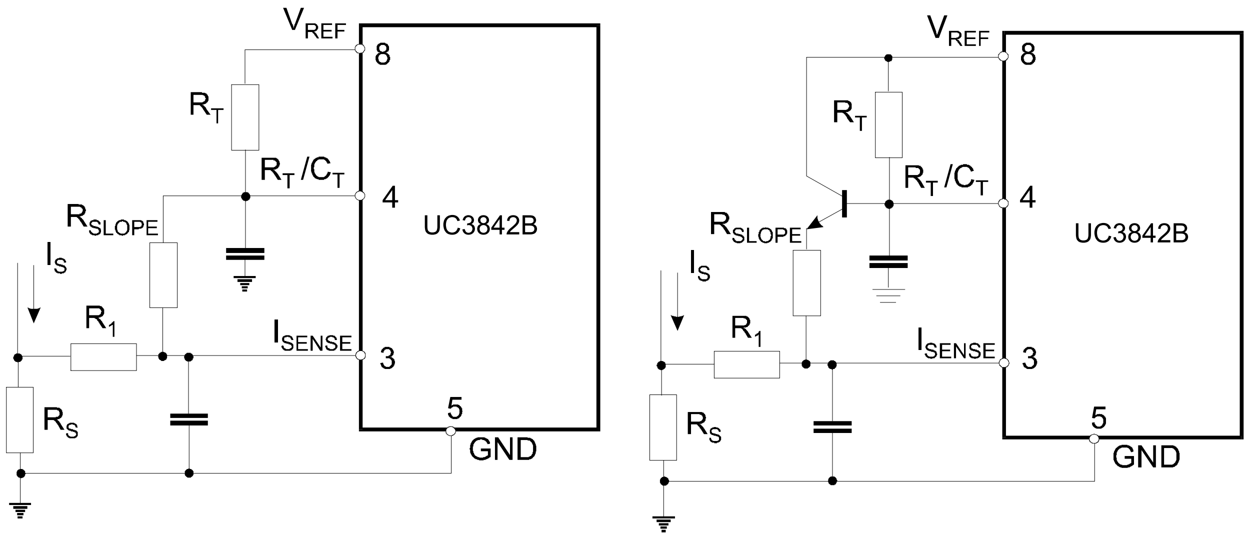
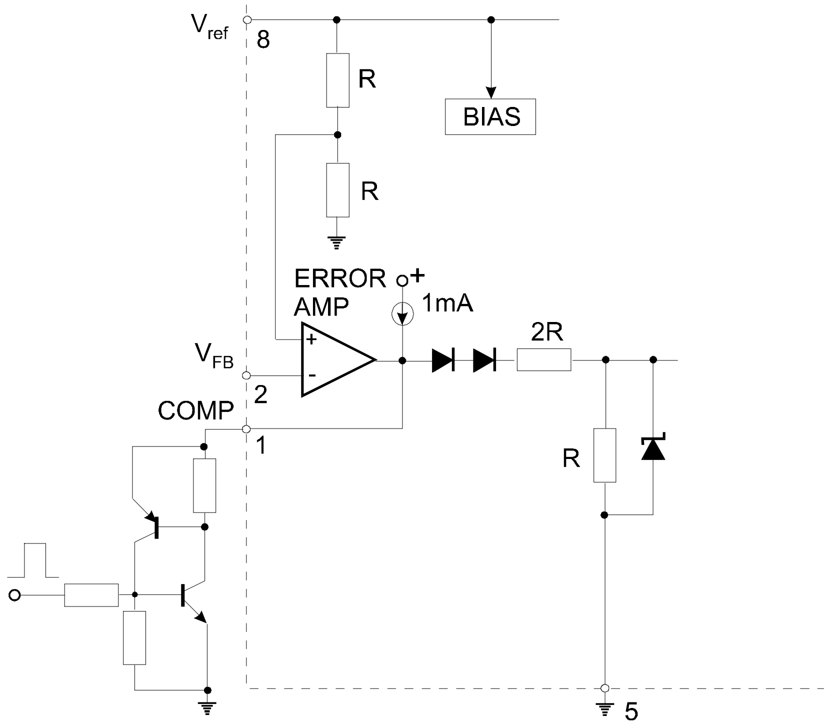
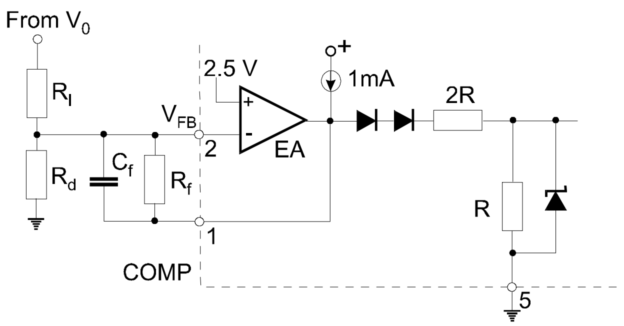


Figure 4. Slope Compensation Techniques

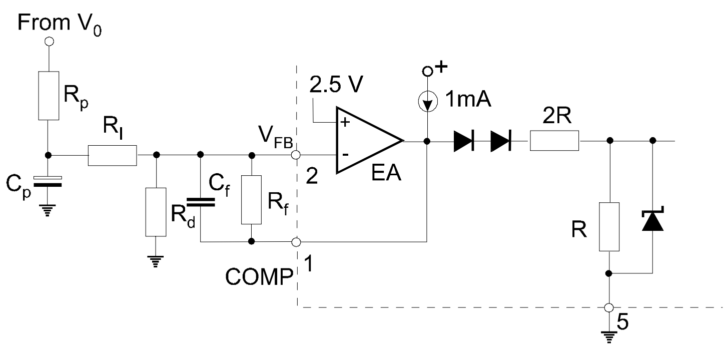


SCR must be selected for a holding current of less than 0.5mA.
The simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

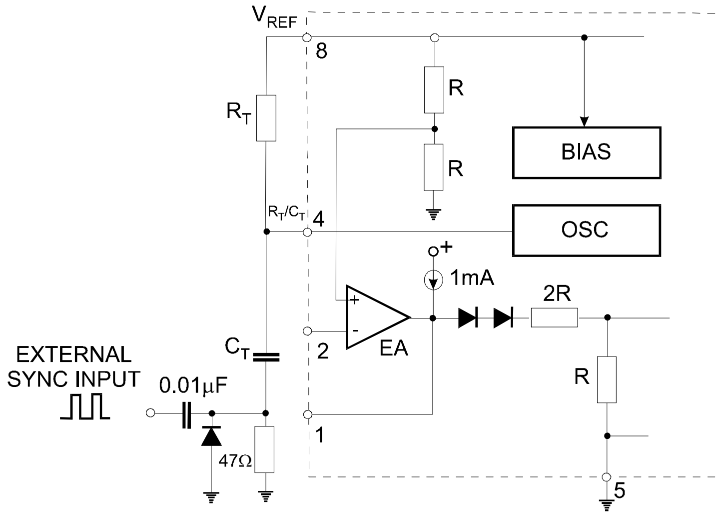


Figure 7. External Clock Synchronization

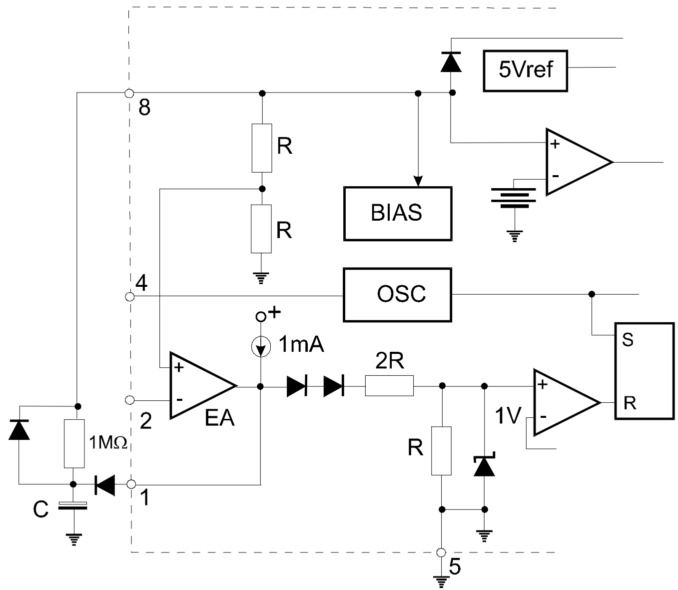


Figure 8. Soft-Start Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

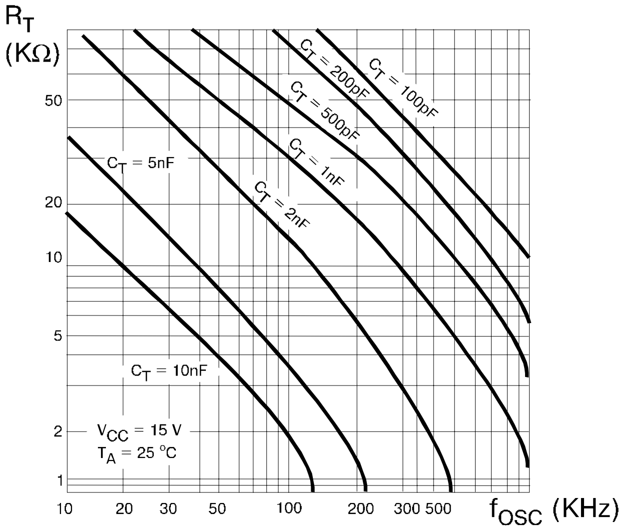


Figure 1. Timing Resistor vs. Oscillator Frequency

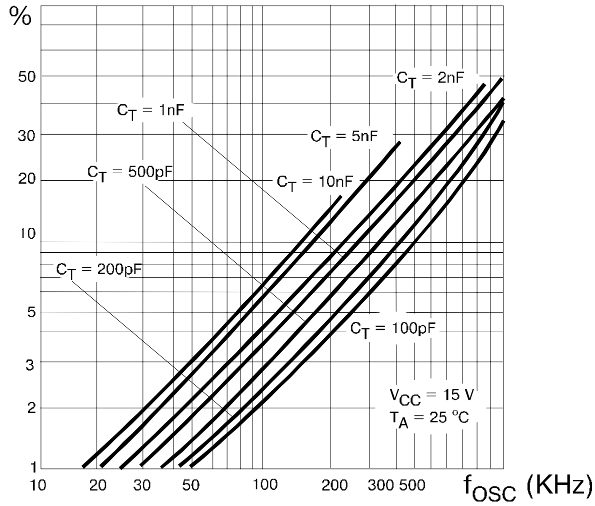


Figure 2. Output Dead-Time vs. Oscillator Frequency

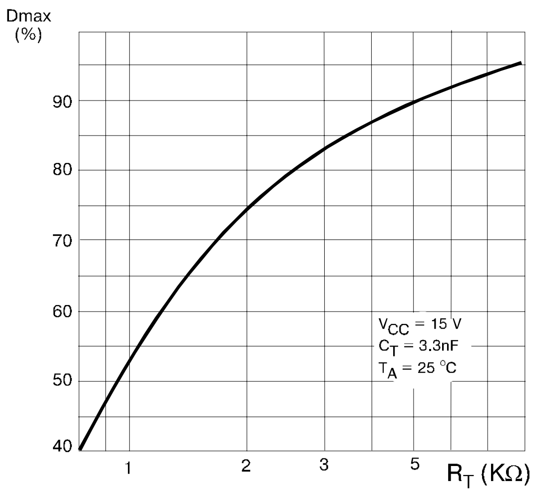


Figure 3. Maximum Output Duty Cycle vs.
Timing Resistor (UC3842B/43B)

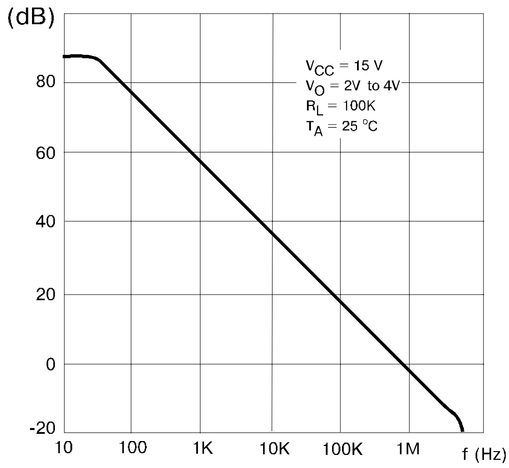


Figure 4. Error Amp Open-Loop Gain vs.
Frequency

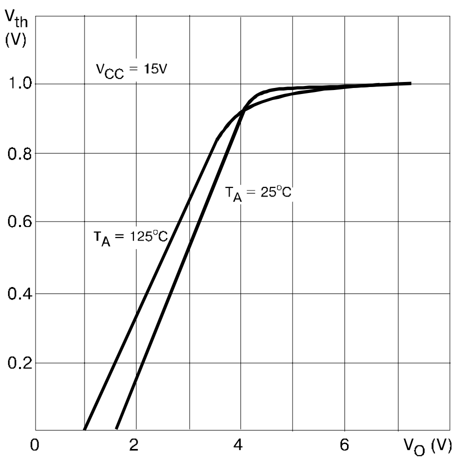


Figure 5. Current Sense Input Threshold vs.
Error Amp Output Voltage

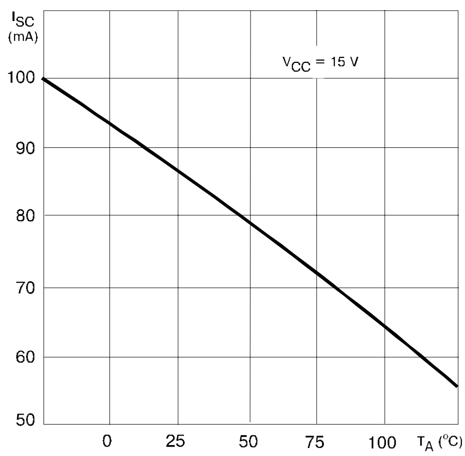


Figure 6. Reference Short Circuit Current vs.
Temperature

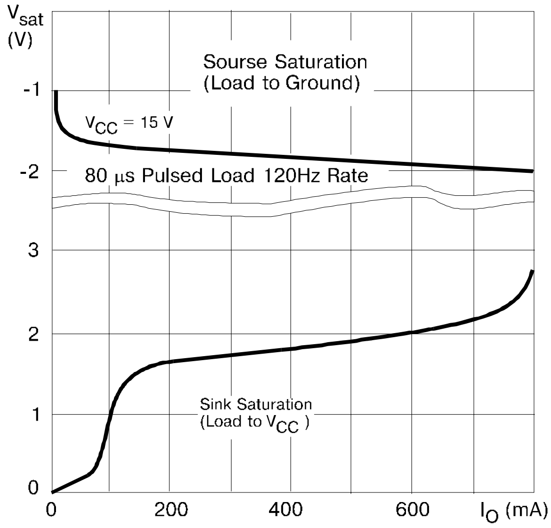


Figure 7. Output Saturation Voltage vs. Load Current
$T_A = 25°C$

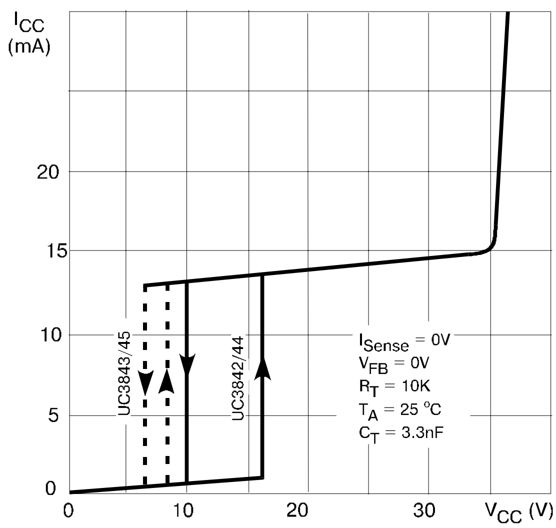


Figure 8. Supply Current vs. Supply Voltage

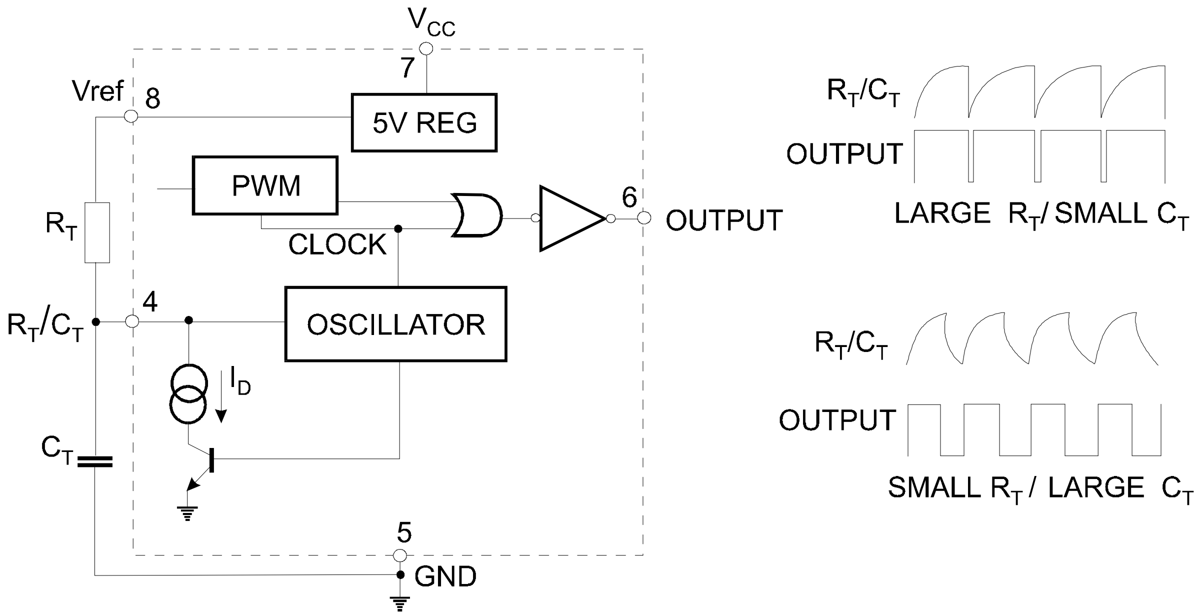
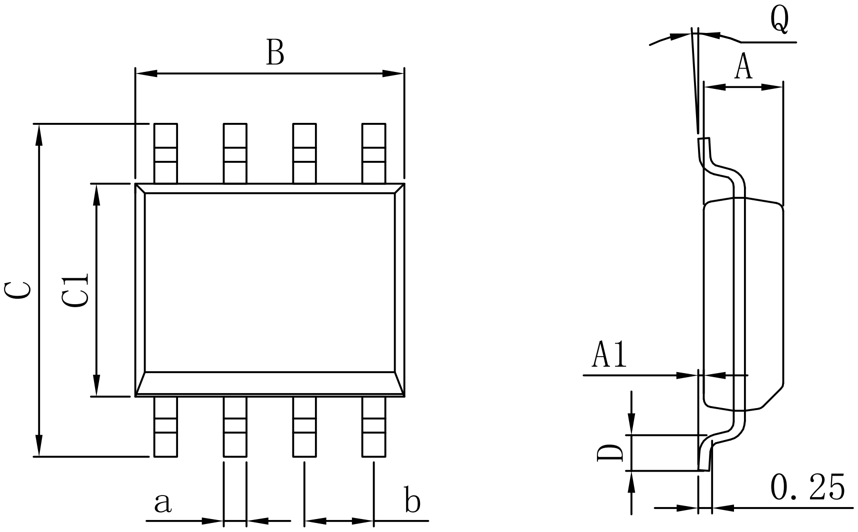


Figure 9. Oscillator and Output Waveforms

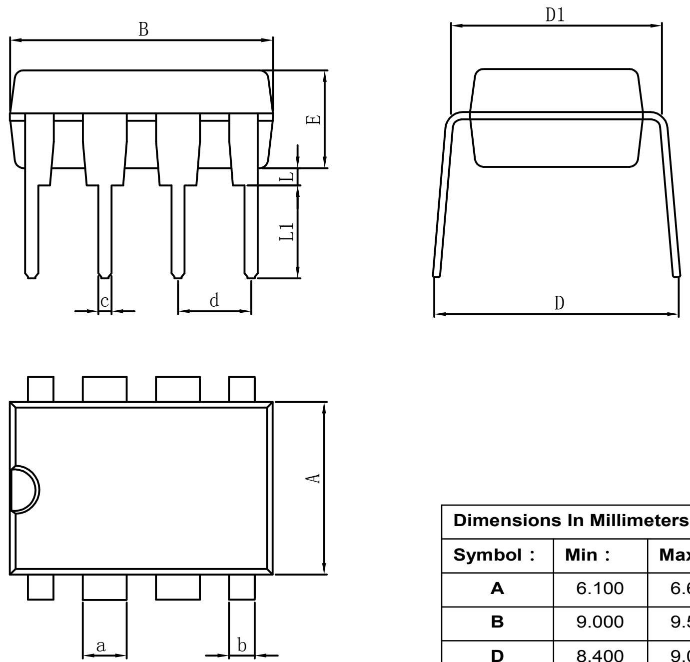
PACKAGE

SOP8



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	4.520	4.620	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	4.800	5.100	**a**	0.420 TYP	
C	5.800	6.250	**b**	1.270 TYP	
C1	3.800	4.000			

DIP8



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	6.100	6.680	**L1**	3.000	3.600
B	9.000	9.500	**a**	1.524 TYP	
D	8.400	9.000	**b**	0.889 TYP	
D1	7.420	7.820	**c**	0.457 TYP	
E	3.100	3.550	**d**	2.540 TYP	
L	0.500	0.700			

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