

# MM54HCT193/MM74HCT193 Synchronous Binary Up/Down Counters

## General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT193/MM74HCT193 is a binary counter having two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT193 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

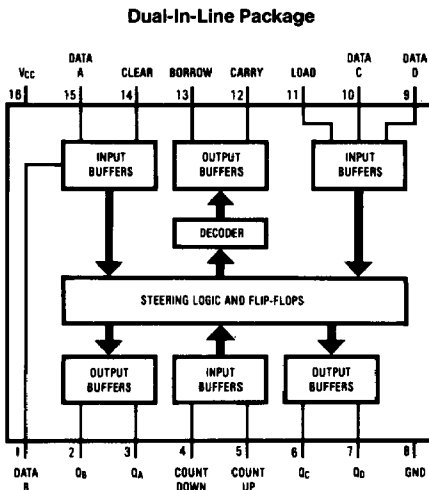
Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

## Features

- Low quiescent supply current: 80  $\mu$ A maximum (74HCT Series)
- Low input current: 1  $\mu$ A maximum
- TTL compatible inputs

## Connection Diagram



**Order Number MM54HCT193\* or MM74HCT193\***

\*Please look into Section 8, Appendix D for availability of various package types.

## Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level

L = low level

↑ = transition from low-to-high

X = don't care

**Absolute Maximum Ratings** (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5V to $V_{CC}$ + 1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC}$ + 0.5V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per Pin ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ or GND Current, per Pin ( $I_{CC}$ )	±50 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )		500	ns

**DC Electrical Characteristics**  $V_{CC} = 5V \pm 10\%$  unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
					$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	
$V_{IH}$	Minimum High Level Input Voltage			2.0	2.0	2.0	V
$V_{IL}$	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$ $ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5\text{V}$ $ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5\text{V}$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
			4.2	3.98	3.84	3.7	V
			5.2	4.98	4.84	4.7	V
$V_{OL}$	Maximum Low Level Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$ $ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5\text{V}$ $ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5\text{V}$	0	0.1	0.1	0.1	V
			0.2	0.26	0.33	0.4	V
			0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$		±0.1	±1.0	±1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$		8.0	80	160	μA
		$V_{IN} = 2.4\text{V}$ or 0.5V (Note 4)		1.0	1.2	1.3	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** Measured per pin, all other inputs held at  $V_{CC}$  or GND.

**AC Electrical Characteristics**(Note 6)  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified)

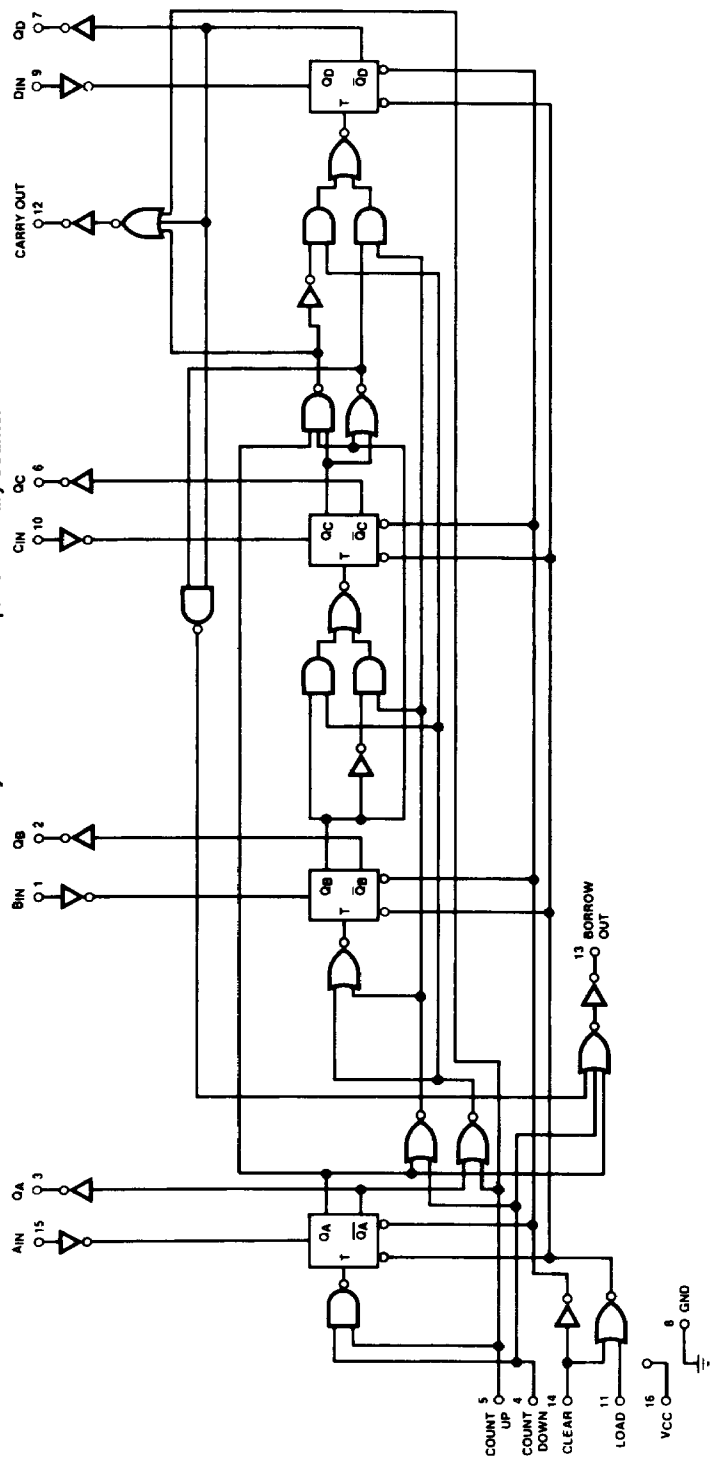
Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Clock Frequency				35		MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A, B, C, D,	QA, QB, QC, QD		25		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Dn	Borrow		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB, QC, QD		25		ns

**AC Electrical Characteristics** (Note 6) $V_{CC} = 5V$ ,  $\pm 10\%$ ,  $C_L = 50\text{ pF}$  (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	T = 25°C	T = 25°C	74HC	54HC	Units
				Typ	Typ	T = -40° to 85°C	T = -55° to 125°C	
				Guaranteed Limits				
$f_{MAX}$	Maximum Clock Frequency			32	20	16	13	MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD	29	44	55	66	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A	QA, QB, QC, QD	28	40	50	60	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB, QC, QD	30	43	54	65	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Down	Borrow	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB, QC, QD	28	35	44	53	ns
$t_W$	Minimum Clock Pulse Width			16	25	31	38	ns
$t_S$	Minimum Setup Time Data before Load-LH			20	25	25	30	ns
$t_H$	Minimum Hold Time Data after Load-LH			-3	5	6	8	ns
$t_{REM}$	Minimum Removal Time Load to Count			-2	5	6	8	ns
$t_{REM}$	Minimum Removal Time Clear to Count			2	5	6	8	ns
$t_W$	Minimum Load Pulse Width			18	20	25	30	ns
$t_W$	Minimum Clear Pulse Width			8	20	25	30	ns
$t_{TLH, THL}$	Output Rise or Fall Time			10	15	19	22	ns
$C_{PD}$	Power Dissipation Capacitance			40				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_s = C_{PD} V_{CC} f + I_{CC}$ .**Note 6:** Refer to Section 1 for Typical MM54/74HCT AC Switchforms and Test Circuits.

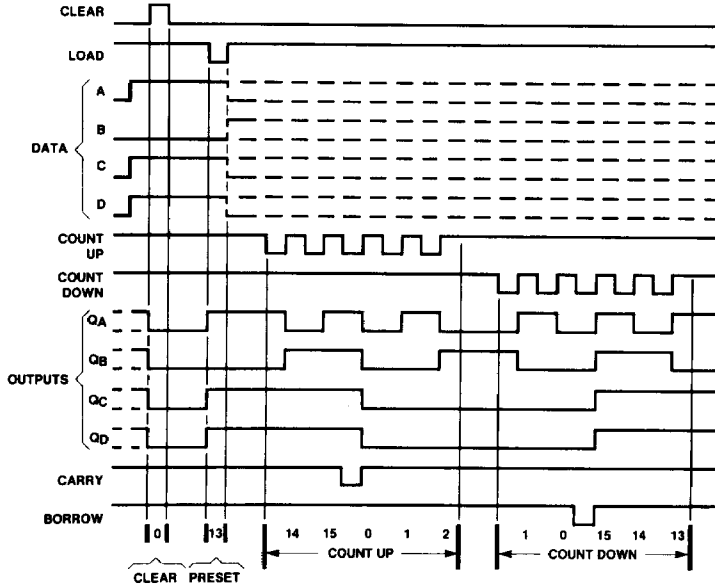
MM54HCT193/MM74HCT193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5742-2

# Logic Waveforms

**'HCT193 Synchronous Binary Counters  
Typical Clear, Load, and Count Sequences**



TL/F/5742-3

**Sequence:**

- (1) Clear outputs to zero.
- (2) Load (preset) to binary thirteen
- (3) Count up to fourteen, fifteen, carry, zero, one, and two.
- (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

**Note A:** Clear overrides load data, and count inputs.

**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.