

# 4-Bit Bidirectional Universal Shift Register

## High-Performance Silicon-Gate CMOS

The MC74HC194 is identical in pinout to the LS194 and the MC14194B metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity 164 FETs or 41 Equivalent Gates

### MC74HC194



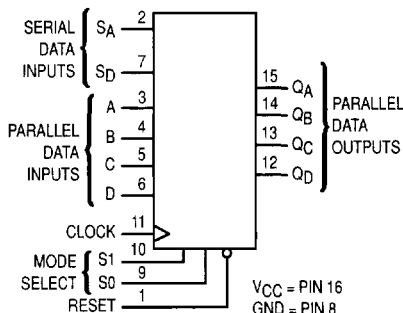
**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

**ORDERING INFORMATION**  
MC74HCXXXN Plastic

#### PIN ASSIGNMENT

|                |   |    |                 |
|----------------|---|----|-----------------|
| RESET          | 1 | 16 | V <sub>CC</sub> |
| S <sub>A</sub> | 2 | 15 | Q <sub>A</sub>  |
| A              | 3 | 14 | Q <sub>B</sub>  |
| B              | 4 | 13 | Q <sub>C</sub>  |
| C              | 5 | 12 | Q <sub>D</sub>  |
| D              | 6 | 11 | CLOCK           |
| S <sub>D</sub> | 7 | 10 | S <sub>1</sub>  |
| GND            | 8 | 9  | S <sub>0</sub>  |

#### LOGIC DIAGRAM



#### FUNCTION TABLE

| Reset | Mode Select    |                | Clock | Serial Data    |                |   |   | Parallel Data |   |                 |                 | Outputs         |                 |               |  | Operating Mode |
|-------|----------------|----------------|-------|----------------|----------------|---|---|---------------|---|-----------------|-----------------|-----------------|-----------------|---------------|--|----------------|
|       | S <sub>1</sub> | S <sub>0</sub> |       | S <sub>D</sub> | S <sub>A</sub> | A | B | C             | D | Q <sub>A</sub>  | Q <sub>B</sub>  | Q <sub>C</sub>  | Q <sub>D</sub>  |               |  |                |
| L     | X              | X              | X     | X              | X              | X | X | X             | X | L               | L               | L               | L               | Reset         |  |                |
| H     | H              | H              | ↗     | X              | X              | a | b | c             | d | a               | b               | c               | d               | Parallel Load |  |                |
| H     | L              | H              | ↗     | X              | H              | X | X | X             | X | H               | Q <sub>An</sub> | Q <sub>Bn</sub> | Q <sub>Cn</sub> | Shift Right   |  |                |
| H     | L              | H              | ↘     | X              | L              | X | X | X             | X | L               | Q <sub>An</sub> | Q <sub>Bn</sub> | Q <sub>Cn</sub> |               |  |                |
| H     | H              | L              | ↗     | H              | X              | X | X | X             | X | Q <sub>Bn</sub> | Q <sub>Cn</sub> | Q <sub>Dn</sub> | H               | Shift Left    |  |                |
| H     | H              | L              | ↘     | L              | X              | X | X | X             | X | Q <sub>Bn</sub> | Q <sub>Cn</sub> | Q <sub>Dn</sub> | L               |               |  |                |
| H     | L              | L              | X     | X              | X              | X | X | X             | X | No Change       |                 |                 |                 | Hold          |  |                |
| H     | X              | X              | L     | X              | X              | X | X | X             | X | No Change       |                 |                 |                 |               |  |                |
| H     | X              | X              | H     | X              | X              | X | X | X             | X | No Change       |                 |                 |                 |               |  |                |

H = high level (steady state)

L = low level (steady state)

X = don't care

↗ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the most recent ↗ transition of the clock.

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**MAXIMUM RATINGS\***

| Symbol           | Parameter   | Value                          | Unit |    |
|------------------|---|--------------------------------|------|----|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)                         | - 0.5 to + 7.0                 | V    |    |
| V <sub>in</sub>  | DC Input Voltage (Referenced to GND)                          | - 1.5 to V <sub>CC</sub> + 1.5 | V    |    |
| V <sub>out</sub> | DC Output Voltage (Referenced to GND)                         | - 0.5 to V <sub>CC</sub> + 0.5 | V    |    |
| I <sub>in</sub>  | DC Input Current, per Pin                                     | ± 20                           | mA   |    |
| I <sub>out</sub> | DC Output Current, per Pin                                    | ± 25                           | mA   |    |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins               | ± 50                           | mA   |    |
| P <sub>D</sub>   | Power Dissipation in Still Air                                | Plastic DIP†                   | 750  | mW |
| T <sub>stg</sub> | Storage Temperature   | - 65 to + 150                  | °C   |    |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) | 260                            | °C   |    |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol                             | Parameter  | Min   | Max             | Unit               |    |
|------------------------------------|--|---|-----------------|--------------------|----|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                | 2.0   | 6.0             | V                  |    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0   | V <sub>CC</sub> | V                  |    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types             | - 55  | + 125           | °C                 |    |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time (Figure 1)                  | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0<br>0<br>0     | 1000<br>500<br>400 | ns |

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**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|--|----------------------|------------------|--------|---------|------|
|                 |  |  |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                   | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |  |  | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |  |  | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                   | 2.0                  | 0.3              | 0.3    | 0.3     | V    |
|                 |  |  | 4.5                  | 0.9              | 0.9    | 0.9     |      |
|                 |  |  | 6.0                  | 1.2              | 1.2    | 1.2     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                  | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |  |  | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |  | 6.0  | 5.9                  | 5.9              | 5.9    |         |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 4.5                  | 3.98             | 3.84   | 3.70    |      |
| 6.0             | 5.48   |  | 5.34                 | 5.20             |        |         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                  | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |  | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  | 6.0  | 0.1                  | 0.1              | 0.1    |         |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 4.5                  | 0.26             | 0.33   | 0.40    |      |
| 6.0             | 0.26   |  | 0.33                 | 0.40             |        |         |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA  | 6.0                  | 8                | 80     | 160     | μA   |

NOTE: Information on typical parametric values can be found in Chapter 2.

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|--|---|----------------------|------------------|--------|---------|------|
|  |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 4)   | 2.0                  | 6.0              | 4.8    | 4.0     | MHz  |
|  |   | 4.5                  | 30               | 24     | 20      |      |
|  |   | 6.0                  | 35               | 28     | 24      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q<br>(Figures 1 and 4)      | 2.0                  | 145              | 180    | 220     | ns   |
|  |   | 4.5                  | 29               | 36     | 44      |      |
|  |   | 6.0                  | 25               | 31     | 38      |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to Q<br>(Figures 2 and 4)      | 2.0                  | 150              | 190    | 225     | ns   |
|  |   | 4.5                  | 30               | 38     | 45      |      |
|  |   | 6.0                  | 26               | 33     | 38      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 4) | 2.0                  | 75               | 95     | 110     | ns   |
|  |   | 4.5                  | 15               | 19     | 22      |      |
|  |   | 6.0                  | 13               | 16     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                       | —                    | 10               | 10     | 10      | pF   |

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2.
- Information on typical parametric values can be found in Chapter 2.

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |    |
|-----------------|--|---|----|
|                 |  |   | 90 |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2.

**TIMING REQUIREMENTS** (Input  $t_r = t_f = 6$  ns)

| Symbol                          | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|---|----------------------|------------------|--------|---------|------|
|                                 |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>SU</sub>                 | Minimum Setup Time, Parallel Data Inputs to Clock<br>(Figure 3)             | 2.0                  | 100              | 125    | 150     | ns   |
|                                 |   | 4.5                  | 20               | 25     | 30      |      |
|                                 |   | 6.0                  | 17               | 21     | 26      |      |
| t <sub>SU</sub>                 | Minimum Setup Time, S1 or S2 to Clock<br>(Figure 3)                         | 2.0                  | 100              | 125    | 150     | ns   |
|                                 |   | 4.5                  | 20               | 25     | 30      |      |
|                                 |   | 6.0                  | 17               | 21     | 26      |      |
| t <sub>SU</sub>                 | Minimum Setup Time, S <sub>A</sub> or S <sub>D</sub> to Clock<br>(Figure 3) | 2.0                  | 100              | 125    | 150     | ns   |
|                                 |   | 4.5                  | 20               | 25     | 30      |      |
|                                 |   | 6.0                  | 17               | 21     | 26      |      |
| t <sub>H</sub>                  | Minimum Hold Time, Clock to any Input (except Reset)<br>(Figure 3)          | 2.0                  | 3                | 3      | 3       | ns   |
|                                 |   | 4.5                  | 3                | 3      | 3       |      |
|                                 |   | 6.0                  | 3                | 3      | 3       |      |
| t <sub>REC</sub>                | Minimum Recovery Time, Reset Inactive to Clock<br>(Figure 2)                | 2.0                  | 5                | 5      | 5       | ns   |
|                                 |   | 4.5                  | 5                | 5      | 5       |      |
|                                 |   | 6.0                  | 5                | 5      | 5       |      |
| t <sub>W</sub>                  | Minimum Pulse Width, Clock<br>(Figure 1)                                    | 2.0                  | 80               | 100    | 120     | ns   |
|                                 |   | 4.5                  | 16               | 20     | 24      |      |
|                                 |   | 6.0                  | 14               | 17     | 20      |      |
| t <sub>W</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                                    | 2.0                  | 80               | 100    | 120     | ns   |
|                                 |   | 4.5                  | 16               | 20     | 24      |      |
|                                 |   | 6.0                  | 14               | 17     | 20      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)                             | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |   | 4.5                  | 500              | 500    | 500     |      |
|                                 |   | 6.0                  | 400              | 400    | 400     |      |

NOTE: Information on typical parametric values can be found in Chapter 2.

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**PIN DESCRIPTIONS**

**DATA INPUTS**

**A, B, C, D (Pins 3, 4, 5, 6)**

Parallel data inputs.

**S<sub>A</sub> (Pin 2)**

Serial-data input when using shift-right mode.

**S<sub>D</sub> (Pin 7)**

Serial-data input when using shift-left mode.

**OUTPUTS**

**Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub> (Pins 15, 14, 13, 12)**

Parallel data outputs.

**CONTROL INPUTS**

**Clock (Pin 11)**

Clock Input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

**Reset (Pin 1)**

A low level applied to this pin resets all stages and forces all outputs low.

**S<sub>0</sub>, S<sub>1</sub> (Pins 9, 10)**

Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

**Parallel Load Mode (S<sub>1</sub> = H, S<sub>0</sub> = H)**

Data is loaded into the device with a positive transition of the Clock input.

**Shift Right Mode (S<sub>1</sub> = L, S<sub>0</sub> = H)**

With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and data on the S<sub>A</sub> Serial Data Input is shifted into stage A.

**Shift Left Mode (S<sub>1</sub> = H, S<sub>0</sub> = L)**

With a positive transition of the Clock input, each bit is shifted left (in the direction Q<sub>D</sub> toward Q<sub>A</sub>) one stage and data on the S<sub>D</sub> Serial Data Input is shifted into stage D.

**Hold Mode (S<sub>1</sub> = L, S<sub>0</sub> = L)**

Outputs are held.

**SWITCHING WAVEFORMS**

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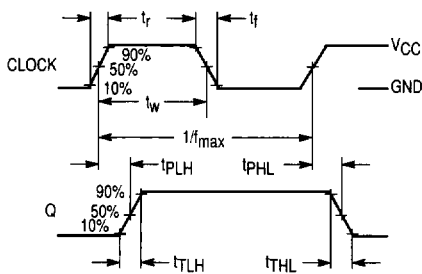


Figure 1.

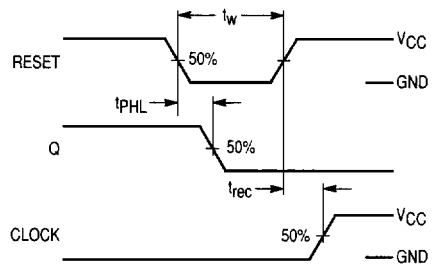


Figure 2.

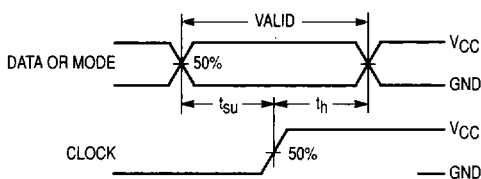
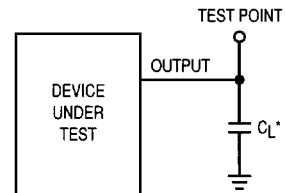


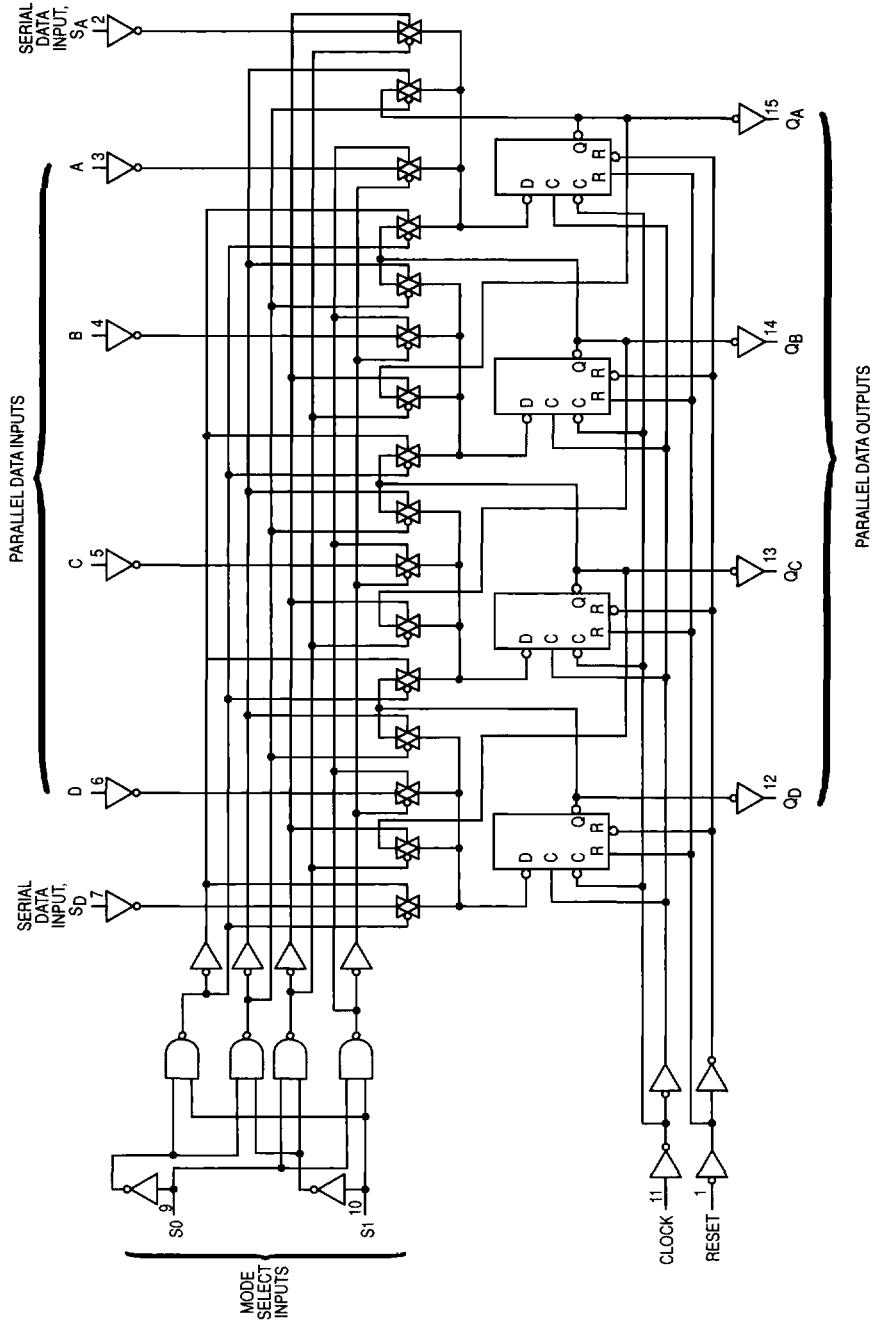
Figure 3.



\* Includes all probe and jig capacitance

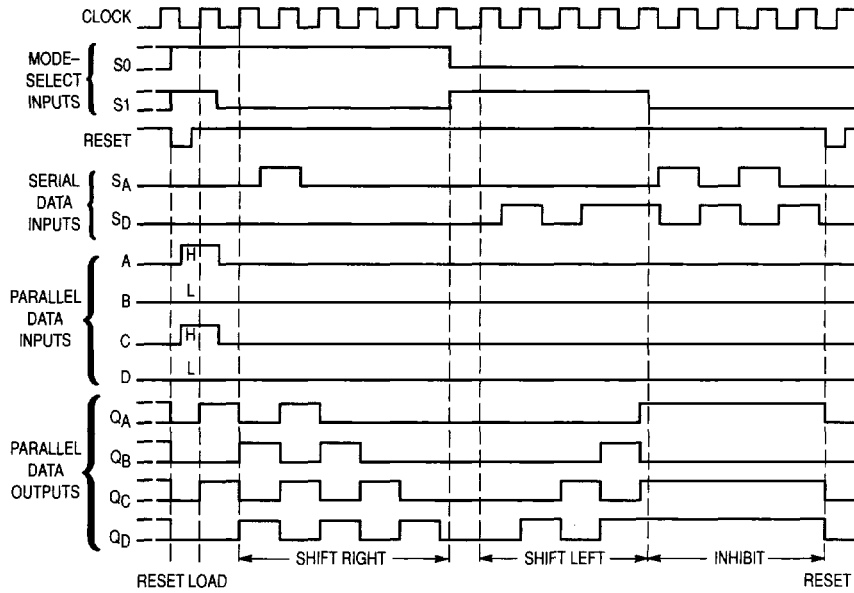
Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



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TIMING DIAGRAM



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