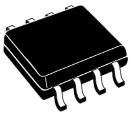
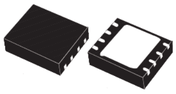
TSB952

Datasheet

High bandwidth (52 MHz), rail-to-rail output, 36 V op amp



SO8



DFN8 (3 x 3 mm)

Maturity status link
TSB952

Related products	
TSB612	For lower current consumption
TSB622	For lower speed
TSB512	For rail-to-rail inputs
TSB712	For precision and rail-to-rail inputs
TSB182	For very high accuracy

Features

- Low offset voltage: 3 mV max @ 25 °C
- Low current consumption: 3.3 mA max / op @ 36 V
- Wide supply voltage: 4.5 to 36 V
- Gain bandwidth product: 52 MHz typ. @ 36 V
- Unity gain stable
- Rail-to-rail output
- Output current: 40 mA typ. @ 36 V
- Input common-mode voltage includes ground
- High ESD tolerance: 4 kV HBM
- EMI hardened
- Extended temperature range: -40 to +125 °C
- Automotive qualification
- Micropackage: SO8, DFN8 3x3 wettable flanks

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB952 is a high-speed dual operational amplifier featuring an extended supply voltage operating range and rail-to-rail output. It also has an excellent speed/current consumption ratio because it is a 52 MHz gain bandwidth product, consuming less than 3.3 mA per channel at 36 V supply voltage.

The TSB952 operates over a wide temperature range from -40 °C to +125 °C, making this device ideal for industrial and automotive applications with the associated qualification.

Thanks to its small package size, the TSB952 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin configuration

Figure 1. Pin connections (top view)

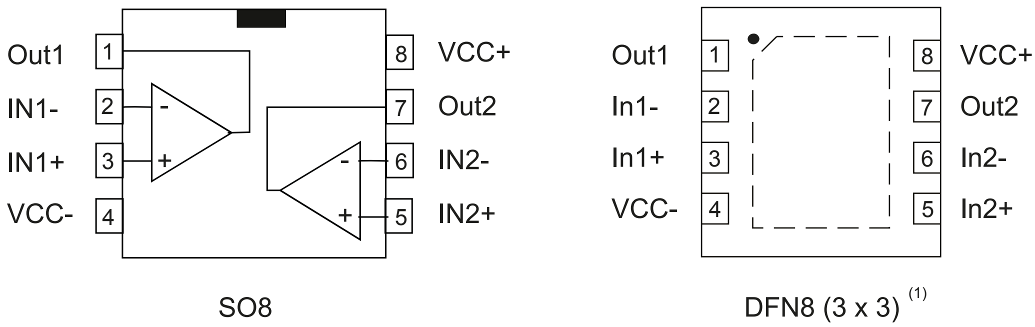


Table 1. Pin description

Pin	Pin name	Description
1	OUT1	Output
2	IN1-	Negative input voltage
3	IN1+	Positive input voltage
4	V_{CC}-	Negative supply voltage
5	IN2+	Positive input voltage
6	IN2-	Negative input voltage
7	OUT2	Output
8	V_{CC}+	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	40	V
V_{ID}	Differential input voltage [2]	±1.4	V
V_{IN}	Input voltage	(V_{CC}-) -0.2 to (V_{CC}+) +0.2	V
I_{IN}	Input current [3]	10	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
R_{TH-JA}	Thermal resistance junction to ambient [4] [5] SO8 DFN8 3x3 WF	 125 40	°C/W
ESD	Human Body Model (HBM) [6]	4000	V
	Charged Device Model (CDM) [7]	1500	

1. *All voltage values, except differential voltage, are with respect to the network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *R_{TH} are typical values.*
5. *Short circuits can cause excessive heating and destructive dissipation.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to ANSI/ESD STM5.3.1.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 36	V
V_{ICM}	Common-mode input voltage range	(V_{CC}-) to (V_{CC}+) -1.5	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics V_{CC} = 5 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	T = 25 °C			±3	mV
		Tmin < T < Tmax			±3.5	
$\lvert \Delta V_{IO}/\Delta T \rvert$	Input offset voltage drift	Tmin < T < Tmax		0.9	5	μV/°C
I_{IB}	Input bias current	T = 25 °C		1	50	pA
		Tmin < T < Tmax			1000	
I_{IO}	Input offset current	T = 25 °C		1	50	
		Tmin < T < Tmax			1000	
A_{VD}	Large signal voltage gain	V_{OUT} = 0.3 to (V_{CC} -0.3 V) R_L = 10 kΩ connected to V_{CC}/2	96	113		dB
		Tmin < T < Tmax	86			
CMR	Common-mode rejection ratio	V_{ICM} = 0 to V_{CC} -1.5 V, V_{OUT} = V_{CC}/2	72	88		dB
		Tmin < T < Tmax	72			
V_{OL}	Output swing from negative rail	No load		4	10	mV
		Tmin < T < Tmax			50	
		I_{SINK} = 2 mA		48	60	
		Tmin < T < Tmax			130	
V_{OH}	Output swing from positive rail	No load		5	15	
		Tmin < T < Tmax			50	
		I_{SOURCE} = 2 mA		51	70	
		Tmin < T < Tmax			120	
I_{OUT}	I_{SINK}	V_{OUT} = V_{CC}+	39	44		mA
		Tmin < T < Tmax	33			
	I_{SOURCE}	V_{OUT} = V_{CC}-	43	48		
		Tmin < T < Tmax	42			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		2.2	3	mA
		Tmin < T < Tmax			3.8	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 22 pF	31	47		MHz
		Tmin < T < Tmax	30			
SR	Slew rate	R_L = 10 kΩ, C_L = 22 pF, AV = 1 V/V, 10% to 90%	18	26		V/μs
		Tmin < T < Tmax	12			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 22 pF		47		°
G_M	Gain margin	R_L = 10 kΩ, C_L = 22 pF		13		dB
E_N	Equivalent input noise density	f = 10 kHz		35		nV/√Hz
		f = 100 kHz		16		
E_N P-P	Input voltage noise	0.1 Hz < f < 10 Hz		45		μV_{PP}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	f = 1 kHz, Gain = 1, V_{OUT} = 2 Vpp		0.003		%
t_{REC}	Overload recovery time			80		ns
t_S	Settling time	0.1%, Gain = -1, 2 V step		180		ns
		0.01%, Gain = -1, 2 V step		245		
C_S	Channel separation	f = 1 kHz		120		dB

Table 5. **Electrical characteristics V_{CC} = 12 V, V_{icm} = V_{CC}/2, T = 25 °C, (unless otherwise specified).**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	T = 25 °C			±3	mV
		Tmin < T < Tmax			±3.5	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		0.8	5	μV/°C
I_{IB}	Input bias current	T = 25 °C		1	50	pA
		Tmin < T < Tmax			1000	
I_{IO}	Input offset current	T = 25 °C		1	50	
		Tmin < T < Tmax			1000	
A_{VD}	Large signal voltage gain	V_{OUT} = 0.3 to (V_{CC} -0.3 V) R_L = 10 kΩ connected to V_{CC}/2	105	113		dB
		Tmin < T < Tmax	94			
CMR	Common-mode rejection ratio	V_{ICM} = 0 to V_{CC} -1.5 V, V_{OUT} = V_{CC}/2	80	94		dB
		Tmin < T < Tmax	80			
V_{OL}	Output swing from negative rail	No load		4	10	mV
		Tmin < T < Tmax			50	
		I_{SINK} = 2 mA		48	60	
		Tmin < T < Tmax			120	
V_{OH}	Output swing from positive rail	No load		5	20	
		Tmin < T < Tmax			50	
		I_{SOURCE} = 2 mA		51	70	
		Tmin < T < Tmax			120	
I_{OUT}	I_{SINK}	V_{OUT} = V_{CC}+	38	43		mA
		Tmin < T < Tmax	33			
	I_{SOURCE}	V_{OUT} = V_{CC}-	43	47		
		Tmin < T < Tmax	41			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		2.3	3	mA
		Tmin < T < Tmax			3.9	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 22 pF	34	50		MHz
		Tmin < T < Tmax	32			
SR	Slew rate	R_L = 10 kΩ, C_L = 22 pF, AV = 1 V/V, 10% to 90%	19	28		V/μs
		Tmin < T < Tmax	12			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 22 pF		49		°
G_M	Gain margin	R_L = 10 kΩ, C_L = 22 pF		12		dB
E_N	Equivalent input noise density	f = 10 kHz		45		nV/√Hz
		f = 100 kHz		14		
E_N P-P	Input voltage noise	0.1 Hz < f < 10 Hz		58		$μV_{PP}$
THD+N	Total harmonic distortion + noise	f = 1 kHz, Gain = 1, V_{OUT} = 2 Vpp		0.0007		%t
t_{REC}	Overload recovery time			80		ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Settling time	0.1%, Gain = -1, 2 V step		265		ns
		0.01%, Gain = -1, 2 V step		300		
C_S	Channel separation	f = 1 kHz		120		dB

Table 6. Electrical characteristics V_{CC} = 36 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	T = 25 °C			±3	mV
		Tmin < T < Tmax			±3.5	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift	Tmin < T < Tmax		1	5	μV/°C
I_{IB}	Input bias current	T = 25 °C		6	100	pA
		Tmin < T < Tmax			2000	
I_{IO}	Input offset current	T = 25 °C		1	100	
		Tmin < T < Tmax			2000	
A_{VD}	Large signal voltage gain	V_{OUT} = 0.3 to (V_{CC} -0.3 V) R_L = 10 kΩ connected to V_{CC}/2	108	116		dB
		Tmin < T < Tmax	97			
CMR	Common-mode rejection ratio	V_{ICM} = 0 to V_{CC} -1.5 V, V_{OUT} = V_{CC}/2	90	105		dB
		Tmin < T < Tmax	90			
SVR	Supply voltage rejection ratio 20 Log(Δ V_{CC} / ΔV_{IO})	V_{CC} = 5 to 36 V, V_{ICM} = 0 V	102	116		
		Tmin < T < Tmax	101			
V_{OL}	Output swing from negative rail	No load		5	15	mV
		Tmin < T < Tmax			50	
		I_{SINK} = 2 mA		51	70	
		Tmin < T < Tmax			120	
		I_{SINK} = 15 mA		370	430	
		Tmin < T < Tmax			700	
V_{OH}	Output swing from positive rail	No load		7	25	
		Tmin < T < Tmax			50	
		I_{SOURCE} = 2 mA		55	80	
		Tmin < T < Tmax			120	
		I_{SOURCE} = 15 mA		390	440	
		Tmin < T < Tmax			700	
I_{OUT}	I_{SINK}	V_{OUT} = V_{CC}+	36	40		mA
		Tmin < T < Tmax	31			
	I_{SOURCE}	V_{OUT} = V_{CC}-	42	46		
		Tmin < T < Tmax	41			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		2.6	3.3	mA
		Tmin < T < Tmax			4.1	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 22 pF	35	52		MHz
		Tmin < T < Tmax	33			
SR	Slew rate	R_L = 10 kΩ, C_L = 22 pF, AV = 1 V/V, 10% to 90%	21	30		V/μs
		Tmin < T < Tmax	16			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 22 pF		52		°
G_M	Gain margin	R_L = 10 kΩ, C_L = 22 pF		12		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E_N	Equivalent input noise density	f = 10 kHz		35		nV/√Hz
		f = 100 kHz		16		
E_N P-P	Input voltage noise	0.1 Hz < f < 10 Hz		45		μV_{PP}
THD+N	Total harmonic distortion + noise	f = 1 kHz, Gain = 1, V_{OUT} = 2 Vpp		0.00045		%
t_{REC}	Overload recovery time			80		ns
t_S	Settling time	0.1%, Gain = -1, 2 V step		320		ns
		0.01%, Gain = -1, 2 V step		345		
C_S	Channel separation	f = 1 kHz		120		dB

4 Typical performance characteristics

R_L = 10 kΩ connected to V_{CC}/2 and C_L = 22 pF, unless otherwise specified.

Figure 2. Supply current vs. supply voltage

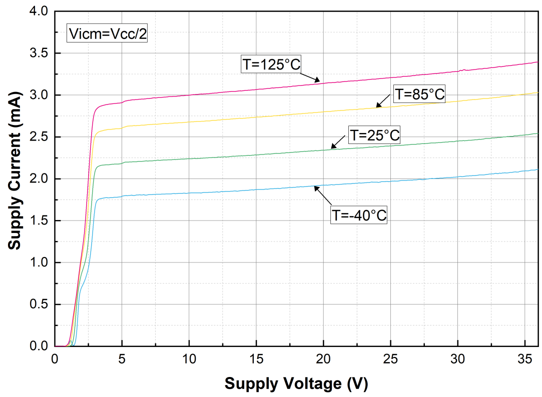


Figure 3. Input offset voltage production distribution at V_{CC} = 5 V

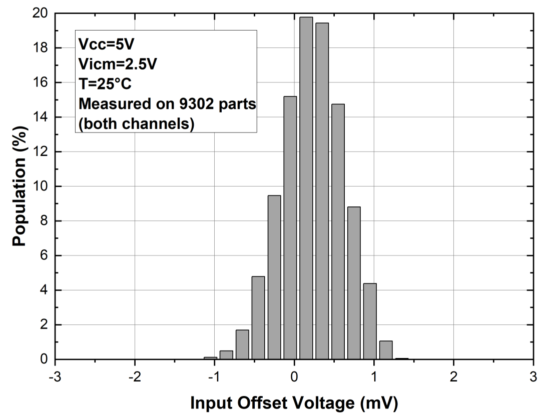


Figure 4. Input offset voltage production distribution at V_{CC} = 36 V

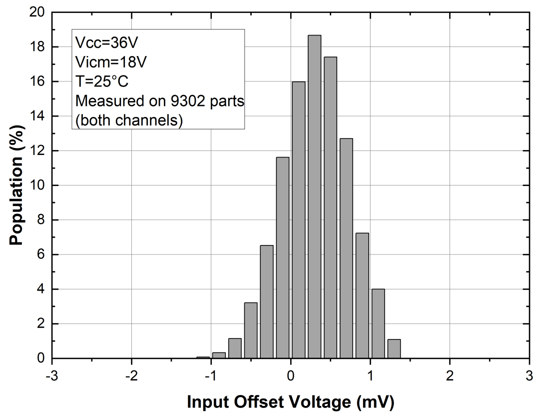


Figure 5. Input offset voltage vs. temperature at V_{CC} = 5 V

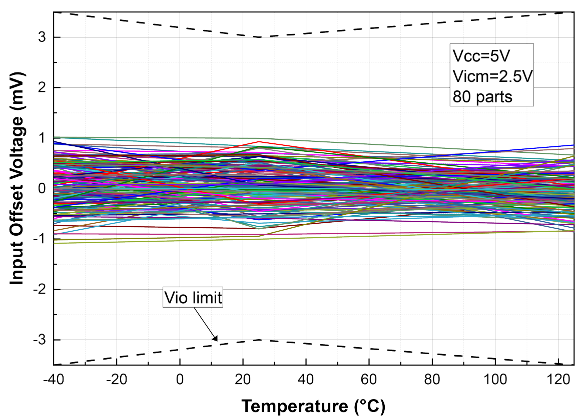


Figure 6. Input offset voltage vs. temperature at V_{CC} = 36 V

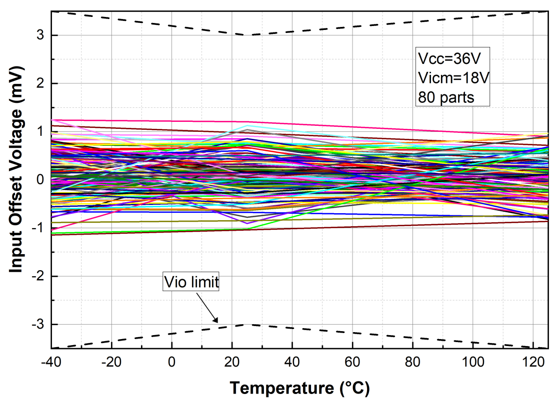


Figure 7. Input offset voltage thermal drift distribution at V_{CC} = 5 V

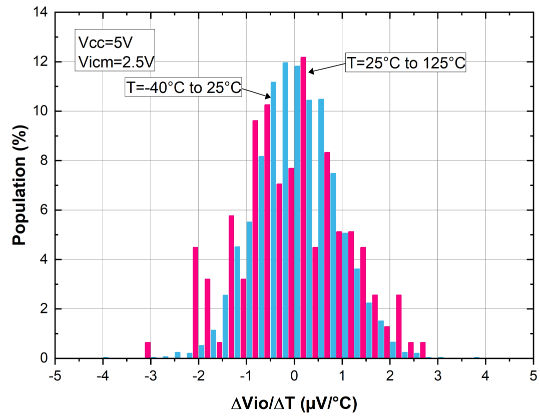


Figure 8. Input offset voltage thermal drift distribution at V_{CC} = 36 V

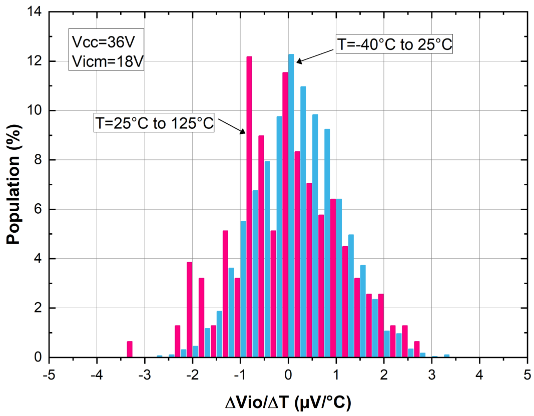


Figure 9. Input offset voltage vs. supply voltage

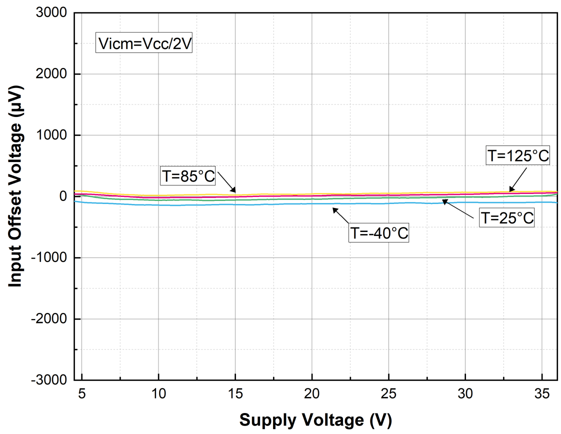


Figure 10. Input offset voltage vs. common-mode voltage at V_{CC} = 5 V

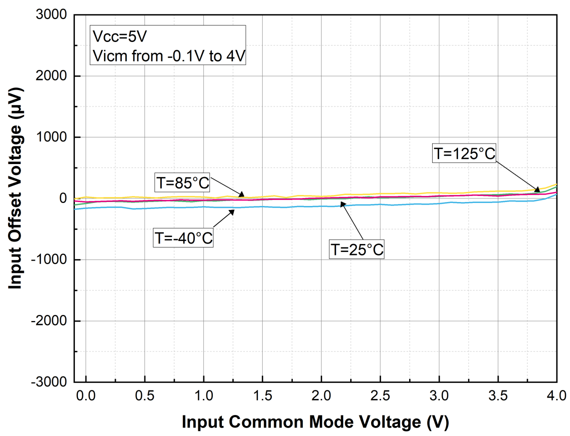
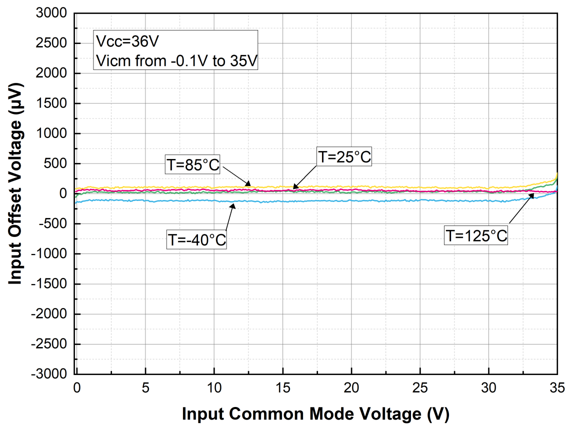


Figure 11. Input offset voltage vs. common-mode voltage at V_{CC} = 36 V



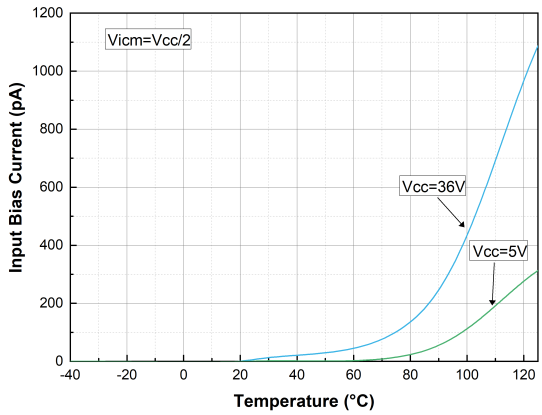


Figure 12. Input bias current vs. temperature

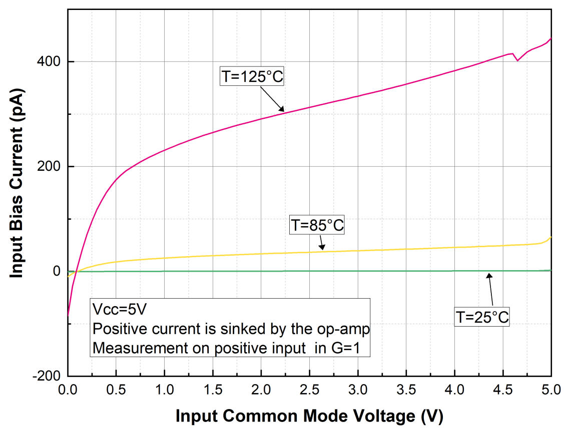


Figure 13. Input bias current vs. common-mode voltage at V_{CC} = 5 V

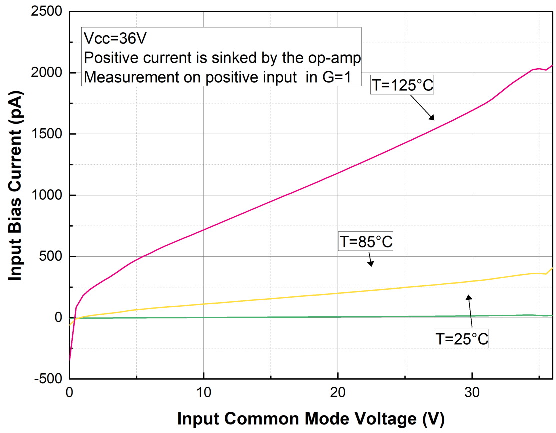


Figure 14. Input bias current vs. common-mode voltage at V_{CC} = 36 V

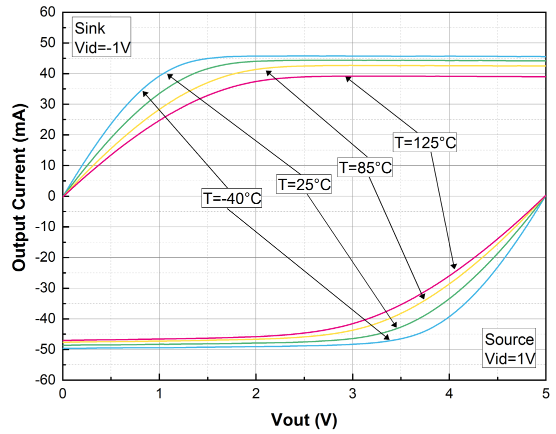


Figure 15. Output current vs. output voltage at V_{CC} = 5 V

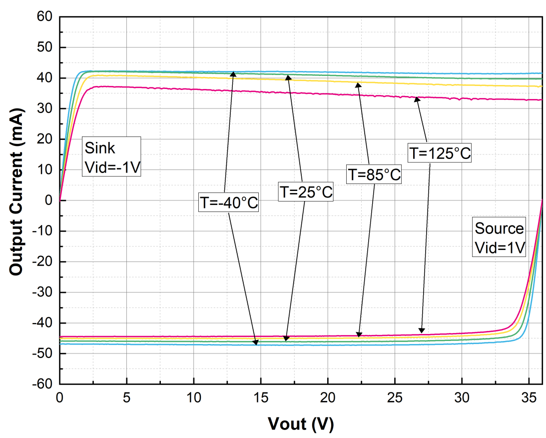


Figure 16. Output current vs. output voltage at V_{CC} = 36 V

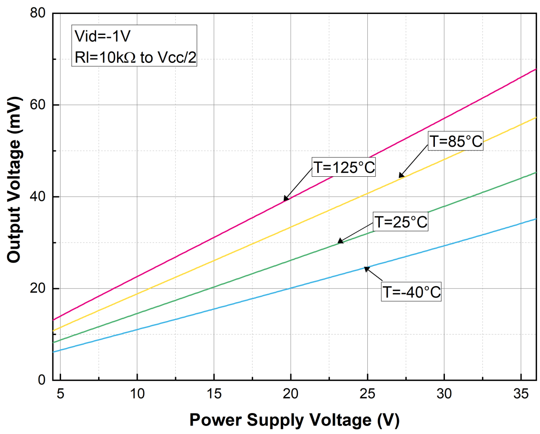


Figure 17. Output saturation voltage (V_{OL}) vs. supply voltage with R_L = 10 kΩ

Figure 18. Output saturation voltage (V_{OH}) vs. supply voltage with R_L = 10 kΩ

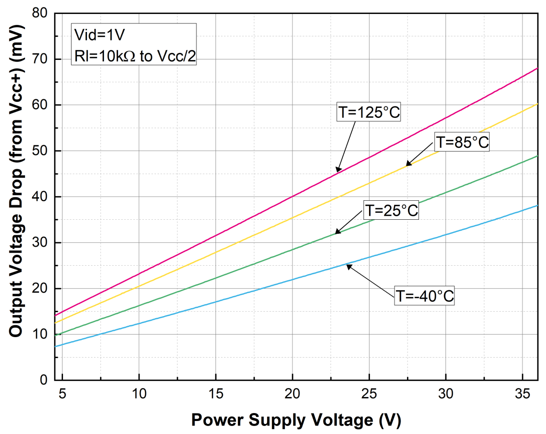


Figure 19. Output saturation voltage (V_{OL}) vs. supply voltage with R_L = 600 Ω

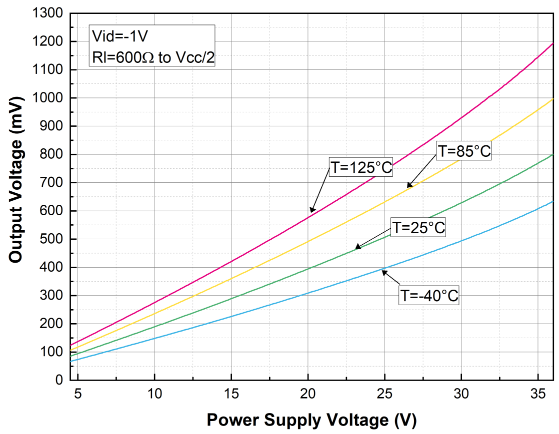


Figure 20. Output saturation voltage (V_{OH}) vs. supply voltage with R_L = 600 Ω

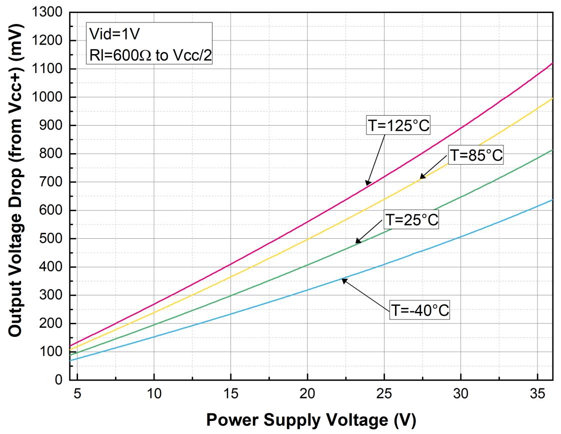


Figure 21. Positive slew rate at V_{CC} = 36 V

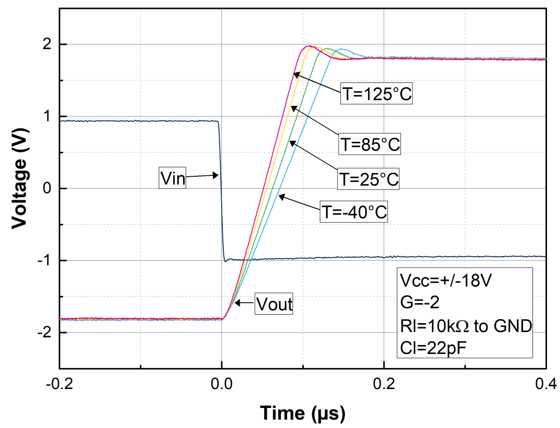


Figure 22. Negative slew rate at V_{CC} = 36 V

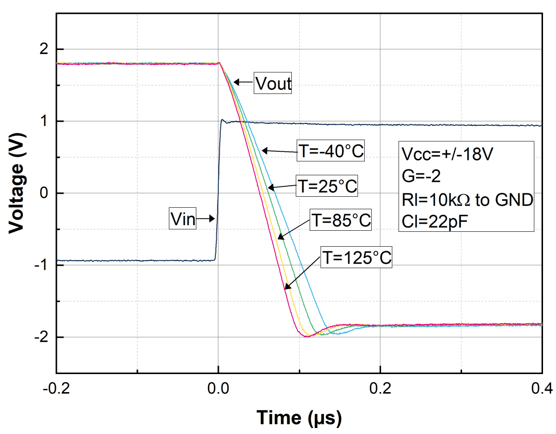


Figure 23. Slew rate vs. V_{CC}

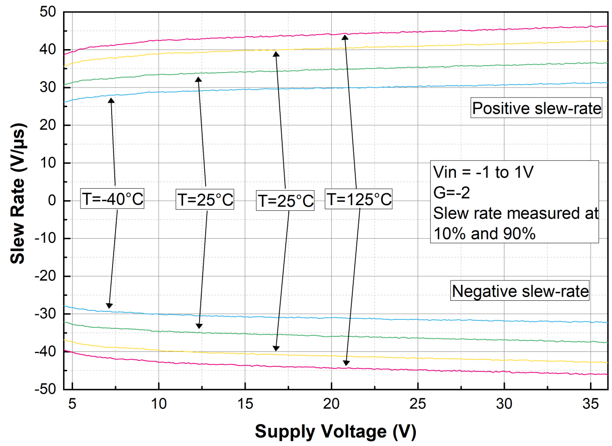


Figure 24. Open loop bode diagram at V_{CC} = 5 V

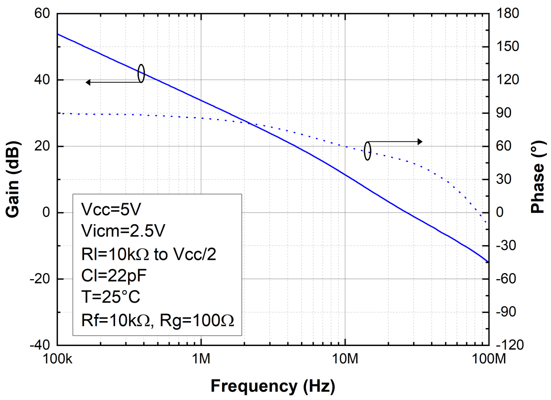


Figure 25. Open loop bode diagram at V_{CC} = 36 V

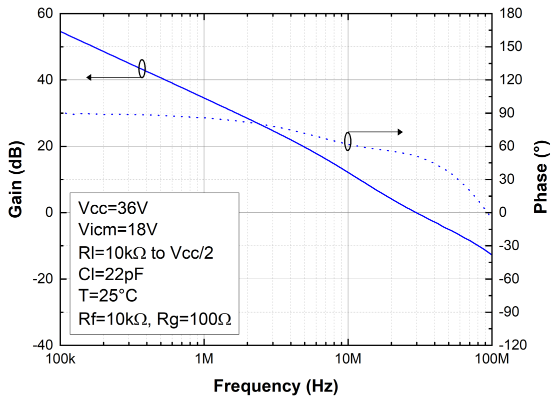


Figure 26. Closed loop bode diagram at V_{CC} = 5 V

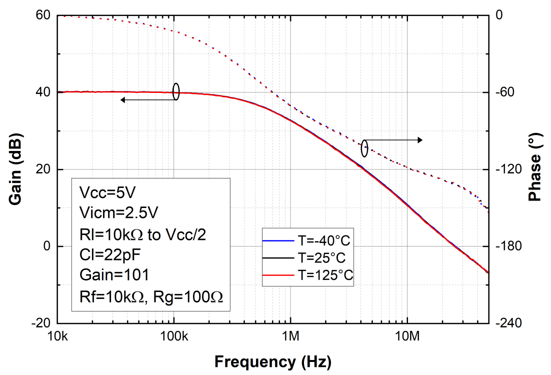


Figure 27. Closed loop bode diagram at V_{CC} = 36 V

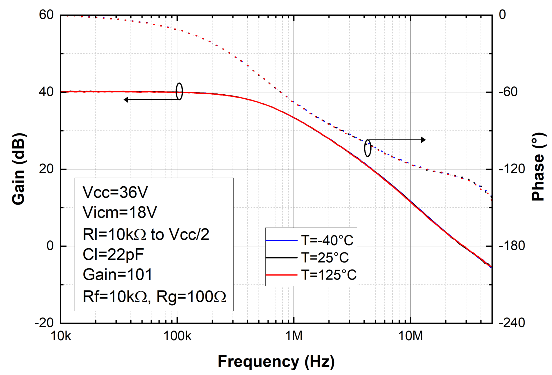


Figure 28. Phase margin vs. common-mode voltage and load current at V_{CC} = 5 V

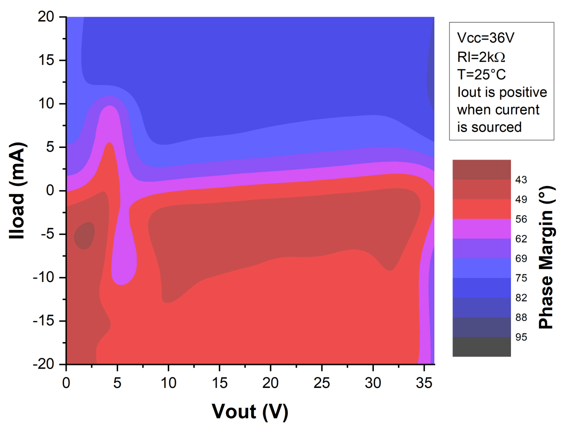


Figure 29. Phase margin vs. capacitive load

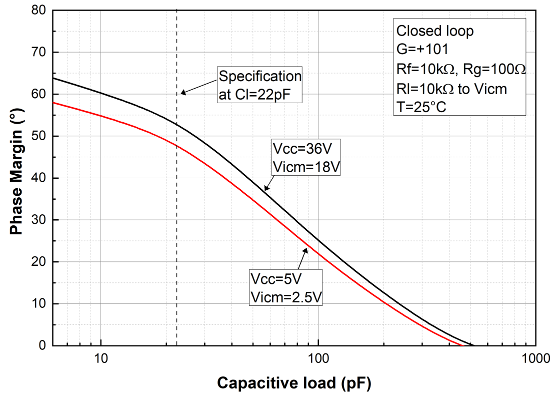


Figure 30. Small step response at V_{CC} = 5 V

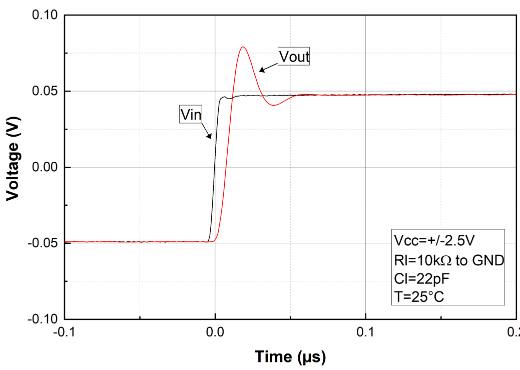


Figure 31. Small step response at V_{CC} = 36 V

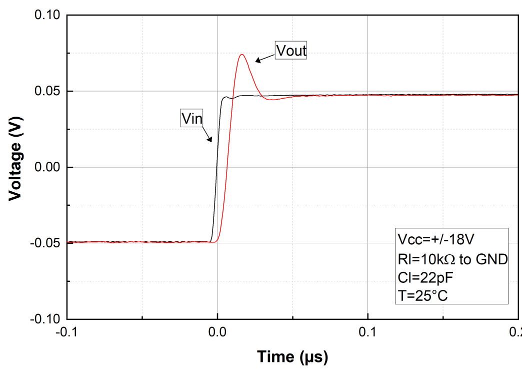


Figure 32. Desaturation from low rail at V_{CC} = 36 V

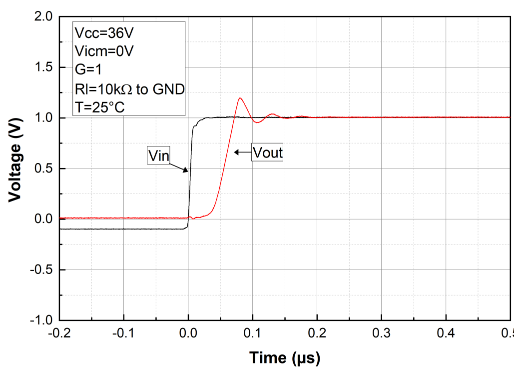


Figure 33. Desaturation from high rail at V_{CC} = 36 V

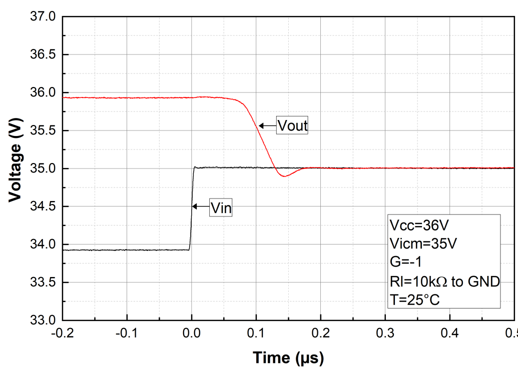


Figure 34. Small step overshoot vs. load capacitance

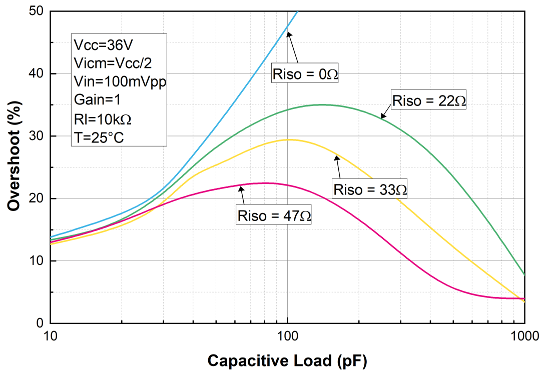


Figure 35. Linearity vs. load resistance at V_{CC} = 5 V

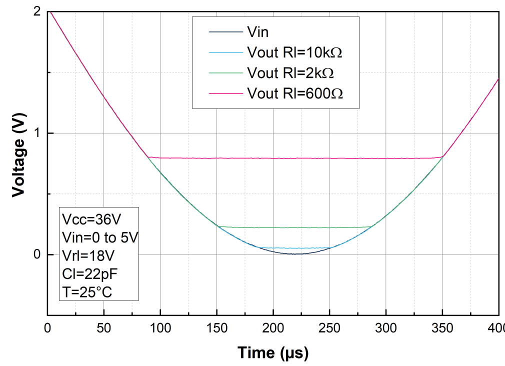


Figure 36. Settling time high to low at V_{CC} = 36 V

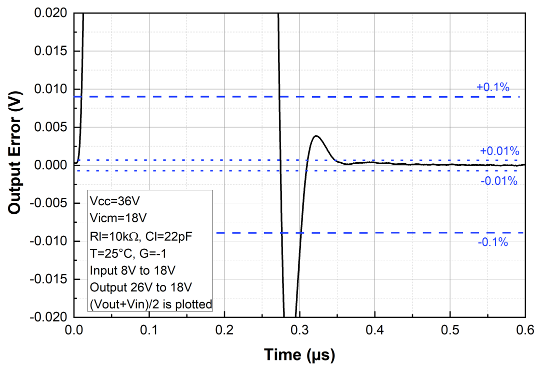


Figure 37. Settling time low to high at V_{CC} = 36 V

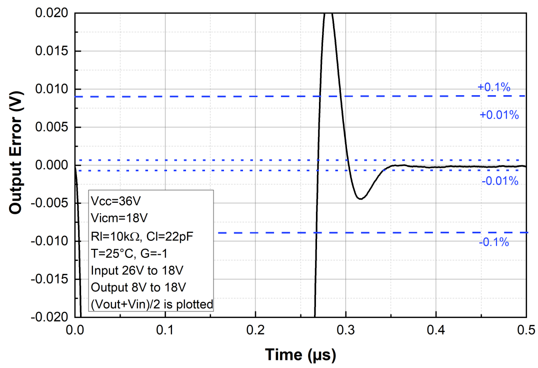


Figure 38. Noise vs. frequency

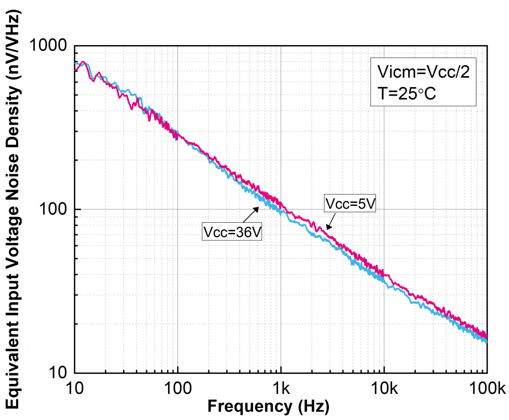


Figure 39. Noise vs. time at V_{CC} = 36 V

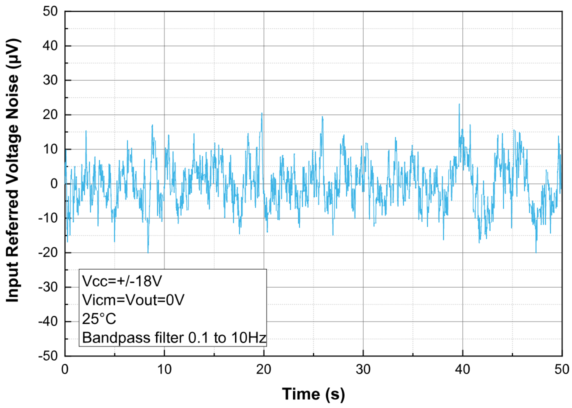


Figure 40. THD+N vs. output voltage at V_{CC} = 36 V

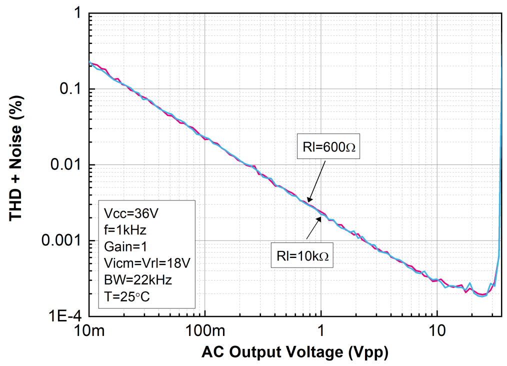


Figure 41. CMRR vs. frequency at V_{CC} = 12 V

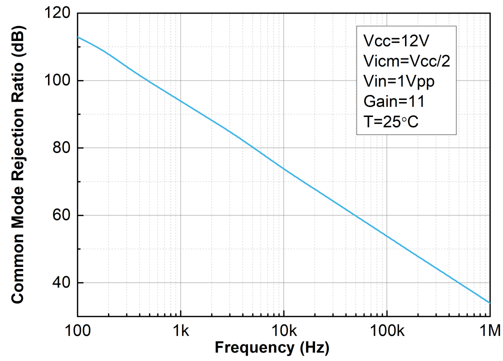
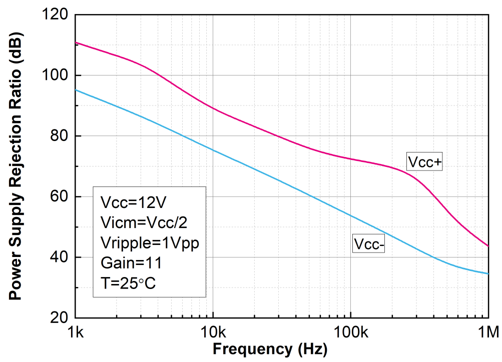


Figure 42. PSRR vs. frequency at V_{CC} = 12 V



5 Application information

5.1 Operating voltages

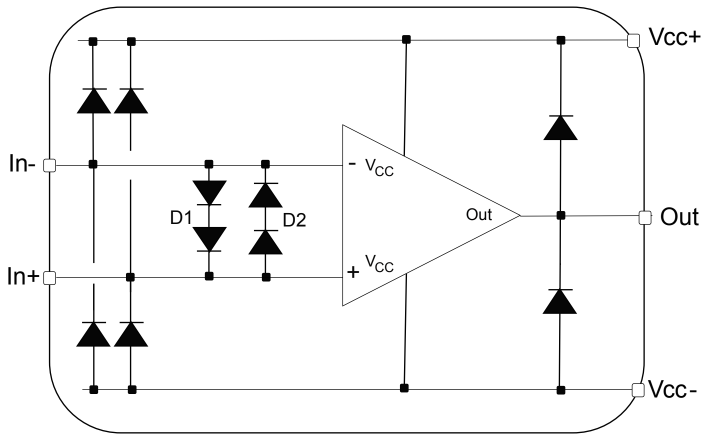
The TSB952 device can operate from 4.5 to 36 V. The parameters are fully specified at 5 V, 12 V, and 36 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSB592 device characteristics over the full operating range. Additionally, the main specifications are guaranteed in an extended temperature range from -40 to +125 °C.

The input common-mode range includes the V_{CC}- (low rail) but is limited to V_{CC}+ -1.5 V.

5.2 Input pin voltage range

The TSB952 has internal ESD diode protections on the inputs. These diodes are connected between the inputs and each supply rail to protect the input stage from electrical discharge, as shown in the figure below.

Figure 43. Input current limitation



When the input pin voltage exceeds the power supply, the ESD diodes become conductive and, depending on this voltage, excessive current can flow through them. Without a limitation this overcurrent can damage the device. Thus, the current has to be limited to 10 mA by adding a resistance in series with the input pin.

Similarly, the differential input voltage is limited by two back-to-back groups of two diodes in series between the positive and negative inputs. In order to avoid excessive current in these diodes, the differential voltage should be limited to ±1.4 V, or the current limited to 10 mA. Such a high differential voltage can be reached when the output is in saturation mode, or slew rate limited. In particular, it can happen when the device is used in comparator mode.

The TSB952 does not show any phase reversal for any input common-mode voltage inside the absolute maximum ratings (AMR) voltage window, (V_{CC}-) -200 mV < V_{ICM} < (V_{CC}+) +200 mV.

5.3 Input offset voltage drift over the temperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{IO}) is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using Eq. (1).

$$\frac{\Delta V_{IO}}{\Delta T} = \max\left|\frac{V_{IO}(T) - V_{IO}(25°C)}{T - 25°C}\right|_{T\,=\,-40°C\ and\ T\,=\,125°C} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a Cpk (process capability index) greater than 1.3.

5.4 Unused channel

When one of the two channels of the TSB952 is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. As the TSB952 is unity gain stable, the simplest solution is to set the unused channel in follower and fix the positive input to any bias within the recommended operating range. A gain configuration can also be used.

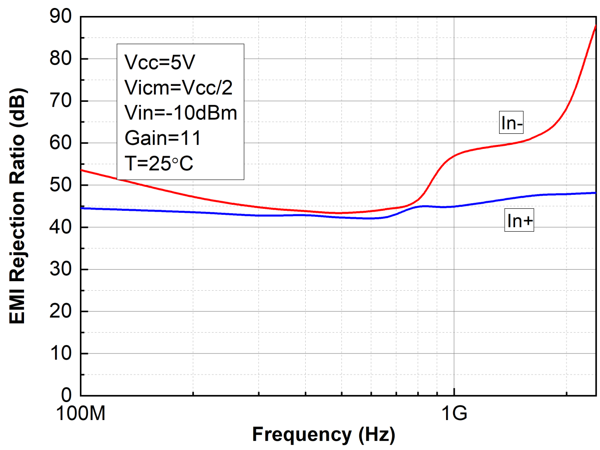
5.5 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in Eq. (2):

$$EMIRR = 20.\log\left(\frac{V_{in\_pp}}{\Delta V_{io}}\right) \quad (2)$$

The TSB952 has been specially designed to minimize susceptibility to the EMIRR and shows a low sensitivity. As visible in Figure 44, the EMI rejection ratio has been measured on both the inputs and the output, from 400 MHz to 2.4 GHz.

Figure 44. EMIRR on In+ and In- pins



EMIRR performance might be improved by adding small capacitances (in the pF range) on the inputs, power supply, and output pins. These capacitances help minimize the impedance of these nodes at high frequencies.

5.6 Maximum power dissipation

The maximum power supply voltage, as well as the usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSB952 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times Rth_{JA} + T_A \quad (3)$$

T_J is the die junction temperature.

P_D is the power dissipated in the package.

$R_{TH\text{-}JA}$ is the junction to ambient thermal resistance of the package.

T_A is the ambient temperature.

The $R_{TH\text{-}JA}$, given in table x for the available packages, is based on the JEDEC standard JESD51, for 2s2p (4 layers) board. This value largely depends on the board layout and is given as a guideline. Be aware that the actual value can differ significantly, and optimize the power dissipation on your board if this is critical for your design. For thermally sensitive designs, favor the DFN8 version of the product that has better thermal dissipation due to its exposed pad.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

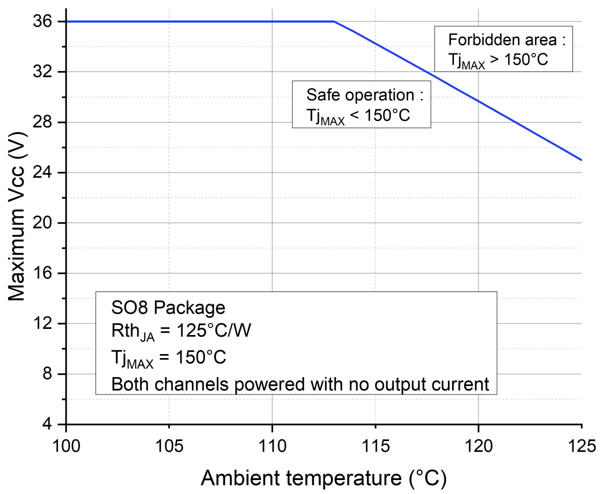
$P_D = (V_{CC} \times I_{CC}) + (V_{cc+} + V_{OUT}) \times ILoad$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} + V_{CC-}) \times ILoad$ when the op amp is sinking the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

Due to the $R_{th\text{-}ja}$ value, the SO8 package cannot be used at V_{CC} = 36 V and at 125 °C ambient temperature, because the maximum junction temperature would be reached. The following figure shows the maximum V_{CC} for a given ambient temperature, considering only the device maximum I_{CC} (output current is negligible).

Figure 45. Maximum V_{CC} for safe operation using SO8 package



Considering the output current limitation, the figures below give the maximum output current for a given output voltage and temperature, at V_{CC} = 36 V, for SO8 and DFN8 packages.

Figure 46. **Maximum output current for safe operation on SO8 package**

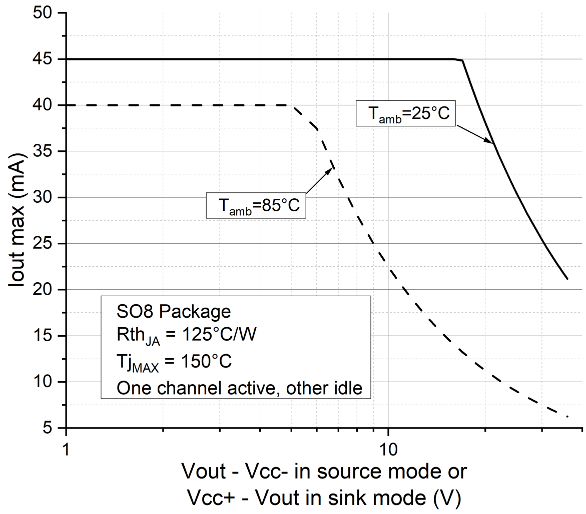
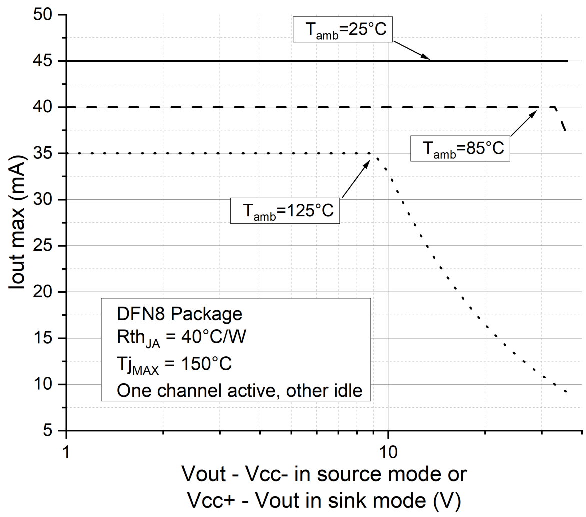


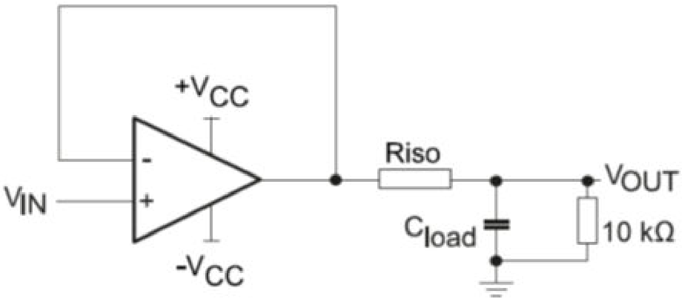
Figure 47. **Maximum output current for safe operation on DFN8 package**



5.7 Capacitive load and stability

A stability analysis must be performed for large capacitive loads over 22 pF. Increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response. Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity gain configurations, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 47 Ω) in series with the output. This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO}/R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point of view as described in the figure below:

Figure 48. **Test configuration for R_{ISO}**



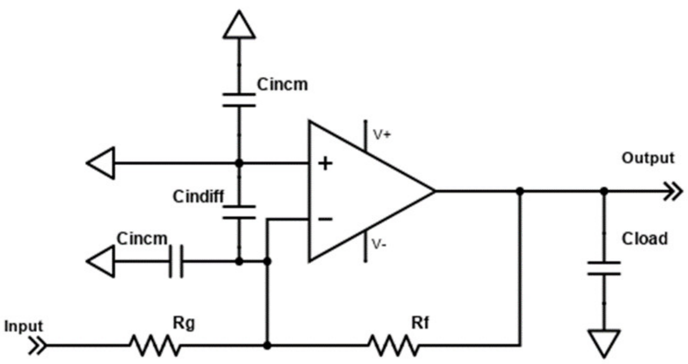
Please note that R_{ISO} = 47 Ω is sufficient to make the TSB952 stable whatever the capacitive load.

5.8 Resistor values for high speed op amp design

Due to its high gain bandwidth product (GBP), this op amp is particularly sensitive to parasitic impedances. Board parasitic elements should be taken into account in any sensitive design. Indeed, excessive parasitic elements (both capacitive and inductive) in the op amp frequency range can alter performance and stability. These issues can often be mitigated by lowering the resistive impedances.

More specifically, the RC network created by the schematic resistors (Rf and Rg) and the parasitic capacitances of both the op amp and the PCB can generate a pole below or in the same order of magnitude as the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically < 5), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor (Rf), typically 600 Ω.

Figure 49. **Inverting amplifier configuration with parasitic input capacitances**



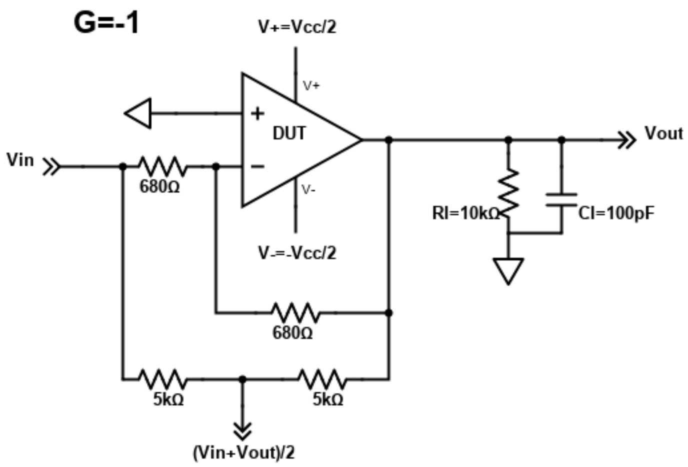
Also, some designs use an input resistor on the positive input, generally of the same value as the input on the negative resistor. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful with the TSB952 as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency.

The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient Spice simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace a hardware evaluation of the application circuit.

5.9 Settling time

Settling time in an application can be defined as the amount of time between the input changes and the output reaching its final value. It is usually defined with a given tolerance, so the output stability is reached when the output stays within the given range around the final value. In figures 36 and 37, the settling time is measured in an inverting configuration, using the so-called “false summing node” circuit.

Figure 50. Settling time measurement configuration



This circuit is used with a step input voltage from a positive or negative value to 0 V. The measurement point being (V_{IN} - V_{OUT})/2, and V_{OUT} being in an ideal circuit equal to -V_{IN}, the measurement point gives half of the error on V_{OUT}, comparatively to V_{IN}. This error is compared to the tolerance, 0.1% or 0.01% for this circuit, to deduce the settling time. This characteristic is particularly useful when driving an ADC. It is related to the slew rate, GBP, and stability of the circuit. It also varies with the circuit gain, the circuit load, and the input voltage step value. However, computing the value of the settling time in a given configuration is not straightforward. The macromodel can give a good estimation, but prototyping can be necessary for fine circuit optimization.

5.10 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.11 Macromodel

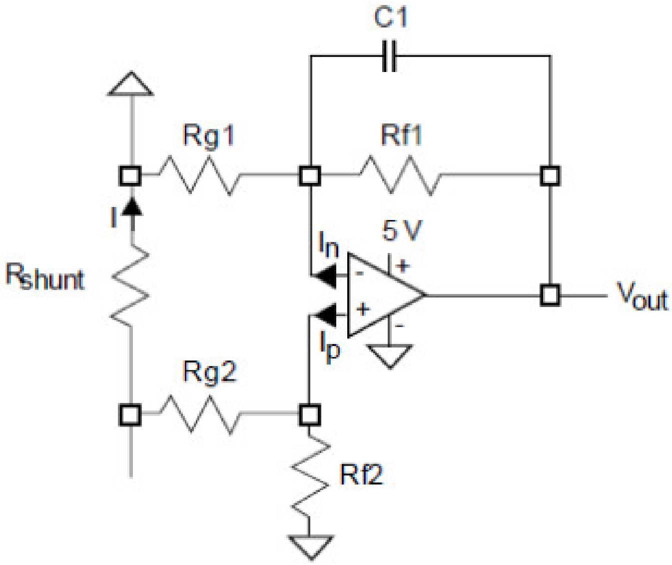
Accurate macromodels of the TSB952 device are available on the STMicroelectronics website at: www.st.com and in the STMicroelectronics simulation software eDSim. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSB952 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSB952 (see the figure below).

Figure 51. Low-side current sensing schematic



V_{OUT} can be expressed as follows:

$$V_{OUT} = R_{shunt} \cdot I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right) \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \cdot R_{f1} - \left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (4)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Eq. (4) can be simplified as follows:

$$V_{OUT} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{IO} \cdot \left(1 + \frac{R_f}{R_g}\right) + R_f \cdot I_{IO} \quad (5)$$

The main advantage of using the TSB952 for low-side current sensing relies on its speed (high bandwidth and slew rate) allowing for a better control of many applications thanks to its fast detection of current change.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO8 package information

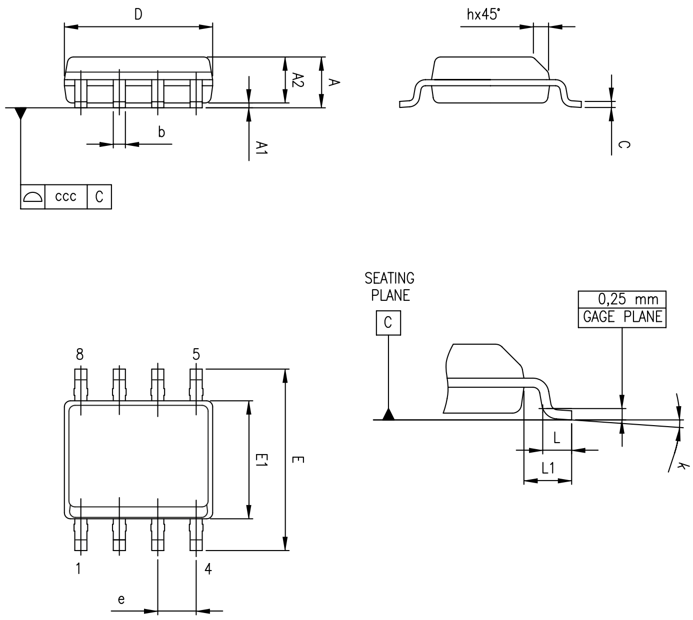
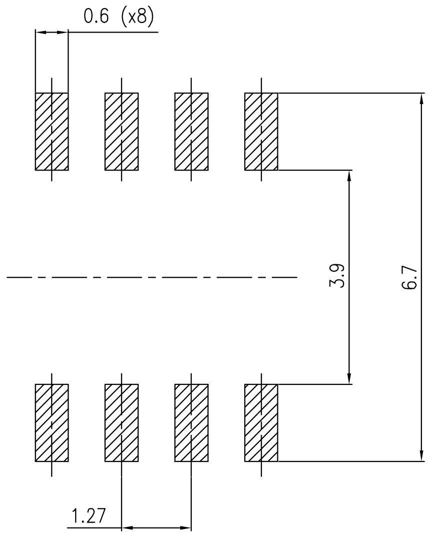


Figure 52. SO8 package outline

Table 7. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

Figure 53. SO8 recommended footprint



7.2 DFN8 3x3 exposed pad, wettable flank package information

Figure 54. DFN8 3x3 exposed pad, wettable flank package outline and mechanical data

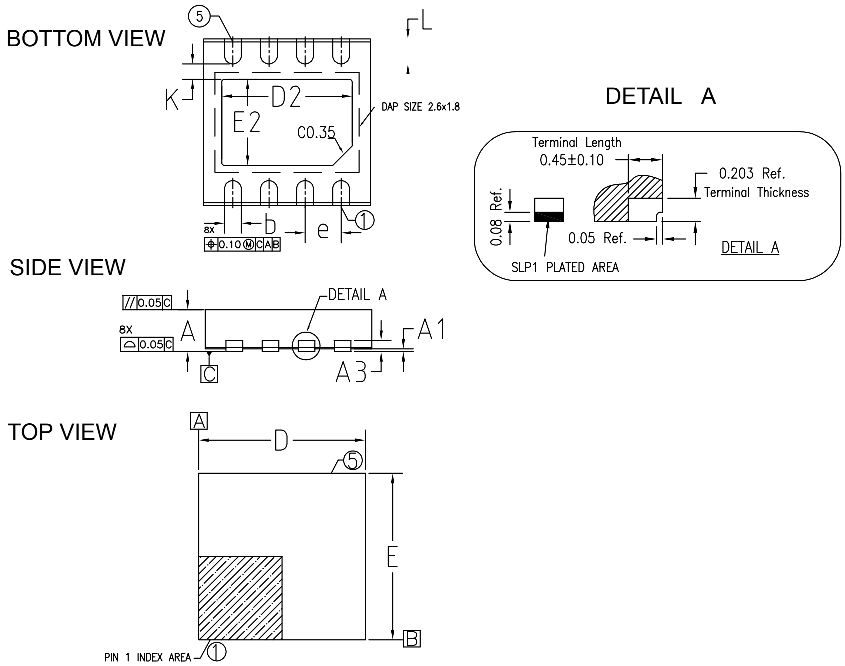
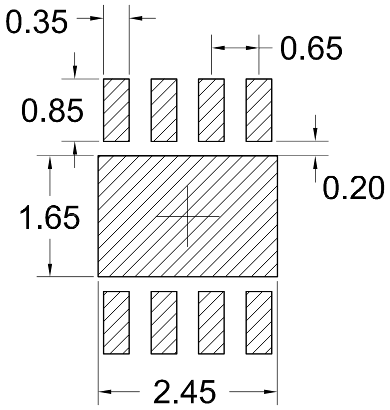


Table 8. DFN8 3x3 exposed pad, wettable flank mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.0		0.05
A3	0.20 Ref.		
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.25	2.35	2.45
e	0.65 BSC		
E	2.95	3.00	3.05
E2	1.45	1.55	1.65
L	0.35	0.45	0.55
K	0.275 Ref.		
N	8		

Figure 55. DFN8 3x3 exposed pad, wettable flank footprint data



8 Ordering information

Table 9. **Order code**

Order code	Package	Packaging	Marking
TSB952IDT	SO8	Tape & Reel	TSB952I
TSB952IYDT [(1)]			TSB952IY
TSB952IQ2T	DFN8 3x3 WF		K2P
TSB952IYQ2T [(1)]			K2Q

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Feb-2024	1	Initial release.
29-Jul-2024	2	Updated V_{OL} max. value in Table 6.

Contents

List of tables

List of figures