

High Efficiency Fast Response, 98% Duty, 6A, 24V Input Synchronous Buck Converter

General Description

The SY83086A is a high efficiency synchronous buck converter operating over a wide input voltage range of 4.5V to 24V and capable of delivering up to 6A current. It integrates low $R_{DS(ON)}$ top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 600kHz, to enable the use of small size inductor and capacitors. The SY83086A also provides a bypass switch which allows the VCC to be powered by external 3.3V power supply, further reduce the power consumption of the entire system.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY83086A provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 28m Ω Top, 16m Ω Bottom
- Wide Input Voltage Range: 4.5V ~ 24V
- Adjustable Output Voltage: 0.6V ~ 12.5V
- High Duty Cycle Capable using On-Time Stretch
- 6A Continuous Output Current Capability
- 600kHz Pseudo-Constant Frequency
- $\pm 1\%$ Internal Reference Voltage
- Internal 1.2ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Integrated 1.2 Ω Bypass Switch
- PFM/FCCM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Adjustable Valley Current Limit Threshold by ILMT Pin
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Output Over Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5x2.5-16

Applications

- LCD-TV/Net-TV/3D-TV
- Set Top Box
- Notebook
- High Power AP

Typical Application

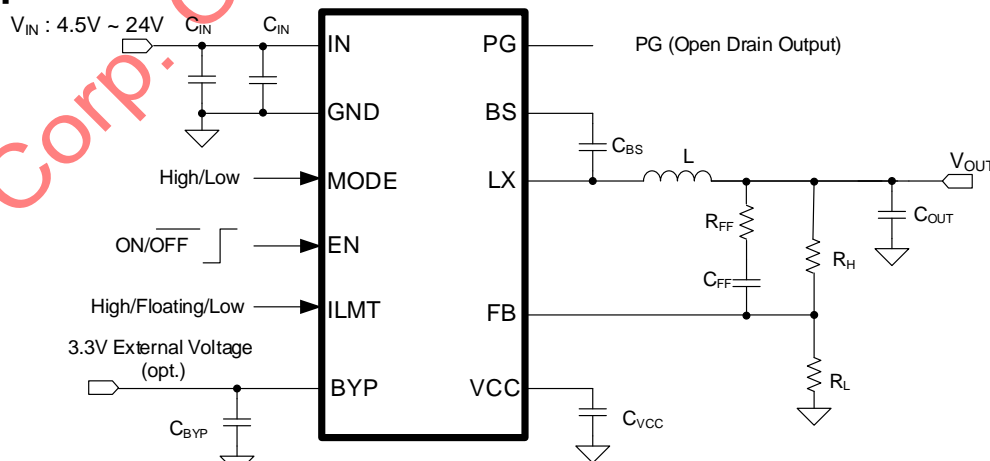


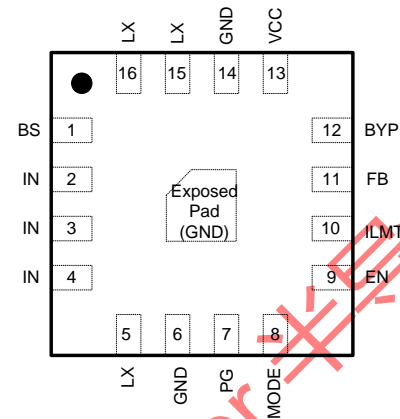
Figure 1. Schematic Diagram

Ordering Information

Ordering Number	Package type	Top Mark
SY83086ARHC	QFN2.5×2.5-16 RoHS Compliant and Halogen Free	GBGxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
2, 3, 4	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
5, 15, 16	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6, 14, EP	GND	Ground pin.
7	PG	Power good indicator pin. PG pin should be connected to V _{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
8	MODE	Light load operation mode selection pin. Pull this pin low for pulse-frequency modulation mode operation and pull this pin high for forced continuous conduction mode operation. Do not leave this pin floating.
9	EN	Enable control pin of the device. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.
10	ILMT	Valley current limit threshold selection pin. See Table1 to find more details.
11	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
12	BYP	External 3.3V bypass power supply input pin. Decouple this pin to ground with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the 3.3V external power ripple is large. Leave this pin floating or connect this pin to the ground if it is not used.
13	VCC	Internal 3.3V LDO output pin. Power supply for internal analog circuits. Decouple this pin to ground with at least a 2.2μF ceramic capacitor.

Block Diagram

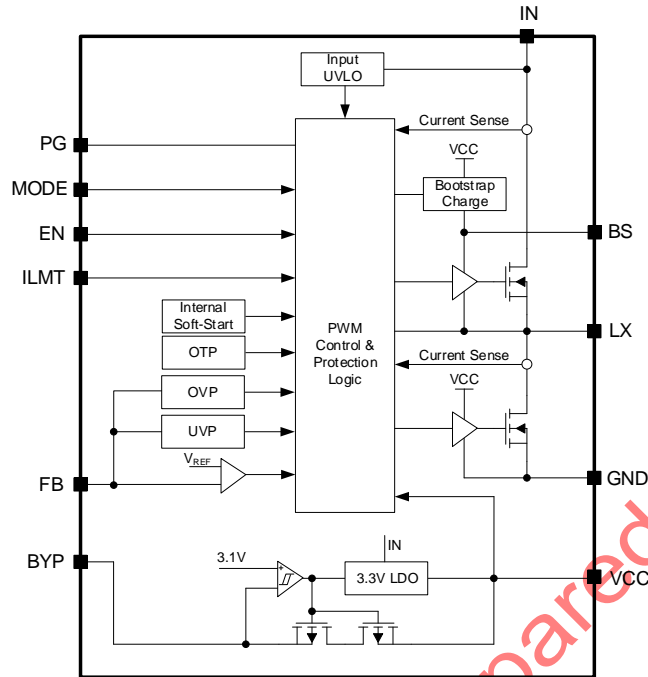


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	26	V
IN-LX, LX, PG, EN, MODE	-0.3	IN + 0.3	
BS-LX, ILMT, VCC, FB	-0.3	4	
BYP	-0.3	6	
LX, 10ns Duration	GND - 5	IN + 3	
LX, 20ns Duration	GND - 1	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	33	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5.5	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	3	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4.5	24	V
Output Voltage	0.6	12.5	
Continuous Output Current		6	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

 (V_{IN} = 12V, C_{OUT} = 66μF, C_{FF} = 220pF, R_{FF} = 1kΩ, T_J = 25°C, I_{OUT} = 1A unless otherwise specified (Note4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input	Voltage Range	V _{IN}	4.5		24	V	
	UVLO Rising Threshold	V _{IN,UVLO}	V _{IN} rising		4.4		
	UVLO Hysteresis	V _{IN,HYS}		0.5			
	Quiescent Current 1	I _{Q1}	EN = High, V _{BYP} = 0V, V _{OUT} = V _{SET} × 105%	190	240	μA	
	Quiescent Current 2	I _{Q2}	EN = High, V _{BYP} = 3.3V, V _{OUT} = V _{SET} × 105%	50	75		
	Shutdown Current	I _{SHDN}	EN = Low	5	9		
Output	Voltage Range	V _{OUT}	0.6		12.5	V	
	Feedback Reference Voltage	V _{REF}	0.594	0.600	0.606		
	FB Input Current	I _{FB}	V _{FB} = 1V	-50		50	nA
	Discharge Current	I _{DIS}	V _{OUT} = 5V		100		mA
	Soft-Start Time	t _{SS}	V _{OUT} from 0% to 100% V _{SET} (Note5)		1.2		ms
	OVP Threshold	V _{OVP}	V _{FB} rising	115	120	125	%V _{REF}
	OVP Hysteresis	V _{OVP,HYS}			5		
	OVP Delay Time	t _{OVP,DLY}	(Note5)		40		μs
	UVP Threshold	V _{UVP}	V _{FB} falling	55	60	65	%V _{REF}
	UVP Delay Time	t _{UVP,DLY}	(Note5)		200		μs
MOSFETs	Top MOSFET R _{DS(ON)}	R _{DS(ON),TOP}		28		mΩ	
	Bottom MOSFET R _{DS(ON)}	R _{DS(ON),BOT}		16			
	Top MOSFET Current Limit Threshold	I _{LMT,TOP}		17		A	
	Bottom MOSFET Current Limit Threshold	I _{LMT,BOT}	ILMT = Low	6			
			ILMT = Floating	8			
Bottom MOSFET Reverse Current Limit Threshold	I _{LMT,RVS}	FCCM mode	2.4	3			
Enable (EN)	Input Voltage High	V _{EN,H}	1			V	
	Input Voltage Low	V _{EN,L}			0.4		
	Input Current	I _{EN}	V _{EN} = 3.3V		0		μA
	De-Glitch Time	t _{EN,DG}	(Note5)		40		μs
MODE	Voltage for PFM Mode	V _{MODE,PFM}	0		0.4	V	
	Voltage for FCCM Mode	V _{MODE,FCCM}	1		V _{IN}		
	Input Current	I _{MODE}	V _{MODE} = 3.3V		0		μA
ILMT	Input Voltage High	V _{ILMT,H}	(Note5)	V _{CC} - 0.8		V	
	Input Voltage Low	V _{ILMT,L}	(Note5)		0.4		
Frequency	Switching Frequency	f _{SW}	V _{OUT} = 5V, CCM	510	600	690	kHz
	Minimum On-Time	t _{ON,MIN}	V _{IN} = V _{IN,MAX}		50		
	Minimum Off-Time	t _{OFF,MIN}			150		ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Power Good (PG)	Rising Threshold	$V_{PG,R}$	V_{FB} rising (good)	86	90	94	% V_{REF}
	Falling Threshold	$V_{PG,F}$	V_{FB} falling (not good)	81	85	89	
	Delay Time	$t_{PG,R}$	Low to high (Note5)		200		μ s
		$t_{PG,F}$	High to low (Note5)		40		
		$t_{PG,OFF}$	IC shuts down (Note5)			0.5	
Low Voltage	$V_{PG,LOW}$	$V_{FB} = 0V, I_{PG} = 5mA$			0.4	V	
VCC	Output Voltage	V_{CC}	VCC adds 1mA load		3.37		
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.2	Ω	
	Turn On Voltage	V_{BYP}		2.97	3.1	3.25	V
	Turn On Hysteresis	$V_{BYP,HYS}$			0.2		
	OVP Voltage	$V_{BYP,OVP}$			120		% V_{CC}
OTP	Temperature	T_{OTP}	T_J rising (Note5)		150		$^{\circ}$ C
	Temperature Hysteresis	$T_{OTP,HYS}$	T_J falling (Note5)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

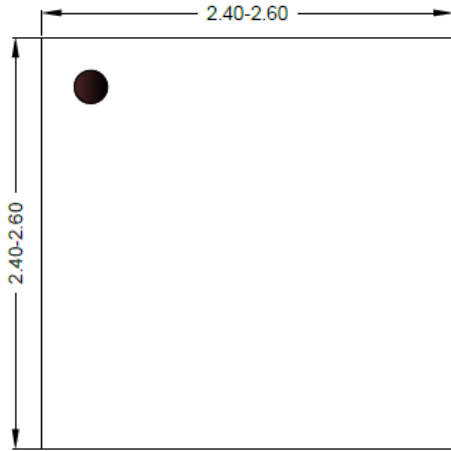
Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^{\circ}$ C on a 8.5cm \times 8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

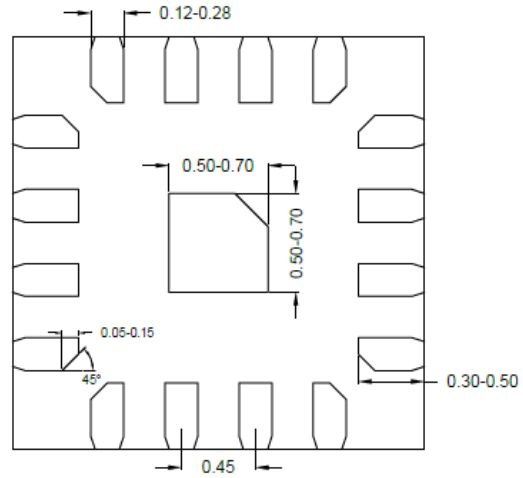
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^{\circ}$ C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design.

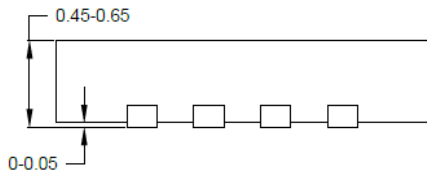
QFN2.5x2.5-16 Package Outline Drawing



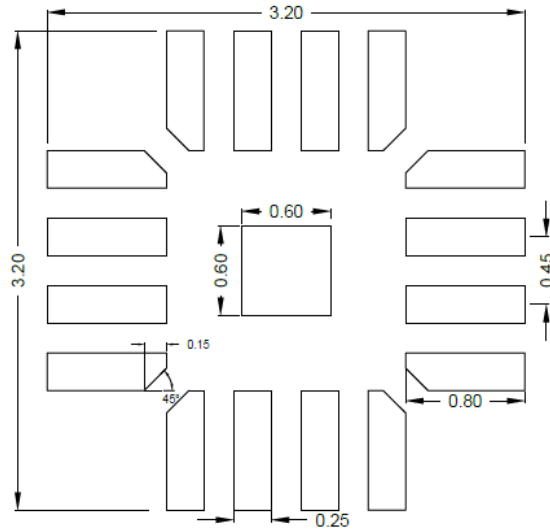
Top view



Bottom view



Side view

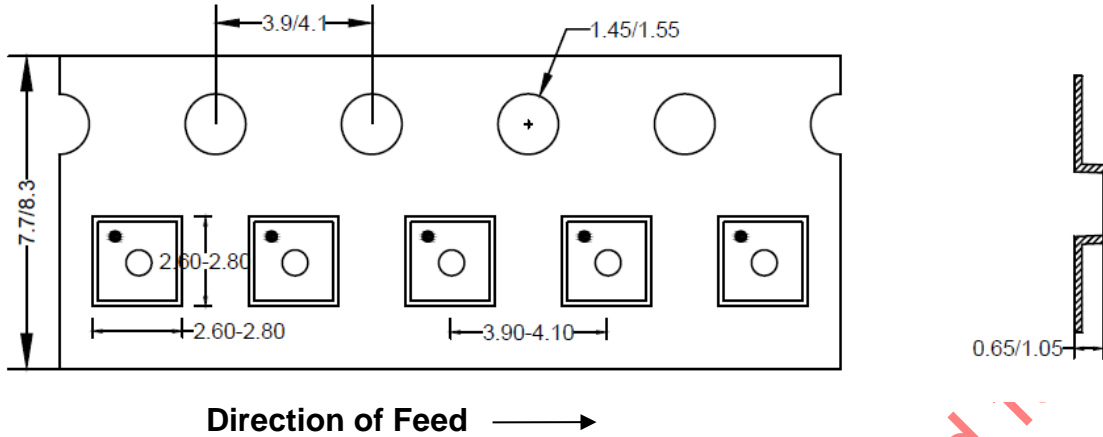


**Recommended PCB layout
(Reference only)**

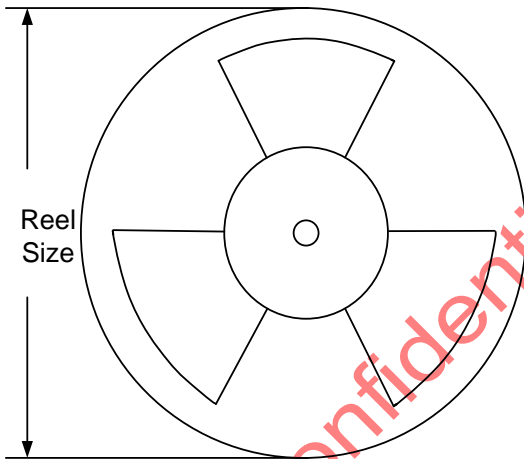
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

1. Tape dimensions and Pin1 orientation



2. Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5x2.5	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
July 10, 2024	1.0	Initial Release	-

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