



S3 Family of Microcontrollers

S3 Embedded Flash Serial Programming

Programming Specification

PRS002402-0315

PRELIMINARY



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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page Number
Mar 2015	02	Corrected title on cover page.	
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Introduction

Zilog's S3 family of products is based on the SAM8 CPU and features an efficient register-oriented architecture. This document describes the serial protocol used to erase and program Flash memory on S3 devices using a programming tool. The S3 Flash Programming protocol is based on the standard Inter-Integrated Circuit (I2C) protocol with the following modifications:

- The S3 Flash programming protocol uses inverted Start and Stop conditions, that is:
 - Start condition $SCLK = V_{DD}$, rising edge on SDAT
 - Stop condition $SCLK = V_{DD}$, falling edge on SDAT
- The S3 Flash programming protocol uses a 24-bit address field as opposed to the 7-bit (or 10-bit) address field used within the standard I2C protocol
- The S3 flash programming protocol does not implement (and does not need to implement) bus arbitration
 - The programming tool is always the Master and the S3 device being programmed is always the Slave
- Unlike the standard I2C protocol, the slave device in the S3 Flash programming protocol does not generate an ACK bit after every 8 address or data bits transmitted by the master
- Unlike the standard I2C protocol the master device in the S3 Flash programming protocol does not generate an ACK bit after every 8 data bits transmitted by the slave
- Unlike the standard I2C protocol, the master device does not abort a transfer if an address or data byte is not acknowledged by the slave

Physical Signalling

The S3 Flash programming protocol requires the following signals between the programming tool and the S3 device being programmed: Serial Data (SDAT), Serial Clock (SCLK), Test (V_{PP}), Reset, V_{DD} , and V_{SS} . Table 1 provides more information about these signals.

Table 1. Programming Protocol Signals

Signal	Programming Tool (master)	S3 Device (slave)	In User mode (if multiplexed with GPIO)
SCLK	Output	Input	Behaves as it is defined by the setting in SFR
SDAT	Output for Flash Programming Input for Reading Flash	Input for FLASH Programming Output for Reading Flash	Behaves as it is defined by the setting in SFR
Reset	Output	Input, Active Low	Input active low, use a pullup to V_{CC}
$V_{PP}/Test$	Output	Input, Active High	Input, connect to the GND by 10k resistor in parallel with 0.1 μ F capacitor

S3 Serial Programming Protocol

Before an S3 device can be programmed, the programming tool must place the S3 device in Tool Mode by performing the following sequence:

1. Activate V_{DD}
2. Assert Reset
3. Assert the $V_{PP}/Test$ Pin

V_{DD} , Reset, and V_{PP} must remain asserted while the S3 Flash programming protocol is used.

Bus Transaction Overview

To program an S3 device, the programming tool issues a single command within an S3 serial programming bus transaction. Figure 1 shows an arbitrary 2-byte bus transaction and Figure 2 shows an S3 serial programming bus transaction for reading/ writing data.

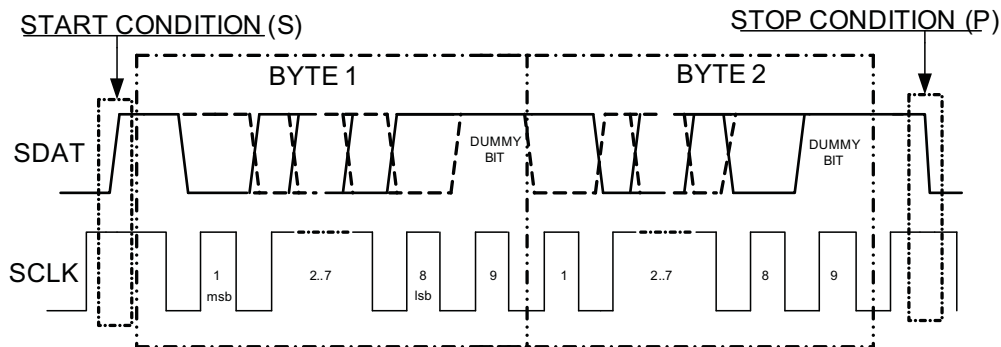


Figure 1. Arbitrary 2-byte Bus Transaction

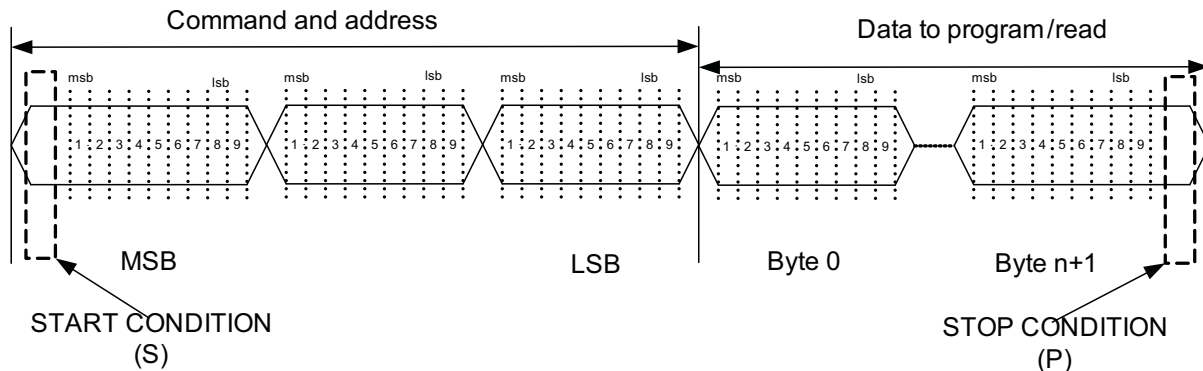


Figure 2. Programming/Reading Device

Each S3 serial programming bus transaction consists of the following components: Start Condition, S3 Command and Address Field, Data Field, and Stop Condition. Following each 8-bit quantity in the address and data fields, the S3 programming protocol appends 1 dummy clock cycle.

Timing requirements are listed in the [Electrical Characteristics](#) section on page 13.

Start Condition

The S3 Flash programming protocol Start condition is identified by a rising edge on SDAT with SCKL at V_{DD} .

Command and Address Field

The Command and Address field of the S3 programming protocol is always 24-bits/ 3-bytes wide. The Address bytes are transferred most significant byte (MSB) first. Within each address byte, bits are transferred most significant bit (msb) first. Four bits within the most significant address byte are control bits that specify whether the command is a read or write, and whether the command targets the main Flash cell or the secondary Flash cell. The remaining 20 bits in the address field specify the start address of the Flash region targeted by that command. Refer to the [S3 Flash Programming Overview](#) section on page 5 for more information.

The address field is sent once at the beginning of the transaction. If there are multiple bytes of data in the data field, then the address field is automatically incremented (inside the S3 chip) after each byte of the data field is processed. This applies to S3 programming commands that target either the main Flash cell (contains the application program) or the secondary flash cell (contains Smart Options and various S3 protection control registers).

Data Field

This field contains the data to be read or written to the memory cell. Each byte in the data field is transferred most significant bit first.

► **Note:** The setting of the Read Lock protection bit in the Smart Options will affect Read/ Verify commands.

When read-lock protection is enabled, the data field of Read/Verify commands will contain bytes of 0x00 regardless of the actual contents of the addressed cell

Stop Condition

The S3 Flash programming protocol Stop condition is identified by a falling edge on SDAT with SCL at V_{DD} .

Dummy Clock

Following each 8-bit quantity transferred in the Address and Data fields, the master device (programming tools) generates one dummy clock cycle. During the dummy clock the SDAT line is held at V_{DD} . It is permissible for the master device (programming tool) to generate a Stop condition within the last dummy clock cycle of the last byte in the data field instead of appending a Stop condition after the dummy clock cycle.

S3 Flash Programming Overview

Application programs running on the S3 can use the LDC instruction to program individual bytes of Flash and use the integrated Flash controller to erase individual Flash sectors. This is referred to as *User Mode*. For more information on User Mode programming, please refer to the appropriate S3 Product Specification. In addition, the S3 family of devices can be programmed by an external device implementing the protocol described in this document. This is referred to as *Tool Mode*.

S3 Family of device contains two areas of Flash:

- Main Flash cell that contains the user code. Programmable in User and Tool modes.
- Secondary Flash cell that contains Smart Option control bits and S3 protection control registers. The Smart Option control bits are used to configure the S3 device at POR and are described in the appropriate S3 Product Specification. The Protection control registers are used to enable LDC, Read and Hard-Lock protection of the S3 device. The Secondary cell is only accessible in Tool mode.

In User Mode, applications are able to erase one or more sectors in the Main Flash cell; but are not able to erase the entire device (Chip Erase). In User Mode, the Secondary Flash cell is not readable or programmable. Tool Mode does not provide any commands to erase individual sectors; only a command to erase the entire S3 device (Chip Erase). A Chip Erase will erase both the Main Flash cell and the Secondary Flash cell containing the Smart Option and Protection control registers. A Chip Erase will disable all protection controls and sets each Smart Option control bit to 1.

Typically, S3 programming tools provide an option to program the Smart Option control bits in the Secondary Flash using data from addresses 0x3C to 0x3F in the Hex file used to program the Main Flash. When this option is enabled, the contents of Main Flash from address 0x3C through 0x3F will contain a "mirror image" of the actual Smart Option control bits in the Secondary cell. However, even if the application modifies Main cell locations 0x3C to 0x3F at run-time, this will have no effect on the actual Smart-Option control bits in the Secondary cell.

Some members of the S3 family have only two Smart Option bytes located at the upper addresses of Smart Option area. Please refer to the appropriate S3 data sheet for more information.

Table 2 lists all available commands for the Tool and User Modes.

Table 2. Available Commands for Tool and User Modes

Command	Description	Supported in the Mode	
		Tool Mode	User Mode
Chip Erase	Erases whole Flash memory of device, including Smart Options and Protection Area	Yes	No
Sector Erase	Erases a single sector in main Flash area of the device	No	Yes
Byte/Sector Program	Programs byte or sector of Main Flash	Yes	Yes
Read Protect	Protects code from being read by external tool. All data appeared as 00 . Can be cleared by Chip Erase.	Yes	No
Hard Lock	Disables Programming of device. Can be cleared by Chip Erase.	Yes	No
LDC Protect	Reading of the Flash by LDC operation is disabled when in User Mode.	Yes	No
Smart Option	Programmes Smart Option Area of the chip.	Yes	No

S3 Serial Programming Protocol Commands

Table 3 lists the set of commands supported by the S3 family when operated in Tool Mode and the format of the Address fields the master device sends in a bus transaction to initiate each command.

Table 3. S3 Serial Programming Protocol Commands

	BYTE 1				BYTE 2	BYTE 3	Data
	23	22-21	20-17	16			
Function	Access Control ¹ (nMain, Secondary/ Both) 0/1	Reserved	A[19:16]	nWrite/ Read 0/1	Address 1	Address 0	D[7:0]
Command							
Chip Erase	1	11	0000	0	55H(15H)	xxH	AAH
Program	0	11	xxxx ²	0	xxH	xxH	xxH
Read/Verify	0	11	xxxx ²	1	xxH	xxH	D[7:0]
Smart Option	1	11	0000	0/1	0EH	38H	xxH
	1	11	0000	0/1	0EH	39H	xxH
	1	11	0000	0/1	0EH	3AH	xxH
	1	11	0000	0/1	0EH	3BH	xxH
LDC Protection	1	11	0000	0/1	0EH	3CH	00H ³
Hard Lock	1	11	0000	0/1	0EH	3DH	00H ³
Read Protection	1	11	0000	0/1	0EH	3EH	00H ³
Notes	<ol style="list-style-type: none"> 1. When the Access Control bit is set to 0 the Main Flash cell is accessed. When the Access Control bit is 1 the command is either targeting the Secondary Flash Cell or both the Main and Secondary Flash cells. 2. Since S3 devices have no more than 64KB of Flash in the main cell, address bits A[19..16] should always be set to 0000b. 3. To enable LDC, Read, or Hard-Lock protection issue a write command (b16=0) with a data byte value of 00H. When reading the current state of the LDC, Read or Hard-Lock protection registers issue a 1-byte read command (b16=1) and the S3 device will return the value currently in the specified register, xxH. 						

Chip Erase Command

The Chip erase command is used to erase the contents of the main Flash cell as well as the secondary cell containing the Smart Options bits and the S3 protection control registers (LDC protection, Read protection and Hard Lock protection).

The address field of the Chip Erase transaction is typically set to 0xE05515 but the value of the 3rd address byte is a don't-care and any other value can be used. It is also permissible to use 0x15 instead of 0x55 in the second address byte.

The Data field of the Chip Erase command consists of a single don't-care value. Typically the data field is set to 0xAA. As with all S3 Flash programming commands in which the nWrite/ Read bit (bit 16 of the address field) set to 0, the Data field is terminated with a dummy byte of 0xFF followed by the Stop Condition. The Stop condition can be generated in the dummy clock of the terminal 0xFF data byte or in a separate clock pulse.

Program Command

Programming Flash is the process of setting one or more bits within a particular byte of Flash to 0. It is not possible to change a 0 bit to a 1 via the Program Command. Therefore prior to programming any byte of Flash, the location to be programmed must have been previously erased (see the Chip Erase Command).

Programming the main Flash cell (where the application program is stored in the S3 device) is initiated when the master issues a command with the Access Control bit (bit 23) and the nWrite/ Read (bit 16) bits of the first address byte set to 0. Address bits A[19..0] specify the address of the first byte to be programmed within the main Flash cell.

The first byte of data in the data field is programmed at the address corresponding to the value of the address bits (A0..A19) in the Address field (n); the second byte of data in the Data field is programmed at address (n+1), etc. In other words, the target Flash address is automatically incremented (inside the S3 device) after each byte in the Data field is programmed to Flash.

The S3 slave starts programming the target Flash address on the falling edge of the dummy clock following the last bit in the data byte about to be programmed. While a byte is being programmed, the S3 programming protocol is able to transfer the data bits of the next byte to be programmed. To ensure that the S3 slave device has time to finish programming the previous data byte, dummy clocks (clock pulses generated after every 8 address or data bits) must be at least 30µs apart. To ensure that the last byte of data is successfully programmed, each Program transaction should include a single dummy byte of 0xFF immediately before the Stop condition.

The number of data bytes in the Program command is only restricted by the size of the Flash cell being programmed. For example, if the target S3 device contains 16KB of Flash then the maximum number of data bytes in the Write command should be less than or equal to 16KB +1 (for the dummy 0xFF byte).

The Stop condition explicitly indicates the end of the Program command and the S3 programming protocol transaction. The master can generate the Stop condition in a clock cycle following the dummy clock cycle of the 0xFF dummy byte, or during the dummy clock cycle of the 0xFF dummy byte.

Read/ Verify Command

Reading data from the main Flash cell is initiated when the master issues a command with the Access Control bit (bit 23) set to 0 and the nWrite/ Read (bit 16) bit set to 1. Address bits A[19..0] specify the offset (n) of the first byte to be read from the main Flash cell. During read transactions the S3 slave device drives SDAT during the 8 clock periods between dummy pulses and the master drives SDAT during the dummy clock cycle.

The S3 slave device reads the first byte of data from location (n) during the dummy clock cycle that follows the 3rd address byte. The S3 slave device transmits the data byte read from Flash (most significant bit first) during the next 8 clock pulses. During the dummy clock cycle after the first data byte, the S3 slave reads the next byte of data from Flash location (n+1) to be transmitted to the master during the next 8 clock periods. In general, during the dummy clock cycle that follows the data byte read from location n the S3 slave device reads the contents of Flash location (n+1) which are transferred to the master during the next 8 clock pulses.

A read operation is explicitly terminated by a Stop condition. The master can generate the S3 programming protocol Stop condition in place of, or immediately after, the dummy clock cycle following the last byte of data the master intended to read during the transaction.

As with the Program transaction, the maximum number of data bytes in the read transaction is limited by the size of the Flash cell being read. For example, if the target S3 device contains 16KB of Flash then the maximum number of data bytes in the read/ Verify command should be less than or equal to 16KB.

Smart Option Command

The S3 Smart Option control bits are used during device Power-On Reset (POR) to set the operating characteristics of the device. The meaning of individual bits within the Smart Option area is specified in the relevant S3 Product Specification.

The Smart Option bits reside in a secondary Flash cell that is in a different address space than the main Flash cell that holds the application program. Smart Option bits cannot be accessed by programs running on an S3 device. The secondary cell containing the Smart Option area is only accessible through S3 programming protocol transactions that have the Access Control bit of the Address field (Bit 23) set to 1. The Smart Option area in the secondary cell is 4 bytes long at offsets 0x38 to 0x3B in the secondary cell.

To read the contents of the entire Smart Option area, the Address field of the Smart Option transaction should be set to `0xE10E38` and the master should read 4 bytes of data by generating 36 clock pulses followed by a Stop condition. Optionally, the Stop condition can be combined with the 36th clock pulse. It is permissible for the master to read 1, 2, 3 or 4 bytes of Smart Option data by altering the Address field of the transaction and number of clock pulses as necessary. For example, to read the two smart option bytes at `0x3A` and `0x3B` the starting address would be set to `0xE10E3A` and 18 clock pulses would be generated (9 per byte).

► **Note:** Typically, the Smart Option bits in S3 Product Specification documents indicate that the Smart Option bits are located at code-space addresses `0x3C` to `0x3F` in the main Flash cell. Technically, this is inaccurate since the Smart Option bits actually reside in the secondary Flash cell. By convention, a copy of the Smart Option bits is often stored in the main cell at offsets `0x3C` to `0x3F`. Additionally, programming tools typically provide an optional control that generates a Smart Option transaction using data located between `0x3C` and `0x3F` from the Hex file used to program the main Flash cell. Data from offset `0x3C` in the Main cell is mapped to Smart Option offset `0x3A` in the secondary cell. Similarly main cell offsets `0x3D` to `0x3F` are mapped to Smart Option offsets `0x3B` to `0x3D` in the secondary cell.

To program the contents of the entire Smart Option area, the Address field of the Smart Option transaction should be set to `0xE00E38` and the Data field contains the 4 bytes of Smart Option Data to be programmed. Similar to main cell programming, the secondary cell Flash target-address automatically increments after each Smart Option byte is programmed. The S3 programming protocol master can write 1, 2, 3, or 4 bytes of Smart option control bits in a single command by altering the start address and number of data bytes included in the command.

As with all S3 programming Protocol commands in which the nWrite / Read bit (bit 16 of the address field) set to 0, the Data field is terminated with a dummy byte of `0xFF` followed by the Stop Condition. The Stop condition can be generated in the dummy clock of the terminal `0xFF` data byte or in a separate clock pulse.

Once a Smart Option bit is programmed to 0 it cannot be changed to 1 until a Chip Erase command is issued. After executing a Chip Erase command, all of the S3 Smart Option bits are all set to 1.

LDC Protection Command

The S3 instruction set includes the LDC command (the LDCD, LDCI, LDCPD, and LDCPI variants) that allow the contents of a byte of Flash in the main cell (where the application program is stored) to be read at run-time if LDC protection is disabled (default). If LDC protection is enabled, then when the S3 CPU executes an LDC instruc-

tion (or one of its variants) the data read from the target address in the main Flash cell will be indeterminate based on the last value on the data bus immediately before the LDC instruction (or one of its variants) and will typically not match the actual contents of the target Flash address.

To read the contents of the LDC protection control register, the Address field of the LDC Protection command is set to `0xE10E3D`. The master then generates 8 clock pulses to read the LDC protection byte followed by a dummy clock and a Stop condition. Alternatively they Stop condition can be generated in place of the dummy clock. If the data value read is non-zero, then LDC protection is disabled. If the value read is zero, then LDC protection is enabled.

To enable LDC protection the Address field of the LDC Protection command is set to `0xE00E3D`. In addition the Data field is set to `0x00` followed by a dummy byte of `0xFF` and the Stop condition. The Stop condition can be generated in the dummy clock of the terminal `0xFF` data byte or in a separate clock pulse. After LDC protection is enabled, it can only be disabled by performing a Chip Erase.

It is permissible to read or program the LDC protection register in combination with other protection control registers and/ or any combination of the Smart Option bytes.

Hard Lock Protection Command

S3 devices typically contain a Flash controller that can be configured by an application program to erase and/ or program one or more sectors of the main Flash cell at run time if, and only if, Hard Lock protection is disabled. When hard-lock protection is enabled, application programs are unable to erase any sector of Flash in the main cell; and unable to program any byte of Flash memory. Regardless of whether hard lock protection is enabled or disabled, application programs are never able to access locations within the secondary cell containing the Smart Option control bits and protection registers.

To read the contents of the hard-lock control register, the Address field of the Hard Lock Protection command is set to `0xE10E3E`. If the data value read is non-zero, then Hard Lock protection is disabled. If the value read is zero, then Hard Lock protection is enabled.

To enable Hard Lock protection the Address field of the Hard Lock Protection command is set to `0xE00E3E`. Additionally, the Data field is set to `0x00` (followed by a dummy byte of `0xFF`). After Hard Lock protection is enabled, it can only be disabled by performing a Chip Erase.

It is permissible to read or program the Hard Lock protection register in combination with other protection control registers and/ or any combination of the Smart Option bytes.

It is permissible for the master device (programming tool) to generate the Stop condition within the last dummy clock cycle of the last byte in the data field instead of appending a Stop condition after the dummy clock cycle.

Read Protection Command

When the S3 programming tool (serial programming protocol master device) issues a Read/ Verify command, the tool is able to read the contents of the main Flash array if, and only if, Read Protection is disabled. If Read Protection is enabled, the S3 slave device will drive the SDAT signal to V_{SS} during each clock pulse for all data bytes in the Read/ Verify transaction. Consequently, every byte read by the programming tool (regardless of the target address or main/ secondary cell) will have the value of 0x00.

To read the contents of the read-protection control register, the Address field of the Read Protection command is set to 0xE10E3F. If the data value read is non-zero, then Read protection is disabled. If the value read is zero, then Read protection is enabled.

To enable Read protection the Address field of the Read Protection command is set to 0xE00E3F. In addition the Data field is set to 0x00 (followed by a dummy byte of 0xFF). Once Read protection is enabled, it can only be disabled by performing a Chip Erase.

It is permissible to read or program the Read protection register in combination with other protection control registers and/ or any combination of the Smart Option bytes.

It is permissible for the master device (programming tool) to generate a Stop condition within the last dummy clock cycle of the last byte in the data field instead of appending a Stop condition after the dummy clock cycle.

Timing Waveforms

Figure 3 illustrates the timing waveforms during a start condition and Figure 4 illustrates the timing waveform during a stop condition.

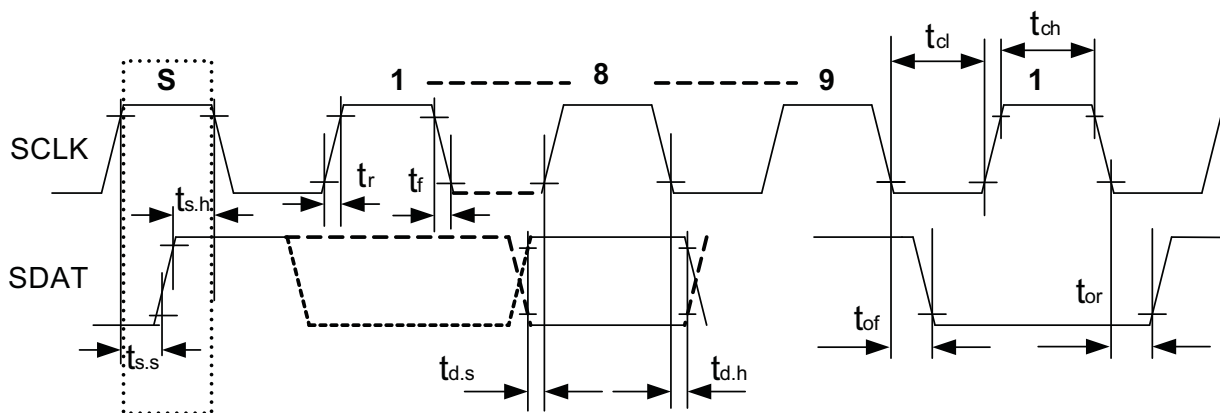


Figure 3. Interface Timing, Start

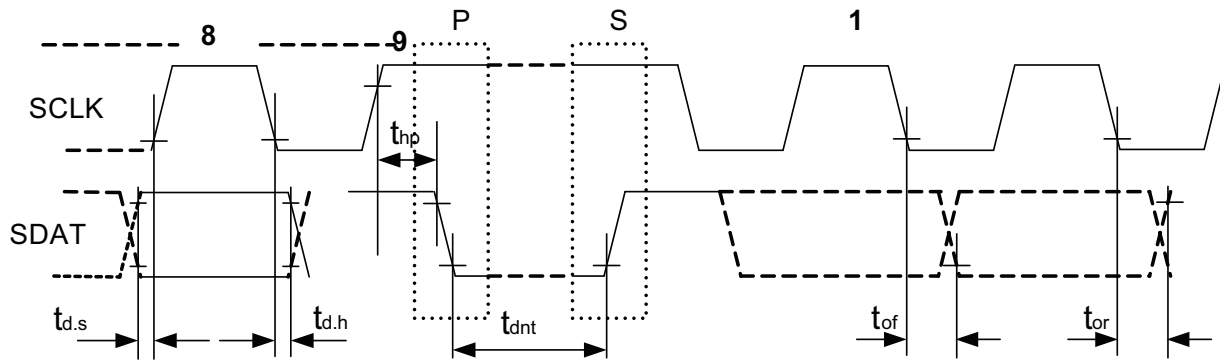


Figure 4. Interface Timing, Stop

Electrical Characteristics

Table 4 lists the electrical characteristics for the S3 series of microcontrollers.

Table 4. Electrical Characteristics

Symbol	Parameter	Min	Typ	Max
V_{DD} , V	Power Supply	3.0	3.3	3.6
V_{PP} , V*	Test pin level	3.0	3.3	3.6
F_{SCLK} , KHz	SCLK Frequency	20	300	300**
$t_{ch} = t_{cl}$, nS	Clock High		1.5	
$t_r = t_f$, nS	SCLK Rise and Fall time		30	
t_{of} , nS	Data Out High to Low		200	
t_{or} , nS	Data Out Low to High		200	
$t_{ds} = t_{dh}$, nS	Data In setup and hold	150		
t_{ss} , uS	Data setup for Start delay	1		
t_{hp} , uS	Data hold for Stop	1		
T_{pgm} , uS	Byte programming cycle time	–	–	30***
T_{ced} , mS	Chip erase delay	–	–	70***

Notes

- * - unless noted differently test pin level is always the same as V_{DD}
- ** - When reading data from the S3 device, the frequency of SCLK can be increased to 3MHz. To guarantee a minimum byte programming time of 30us, SCLK should be restricted to 300kbps when writing data (i.e. programming) to the S3 device.
- *** The programming tool must wait the maximum time indicated after a program or erase command before issuing another command.