



### Features

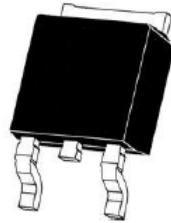
- Super high dense cell design for extremely low RDS(on)
- High power and current handing capability
- Lead free product is acquired

### Application

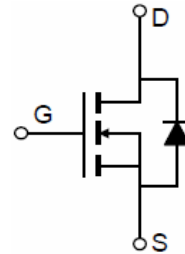
- Load Switch
- PWM Application
- Power management

### Product Summary

BVDSS	20	V
RDS(on),Typ.@VGS=4.5V	20	mΩ
ID	20	A



TO-252-2L top view



Schematic diagram

### Absolute Maximum Ratings (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous	I <sub>D</sub>	20	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub>	80	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	32	W
		0.25	W/°C
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	4	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	50	°C/W

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 12V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -12V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	0.4		1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 8A$		20	42	$m\Omega$
		$V_{GS} = 2.5V, I_D = 6.6A$		25	75	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 8A$		15		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		515		pF
Output Capacitance	$C_{oss}$			220		pF
Reverse Transfer Capacitance	$C_{rss}$			80		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, I_D = 1A,$ $V_{GS} = 4.5V, R_{GEN} = 6\Omega$		19		ns
Turn-On Rise Time	$t_r$			13		ns
Turn-Off Delay Time	$t_{d(off)}$			48		ns
Turn-Off Fall Time	$t_f$			9		ns
Total Gate Charge	$Q_g$	$V_{DS} = 10V, I_D = 8A,$ $V_{GS} = 4.5V$		10		nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			2		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				20	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 4A$			1.3	V

**Notes :**

a.Repetitive Rating : Pulse width limited by maximum junction temperature

b.Pulse Test : Pulse Width < 300 $\mu$ s, Duty Cycle < 2%.

c.Guaranteed by design, not subject to production testing.

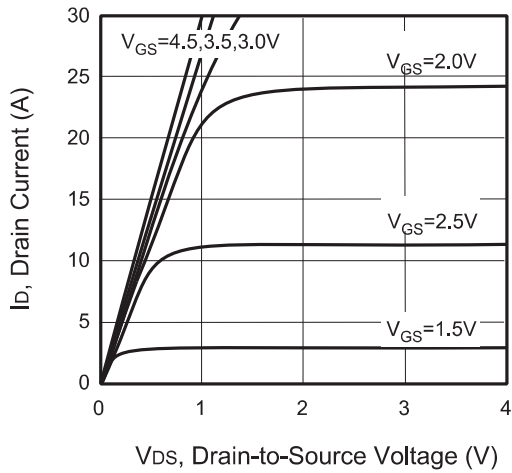


Figure 1. Output Characteristics

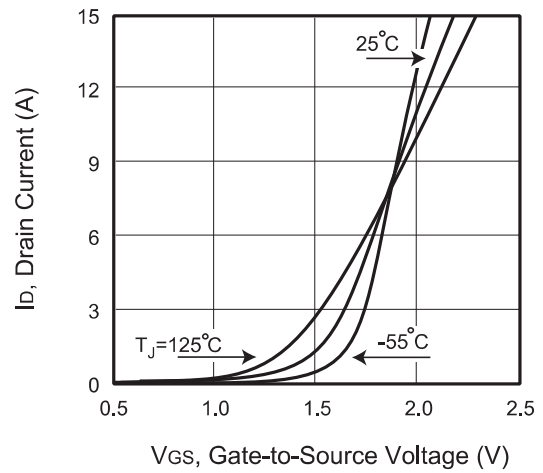


Figure 2. Transfer Characteristics

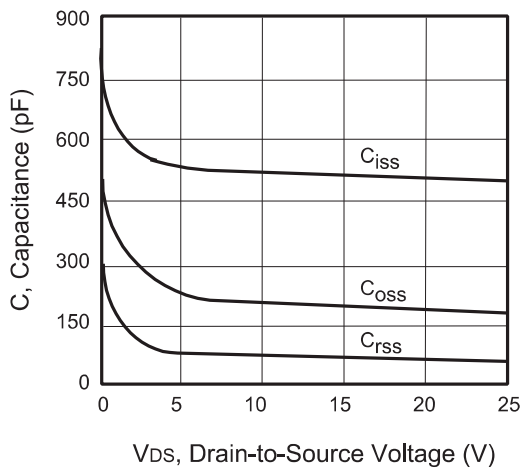


Figure 3. Capacitance

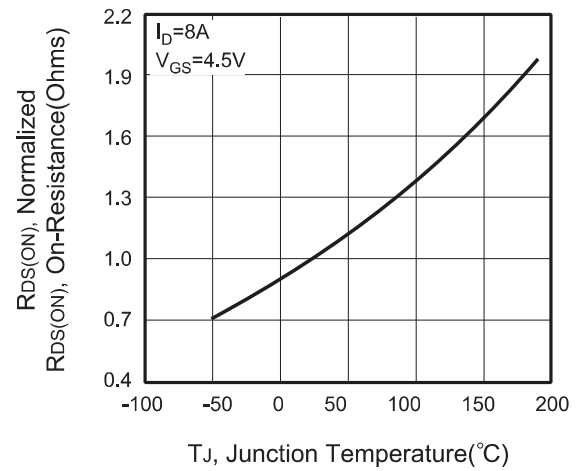


Figure 4. On-Resistance Variation with Temperature

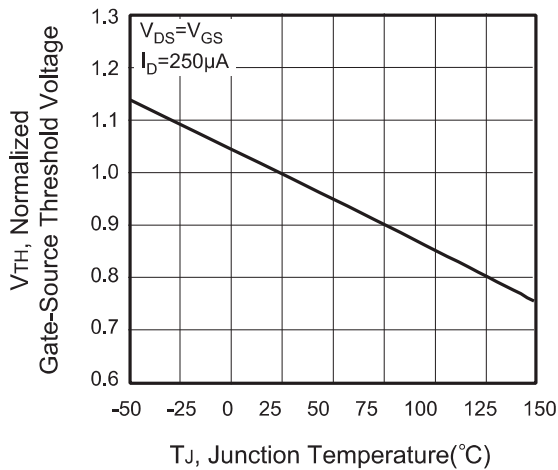


Figure 5. Gate Threshold Variation with Temperature

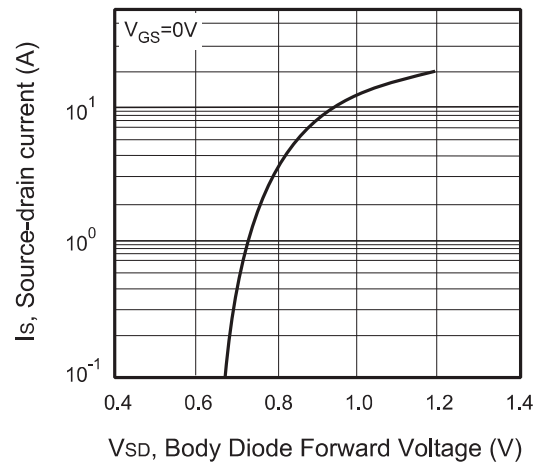


Figure 6. Body Diode Forward Voltage Variation with Source Current

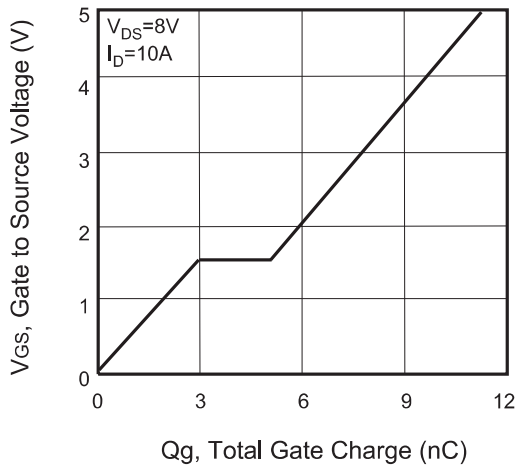


Figure 7. Gate Charge

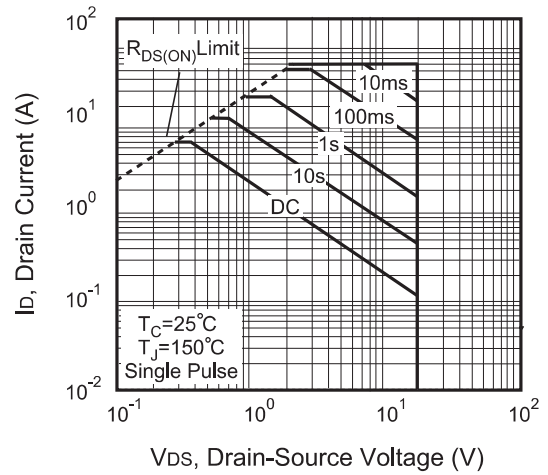


Figure 8. Maximum Safe Operating Area

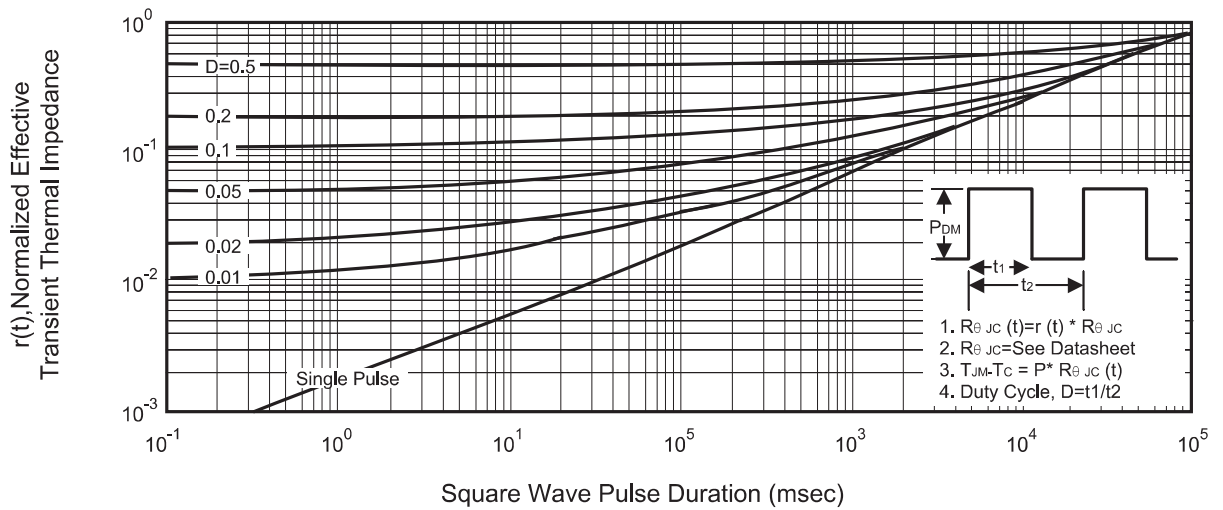
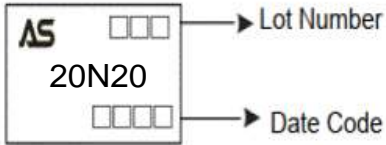


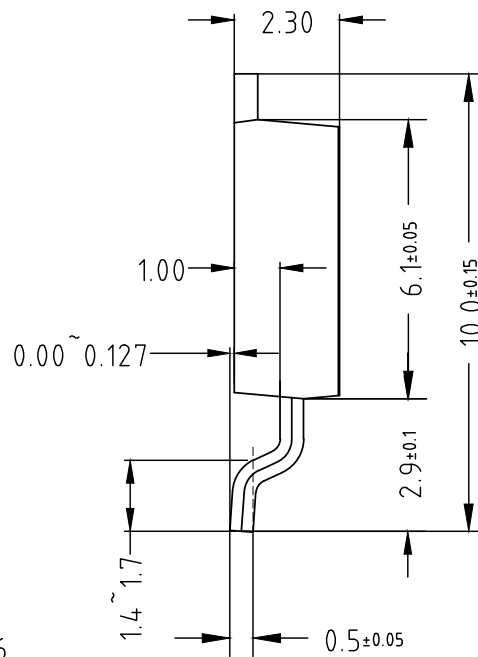
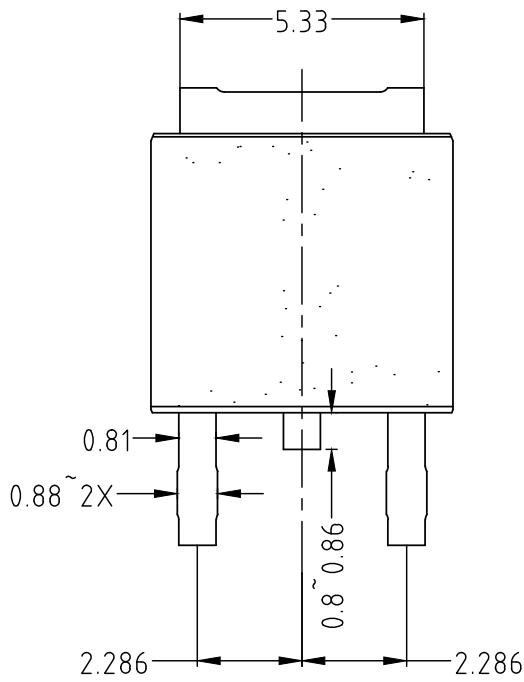
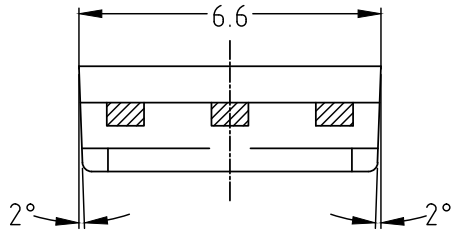
Figure 9 . Normalized Thermal Transient Impedance Curve

### Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM20N20KQ-R	20N20	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>AS    □□ → Lot Number 20N20 □□□□ → Date Code</p>

# TO-252



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