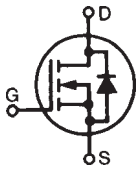
IXYS

PolarHT™ HiPerFET IXFR 102N30P
Power MOSFET

(Electrically Isolated Back Surface)

V_{DSS} = 300 V
I_{D25} = 60 A
$R_{DS(on)}$ ≤ 36 mΩ
t_{rr} ≤ 200 ns

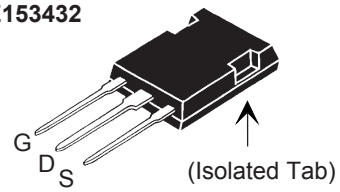
N-Channel Enhancement Mode
Fast Intrinsic Diode
Avalanche Rated



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	300	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	300	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	60	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	250	A
I_{AR}	T_C = 25°C	60	A
E_{AR}	T_C = 25°C	60	mJ
E_{AS}	T_C = 25°C	2.5	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	250	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_C	Mounting force	22..130/5..29	N/lb
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	300			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	μA
	T_J = 125°C			250	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 51 A, Pulse test, t ≤300 μs, duty cycle d ≤ 2 %			36	mΩ

ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect

Advantages

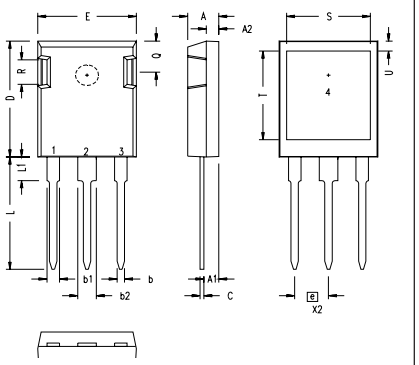
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V; I_D = 51 A, pulse test	45	57		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7500		pF
C_{oss}			1150		pF
C_{rss}			230		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 51 A R_G = 3.3 Ω (External)		30		ns
t_r			28		ns
$t_{d(off)}$			130		ns
t_f			30		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 51 A		224		nC
Q_{gs}			50		nC
Q_{gd}			110		nC
R_{thJC}				0.5	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			102	A
I_{SM}	Repetitive			250	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤300 μs, duty cycle d≤ 2 %			1.5	V
t_{rr}	I_F = 25 A, -di/dt = 100 A/μs			200	ns
Q_{RM}	V_R = 100 V, V_{GS} = 0 V		0.8		μC
I_{RM}			7		A

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Fig. 1. Output Characteristics @ 25ºC

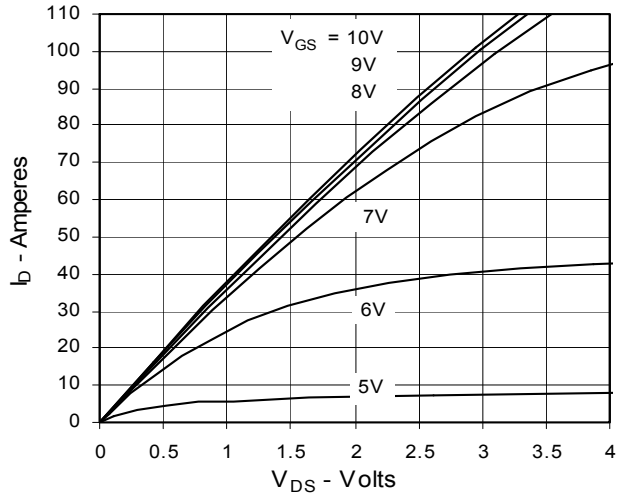


Fig. 2. Extended Output Characteristics @ 25ºC

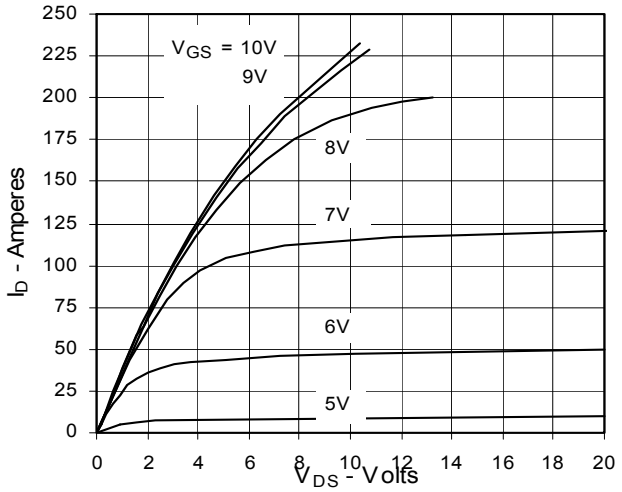


Fig. 3. Output Characteristics @ 125ºC

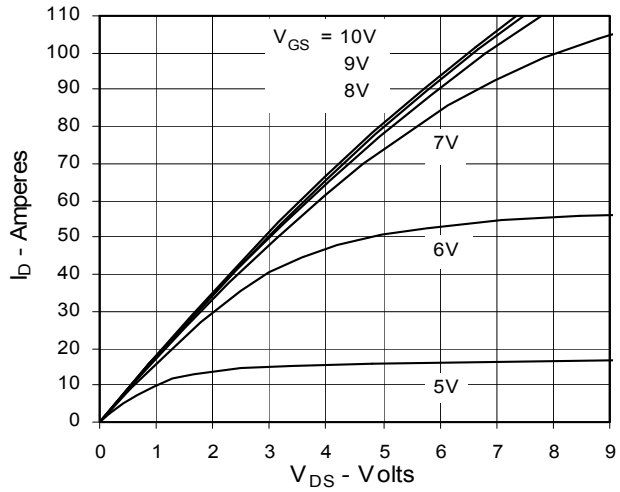


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 51A Value vs. Junction Temperature

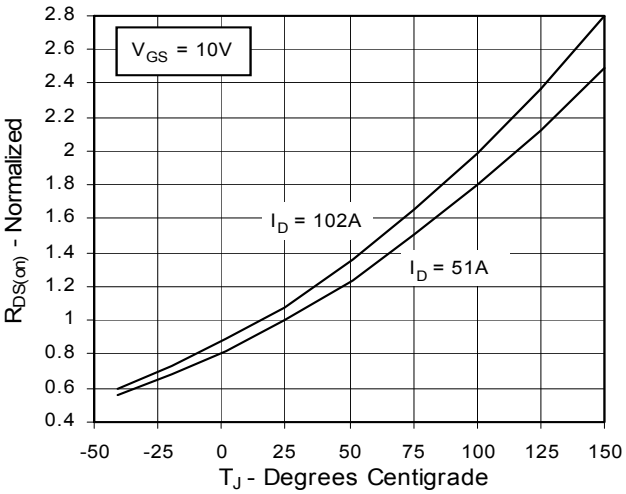


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 51A Value vs. Drain Current

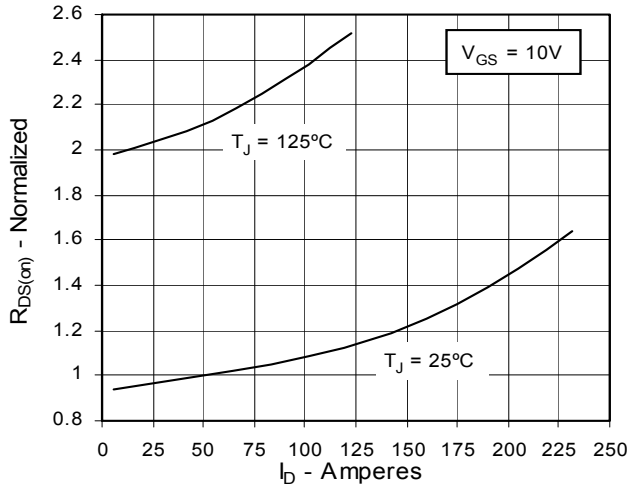


Fig. 6. Drain Current vs. Case Temperature

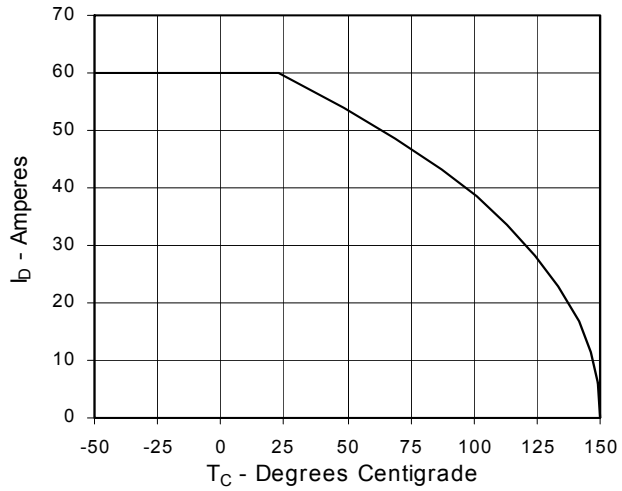


Fig. 7. Input Admittance

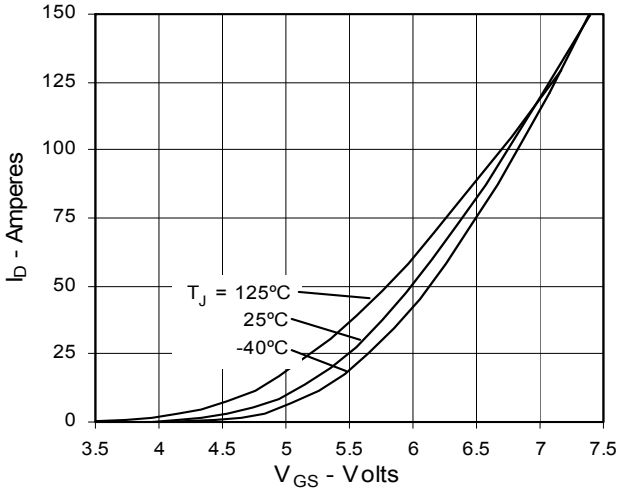


Fig. 8. Transconductance

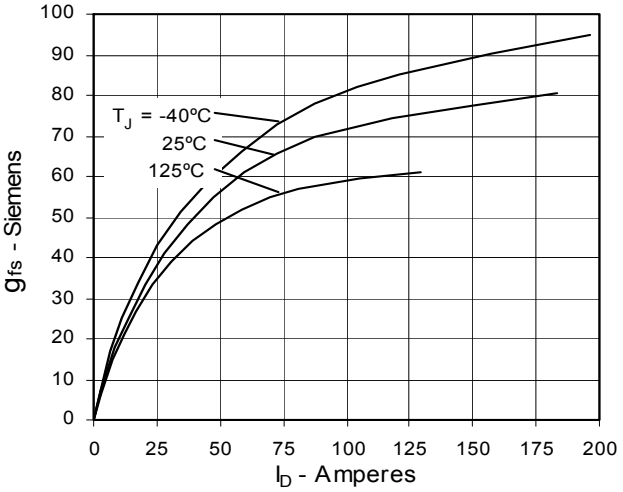


Fig. 9. Source Current vs. Source-To-Drain Voltage

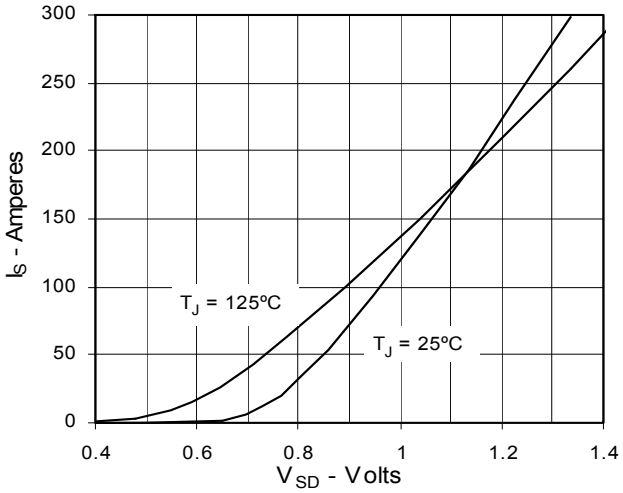


Fig. 10. Gate Charge

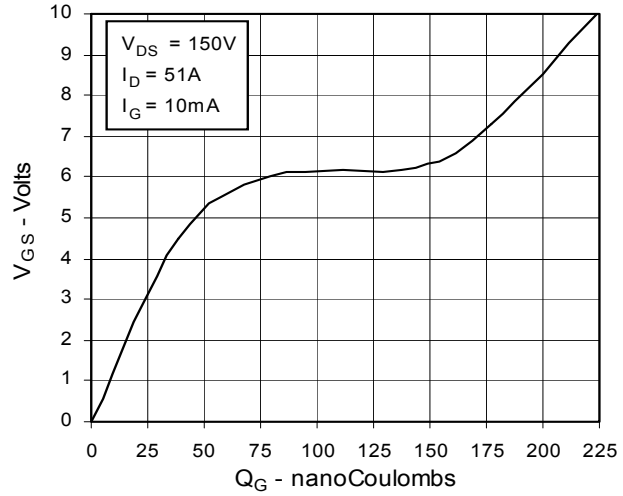


Fig. 11. Capacitance

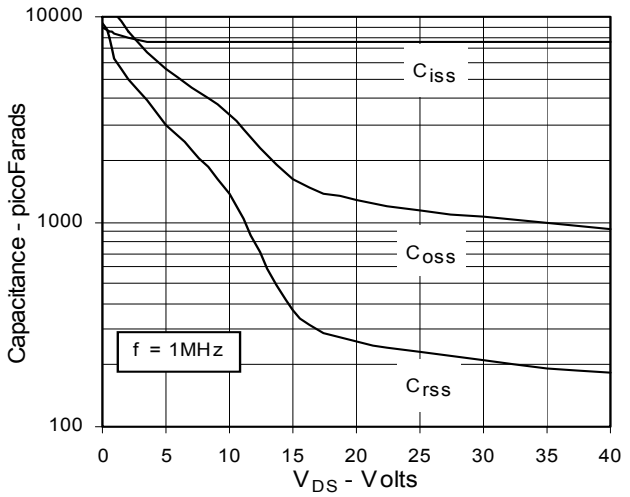


Fig. 12. Forward-Bias Safe Operating Area

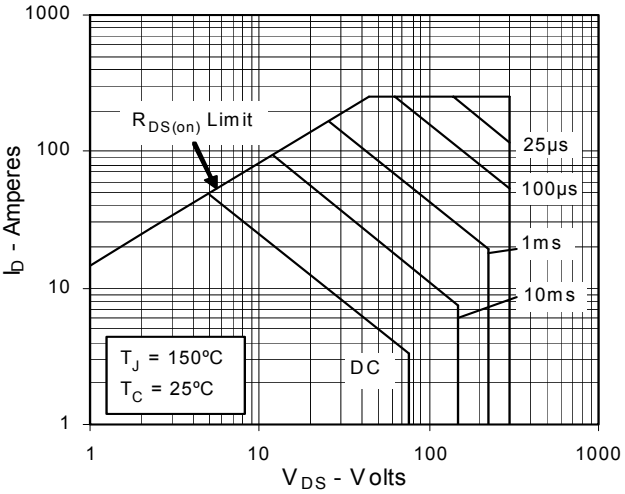


Fig. 13. Maximum Transient Thermal Resistance