

MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X .

Features

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- This part should only be used in new designs where the pulse width is $< 10 \mu\text{s}$
 Note: For designs requiring a pulse width $> 10 \mu\text{s}$, please see MC14538, which is pin-for-pin compatible
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Rating | Symbol | Value | Unit |
|---|-------------------|------------------------|--------------------|
| DC Supply Voltage Range | V_{DD} | -0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | V_{in}, V_{out} | -0.5 to $V_{DD} + 0.5$ | V |
| Input or Output Current (DC or Transient) per Pin | I_{in}, I_{out} | ± 10 | mA |
| Power Dissipation, per Package (Note 1) | P_D | 500 | mW |
| Ambient Temperature Range | T_A | -55 to +125 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}\text{C}$ |
| Lead Temperature (8-Second Soldering) | T_L | 260 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: $-7.0 \text{ mW}/^{\circ}\text{C}$ From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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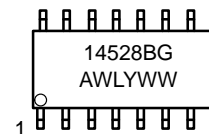


SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM



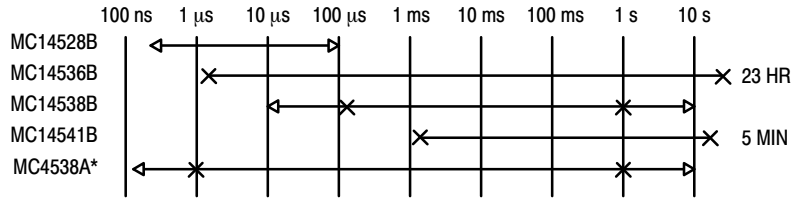
A = Assembly Location
 WL = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

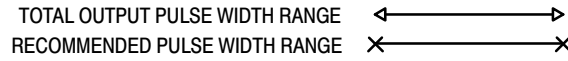
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC14528B

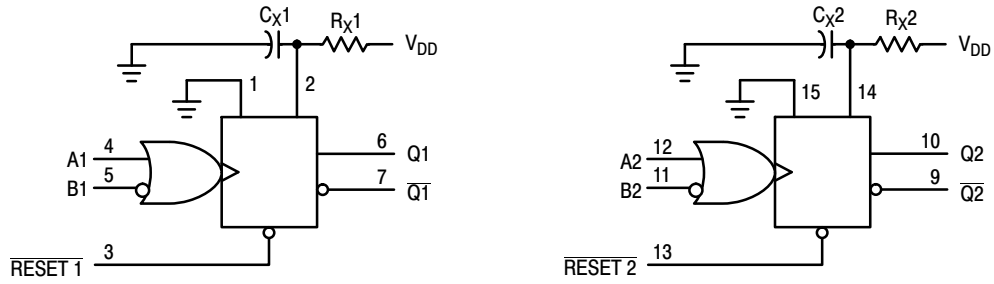
ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6 V)



BLOCK DIAGRAM



V_{DD} = PIN 16
 V_{SS} = PIN 1, PIN 8, PIN 15
 R_x AND C_x ARE EXTERNAL COMPONENTS

FUNCTION TABLE

| Reset | Inputs | | Outputs | |
|-------|--------|-------|---------------|---------------|
| | A | B | Q | \bar{Q} |
| H | | H | | |
| H | L | | | |
| H | | L | Not Triggered | Not Triggered |
| H | H | | Not Triggered | Not Triggered |
| H | L, H, | H | Not Triggered | Not Triggered |
| H | L | L, H, | Not Triggered | Not Triggered |
| L | X | X | L | H |
| | X | X | Not Triggered | Not Triggered |

MC14528B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55° C | | 25° C | | | 125° C | | Unit |
|--|---------------------------|------------------------|--|------|-------|-----------------|------|--------|------|------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | |
| Output Voltage "0" Level V _{in} = V _{DD} or 0 | V _{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| 15 | | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| "1" Level V _{in} = 0 or V _{DD} | V _{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | Vdc |
| | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | |
| | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | |
| Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | V _{IL} | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | Vdc |
| | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | |
| | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | |
| "1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IH} | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | - | Vdc |
| | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | - | |
| | | 15 | 11 | - | 11 | 8.25 | - | 11 | - | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source I _{OH} | 5.0 | -1.2 | - | -1.0 | -1.7 | - | -0.7 | - | mAdc |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | |
| (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | Sink I _{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | mAdc |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | |
| | | 15 | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | |
| Input Current | I _{in} | 15 | - | ±0.1 | - | ±0.00001 | ±0.1 | - | ±1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | C _{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | μAdc |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | |
| Total Supply Current at an external load Capacitance (C _L) and at external timing capacitance (C _X), use the formula. (Note 3) | I _T | - | $I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2 f] \times 10^{-3}$ where: I _T in μA (per circuit), C _L and C _X in pF, R _X in megohms, V _{DD} in Vdc, f in kHz is input frequency. | | | | | | | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

MC14528B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 4)

| Characteristic | Symbol | C_X pF | R_X k Ω | V_{DD} Vdc | Min | Typ (Note 5) | Max | Unit |
|--|--------------------------|-------------|---------------------|-----------------|--------------------|--------------------|-------------------|---------------|
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{TLH} , t_{THL} | – | – | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ | t_{PLH} , t_{PHL} | 15 | 5.0 | 5.0 10 15 | – – – | 325 120 90 | 650 240 180 | ns |
| Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$ | t_{PLH} , t_{PHL} | 1000 | 10 | 5.0 10 15 | – – – | 705 290 210 | – – – | ns |
| Input Pulse Width — A or B | t_{WH} | 15 | 5.0 | 5.0 10 15 | 150 75 55 | 70 30 30 | – – – | ns |
| | | 1000 | 10 | 5.0 10 15 | – – – | 70 30 30 | – – – | ns |
| Output Pulse Width — Q or \bar{Q} (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate V_{DD} level.) | t_W | 15 | 5.0 | 5.0 10 15 | – – – | 550 350 300 | – – – | ns |
| Output Pulse Width — Q or \bar{Q} (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]$) (Note 6) | t_W | 10,000 | 10 | 5.0 10 15 | 15 10 15 | 30 50 55 | 45 90 95 | μs |
| Pulse Width Match between Circuits in the same package | $t_1 - t_2$ | 10,000 | 10 | 5.0 10 15 | – – – | 6.0 8.0 8.0 | 25 35 35 | % |
| Reset Propagation Delay — $\bar{\text{Reset}}$ to Q or \bar{Q} | t_{PLH} , t_{PHL} | 15 | 5.0 | 5.0 10 15 | – – – | 325 90 60 | 600 225 170 | ns |
| | | 1000 | 10 | 5.0 10 15 | – – – | 1000 300 250 | – – – | ns |
| Retrigger Time | t_{rr} | 15 | 5.0 | 5.0 10 15 | 0 0 0 | – – – | – – – | ns |
| | | 1000 | 10 | 5.0 10 15 | 0 0 0 | – – – | – – – | ns |
| External Timing Resistance | R_X | – | – | – | 5.0 | – | 1000 | k Ω |
| External Timing Capacitance | C_X | – | – | – | No Limits (Note 7) | | | μF |

4. The formulas given are for the typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6. If $C_X > 15 \mu\text{F}$, Use Discharge Protection Diode D_X , per Figure 9.

7. R_X is in Ω , C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

MC14528B

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|--------------------|
| MC14528BDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14528BDR2G | SOIC-16 (Pb-Free) | 2500 / Tape & Reel |
| NLV14528BDR2G* | SOIC-16 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

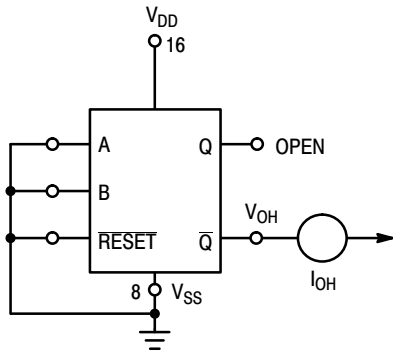


Figure 1. Output Source Current Test Circuit

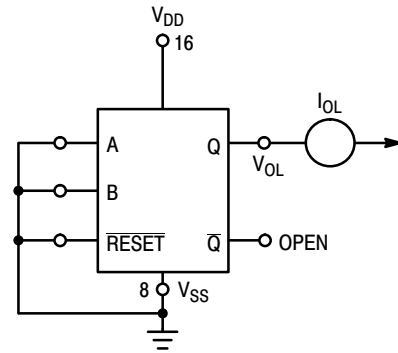


Figure 2. Output Sink Current Test Circuit

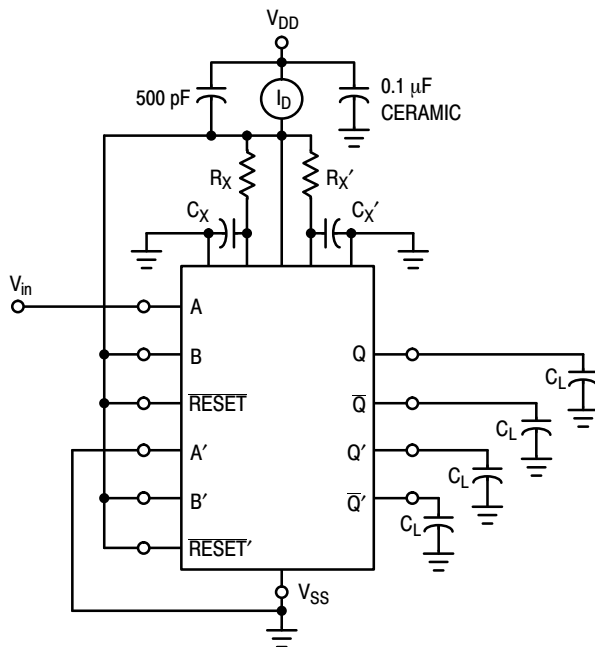


Figure 3. Power Dissipation Test Circuit and Waveforms

MC14528B



INPUT CONNECTIONS

| Characteristics | Reset | A | B |
|---|----------|----------|----------|
| $t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W$ | V_{DD} | PG1 | V_{DD} |
| $t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W$ | V_{DD} | V_{SS} | PG2 |
| $t_{PLH(R)}, t_{PHL(R)}, t_W$ | PG3 | PG1 | PG2 |

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.



Figure 4. AC Test Circuit

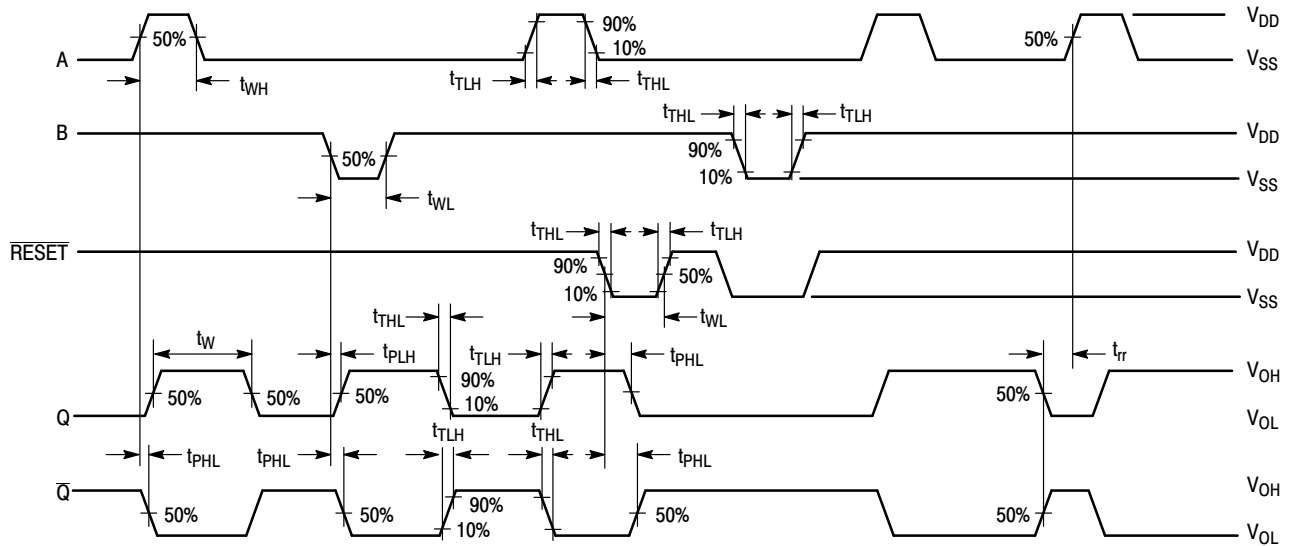


Figure 5. AC Test Waveforms

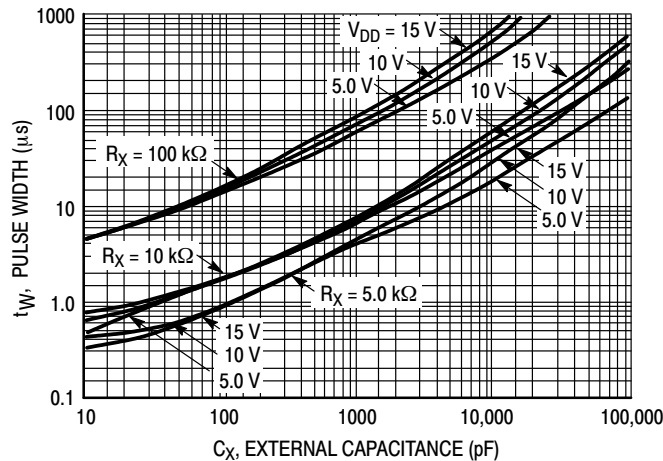


Figure 6. Pulse Width versus C_X

MC14528B

TYPICAL APPLICATIONS

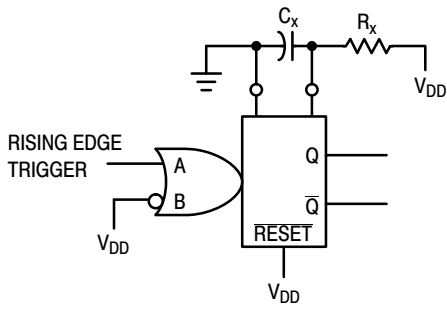


Figure 7. Retriggerable Monostables Circuitry

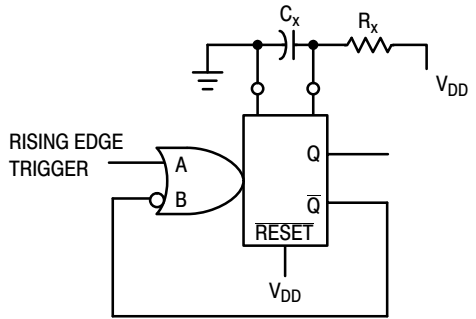


Figure 8. Non-Retriggerable Monostables Circuitry

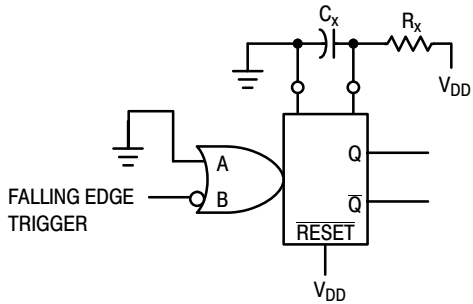


Figure 9. Use of a Diode to Limit Power Down Current Surge

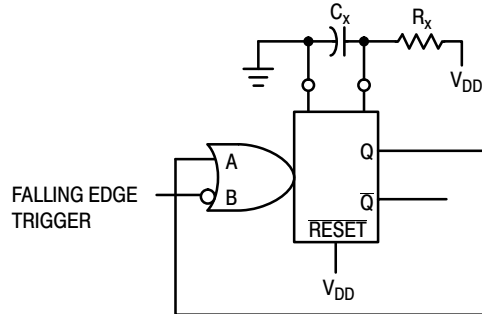


Figure 10. Connection of Unused Sections

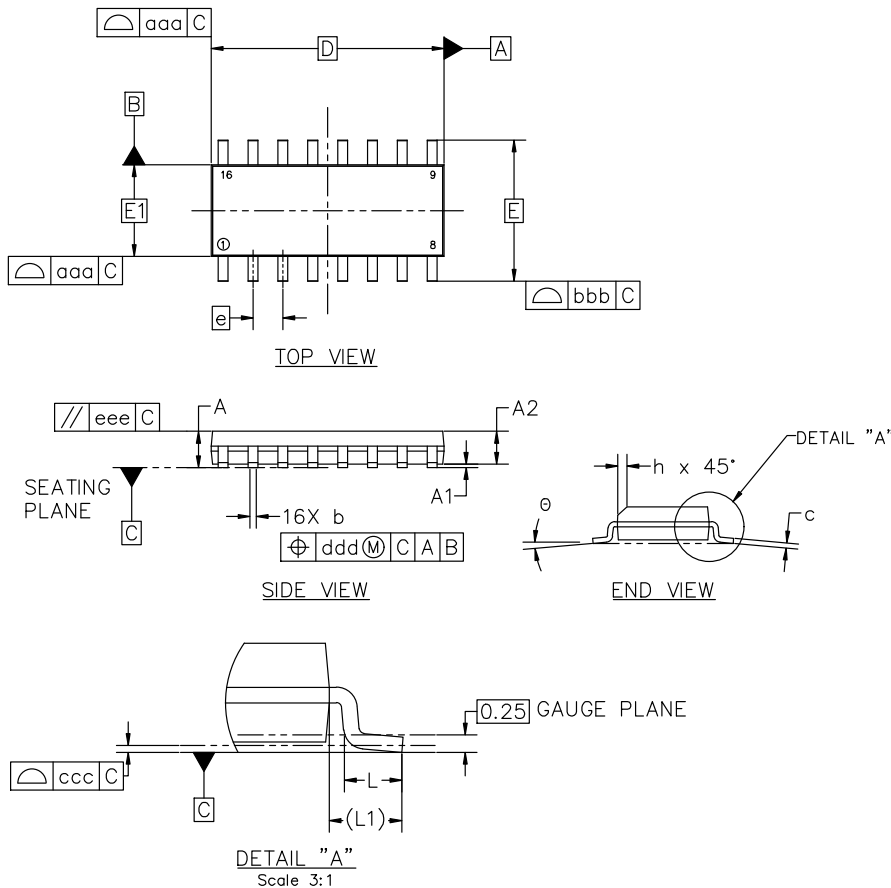


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS | | | |
|--------------------------------|----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | --- | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

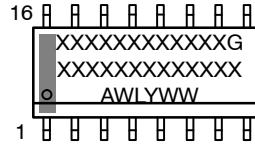
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SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

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