MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

Features

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- This part should only be used in new designs where the pulse width is < 10 μs
  Note: For designs requiring a pulse width > 10 μs, please see MC14538, which is pin−for−pin compatible
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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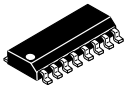
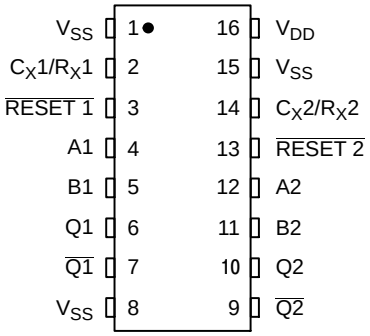


SOIC−16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



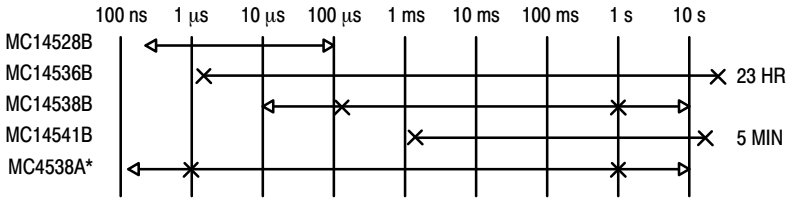
MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

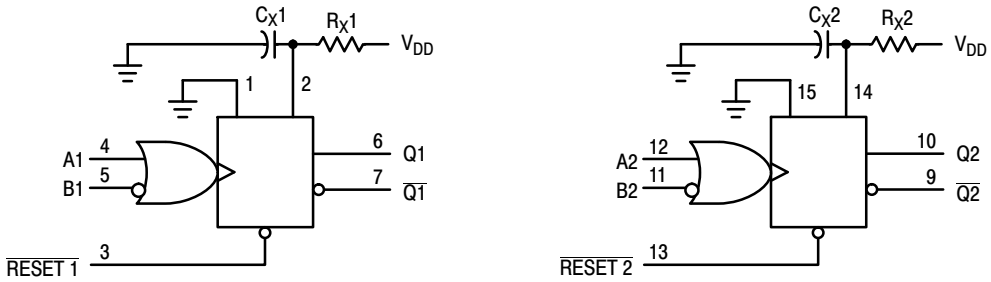
ONE−SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2−6 V)

TOTAL OUTPUT PULSE WIDTH RANGE
RECOMMENDED PULSE WIDTH RANGE

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 1, PIN 8, PIN 15
R_X AND C_X ARE EXTERNAL COMPONENTS

FUNCTION TABLE

Inputs			Outputs	
Reset	**A**	**B**	**Q**	**$\overline{Q}$**
H	↗	H	⌐¬	¬⌐
H	L	↘	⌐¬	¬⌐
H	↗↘	L	Not Triggered	
H	H	↗↘	Not Triggered	
H	L, H, ↘	H	Not Triggered	
H	L	L, H, ↗	Not Triggered	
L	X	X	L	H
↘↗	X	X	Not Triggered	

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	–1.2 –0.64 –1.6 –4.2	− − − −	–1.0 –0.51 –1.3 –3.4	–1.7 –0.88 –2.25 –8.8	− − − −	–0.7 –0.36 –0.9 –2.4	− − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula. (Note 3)	I_T	−	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2x10^{-8} R_XC_X(V_{DD}^{-2})^2f] \times 10^{-3}$ where: I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C) (Note 4)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ (Note 5)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	–	–	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Turn−Off, Turn−On Delay Time — A or B to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	t_{PLH}, t_{PHL}	15	5.0	 5.0 10 15	 – – –	 325 120 90	 650 240 180	ns
Turn−Off, Turn−On Delay Time — A or B to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns	t_{PLH}, t_{PHL}	1000	10	 5.0 10 15	 – – –	 705 290 210	 – – –	ns
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0 10 15	150 75 55	70 30 30	– – –	ns
	t_{WL}	1000	10	5.0 10 15	– – –	70 30 30	– – –	ns
Output Pulse Width — Q or $\overline{Q}$ (For C_X < 0.01 μF use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0 10 15	– – –	550 350 300	– – –	ns
Output Pulse Width — Q or $\overline{Q}$ (For C_X > 0.01 μF use formula: t_W = 0.2 R_X C_X Ln [V_{DD} – V_{SS}]) (Note 6)	t_W	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	μs
Pulse Width Match between Circuits in the same package	t1 – t2	10,000	10	5.0 10 15	– – –	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\overline{Reset}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0 10 15	– – –	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	– – –	1000 300 250	– – –	ns
Retrigger Time	t_{rr}	15	5.0	5.0 10 15	0 0 0	– – –	– – –	ns
		1000	10	5.0 10 15	0 0 0	– – –	– – –	ns
External Timing Resistance	R_X	–	–	–	5.0	–	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits (Note 7)			μF

4. The formulas given are for the typical characteristics only at 25°C.
5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
6. If C_X > 15 μF, Use Discharge Protection Diode D_X, per Figure 9.
7. $R_X$is in Ω, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

ORDERING INFORMATION

Device	Package	Shipping†
MC14528BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14528BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14528BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

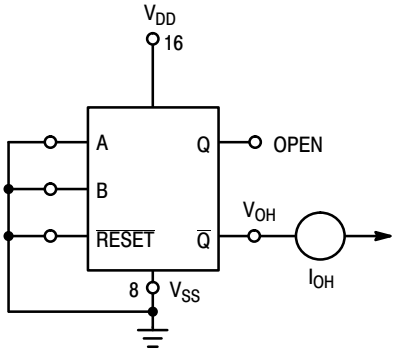


Figure 1. Output Source Current Test Circuit

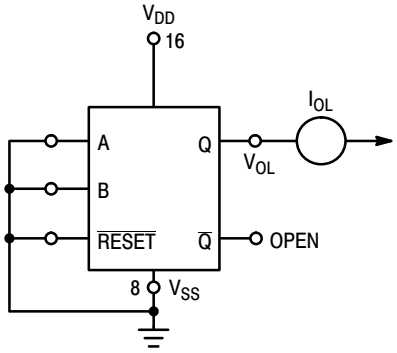
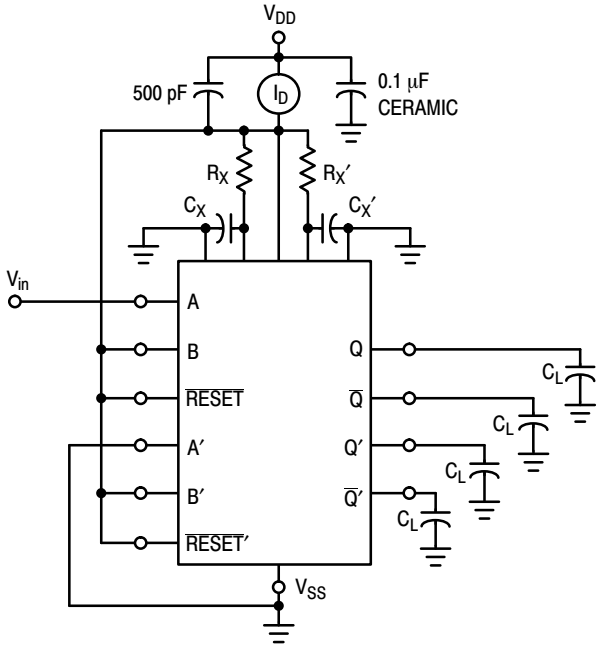


Figure 2. Output Sink Current Test Circuit



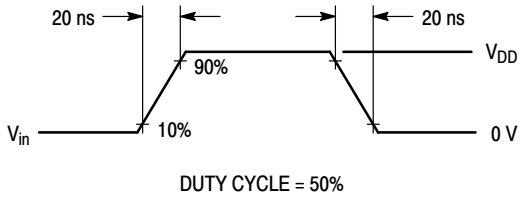
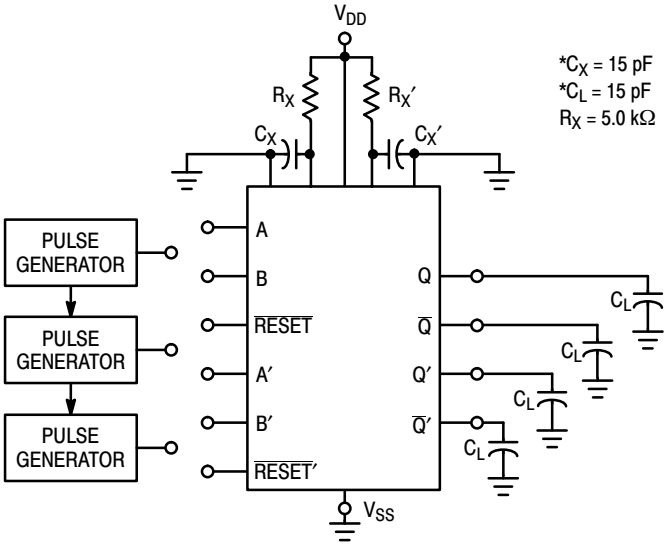


Figure 3. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

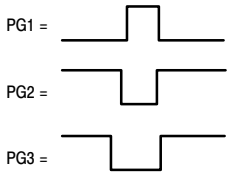


Figure 4. AC Test Circuit

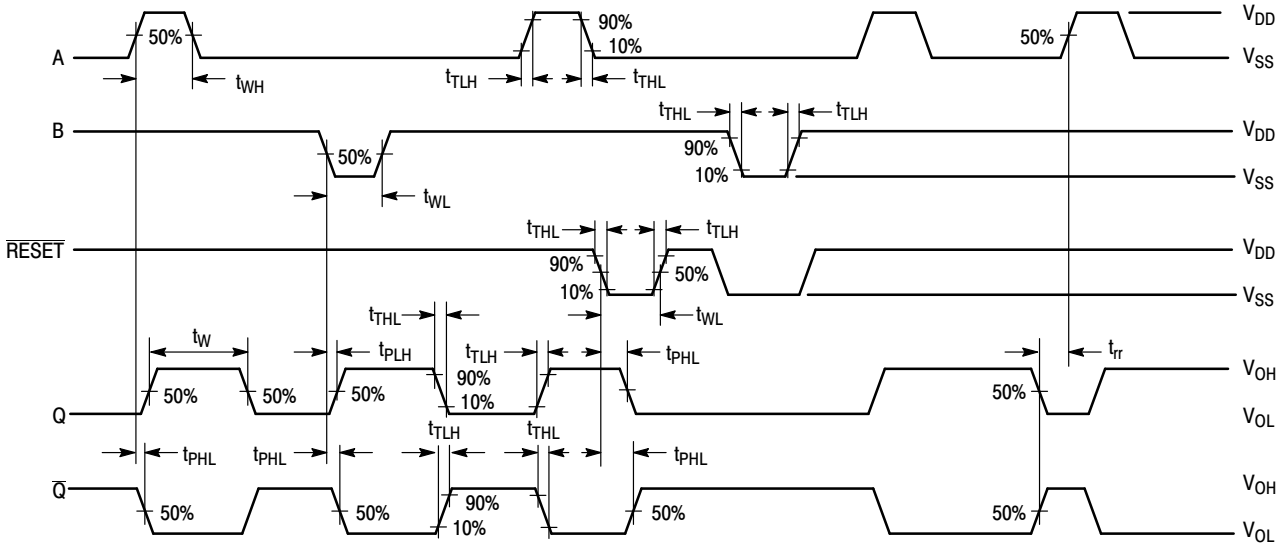


Figure 5. AC Test Waveforms

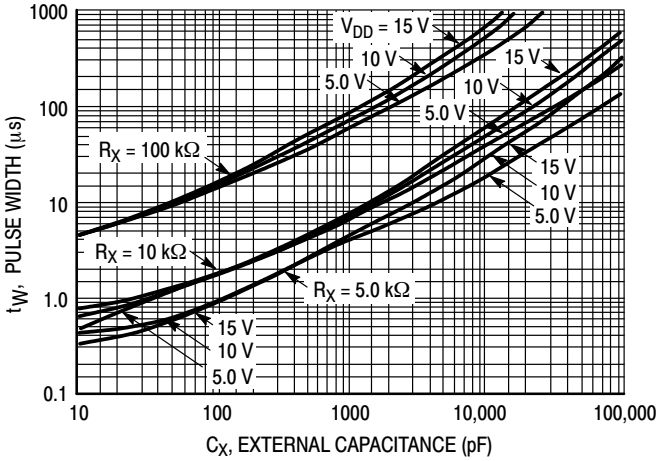


Figure 6. Pulse Width versus C_X

TYPICAL APPLICATIONS

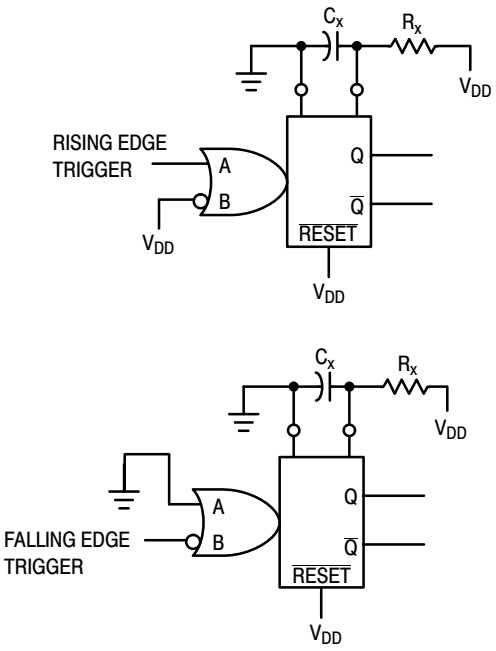


Figure 7. Retriggerable Monostables Circuitry

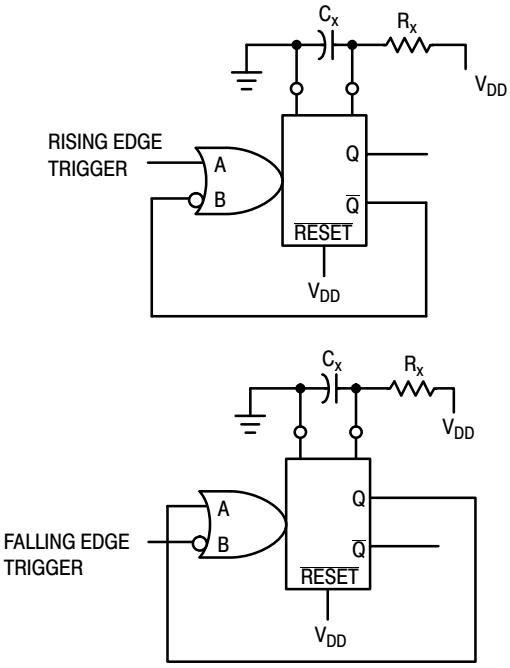


Figure 8. Non−Retriggerable Monostables Circuitry

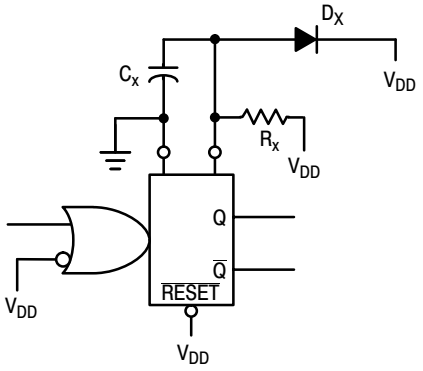


Figure 9. Use of a Diode to Limit Power Down Current Surge

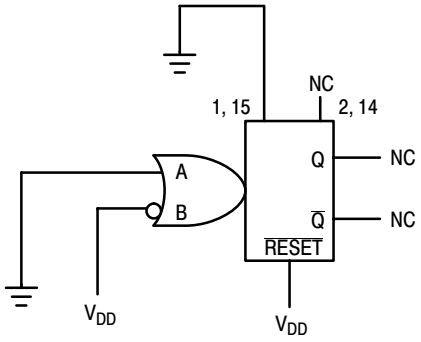
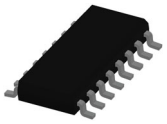


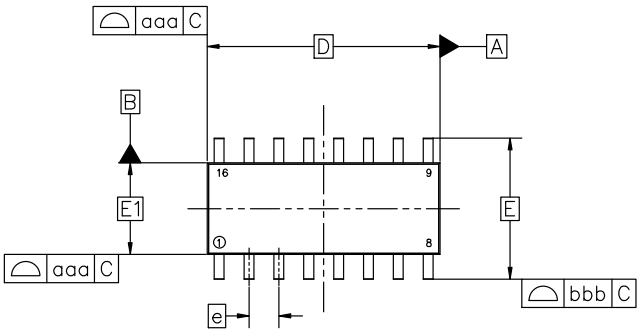
Figure 10. Connection of Unused Sections



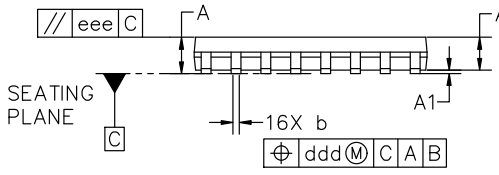
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

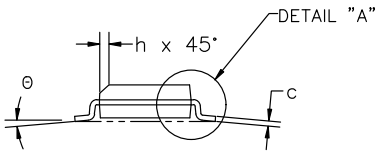
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

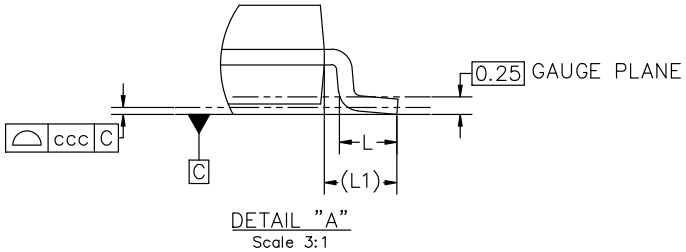


SIDE VIEW

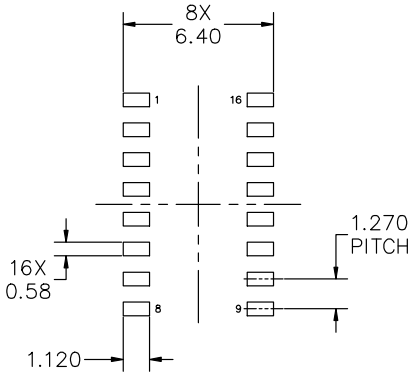


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

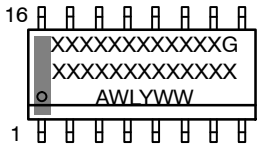
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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