# SY75602A/02B/603A/03B/604A/04B

## 2/4 Outputs Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 Clock Buffer

### Features

- Two (SY75602A/02B/603A/03B) and Four (SY75604A/04B) PCIe 1.0, 2.0, 3.0, 4.0, 5.0, and 6.0 Compliant Outputs.
- Ultra-Low Additive Jitter 10 fs (PCIe Gen5) and 6 fs (PCIe Gen6)
- Supports Frequencies of up to 250 MHz
- Transparent for Spread Spectrum
- Supports 1.8V ±10%, 2.5V ±10%, and 3.3V ±10% Power Supplies
- Outputs Low Power HCSL with Embedded 85Ω (SY75602A/03A/04A) and 100Ω (SY75602B/03B/04B) Termination Resistors
- Individual Glitch Free Output Enable (OExb) Control Pins on SY75603/604
- Accepts DC-Coupled HCSL Input Signal and AC-Coupled PECL, LVDS, and CML
- Extended Temperature Range: –40°C to +105°C
- 1.4 mm x 1.6 mm VDFN (SY75602A/02B) and 3 mm x 3 mm VQFN (SY75603A/03B/604A/04B) Package

### Applications

- PCIe Graphics Cards
- PCIe Based SSD drives
- Laptops and Desktop Computers
- Servers

### General Description

The SY75602A/02B/03A/03B/04A/04B are industry leading PCIe clock buffers with ultra-low additive jitter:

- 6 fs (PCIe 6.0)
- 10 fs (PCIe 5.0)
- 20 fs (PCIe 3.0/4.0)
- 52 fs in 12 kHz to 20 MHz band

They can be used in all PCIe 1/2/3/4/5/6 common clock and SRIS applications.

SY75602A/02B are the industry's smallest (1.4 mm x 1.6 mm VDFN) two output PCIe clock buffers.

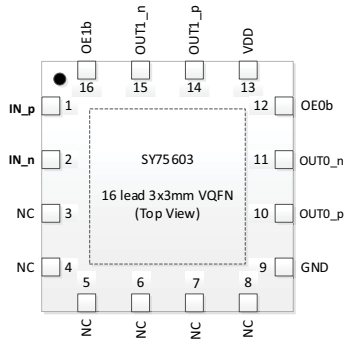
SY75603A/03B and SY75604A/04B are two and four output PCIe clock buffers with glitch free per-output enable/disable control hardware pins. Both devices are packaged in 3 mm x 3 mm VQFN.

The devices have embedded low-dropout regulators (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with tolerance of ±10% which exceeds ±9% required by PCIe Card Electro Mechanical Specification.

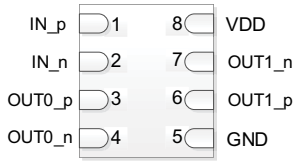
All six parts have extended temperature range: –40°C to +105°C.

### Package Types

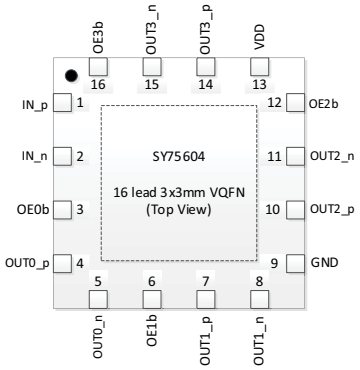
**SY75603**
16-Lead 3 mm x 3 mm VQFN
Top View



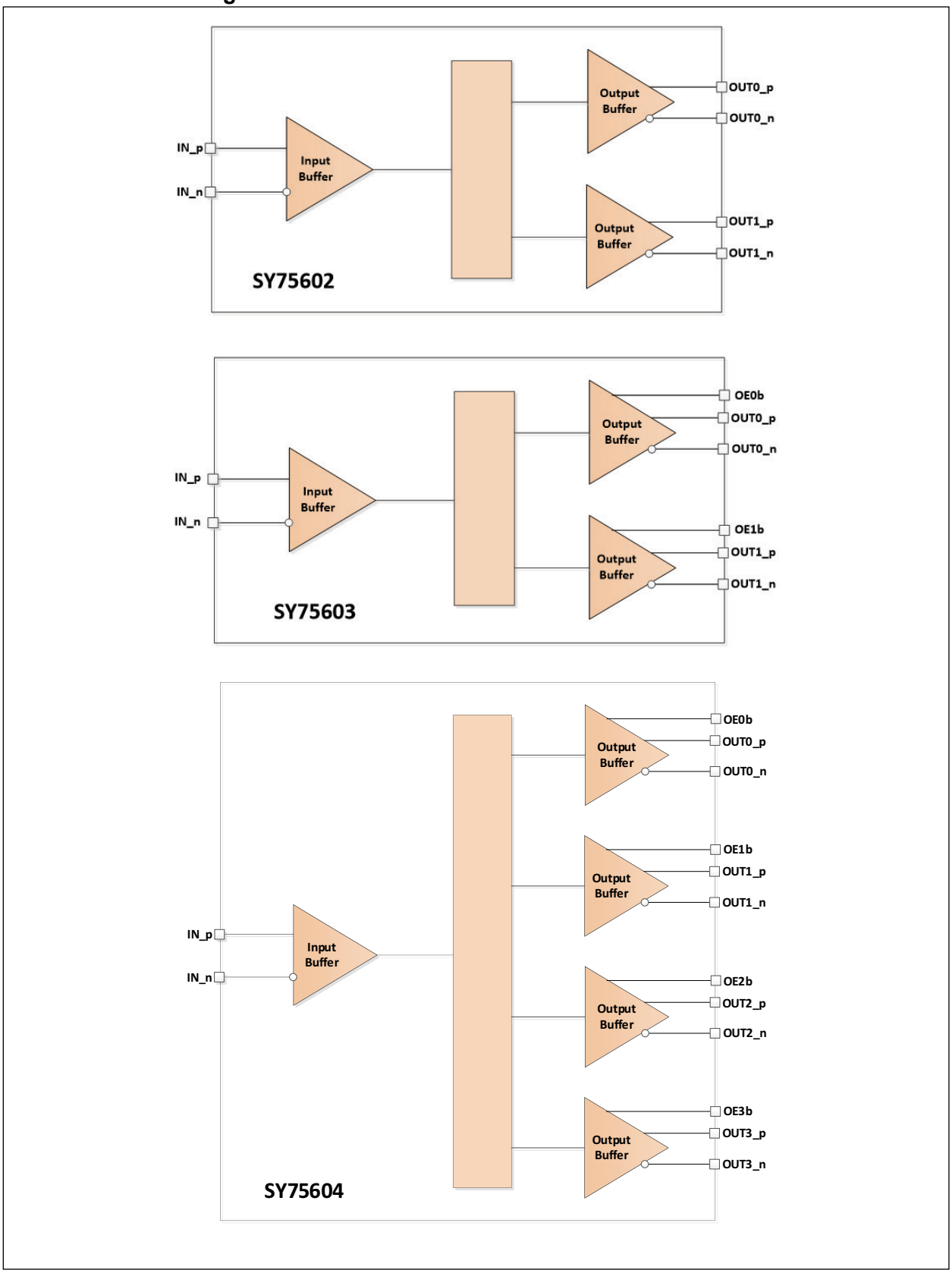

**SY75602**
8-Lead 1.4 mm x 1.6 mm VDFN
Top View




**SY75604**
16-Lead 3 mm x 3 mm VQFN
Top View



## Functional Block Diagrams



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ($V_{DD}$).....–0.5V to +4.6V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{DD}$ +0.5V
Input ESD Protection (HBM)..... 2 kV

### Operating Ratings ‡

1.8V Operating Voltage ($V_{DD}$).....+1.62V to +1.98V
2.5V Operating Voltage ($V_{DD}$).....+2.25V to +2.75V
3.3V Operating Voltage ($V_{DD}$).....+2.97V to +3.63V

**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions may affect device reliability.

**‡ Notice:** The data sheet limits are not ensured if the device is operated beyond the recommended operating conditions.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 3.3V ±10%, 2.5V±10%; 1.8V±10%; $T_A$ = –40°C to +105°C, unless noted.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | |
| Core Device Current | $I_{DD}$ | — | 9 | 13 | mA | SY75602, Output current excluded (no load) |
| | | — | 9 | 13 | | SY75603/04, all outputs disabled |
| Current dissipation per each LP-HCSL output (100Ω) | $I_{OUT\_HCSL\_100\Omega}$ | — | 3.5 | 3.9 | mA | Note 1 |
| Current dissipation per each LP-HCSL output (85Ω) | $I_{OUT\_HCSL\_85\Omega}$ | — | 4.0 | 4.4 | mA | Note 1 |
| **Power Supply Noise Rejection Ratio Characteristics** | | | | | | |
| Power Supply Noise Rejection Ratio | $PSNRR_{HSCL}$ | — | 70 | — | dB | 100 $mV_{PP}$, 100 kHz noise injected to $V_{DD}$. Clock Frequency 100 MHz, $V_{DD}$ = 3.3V |
| **Input Characteristics** | | | | | | |
| Input Slew Rate | $SR_{IN}$ | 0.6 | — | — | V/ns | — |
| Differential Input High Voltage | $V_{IH}$ | 0.15 | — | — | V | — |
| Differential Input Low Voltage | $V_{IL}$ | — | — | –0.15 | V | — |
| Input Voltage Swing | $V_{SWING}$ | 0.15 | — | — | $V_{DIFF}$ | — |
| Absolute Crossing Point Voltage | $V_{CROSS}$ | 0.25 | — | 0.55 | V | — |
| Variation of $V_{CROSS}$ Over All Edges | $V_{CROSS\_DELTA}$ | — | — | 0.14 | V | — |
| Voltage High for Output Enable | $V_{IH\_OE}$ | 0.7* $V_{DD}$ | — | — | V | SY75603/4 only |
| Voltage Low for Output Enable | $V_{IL\_OE}$ | — | — | 0.3* $V_{DD}$ | V | SY75603/4 only |
| Input Leakage Current | $I_{IL\_IN}$ | –5 | — | 5 | µA | $V_{IN}$ = $V_{IN(MAX)}$, $V_{IN}$ = GND |
| Input Capacitance | $C_{IN}$ | — | — | 5 | pF | — |

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 3.3V ±10%, 2.5V±10%; 1.8V±10%; $T_A$ = –40°C to +105°C, unless noted.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Leakage Current for OExb Inputs (Includes Current due to Pull-Down Resistors) | $I_{IL\_OE}$ | –5 | — | 50 | µA | $V_{IN} = V_{DD}$, $V_{IN}$ = GND SY75603/4 only |
| Single Ended Input Common Mode Voltage (IN_p) (HCSL Common Mode) | $V_{SIC}$ | 0.25 | — | 0.55 | V | — |
| Single Ended Input Voltage Swing for IN_p | $V_{SID}$ | 0.3 | — | 1.45 | V | — |
| Maximum Input Voltage | $V_{IN(MAX)}$ | — | — | 1.15 | V | — |
| Minimum Input Voltage | $V_{IN(MIN)}$ | –0.3 | — | — | V | — |
| Input Frequency (Differential) | $f_{IN}$ | 0 | — | 250 | MHz | — |
| Input Frequency (Single Ended) | $f_{IN\_SE}$ | 0 | — | 250 | MHz | — |
| Input Duty Cycle (250 MHz Input Clock) | DC | 35 | — | 65 | % | Note 3 |

**Note 1:** Tested with 100 MHz clock with outputs driving 5” long trace terminated with 2 pF capacitors to ground.

**2:** Output Enable control pins are synchronous with the input clock and it takes four rising edges before outputs get enabled and five rising edges before outputs get disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

**3:** Minimum and maximum duty cycles should be scaled for different input frequencies. For example, a 10 MHz input clock would have the minimum duty cycle of 1.5% and the maximum duty cycle of 98.5%.

## OUTPUT ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 3.3V ±10%, 2.5V±10%; 1.8V±10%; $T_A$ = –40°C to +105°C, $C_{LOAD}$ = 2 pF unless noted.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Rising Edge Rate | — | 1 | 2.5 | 4 | V/ns | Note 2, Note 3 |
| Falling Edge Rate | — | 1 | 2.5 | 4 | V/ns | Note 2, Note 3 |
| Differential Output High Voltage | $V_{OH}$ | 0.6 | — | 0.9 | V | Note 2 |
| Differential Output Low Voltage | $V_{OL}$ | –0.9 | — | –0.6 | V | Note 2 |
| Absolute Crossing Voltage | $V_{CROSS}$ | 0.25 | — | 0.55 | V | Note 1, Note 4, Note 5 |
| Variation of $V_{CROSS}$ Over All Rising Clock Edges | $V_{CROSS\_DELTA}$ | — | — | 0.14 | V | Note 1, Note 4, Note 8 |
| Ring Back Voltage Margin | $V_{RB}$ | –0.1 | — | 0.1 | V | Note 2, Note 10 |
| Time Before $V_{RB}$ is Allowed | $t_{STABLE}$ | 500 | — | — | ps | Note 2, Note 10 |
| Cycle-to-Cycle Additive Jitter | $t_{CCJITTER}$ | — | 6.5 | 8.1 | ps | Note 2 |
| Absolute Maximum Output Voltage | $V_{MAX}$ | — | — | 1.15 | V | Note 1, Note 6 |
| Absolute Minimum Output Voltage | $V_{MIN}$ | –0.3 | — | — | V | Note 1, Note 7 |
| Output Duty Cycle | $V_{DC}$ | 48 | 50 | 52 | % | When input has 50% duty cycle and $V_{IN} \geq$ 200 mV, Note 2 |
| Rising to Falling Edge Matching | Rise-Fall Matching | — | — | 20 | % | Note 1, Note 11 |

## OUTPUT ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** $V_{DD}$ = 3.3V ±10%, 2.5V±10%; 1.8V±10%; $T_A$ = –40°C to +105°C, $C_{LOAD}$ = 2 pF unless noted.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Clock Source DC Impedance (OUTx_p) for part with 85Ω embedded differential series resistance (parts with suffix “A”) | $Z_{C\text{-}DC\_OUT\_p}$ | 34 | — | 51 | Ω | Note 1, Note 9 |
| Clock Source DC Impedance (OUTx_n) for part with 85Ω embedded differential series resistance (parts with suffix “A”) | $Z_{C\text{-}DC\_OUT\_n}$ | 34 | — | 51 | Ω | Note 1, Note 9 |
| Clock Source DC Impedance (OUTx_p) for part with 100Ω embedded differential series resistance (parts with suffix “B”) | $Z_{C\text{-}DC\_OUT\_p}$ | 40 | — | 60 | Ω | Note 1, Note 9 |
| Clock Source DC Impedance (OUTx_n) for part with 100Ω embedded differential series resistance (parts with suffix “B”) | $Z_{C\text{-}DC\_OUT\_n}$ | 40 | — | 60 | Ω | Note 1, Note 9 |
| Output Frequency | $F_{MAX}$ | 0 | — | 250 | MHz | — |
| Output to Output Skew | $t_{OOSK}$ | — | — | 30 | ps | — |
| Device to Device Output Skew | $t_{POOSK}$ | — | — | 50 | ps | — |
| Input to Output Delay | $t_{IOD}$ | 0.9 | 1.2 | 1.5 | ns | — |
| Output Enable Time | $t_{EN}$ | — | — | 3.5 | cycles | Note 12 |
| Output Disable Time | $t_{DIS}$ | — | — | 4.5 | cycles | Note 12 |

**Note 1:** Measurement taken from single ended waveform.

**2:** Measurement taken from differential waveform.

**3:** Measured from –150 mV to +150 mV on the differential waveform (derived from OUTx_p to OUTx_n). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 1-5.

**4:** Measured at crossing point where the instantaneous voltage value of the rising edge of OUTx_p equals the falling edge of OUTx_n. See Figure 1-1.

**5:** Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 1-1.

**6:** Defined as the maximum instantaneous voltage including overshoot. See Figure 1-1.

**7:** Defined as the minimum instantaneous voltage including undershoot. See Figure 1-1.

**8:** Defined as the total variation of all crossing voltages of Rising OUTx_p and Falling OUTx_n. This is the maximum allowed variance in $V_{CROSS}$ for any particular system. See Figure 1-2.

**9:** System board compliance measurements must use the test load card described in Figure 1-7. OUTx_p and OUTx_n are to be measured at the load capacitors $C_{LOAD}$. Single-ended probes must be used for measurements requiring single-ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements.

**10:** $t_{STABLE}$ is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the $V_{RB}$ ±100 mV differential range. See Figure 1-6.

**11:** Matching applies to rising edge rate for OUTx_p and falling edge rate for OUTx_n. It is measured using a ±75 mV window centered on the median cross point where OUTx_p rising meets OUTx_n falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of OUTx_p should be compared to the Fall Edge Rate of OUTx_n; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 1-3.

**12:** Output Enable control pins are synchronous with the input clock and it takes four rising edges before outputs get enabled and five rising edges before outputs get disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

## JITTER AND PHASE NOISE

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Peak-to-Peak Additive Jitter | p-p $A_{JRMS}$ | — | — | 4.5 | ps | Note 1, Note 2 |
| Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz) | $t_{jPCIe\_1.0}$ | — | 0.7 | 0.8 | $ps_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz) | $t_{jPCIe\_2.0\_high}$ | — | 70 | 90 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz) | $t_{jPCIe\_2.0\_low}$ | — | 14 | 20 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz) | $t_{jPCIe\_2.0\_mid}$ | — | 55 | 74 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5 MHz, CDR = 10 MHz) | $t_{jPCIe\_3.0}$ | — | 18 | 22 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5 MHz, CDR = 10 MHz) | $t_{jPCIe\_4.0}$ | — | 18 | 22 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8 MHz, CDR for 32 GT/s CC) | $t_{jPCIe\_5.0}$ | — | 7 | 10 | $fs_{RMS}$ | Note 2, Note 3 |
| Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 to 1 MHz, CDR for 64 GT/s CC) | $t_{jPCIe\_6.0}$ | — | 4.5 | 6 | $fs_{RMS}$ | Note 2, Note 3 |
| Additive jitter as per Intel QPI 9.6 Gbps | $t_{jQPI}$ | — | 35 | 45 | $fs_{RMS}$ | Note 1, Note 2 |
| Additive RMS jitter in 1 MHz to 20 MHz band | $t_{j\_1M\_20M}$ | — | 51 | 66 | $fs_{RMS}$ | Note 1, Note 2 (100 MHz clock) |
| | | — | 40 | 54 | $fs_{RMS}$ | Note 1, Note 2 (133 MHz clock) |
| Additive RMS jitter in 12 kHz to 20 MHz band | tj_12k_20M | — | 52 | 68 | $fs_{RMS}$ | Note 1, Note 2 (100 MHz clock) |
| | | — | 44 | 58 | $fs_{RMS}$ | Note 1, Note 2 (133 MHz clock) |
| Noise Floor | NF | — | –165 | –163 | dBc/Hz | Note 1, Note 2 (100 MHz clock) |
| | | — | –165 | –163 | dBc/Hz | Note 1, Note 2 (133 MHz clock) |

**Note 1:** Measured into AC test load as per Figure 1-7.

**2:** Measured from differential crossing point to differential crossing point.

**3:** Measured with 50Ω termination in instrument without a test load.

## TEMPERATURE SPECIFICATIONS

| Parameters | Symbol | Min. | Typ. | | Max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | | |
| Ambient Operating Temperature Range | $T_A$ | –40 | — | | +105 | °C | — |
| Storage Temperature Range | $T_S$ | –65 | — | | +150 | °C | — |
| **Package Thermal Resistances** | | | **VDFN 8-Ld** | **VQFN 16-Ld** | | | |
| Junction-to-Ambient Thermal Resistance | $\theta_{JA}$ | — | 138 | 35.7 | — | °C/W | Still air |
| | | — | 132 | 30.8 | — | | 1m/s airflow |
| | | — | 127 | 28.6 | — | | 2.5m/s airflow |
| Junction-to-Board Thermal Resistance | $\theta_{JB}$ | — | 104 | 5 | — | °C/W | — |
| Junction-to-Case Thermal Resistance | $\theta_{JC}$ | — | 105 | 49.5 | — | °C/W | — |
| Thermal Characterization, Junction-to-Top of Package | $\Psi_{JT}$ | — | 11.5 | 3 | — | °C/W | Still air |

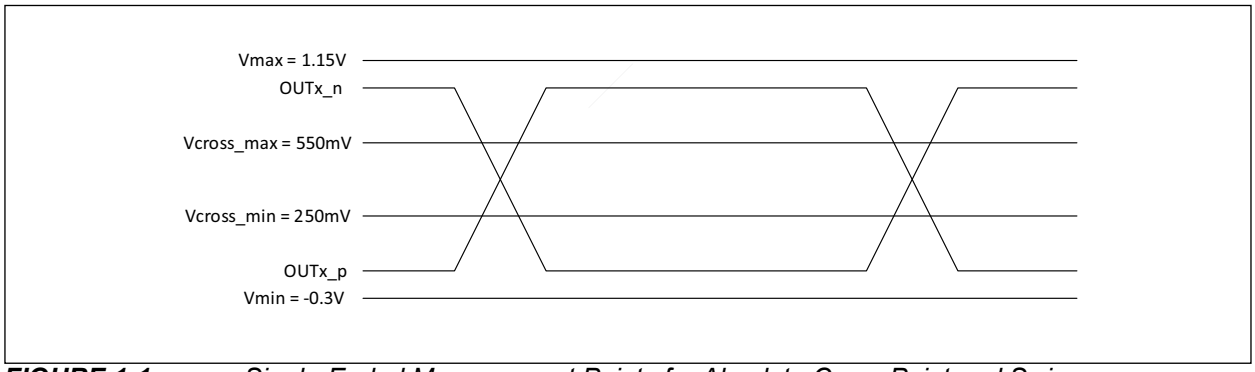



***FIGURE 1-1:*** *Single-Ended Measurement Points for Absolute Cross Point and Swing.*

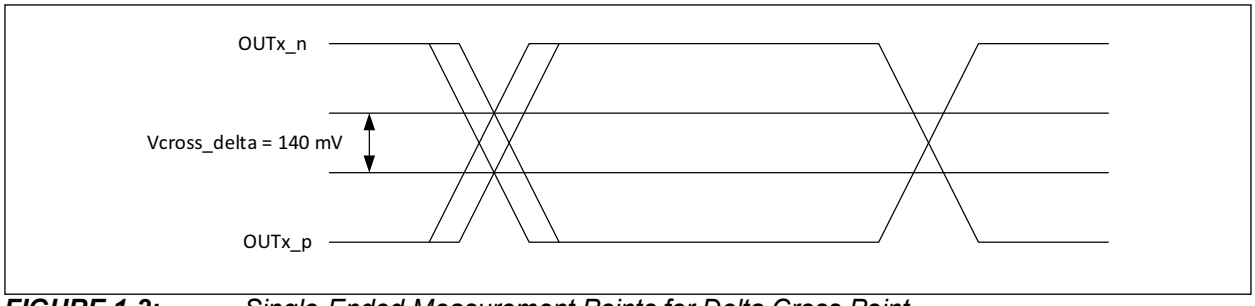



***FIGURE 1-2:*** *Single-Ended Measurement Points for Delta Cross Point.*

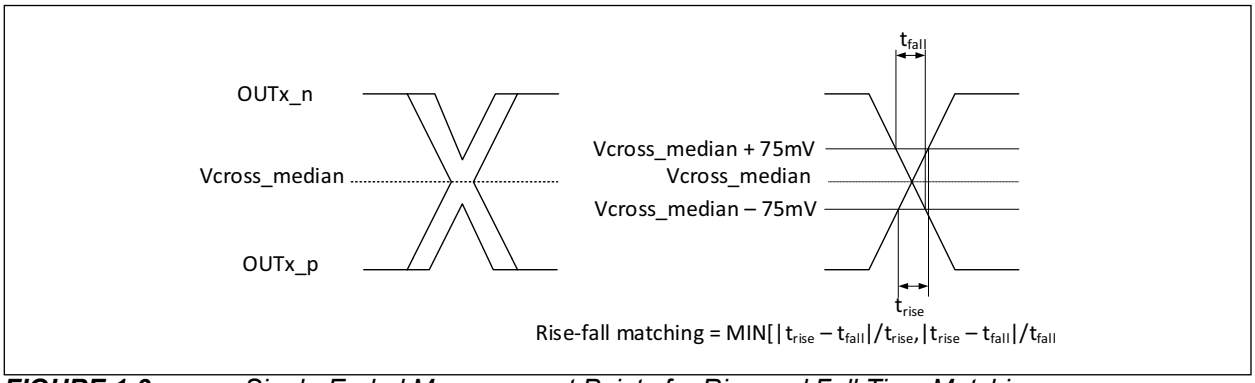



***FIGURE 1-3:*** *Single-Ended Measurement Points for Rise and Fall Time Matching.*

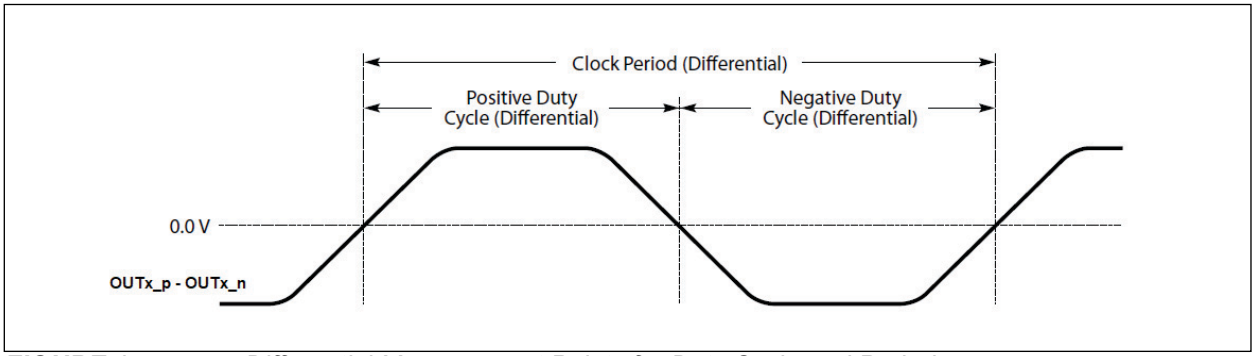



***FIGURE 1-4:*** *Differential Measurement Points for Duty Cycle and Period.*

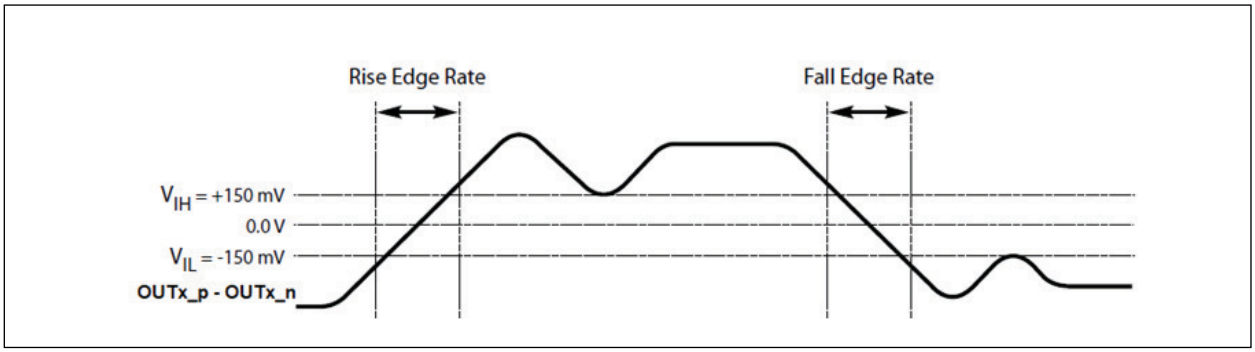



***FIGURE 1-5:*** *Differential Measurement Points for Rise and Fall Time.*

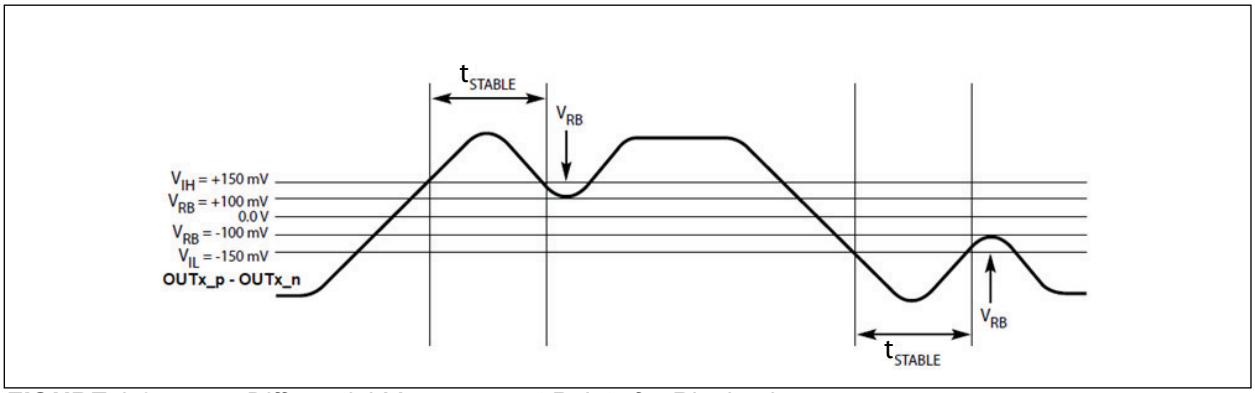



***FIGURE 1-6:*** *Differential Measurement Points for Ringback.*

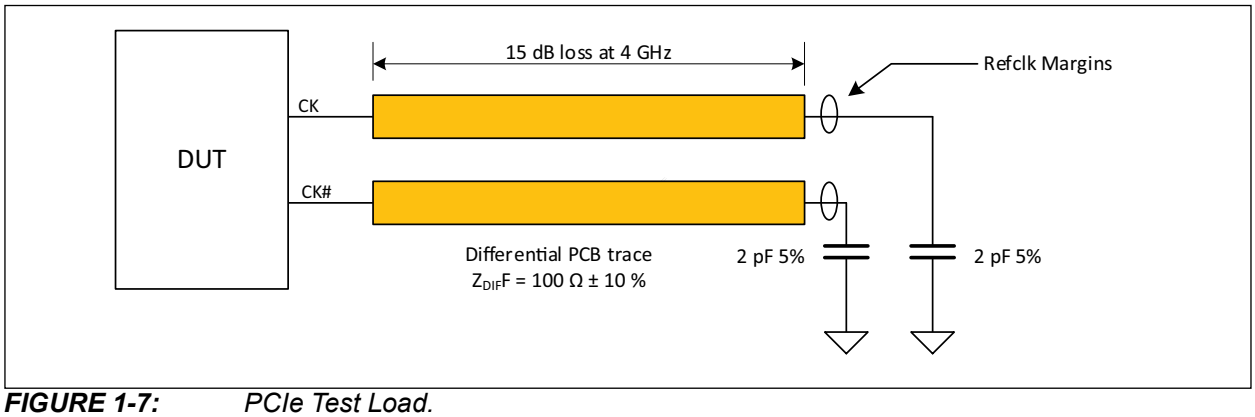



***FIGURE 1-7:*** *PCIe Test Load.*

## 2.0 TYPICAL OPERATING CHARACTERISTICS

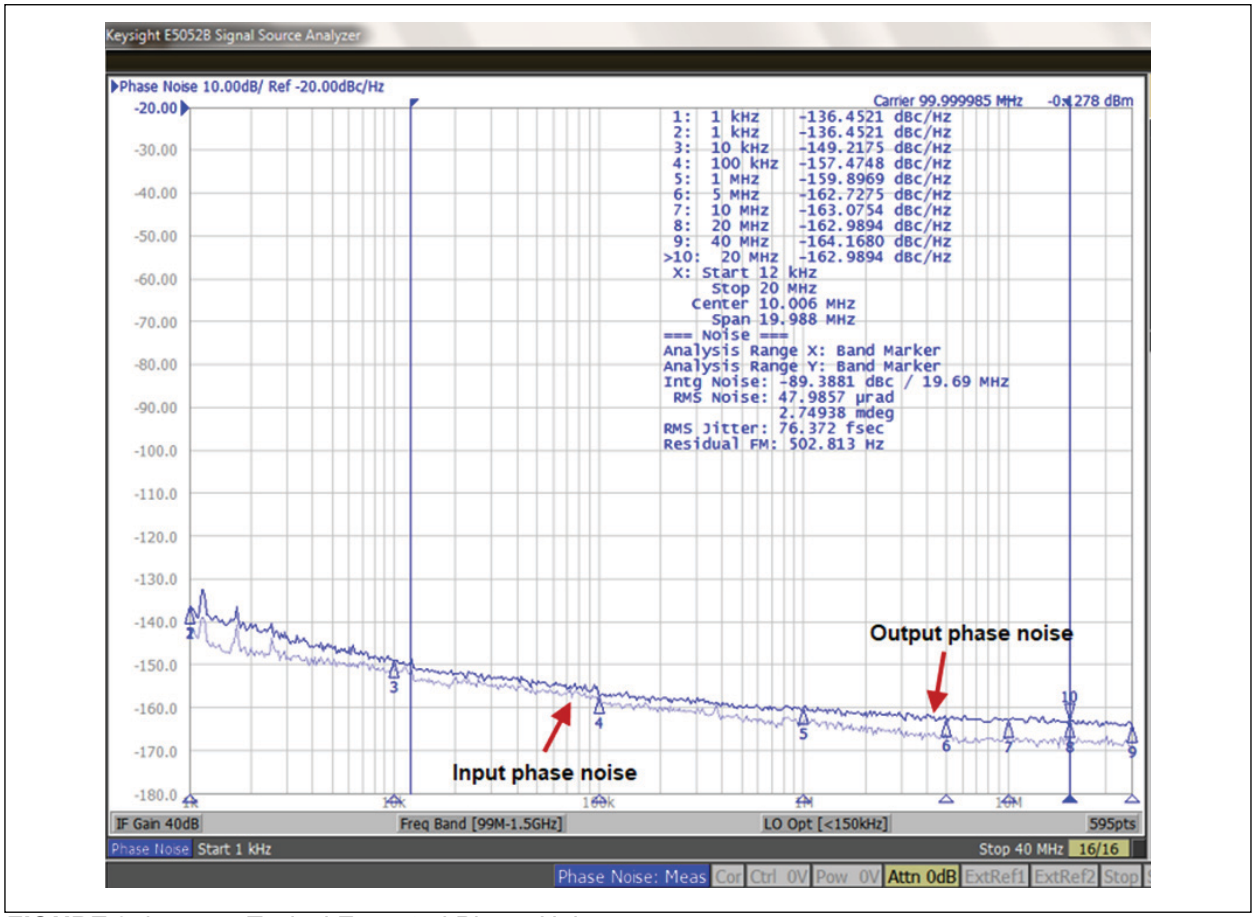



***FIGURE 2-1:*** *Typical Expected Phase Noise.*

## 3.0 PIN DESCRIPTIONS

All device inputs and outputs are LP-HCSL unless described otherwise. The Type column uses the following symbols:

- I: Input
- IPD: Input with 100 kΩ internal pull-down resistor
- O: Output
- P: Power supply

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

**TABLE 3-1: SY75602A/02B PIN FUNCTION TABLE**

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| **Input Reference** | | | |
| 1 | IN_p | I | **Differential/Single Ended Input Reference**<br><br>Input frequency range >0 Hz to 250 MHz.<br><br>**Note 1:** >0 Hz means frequency higher than DC. On the power up, the device needs four clock cycles before the outputs get enabled. This feature filters any initial glitch or runt pulse from the clock source.<br><br>**Note 2:** The differential input has hysteresis of 30 mV that prevents outputs from randomly toggling when both p and n inputs are at the same voltage level. For example, when p and n inputs are held low as in the case when the buffer is driven from an HCSL driver that is disabled. |
| 2 | IN_n | | |
| **Output Clocks** | | | |
| 3 | OUT0_p | O | **Ultra-Low Additive Jitter Differential Outputs 0 and 1**<br><br>Output frequency range >0 Hz to 250 MHz. |
| 4 | OUT0_n | | |
| 6 | OUT1_p | | |
| 7 | OUT1_n | | |
| **Power and Ground** | | | |
| 8 | VDD | P | **Positive Supply Voltage:** Connect to either 3.3V, 2.5V, or 1.8V supply. |
| 5 | GND | P | **Ground:** Connect to ground. |

**TABLE 3-2: SY75604A/04B AND SY75603A/03B PIN FUNCTION TABLE**

| Pin Number | Pin Name SY75604A/04B | Pin Name SY75603A/03B | Type | Description |
|---|---|---|---|---|
| **Input Reference** | | | | |
| 1 | IN_p | IN_p | I | **Differential/Single Ended Input Reference**<br><br>Input frequency range >0 Hz to 250 MHz<br><br>**Note 1:** >0 Hz means frequency higher than DC. Output Enable control pins (OExb) need four clock cycles before the corresponding output get enabled/disable. This feature ensures glitch free transition of the outputs.<br><br>**Note 2:** The differential input has hysteresis of 30 mV that prevents outputs from randomly toggling when both p and n inputs are at the same voltage level. For example, when p and n inputs are held low as in the case when the buffer is driven from an HCSL driver that is disabled. |
| 2 | IN_n | IN_n | | |
| **Output Clocks** | | | | |
| 4 | OUT0_p | NC | O | **Ultra-Low Additive Jitter Differential Outputs 0 to 1 (SY75603A/03B) and 0 to 3 (SY75604A/04B)**<br><br>Output frequency range >0 Hz to 250 MHz<br><br>NC are no connect pins. They are not bonded to the die but they should be soldered to the board for mechanical reasons. |
| 5 | OUT0_n | NC | | |
| 7 | OUT1_p | NC | | |
| 8 | OUT1_n | NC | | |
| 10 | OUT2_p | OUT0_p | | |
| 11 | OUT2_n | OUT0_n | | |
| 14 | OUT3_p | OUT1_p | | |
| 15 | OUT3_n | OUT1_n | | |
| **Control Inputs** | | | | |
| 3 | OE0b | NC | IPD | **Output Enable Control**<br><br>When OExb is low the output x where x = {0,1} for SY75603A/03B and x = {0,1,2,3} for SY75604A/04B is active.<br><br>OExb is synchronous and it takes 3.5 clock cycles of the input clock to enable and 4.5 clock to disable the output.<br>OExb pins are pulled-down with 100 kΩ resistor<br><br>NC are no connect pins. They are not bonded to the die but they should be soldered to the board for mechanical reasons. |
| 6 | OE1b | NC | | |
| 12 | OE2b | OE0b | | |
| 16 | OE3b | OE1b | | |
| **Power and Ground** | | | | |
| 13 | VDD | VDD | P | **Positive Supply Voltage:** Connect to either 3.3V, 2.5V, or 1.8V supply. |
| 9<br>ePad | GND | GND | P | **Ground:** Connect to ground. |

## 4.0 FUNCTIONAL DESCRIPTION

The SY75602A/02B/603A/03B/604A/04B are PCIe clock buffers with ultra-low additive jitter. They can be used in all PCIe 1/2/3/4/5/6 common clock and SRIS applications.

SY75602A/02B are the industry's smallest (1.4 mm x 1.6 mm VDFN) two output PCIe clock buffers.

SY75603A/03B and SY75604A/04B are two and four output PCIe clock buffers with glitch free per-output enable/disable control hardware pins. Both devices are packaged in 3 mm x 3 mm VQFN.

The devices have embedded low-dropout regulators (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with tolerance of ±10% which exceeds ±9% required by PCIe Card Electro Mechanical Specification.

### 4.1 Clock Input

Please refer to the Functional Block Diagrams on how to terminate different signals fed to the input of the device.

Figure 4-1 and Figure 4-2 show how to terminate input of the device in most common cases: Low Power HCSL (LPHCSL), HCSL, and single-ended LVCMOS.

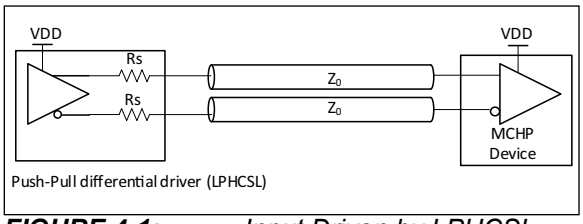



***FIGURE 4-1:*** *Input Driven by LPHCSL Driver.*

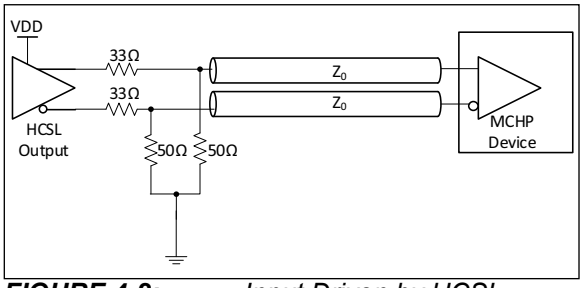



***FIGURE 4-2:*** *Input Driven by HCSL Driver.*

Figure 4-3 shows how to interface an LVDS driver to the SY75602/3/4 input for 3.3V. 2.5V, and 1.8V supply voltages.

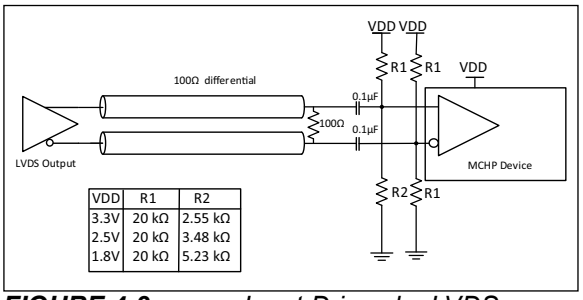



***FIGURE 4-3:*** *Input Driven by LVDS Driver.*

Figure 4-4 shows how to terminate a single-ended output, such as LVCMOS. This example assumes 50Ω transmission line which is the most common for single ended CMOS signaling. Ideally, resistors R1 and R2 should be 100Ω each and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor $R_S$ should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (0.3V). The source resistors of $R_S$ = 270Ω could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) * (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

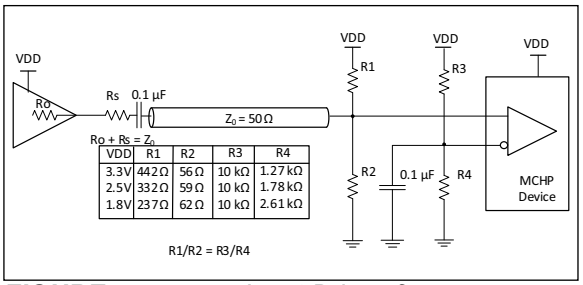



***FIGURE 4-4:*** *Input Driven from a Single-Ended CMOS Output.*

The differential input has hysteresis of 30 mV that prevents outputs from randomly toggling when both p and n inputs are at the same voltage level. For example, when p and n inputs are held low as in the case when the buffer is driven from an HCSL driver that is disabled.

## 4.2 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 4-5. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential output.

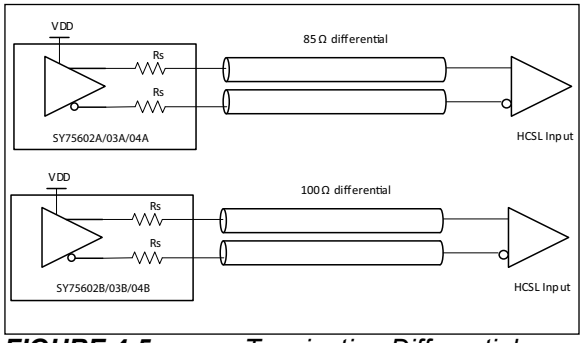
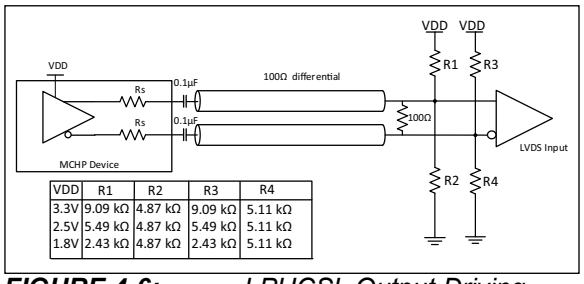



***FIGURE 4-5:*** *Terminating Differential Outputs.*

Embedded termination resistors in SY75602A/603A/604A are matched for 85Ω and embedded termination resistors in SY75602B/603B/604B are matched for 100Ω differential transmission line.

Figure 4-6 shows how to interface the SY75602/3/4 output with an LVDS input for 3.3V. 2.5V, and 1.8V supply voltages. The biasing resistors R1, R2, R3, and R4 are used to provide 1.2V common mode voltage for LVDS input and to add 20 mV to 30 mV hysteresis. The hysteresis prevents the LVDS driver from generating random transitions when its input is not driven. If the LVDS receiver has built in hysteresis, then R1 = R3 and R2 = R4.




| VDD | R1 | R2 | R3 | R4 |
|---|---|---|---|---|
| 3.3V | 9.09 kΩ | 4.87 kΩ | 9.09 kΩ | 5.11 kΩ |
| 2.5V | 5.49 kΩ | 4.87 kΩ | 5.49 kΩ | 5.11 kΩ |
| 1.8V | 2.43 kΩ | 4.87 kΩ | 2.43 kΩ | 5.11 kΩ |

***FIGURE 4-6:*** *LPHCSL Output Driving LVDS Input.*

## 4.3 Output Enable

Each output of SY75603A/03B/04A/04B has an active low Output Enable (OExb) control pin. Output Enable and Disable function is synchronous with the input clock which results in glitchless transitions as shown in Figure 4-7 and Figure 4-8. The OExb is sampled on the falling edge of the differential input (or falling edge of IN_p signal). It takes 3.5 clock cycles of the input clock to enable an output and 4.5 clock cycles to disable the output, after the change of OExb is sampled.

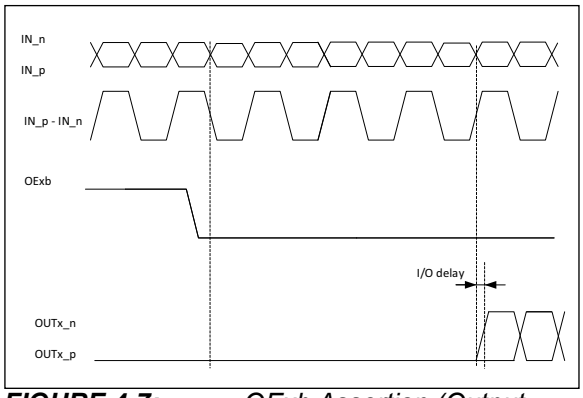



***FIGURE 4-7:*** *OExb Assertion (Output Enable) Timing Diagram.*

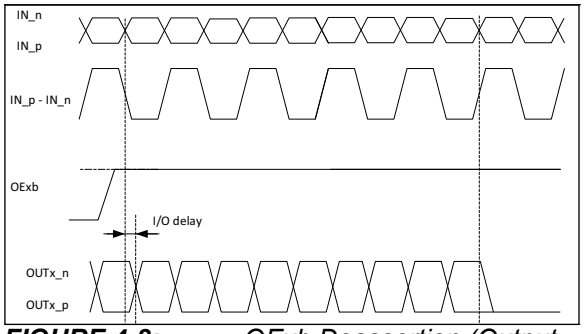
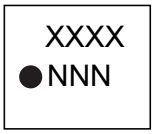



***FIGURE 4-8:*** *OExb Deassertion (Output Disable) Timing Diagram.*

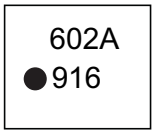
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

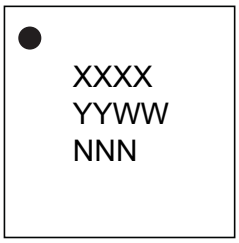
8-Lead VDFN*



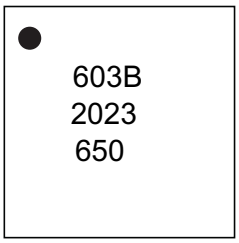

Example




16-Lead VQFN*




Example

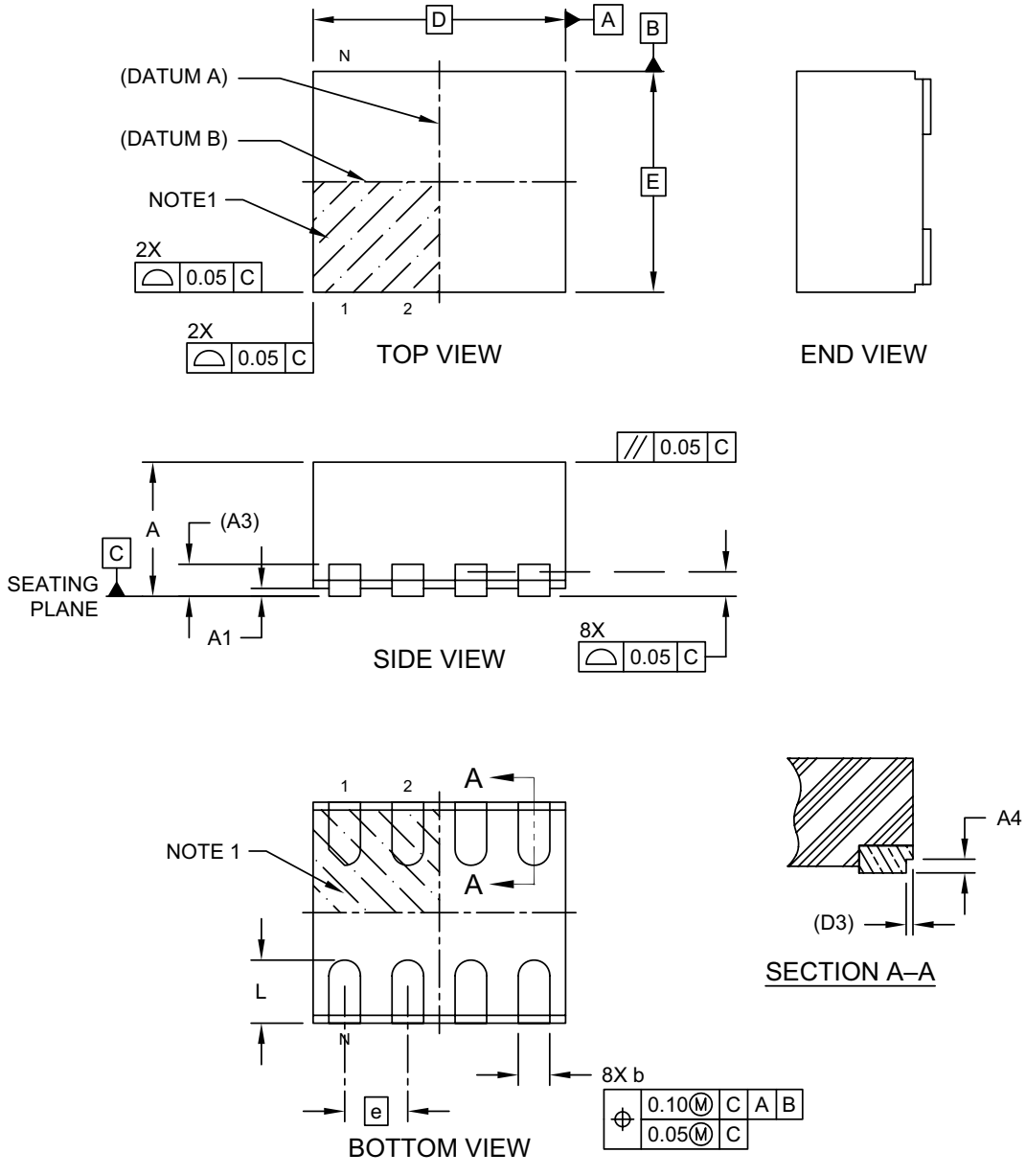



| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| **Note**: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar (_) and/or Overbar (¯) symbol may not be to scale. | |

## 8-Lead VDFN 1.6 mm x 1.4 mm Package Outline and Recommended Land Pattern

**8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN] With Stepped Wettable Flanks**

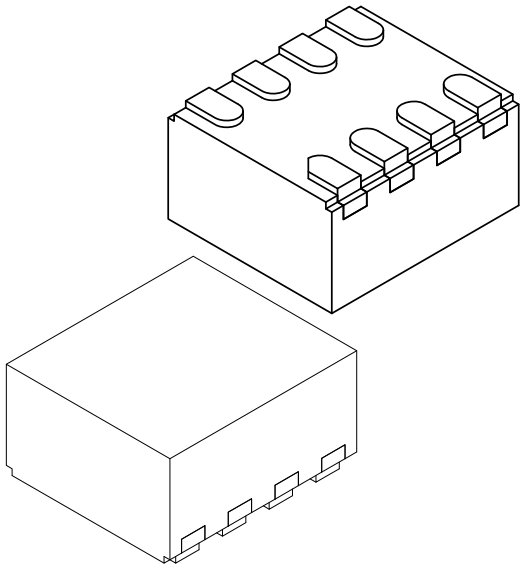
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-25509 Rev A Sheet 1 of 2

**8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN] With Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.40 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 1.60 BSC | |
| Overall Width | E | | 1.40 BSC | |
| Terminal Width | b | 0.15 | 0.20 | 0.25 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Wettable Flank Step Length | D3 | | 0.05 REF | |
| Wettable Flank Step Height | A4 | 0.10 | – | – |

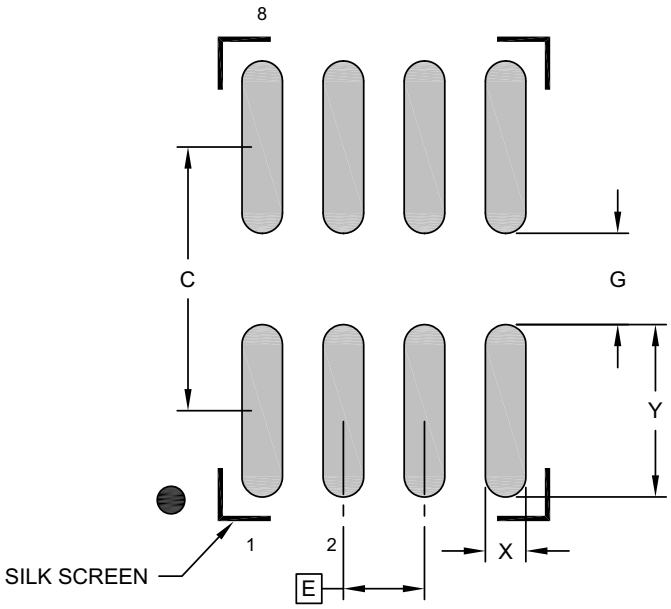
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25509 Rev A Sheet 2 of 2

**8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN]**
**With Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Contact Pad Spacing | C | | 1.30 | |
| Contact Pad Width (Xnn) | X | | | 0.20 |
| Contact Pad Length (Xnn) | Y | | | 0.85 |
| Contact Pad to Contact Pad (Xnn) | G | 0.45 | | |

Notes:

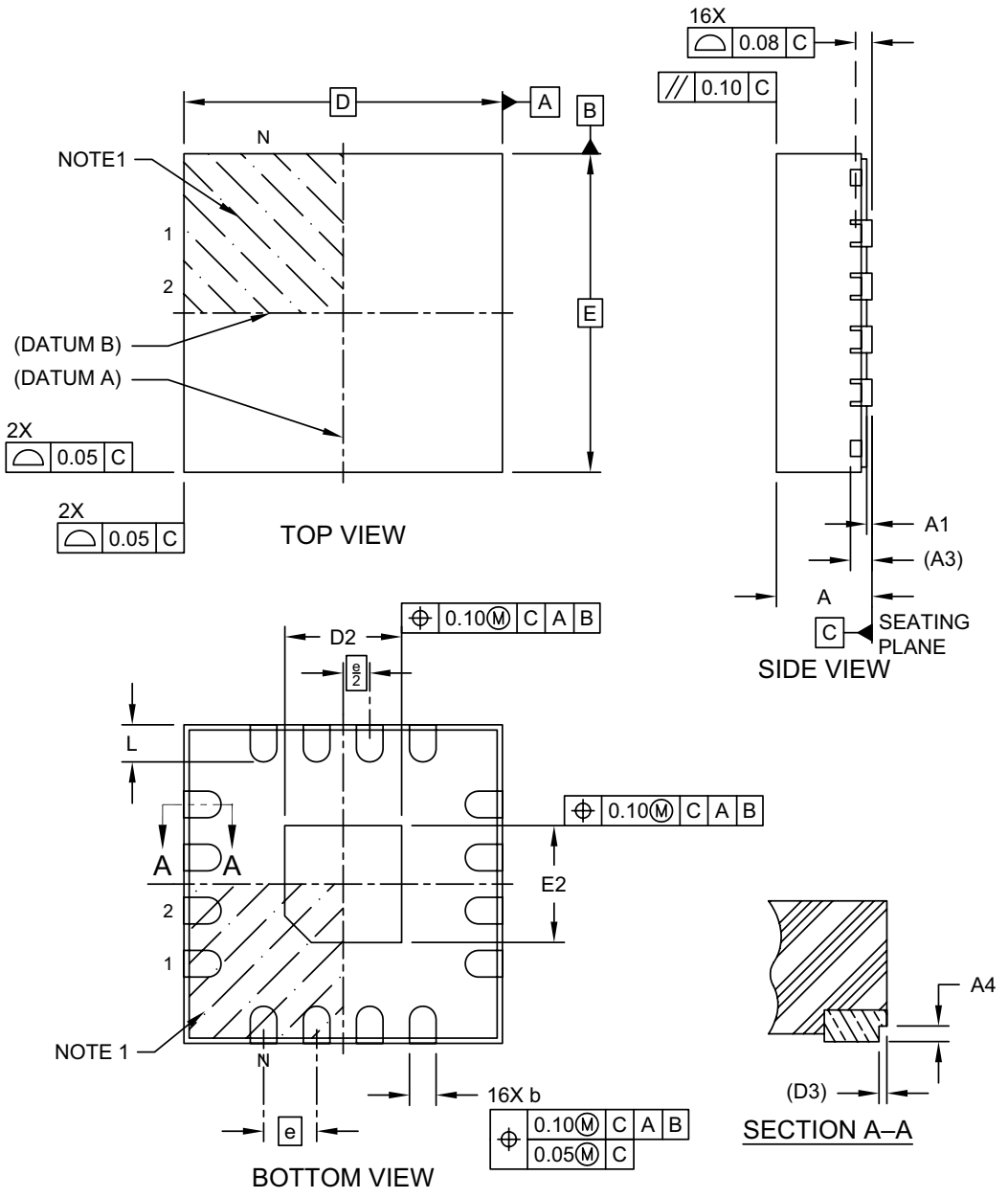
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27509 Rev A

## 16-Lead VQFN 3.0 mm x 3.0 mm Package Outline and Recommended Land Pattern

**16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]**
**With 1.10 mm Exposed Pad and Stepped Wettable Flanks**

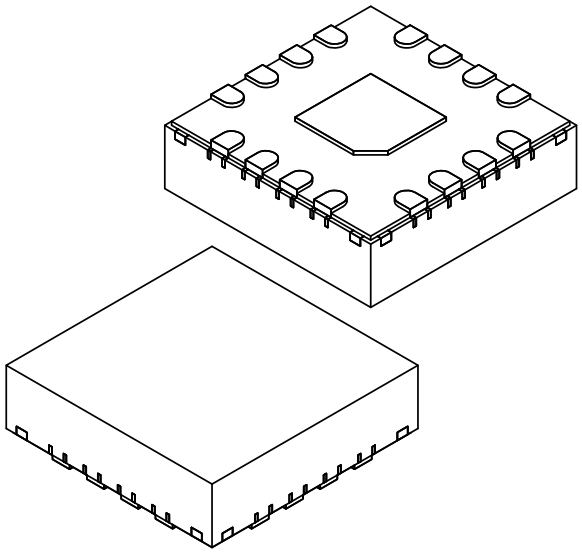
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-508 Rev A Sheet 1 of 2

**16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]**
**With 1.10 mm Exposed Pad and Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.20 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.20 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.35 | 0.45 |
| Wettable Flank Step Length | D3 | | 0.05 REF | |
| Wettable Flank Step Height | A4 | 0.10 | - | 0.19 |

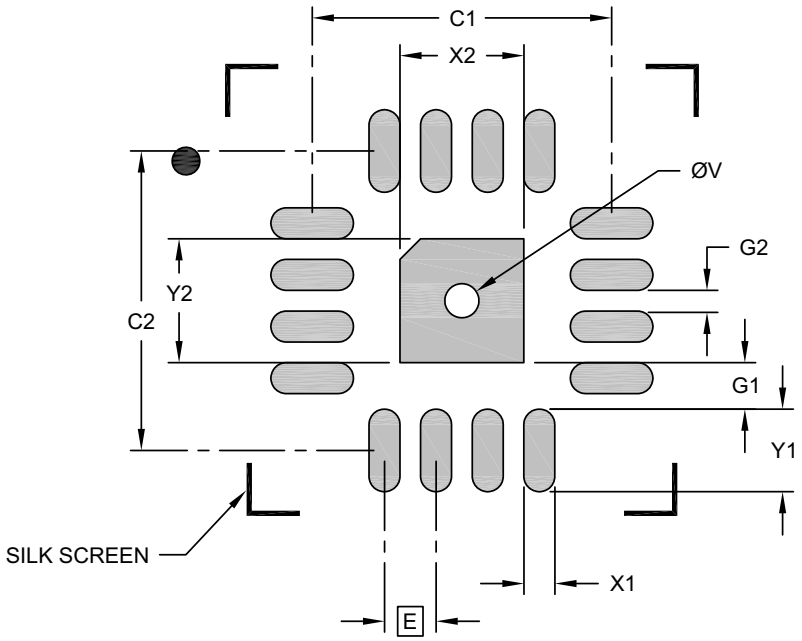
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-508 Rev A Sheet 2 of 2

**16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]**
**With 1.10 mm Exposed Pad and Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.20 |
| Optional Center Pad Length | Y2 | | | 1.20 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Spacing | C2 | | 2.90 | |
| Contact Pad Width (X16) | X1 | | | 0.30 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X16) | G1 | 0.45 | | |
| Contact Pad to Contact Pad (X12) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2508 Rev A

# APPENDIX A: REVISION HISTORY

## Revision A (September 2021)

- Initial release of SY75602A/02B/603A/03B/604A/04B as Microchip data sheet DS20006508A.

## Revision B (October 2021)

- Updated various values in the Electrical Characteristics, Output Electrical Characteristics, and Jitter and Phase Noise tables.
- Updated Note 12 in the Output Electrical Characteristics table.
- Updated Input Reference description in Table 3-1 and Table 3-2.
- Updated Control Inputs description in Table 3-2.
- Added paragraph immediately after Figure 4-4.

## Revision C (July 2022)

- Added information specific to the 85Ω devices to the Current Consumption section of the Electrical Characteristics table.

## Revision D (May 2023)

- Added PCIe Gen6 information to Features, General Description, and Jitter and Phase Noise.
- Added temperature range information to the Temp Spec table.

## Revision E (May 2024)

- Added new Figure 4-3 and Figure 4-6.
- Added content to the Clock Outputs section.
- Added Note 3 regarding Duty Cycle to the Electrical Characteristics table.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XXX | [-XX] |
|---|---|---|
| Device | Package | Media Type |

| | | |
|---|---|---|
| **Device:** | SY75602A: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 85Ω Clock Buffer |
| | SY75602B: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 100Ω Clock Buffer |
| | SY75603A: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 85Ω Clock Buffer |
| | SY75603B: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 100Ω Clock Buffer |
| | SY75604A: | 4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 85Ω Clock Buffer |
| | SY75604B: | 4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 100Ω Clock Buffer |
| **Package:** | TWL = | 8-Lead 1.4 mm x 1.6 mm VDFN (Wettable Flank) |
| | TWL = | 16-Lead 3 mm x 3 mm VQFN (Wettable Flank) |
| **Media Type:** | <blank> = | 120/Tube |
| | TR = | 2,000/Reel (8-Lead Package Option) |
| | TR = | 3,300/Reel (16-Lead Package Option) |

**Examples:**

| | |
|---|---|
| a) SY75603ATWL: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 85Ω Clock Buffer, 16-Lead 3 mm x 3 mm VQFN, 120/Tube |
| b) SY75602BTWL-TR: | 2 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 100Ω Clock Buffer, 8-Lead 1.4 mm x 1.6 mm VDFN, 2,000/Reel |
| c) SY75604ATWL-TR: | 4 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 85Ω Clock Buffer, 16-Lead 3 mm x 3 mm VQFN, 3,300/Reel |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

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