芯伯乐®
XINBOLE

Product Specification

XBLW SN74LS192

Synchronous BCD Up/Down Counter

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Description

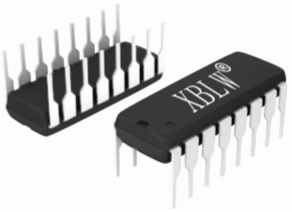
The SN74LS192 is a synchronous BCD up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behavior. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW. $\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

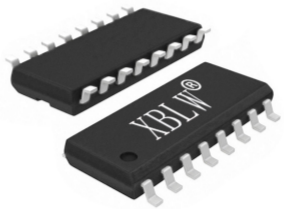
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features

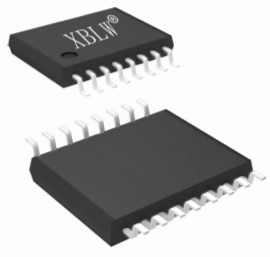
- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Specified from -20°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

ORDERING INFORMATION

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS192N	DIP-16	74LS192N	Tube	1000Pcs/Box
XBLW SN74LS192DTR	SOP-16	74LS192	Tape	2500Pcs/Reel
XBLW SN74LS192TDTR	TSSOP-16	74LS192	Tape	3000Pcs/Reel

Block Diagram

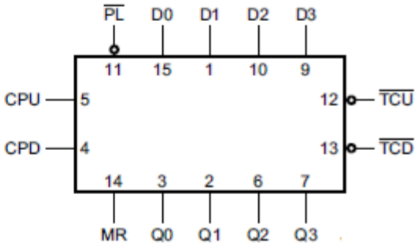


Figure 1. Logic symbol

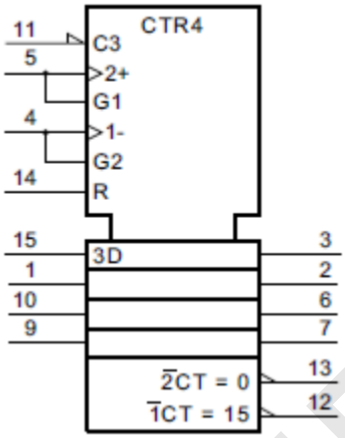


Figure 2. IEC Logic symbol

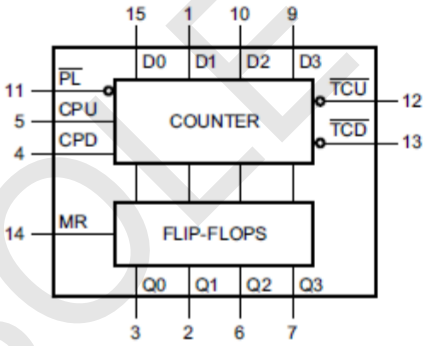


Figure 3. Functional diagram

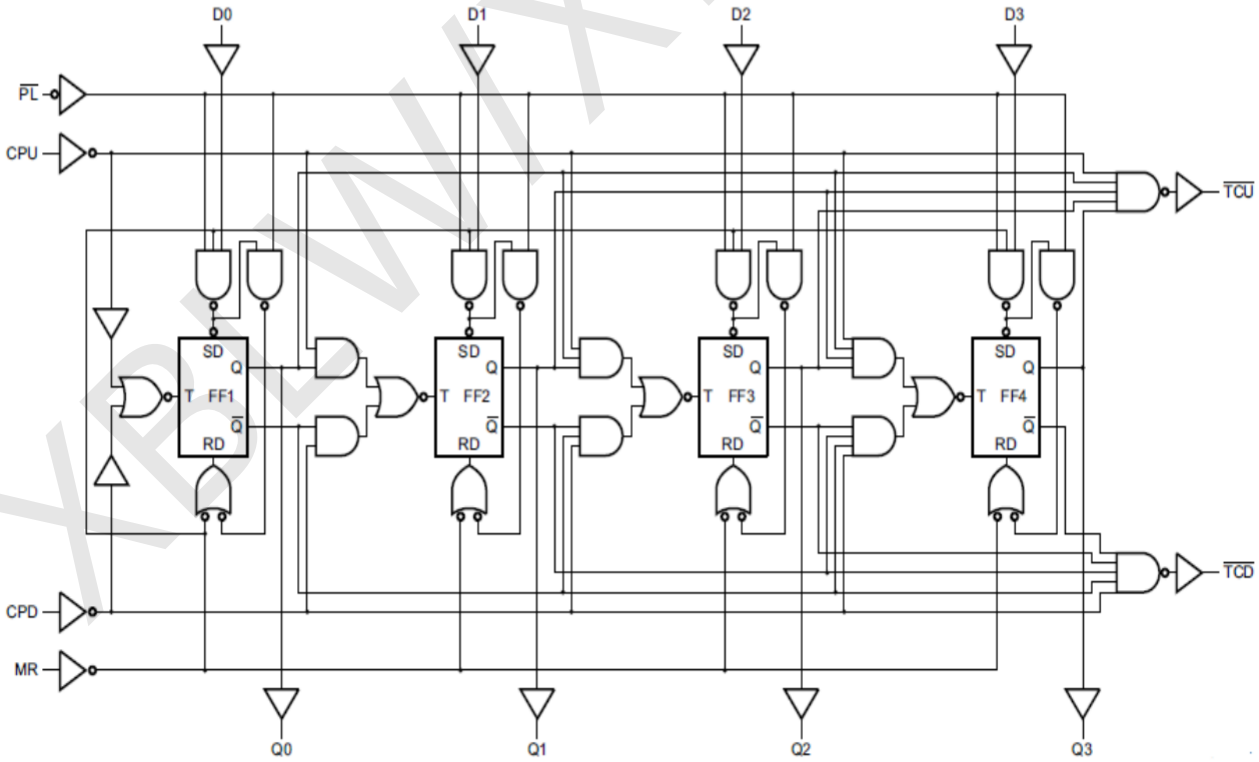


Figure 4. Logic diagram

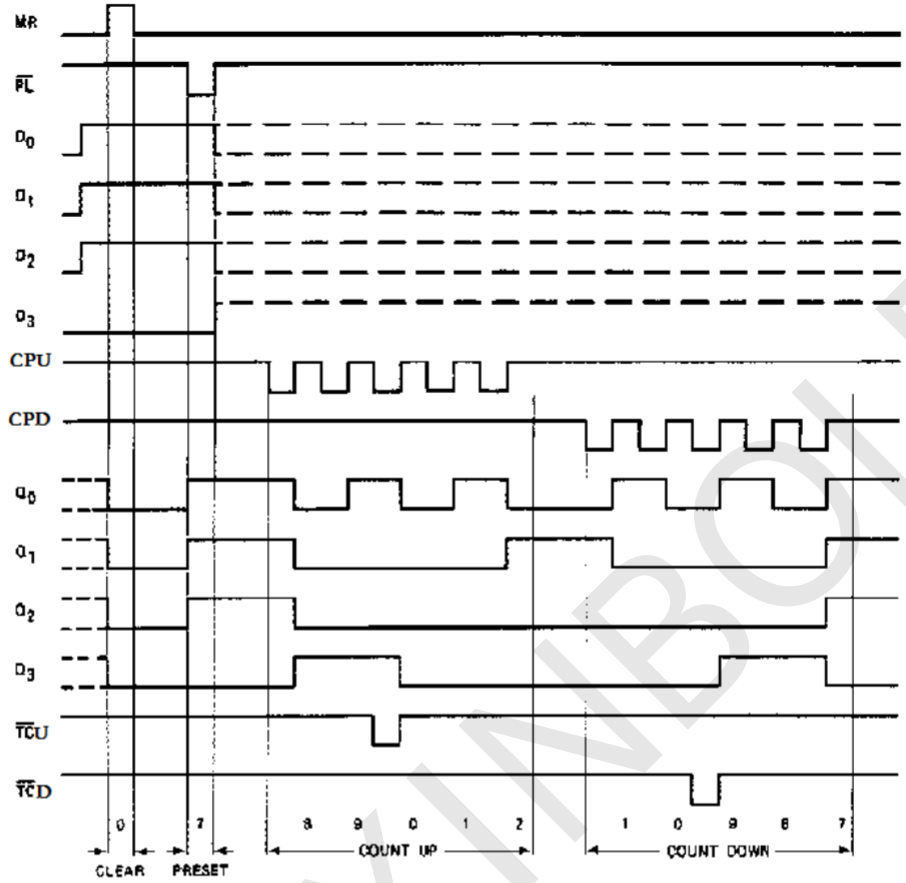
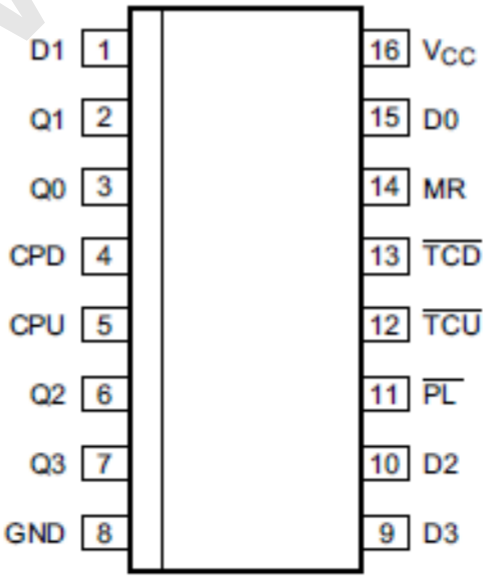


Figure 5. Typical clear, load and count sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	D1	data input 1
2	Q1	flip-flop output 1
3	Q0	flip-flop output 0
4	CPD	count down clock input
5	CPU	count up clock input
6	Q2	flip-flop output 2
7	Q3	flip-flop output 3
8	GND	ground(0V)
9	D3	data input 3
10	D2	data input 2
11	$\overline{PL}$	asynchronous parallel load input(active LOW)
12	$\overline{TCU}$	terminal count up (carry)output(active LOW)
13	$\overline{TCD}$	terminal count down (borrow)output(active LOW)
14	MR	asynchronous master reset input(active HIGH)
15	D0	data input 0
16	V_{CC}	supply voltage

Note: CPD, CPU is LOW-to-HIGH, edge triggered.

Function Table

Operating mode	Input								Output					
	MR	$\overline{PL}$	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TCU}$	$\overline{TCD}$
reset (clear)	H	X	X	L	X	X	X	X	L	I	L	L	H	L
	H	X	X	H	X	X	X	X	I	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	I	L	L	H	H
	L	L	L	X	H	X	X	H	Qn=Dn				L	H
	L	L	H	X	H	X	X	H	Qn=Dn				H	H
count up	L	H	↑	H	X	X	X	X	count up				H	H
count down	L	H	H	↑	X	X	X	X	count down				H	H

Note:
[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH transition.
[2] $\overline{TCU}$=CPU at terminal count up (HLLH).
[3] $\overline{TCD}$=CPD at terminal count down (LLLL).

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O=-0.5V to (V_{CC}+0.5V)		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-	-50	mA
storage temperature	T_{stg}	-		-65	+150	°C
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		°C
			SOP	250		

Note:
[1] For DIP16 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.
[2] For SOP16 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.
[3] For (T)SSOP16 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-		2.0	5.0	6.0	V
input voltage	V_I	-		0	-	V_{CC}	V
output voltage	V_O	-		0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	-	V_{CC}=2.0V	-		625	ns/V
			V_{CC}=4.5V	-	1.67	139	ns/V
			V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-		-20	-	+85	℃

Electrical Characteristics

DC Characteristics 1

(Tamb=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2. 1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA;V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA;V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA;V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA;V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA;V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA;V_{CC}=2.0V	-	0	0. 1	V
			I_O=20uA;V_{CC}=4.5V	-	0	0. 1	V
			I_O=20uA;V_{CC}=6.0V	-	0	0. 1	V
			I_O=4.0mA;V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA;V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=Vcc or GND;V_{CC}=6.0V		-	-	±1	μA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A;V_{CC}=6.0V		-	-	8.0	μA
input apacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(Tamb=-20℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I= V_{IH} or V_{IL}	I_O=-20uA;V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA;V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA;V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA;V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA;V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I= V_{IH} or V_{IL}	I_O=20uA;V_{CC}=2.0V	-	-	0. 1	V
			I_O=20uA;V_{CC}=4.5V	-	-	0. 1	V
			I_O=20uA;V_{CC}=6.0V	-	-	0. 1	V
			I_O=4.0mA;V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA;V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=Vcc or GND;V_{CC}=6.0V		-	-	±1	μA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A;V_{CC}=6.0V		-	-	80	μA
input apacitance	C_I	-		-	-	-	pF

AC Characteristics 1

(Tamb=25°C, GND =0V, $t_r=t_f$=6ns,C_L=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Propagation delay	t_{pd}	CPU,CPD to Qn; see Figure7	V_{CC}=2.0V	-	66	215	ns
			V_{CC}=4.5V	-	23	43	ns
			VCC=5.0V;CL= 15pF	-	24	-	ns
			V_{CC}=6.0V	-	19	37	ns
		CPU to $\overline{TCU}$; see Figure8	V_{CC}=2.0V	-	33	125	ns
			V_{CC}=4.5V	-	12	25	ns
			V_{CC}=6.0V	-	10	21	ns
		CPU to $\overline{TCD}$; see Figure8	V_{CC}=2.0V	-	39	125	ns
			V_{CC}=4.5V	-	14	25	ns
			V_{CC}=6.0V	-	11	21	ns
		$\overline{PL}$ to Qn; see Figure9	V_{CC}=2.0V	-	69	215	ns
			V_{CC}=4.5V	-	25	43	ns
			V_{CC}=6.0V	-	20	37	ns
		MR to Qn; see Figure10	V_{CC}=2.0V	-	63	200	ns
			V_{CC}=4.5V	-	23	40	ns
			V_{CC}=6.0V	-	18	34	ns
		Dn to Qn; see Figure9	V_{CC}=2.0V	-	91	275	ns
			V_{CC}=4.5V	-	33	55	ns
			V_{CC}=6.0V	-	26	47	ns
		MR to $\overline{TCU}$; MR to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	102	315	ns
			V_{CC}=4.5V	-	37	63	ns
			V_{CC}=6.0V	-	30	54	ns
		MR to $\overline{TCU}$; MR to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	96	285	ns
			V_{CC}=4.5V	-	35	57	ns
			V_{CC}=6.0V	-	28	48	ns
		MR to $\overline{TCU}$; MR to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	83	290	ns
			V_{CC}=4.5V	-	30	58	ns
			V_{CC}=6.0V	-	24	49	ns
transition time	t_t	see Figure10	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_w	up clock pulse width HIGH or LOW;see Figure7	V_{CC}=2.0V	120	39	-	ns
			V_{CC}=4.5V	24	14	-	ns
			V_{CC}=6.0V	20	11	-	ns
		down clock pulse width HIGH or LOW;see Figure7	V_{CC}=2.0V	140	50	-	ns
			V_{CC}=4.5V	28	18	-	ns
			V_{CC}=6.0V	24	14	-	ns

		master reset pulse width HIGH; see Figure10	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
		parallel load pulse width LOW; see Figure9	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
Recovery time	t_{rec}	$\overline{PL}$ to CPU,CPD; see Figure9	V_{CC}=2.0V	50	3	-	ns
			V_{CC}=4.5V	10	1	-	ns
			V_{CC}=6.0V	9	1	-	ns
		MR to CPU,CPD; see Figure10	V_{CC}=2.0V	50	0	-	ns
			V_{CC}=4.5V	10	0	-	ns
			V_{CC}=6.0V	9	0	-	ns
Set-up time	t_{su}	Dn to $\overline{PL}$; see Figure11;note: CPU= CPD= HIGH	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
Hold time	t_h	Dn to $\overline{PL}$ see Figure11	V_{CC}=2.0V	0	-14	-	ns
			V_{CC}=4.5V	0	-5	-	ns
			V_{CC}=6.0V	0	-4	-	ns
		CPU to CPD, CPD to CPU; see Figure13	V_{CC}=2.0V	80	19	-	ns
			V_{CC}=4.5V	16	7	-	ns
			V_{CC}=6.0V	14	6	-	ns
Maximum frequency	f_{MAX}	CPU,CPD; see Figure8	V_{CC}=2.0V	4.0	12	-	MHz
			V_{CC}=4.5V	20	36	-	MHz
			VCC=5.0V;CL= 15pF	-	40	-	MHz
			V_{CC}=6.0V	24	43	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}		-	24	-	pF

Note:
[1]t_{pd} is the same as t_{PLH} and t_{PHL}.
[2]t_t is the same as t_{THL} and t_{TLH}.
[3]C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:
f_i=input frequency in MHz;
f_o=output frequency in MHz;
C_L=output load capacitance in pF;
V_{CC}=supply voltage in V;
N=number of inputs switching;
$\sum(C_L\times V_{CC}^2\times f_\cdot)$=sum of outputs.

AC Characteristics 2

(Tamb=-20℃ to +85℃, GND =0V, t_r=t_f=6ns,C_L=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Propagation delay	t_{pd}	CPU,CPD to Qn; see Figure7	V_{CC}=2.0V	-	-	270	ns
			V_{CC}=4.5V	-	-	54	ns
			VCC=5.0V;CL= 15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	46	ns
		CPU to $\overline{TCU}$; see Figure8	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
		CPU to $\overline{TCD}$; see Figure8	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
		$\overline{PL}$ to Qn; see Figure9	V_{CC}=2.0V	-	-	270	ns
			V_{CC}=4.5V	-	-	54	ns
			V_{CC}=6.0V	-	-	46	ns
		MR to Qn; see Figure10	V_{CC}=2.0V	-	-	25	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
		Dn to Qn; see Figure9	V_{CC}=2.0V	-	-	345	ns
			V_{CC}=4.5V	-	-	69	ns
			V_{CC}=6.0V	-	-	59	ns
		$\overline{PL}$ to $\overline{TCU}$; $\overline{PL}$ to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	-	395	ns
			V_{CC}=4.5V	-	-	79	ns
			V_{CC}=6.0V	-	-	67	ns
		MR to $\overline{TCU}$; MR to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	-	355	ns
			V_{CC}=4.5V	-	-	71	ns
			V_{CC}=6.0V	-	-	60	ns
		Dn to $\overline{TCU}$; Dn to $\overline{TCD}$; see Figure12	V_{CC}=2.0V	-	-	365	ns
			V_{CC}=4.5V	-	-	73	ns
			V_{CC}=6.0V	-	-	62	ns
transition time	t_t	see Figure10	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_w	up clock pulse width HIGH or LOW;see Figure7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		down clock pulse width HIGH or LOW;see Figure7	V_{CC}=2.0V	175	-	-	ns
			V_{CC}=4.5V	35	-	-	ns
			V_{CC}=6.0V	30	-	-	ns

		master reset pulse width HIGH; see Figure10	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		parallel load pulse width LOW; see Figure9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
Recovery time	t_{rec}	$\overline{PL}$ to CPU,CPD; see Figure9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
		MR to CPU,CPD; see Figure10	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
Set-up time	t_{su}	Dn to $\overline{PL}$; see Figure11; note: CPU= CPD= HIGH	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
Hold time	t_h	Dn to $\overline{PL}$ see Figure11	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		CPU to CPD, CPD to CPU; see Figure13	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
Maximum frequency	f_{MAX}	CPU,CPD; see Figure8	V_{CC}=2.0V	3.2	-	-	MHz
			V_{CC}=4.5V	16	-	-	MHz
			VCC=5.0V;CL= 15pF	-	-	-	MHz
			V_{CC}=6.0V	19	-	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}		-	-	-	pF

Note:
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)$ where:
f_i=input frequency in MHz;
f_o=output frequency in MHz;
C_L=output load capacitance in pF; V_{CC}=supply voltage in V;
$\sum(CL\times VCC\ 2\times fo)$=sum of outputs.

Testing Circuit

AC Testing Circuit

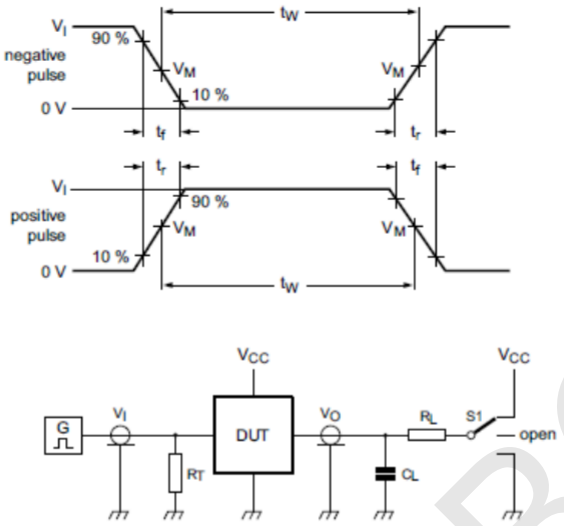


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator. R_L=Load resistance
S1=Test selection switch

AC Testing Waveforms

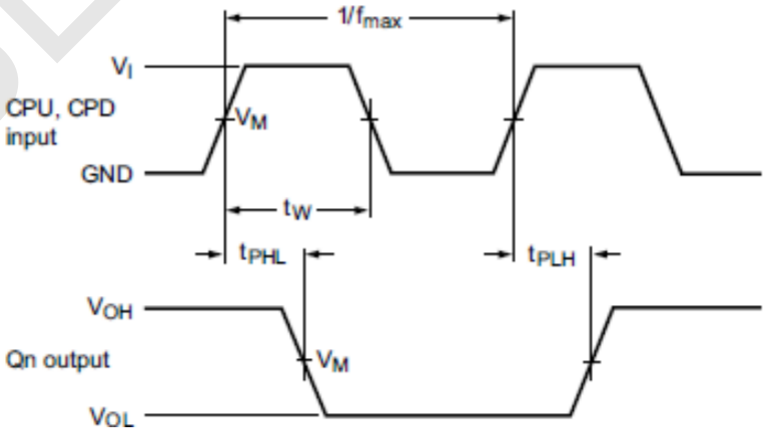


Figure 7. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

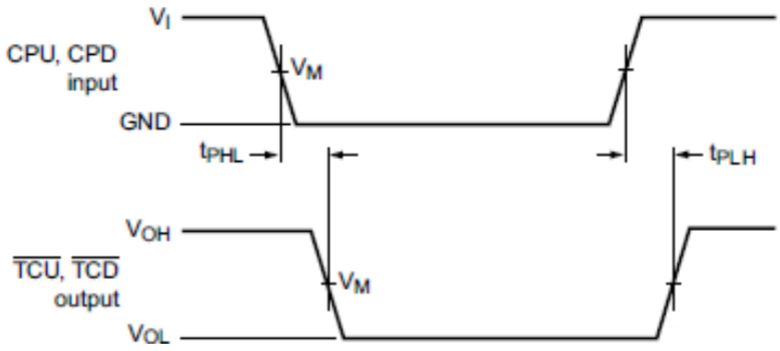


Figure 8. The clock (CPU, CPD) to terminal count output ($\overline{TCU}$, $\overline{TCD}$) propagation delays

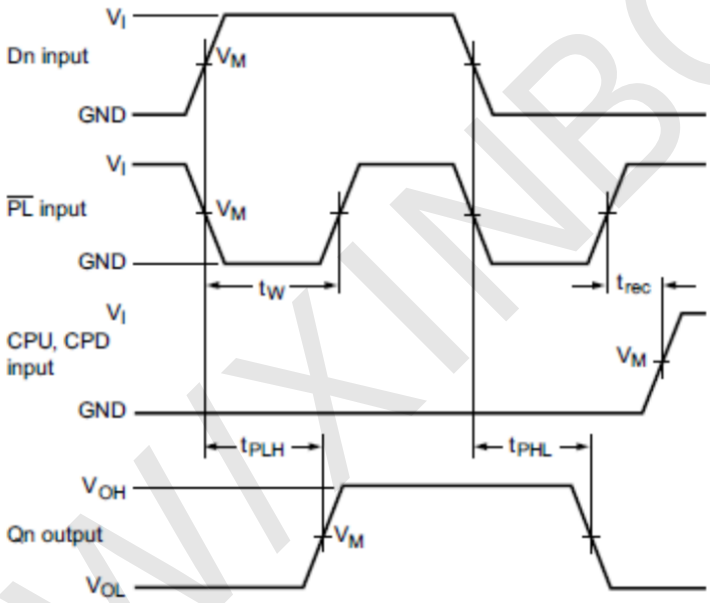


Figure 9. The parallel load input ($\overline{PL}$) and data (Dn) to Qn output propagation delays and $\overline{PL}$ removal time to clock input (CPU, CPD)

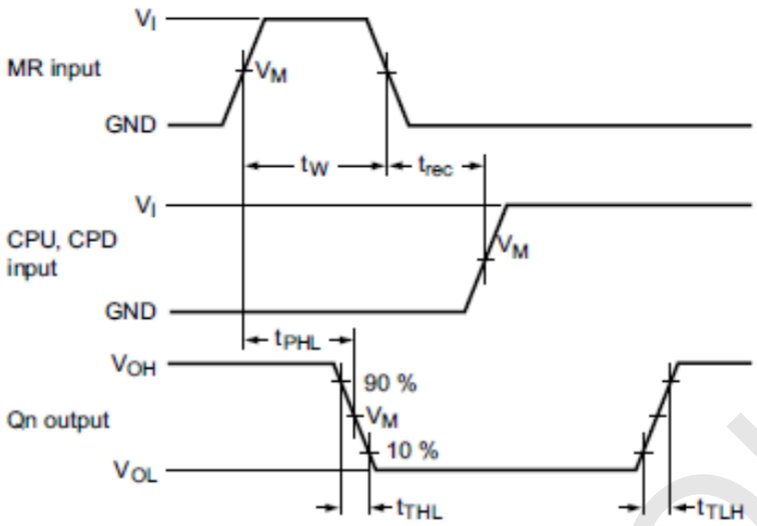


Figure 10. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

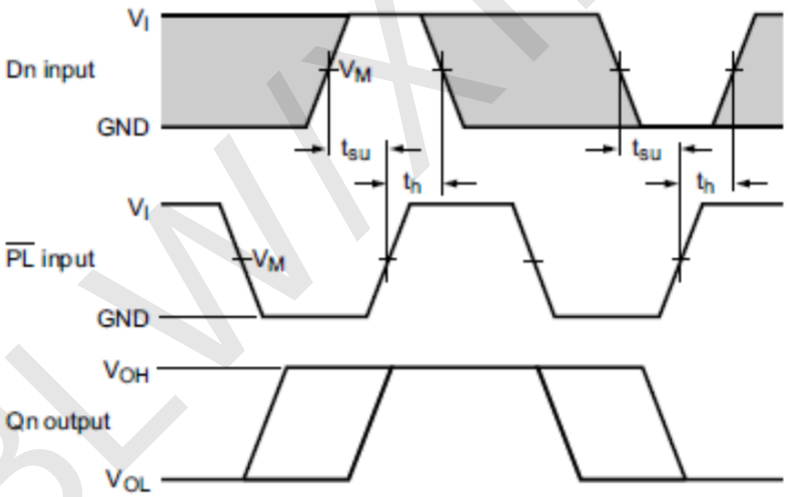


Figure 11. The data input (Dn) to parallel load input ($\bar{P}L$) set-up and hold times

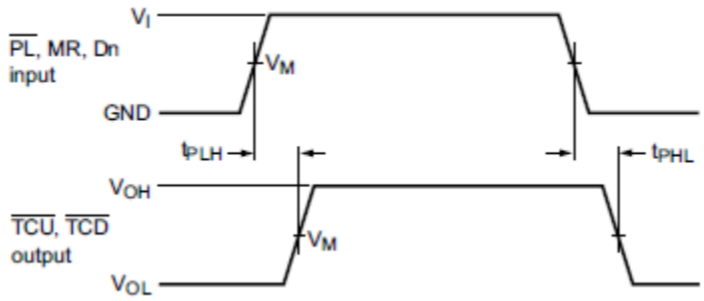


Figure 12. The data input (Dn), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TCU}$, $\overline{TCD}$) propagation delays

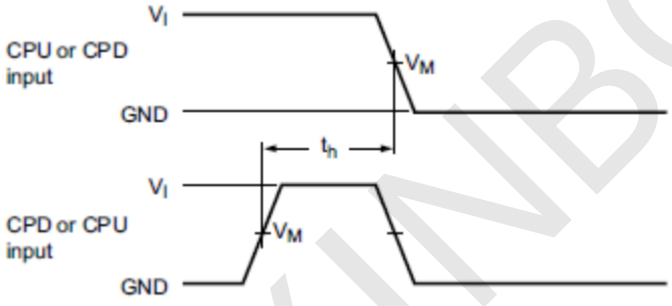


Figure 13. The CPU to CPD or CPD to CPU hold times

Measurement Points

Type	Input		Output
	V_I	V_M	V_M
SN74LS192	GND to V_{CC}	0.5×V_{CC}	0.5×V_{CC}

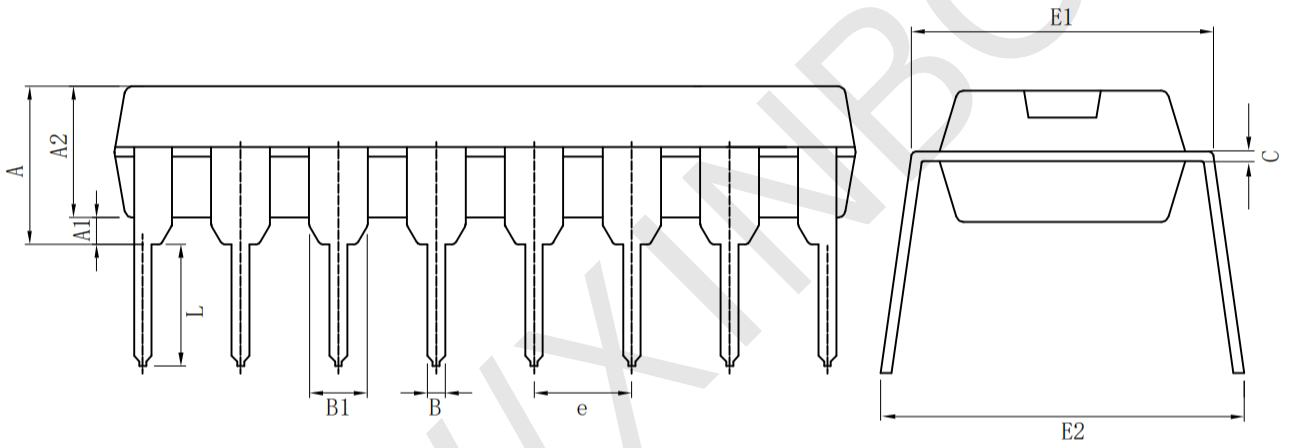
Test Data

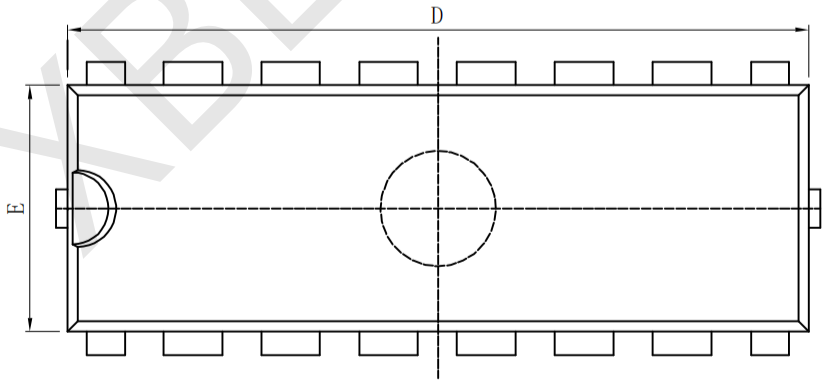
Type	Input		Load		S1 position
	V_I	t_r,t_f	C_L	R_L	t_{PHL},t_{PLH}
SN74LS192	V_{CC}	6.0ns	15pF,50pF	1KΩ	open

PackageInformation

· DIP-16

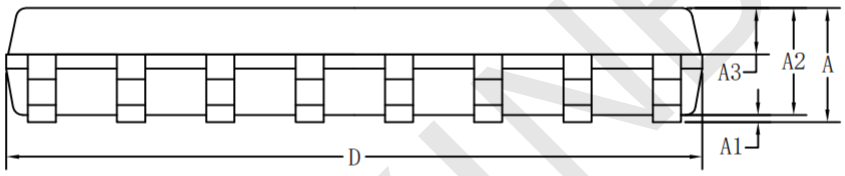
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

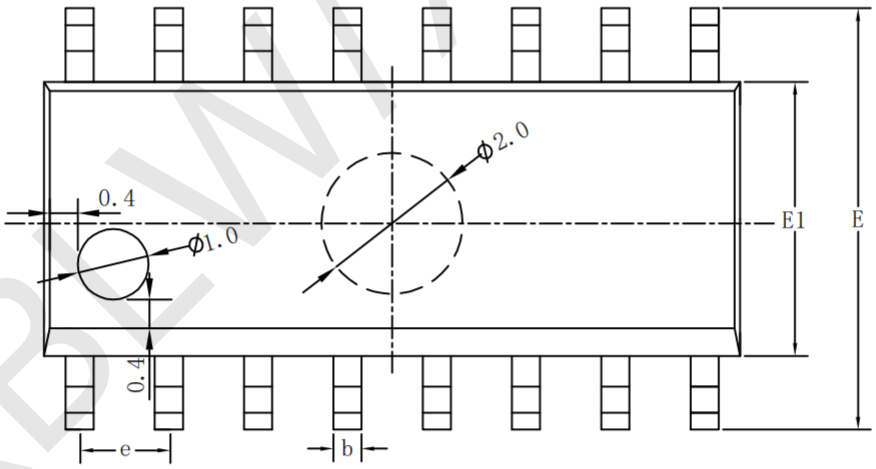


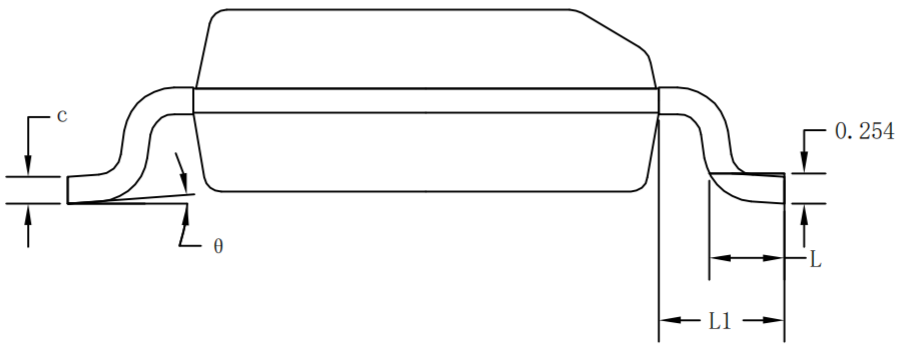


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e		1.27(BSC)		e		0.050(BSC)	
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1		1.05(BSC)		L1		0.041(BSC)	
θ	0°	4°	8°	θ	0°	4°	8°

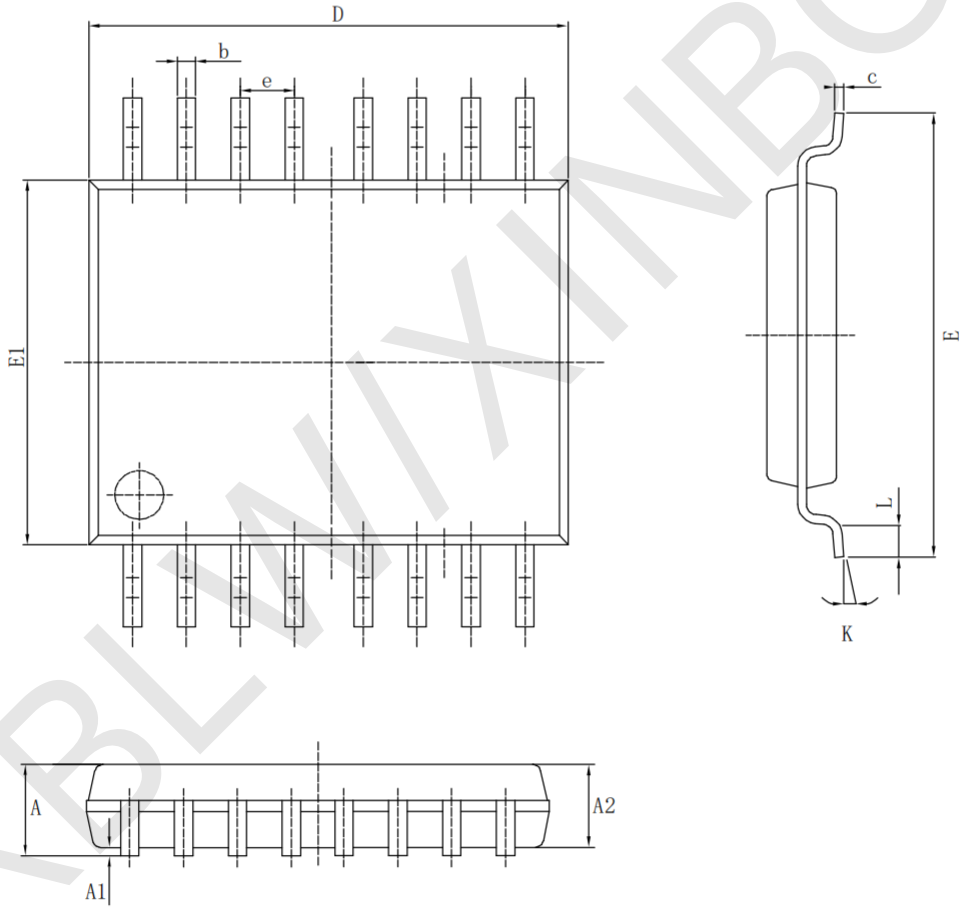






· TSSOP-16

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65(BSC)		e	0.0256(BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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