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## MAX98365

## Tiny, Cost-Effective, 14V Plug-and-Play Digital Class-D Amplifier

### General Description

The MAX98365 is an easy-to-use, low-cost, digital input Class-D amplifier that provides industry-leading, Class-AB audio performance with Class-D efficiency. The digital audio interface automatically recognizes different PCM and TDM clocking schemes which eliminates the need for I<sup>2</sup>C programming: Simply supply power, LRCLK, BCLK, and digital audio to generate sound. Furthermore, a novel pinout allows customers to use the cost-effective wafer-level package (WLP) with no need for expensive in-pad vias. A wide 3V to 14V supply range allows the device to deliver 13.8W into an 8Ω load.

The digital audio interface is highly flexible. The devices support I<sup>2</sup>S, left-justified, and 8-channel time division multiplexed (TDM) data formats. The digital audio interface accepts 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz sample rates. Data words can be 16-bit, 24-bit, or 32-bit in I<sup>2</sup>S and left-justified modes and 16-bit or 32-bit in TDM mode.

Digital audio interface input thresholds are ideal for interfacing to 1.2V and 1.8V logic. The devices can tolerate logic input voltages up to 5.5V.

The MAX98365A and MAX98365B have fast 1ms turn-on times while the MAX98365C and MAX98365D ramp the volume over 13ms during turn-on and turn-off.

The devices eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count. The devices also feature a very high wideband jitter tolerance (12ns, typ) on BCLK and LRCLK to provide robust operation.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class-D devices and reduces the component count of the solution.

The devices are specified over the -40°C to +85°C temperature range.

### Applications

- Smart Speakers
- Notebook Computers
- IoT Devices
- Gaming Devices (Audio and Haptics)
- Smartphones
- Tablets
- Cameras

### Benefits and Features

- Simple Plug-and-Play Design
- Wide Amplifier Supply Range (3V to 14V)
- 13.8W Output Power into 8Ω at 14V
- 17.6W Output Power into 6Ω at 14V
- 30mW Quiescent Power
- 1ms Turn-On Time (for MAX98365A and MAX98365B)
- 92.7% Efficiency (7.0W into R<sub>L</sub> = 8Ω, PVDD = 12V)
- 22μV<sub>RMS</sub> Output Noise
- 111.5dB Dynamic Range
- -85dB THD+N at 1kHz
- No MCLK Required
- Sample Rates of 8kHz to 192kHz
- Supports Left, Right, or (Left/2 + Right/2) Output in I<sup>2</sup>S and Left-Justified Modes
- Sophisticated Edge Rate Control Enables Filterless Class-D Outputs
- Low 0.5μA Shutdown Current
- Low RF Susceptibility Rejects TDMA Noise from GSM Radios
- Class-D Switching Frequency Trimmed to 6% for Better EMI Planning
- Extensive Click-and-Pop Reduction Circuitry
- Robust Short-Circuit and Thermal Protection
- Available in Space-Saving Package: 12 Bump, WLP (1.21mm x 1.78mm, 0.4mm Pitch)

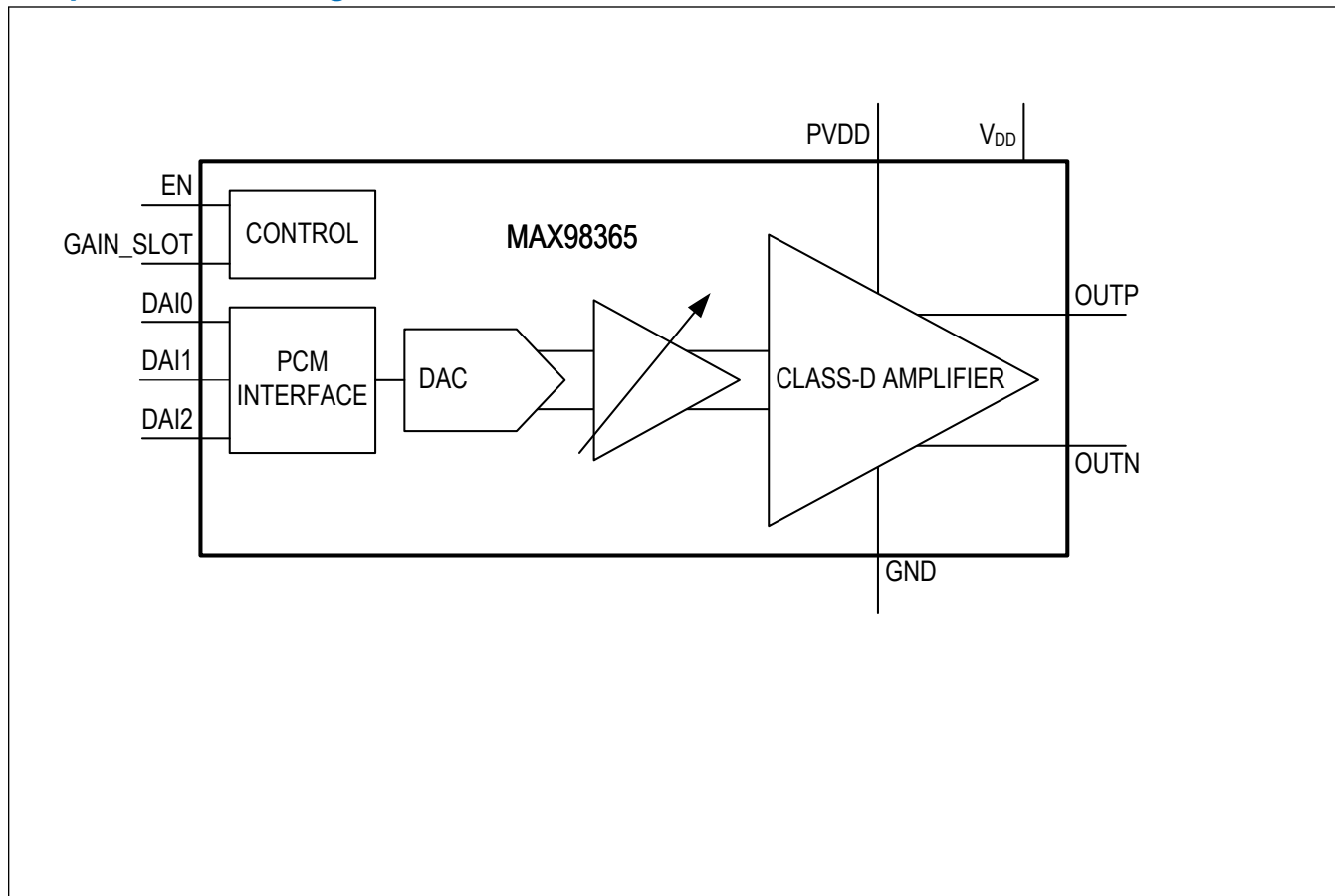
**Ordering Information** appears at end of data sheet.

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Simplified Block Diagram



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## Absolute Maximum Ratings

PVDD to GND.....	-0.3V to +16V	Duration of OOTP short to OUTN .....	Continuous
V <sub>DD</sub> , EN, DAI0, DAI1, and DAI2 to GND.....	-0.3V to +6V	Continuous power dissipation (T <sub>A</sub> = +70°C) WLP (derate 20.83mW/°C above +70°C) .....	1.67mW
OOTP, OUTN to GND .....	-0.3V to V <sub>PVDD</sub> + 0.3V	Junction temperature .....	+150°C
GAIN_SLOT to GND .....	-0.3V to V <sub>VDD</sub> + 0.3V	Operating temperature range.....	-40°C to +85°C
Continuous current in or out of PVDD, GND, OOTP, or OUTN .....	-3.5A to +3.5A	Storage temperature range.....	-65°C to +150°C
Continuous input current (all other pins) .....	-20mA to +20mA	Soldering temperature (reflow) .....	+260°C
Duration of OOTP or OUTN short circuit to GND or V <sub>DD</sub> .....	Continuous		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### WLP

Package Code	W121D1+1
Outline Number	<a href="#">21-100536</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	48°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	N/A

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SYSTEM</b>						
PVDD Supply Voltage Operating Range	$V_{PVDD}$	Guaranteed by PSRR test	3.0		14	V
PVDD Supply Voltage	$V_{PVDD}$	Device is functional but parametric performance is not guaranteed	2.3			V
$V_{DD}$ Supply Voltage Range	$V_{DD}$	Guaranteed by PSRR test	1.71		5.5	V
PVDD Undervoltage Lockout	$V_{UVLO}$	$V_{PVDD}$ rising	2.15		2.4	V
		$V_{PVDD}$ falling	1.85		2.1	
$V_{DD}$ Undervoltage Lockout	$V_{UVLO}$	$V_{DD}$ rising	1.3		1.6	V
		$V_{DD}$ falling	1.2		1.5	
Quiescent Power		$T_A = +25^\circ C$		30		mW
PVDD Shutdown Current	$I_{PVDD\_SHDN}$	EN = 0V, $T_A = +25^\circ C$		0.52	2.8	$\mu A$
$V_{DD}$ Shutdown Current	$I_{VDD\_SHDN}$	EN = 0V, $T_A = +25^\circ C$		0.02	0.3	$\mu A$
PVDD Standby Current	$I_{PVDD\_STNDBY}$	EN = 1.8V, $T_A = +25^\circ C$ , all DAI <sub>n</sub> pins at 0V		0.52	2.8	$\mu A$
		EN = 1.8V, $T_A = +25^\circ C$ , no toggling on DAI <sub>n</sub> pins			2.8	
$V_{DD}$ Standby Current	$I_{VDD\_STNDBY}$	EN = 1.8V, $T_A = +25^\circ C$ , all DAI <sub>n</sub> pins at 0V		1.8	10.7	$\mu A$
		EN = 1.8V, $T_A = +25^\circ C$ , no toggling on DAI <sub>n</sub> pins			80	
Turn-On Time	$t_{ON}$	Time from shutdown or standby to full gain audio out, MAX98365A and MAX98365B			1.0	ms
		Time from shutdown or standby to full gain audio out, MAX98365A and MAX98365B, $f_S = 8kHz$ , $f_S = 16kHz$			2.1	
		Time from shutdown or standby to full gain audio out, MAX98365C and MAX98365D			12.2	
Thermal Shutdown Temperature				154		$^\circ C$
Thermal Shutdown Recovery Hysteresis				20		$^\circ C$
<b>CLASS-D AMPLIFIER</b>						
Output Offset Voltage	$V_{OS}$	$T_A = +25^\circ C$	-3.0	$\pm 0.3$	+3.0	mV



**Electrical Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click-and-Pop Level	$K_{CP}$	Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$ , into Standby or Shutdown			-70		dBV
		Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$ , out of Standby or Shutdown			-70		
PVDD Supply Rejection DC	PSRR	DC, digital silence used for input signal, $Z_{SPK} = \infty$ , $V_{PVDD} = 3V$ to $14V$		68	85		dB
PVDD Supply Rejection AC	PSRR	$V_{RIPPLE} = 200mV_{PP}$	$f_{RIPPLE} = 217Hz$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		85		dB
			$f_{RIPPLE} = 1kHz$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		85		
			$f_{RIPPLE} = 10kHz$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		76		
$V_{DD}$ Supply Rejection DC	PSRR	$T_A = +25^\circ C$ , digital silence used for input signal, $Z_{SPK} = \infty$ , DC, $V_{DD} = 2.5V$ to $5.5V$		94	100		dB
$V_{DD}$ Supply Rejection AC	PSRR	$V_{RIPPLE} = 200mV_{PP}$	$f_{RIPPLE} = 217Hz$ , $T_A = +25^\circ C$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		100		dB
			$f_{RIPPLE} = 1kHz$ , $T_A = +25^\circ C$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		100		
			$f_{RIPPLE} = 10kHz$ , $T_A = +25^\circ C$ , digital silence used for input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$		100		

**Electrical Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OOTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Intermodulation		$T_A = +25^\circ C$ , $f_{IN} = 1kHz$ , $P_{OUT} = 400mW$ , $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$	$PVDD$ $f_{RIPPLE} = 217Hz$ , $V_{RIPPLE} = 100mV_{PP}$		-80		dB
			$V_{DD}$ $f_{RIPPLE} = 217Hz$ , $V_{RIPPLE} = 100mV_{PP}$		-80		
Output Power	$P_{OUT}$	$V_{PVDD} = 11V$ , THD+N $\leq 10\%$ , $Z_{SPK} = 4\Omega + 33\mu H$			14.7		W
			$V_{PVDD} = 12V$ , THD+N $\leq 10\%$ , $Z_{SPK} = 8\Omega + 33\mu H$		10.3		
			$V_{PVDD} = 14V$ , THD+N $\leq 10\%$ , $Z_{SPK} = 8\Omega + 33\mu H$		13.8		
			$V_{PVDD} = 12V$ , THD+N $\leq 1\%$ , $Z_{SPK} = 4\Omega + 33\mu H$		14		
			$V_{PVDD} = 12V$ , THD+N $\leq 1\%$ , $Z_{SPK} = 8\Omega + 33\mu H$		8.2		
			$V_{PVDD} = 14V$ , THD+N $\leq 1\%$ , $Z_{SPK} = 8\Omega + 33\mu H$		11.2		
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$ , $T_A = +25^\circ C$	$P_{OUT} = 1W$ , $Z_{SPK} = 8\Omega + 33\mu H$		-85	-76	dB
			$P_{OUT} = 6W$ , $Z_{SPK} = 8\Omega + 33\mu H$		-85		
			$P_{OUT} = 8W$ , $Z_{SPK} = 4\Omega + 33\mu H$		-85		
Intermodulation Distortion	IMD	ITU-R, 19kHz/20kHz, 1:1, $V_{IN} = -3dBFS$ , $Z_{SPK} = 8\Omega + 33\mu H$		-63		dB	
Dynamic Range	DR	A-weighted, $Z_{SPK} = 8\Omega + 33\mu H$ , -60dB 1kHz output signal, normalized to full scale (THD+N = 1%), 24- or 32-bit data		111.5		dB	
Output Noise	$e_{Nd}$	A-weighted, 24-bit or 32-bit data		22		$\mu V_{RMS}$	
Full-Scale Output Voltage	FS	$I^2S$ or left-justified mode with $GAIN\_SLOT = GND$ , or TDM mode (Note 3)		21.1	21.5	21.9	dBV
			$I^2S$ or left-justified mode with $GAIN\_SLOT = \text{unconnected}$	18.1	18.5	18.9	
			$I^2S$ or left-justified mode with $GAIN\_SLOT = V_{DD}$	15.1	15.5	15.9	
			$I^2S$ or left-justified mode with $GAIN\_SLOT = V_{DD}$ through 100k $\Omega$	12.1	12.5	12.9	
			$I^2S$ or left-justified mode with $GAIN\_SLOT = GND$ through 100k $\Omega$	9.1	9.5	9.9	
Output Current Limit	$I_{LIM}$		3.5			A	
Output Current Limit Autorestart Time				27		ms	

**Electrical Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	$\eta$	$Z_{SPK} = 8\Omega + 33\mu H$ , $P_{OUT} = 7W$ , $f = 1kHz$		92.7		%
		$Z_{SPK} = 8\Omega + 33\mu H$ , $P_{OUT} = 1W$ , $f = 1kHz$		88.9		
		$Z_{SPK} = 4\Omega + 33\mu H$ , $P_{OUT} = 1W$ , $f = 1kHz$		84.8		
Frequency Response			-0.25		+0.3	dB
Class-D Switching Frequency	$f_{SW}$		282	300	318	kHz
Spread-Spectrum Bandwidth	$f_{SSM}$			$\pm 4$		kHz
Output Stage On-Resistance	$R_{ON}$	PMOS + NMOS (Full H-Bridge), $T_A = +25^\circ C$		0.33		$\Omega$
Minimum Load Resistance	$R_L$	$PVDD > 12V$		3.7		$\Omega$
		$8.4V < PVDD < 12V$		3.1		
		$PVDD \leq 8.4V$		2.1		
Maximum Device to Device Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz across all sample rates and DAI operating modes		3		deg
<b>DAC DIGITAL FILTER (LRCLK &lt; 50kHz)</b>						
Passband Cutoff	$f_{PLP}$	Ripple < $\delta_p$		$0.455 \times f_S$		Hz
		Droop < -3dB		$0.459 \times f_S$		Hz
Passband Ripple	$\delta_p$	$f < f_{PLP}$ , referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband Cutoff	$f_{SLP}$	Attenuation > $\delta_S$			$0.49 \times f_S$	Hz
Stopband Attenuation	$\delta_S$	$f > f_{SLP}$	75			dB
Group Delay		$f = 1kHz$		5		samples
<b>DAC DIGITAL FILTER (LRCLK &gt; 50kHz)</b>						
Passband Cutoff	$f_{PLP}$	Ripple < $\delta_p$ , $88.2kHz \leq f_S \leq 96kHz$		$0.227 \times f_S$		Hz
		Droop < -3dB, $88.2kHz \leq f_S \leq 96kHz$		$0.314 \times f_S$		Hz
	$f_{PLP}$	Ripple < $\delta_p$ , $176.4kHz \leq f_S \leq 192kHz$		$0.1135 \times f_S$		Hz
		Droop < -3dB cutoff, $176.4kHz \leq f_S \leq 192kHz$		$0.232 \times f_S$		Hz
Passband Ripple	$\delta_p$	$f < f_{PLP}$ , referenced to signal level at 1kHz	-0.25		+0.25	dB
Stopband Cutoff	$f_{SLP}$	Attenuation < $\delta_S$			$0.49 \times f_S$	Hz
Stopband Attenuation	$\delta_S$	$f > f_{SLP}$	75			dB
Max Group Delay		$f = 1kHz$		5.5		samples
<b>DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER</b>						
DC Attenuation			80			dB

**Electrical Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OOTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Blocking Filter -3dB Cutoff Frequency	$f_C$	For $f_s = 8kHz, 16kHz, 32kHz, 48kHz, 96kHz, \text{ and } 192kHz$		1.872		Hz
		For $f_s = 44.1kHz, 88.2kHz, \text{ and } 176.4kHz$		1.72		
<b>DIGITAL I/O</b>						
LRCLK tolerance				2.5		%
Resolution		I <sup>2</sup> S/left-justified mode		16/24/32		Bits
		TDM mode		16/32		
BCLK Frequency Range	$f_{BCLK}$	BCLK frequency required for DAI Configuration and unmuting (Note 2)	0.2496		25.19	MHz
BCLK Duty Cycle	DC		40		60	%
Maximum High Frequency BCLK and LRCLK Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		12		ns
Maximum Low Frequency BCLK and LRCLK Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter $\leq$ 40kHz		0.5		ns
Input High Voltage	$V_{IH}$	DAI0, DAI1, DAI2	0.84			V
		EN	0.84			
Input Low Voltage	$V_{IL}$	DAI0, DAI1, DAI2			0.54	V
		EN			0.2	
Input Hysteresis	$V_{HYS}$	DAI0, DAI1, DAI2	55			mV
		EN		25		
Input Leakage Current	$I_{IH}, I_{IL}$	$V_{IN} = 0V, T_A = +25^\circ C, \text{ DAI0, DAI1, DAI2}$	-1			$\mu A$
		$V_{IN} = 5.5V, T_A = +25^\circ C, \text{ DAI0, DAI1, DAI2}$			+4	
Input Capacitance	$C_{IN}$			3		pF
DIN to BCLK Setup Time	$t_{SETUP}$		4			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$		4			ns
DIN to BCLK Hold Time	$t_{HOLD}$		4			ns
LRCLK to BCLK Hold Time	$t_{SYNHOLD}$		4			ns

**Electrical Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{VDD} = 1.8V$ ,  $V_{GND} = 0V$ , gain = 21.5dB,  $f_{BCLK} = 3.072MHz$ ,  $f_{LRCLK} = 48kHz$ ,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $T_A = T_{MIN}$  to  $T_{MAX}$ , typical values are at  $T_A = +25^\circ C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GAIN_SLOT COMPARATOR TRIP POINTS</b>						
GAIN_SLOT Comparator Trip Points	$V_{GAIN\_SLOT}$	15.5dBV output setting in I <sup>2</sup> S and left-justified modes, channel 1, 3, or 7 in TDM mode	0.9 x $V_{DD}$		$V_{DD}$	V
		12.5dBV output setting in I <sup>2</sup> S and left-justified modes	0.65 x $V_{DD}$		0.85 x $V_{DD}$	
		18.5dBV output setting in I <sup>2</sup> S and left-justified modes, channel 2 or 6 in TDM mode	0.4 x $V_{DD}$		0.6 x $V_{DD}$	
		9.5dBV output setting in I <sup>2</sup> S and left-justified modes	0.15 x $V_{DD}$		0.35 x $V_{DD}$	
		21.5dBV output setting in I <sup>2</sup> S and left-justified modes, channel 0, 4, or 5 in TDM mode	0		0.1 x $V_{DD}$	

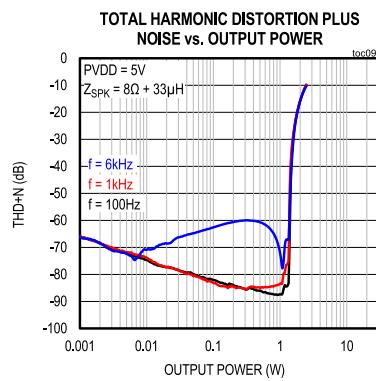
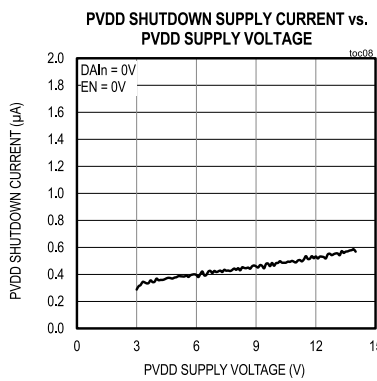
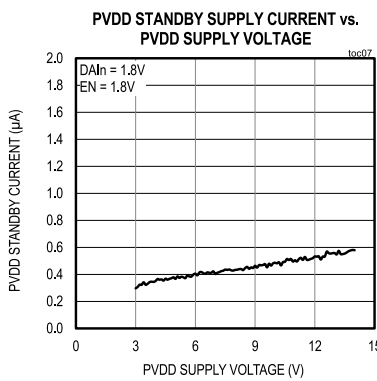
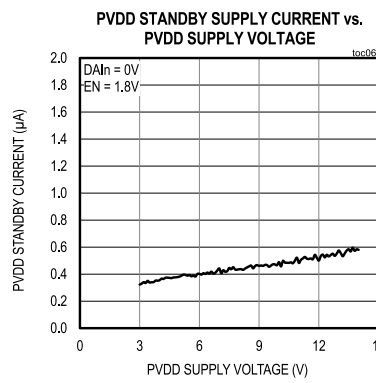
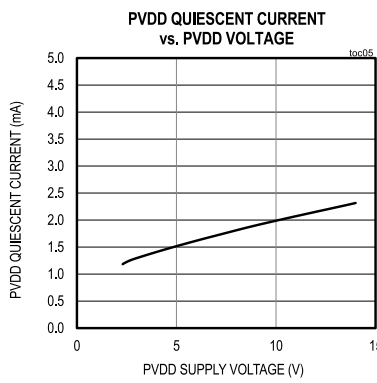
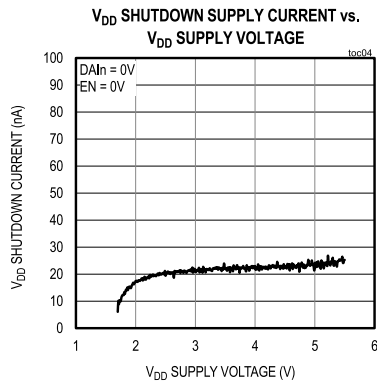
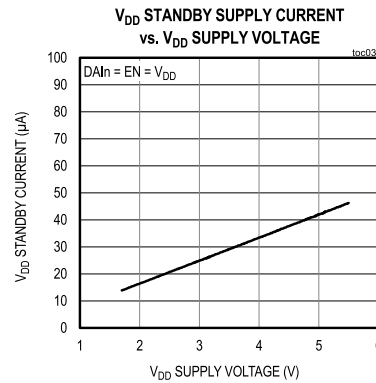
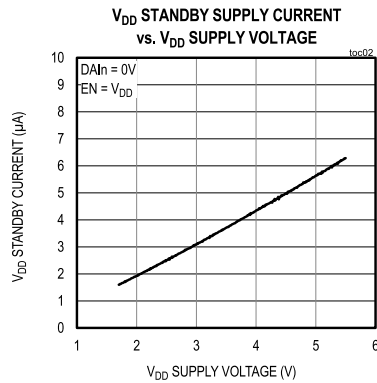
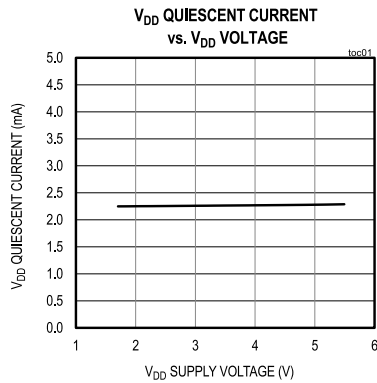
**Note 1:** Limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 2:** See the [Digital Audio Interface Configuration](#) and [Valid Clock Frequencies](#) sections for more information.

**Note 3:** PVDD level limits the achievable output swing due to clipping.

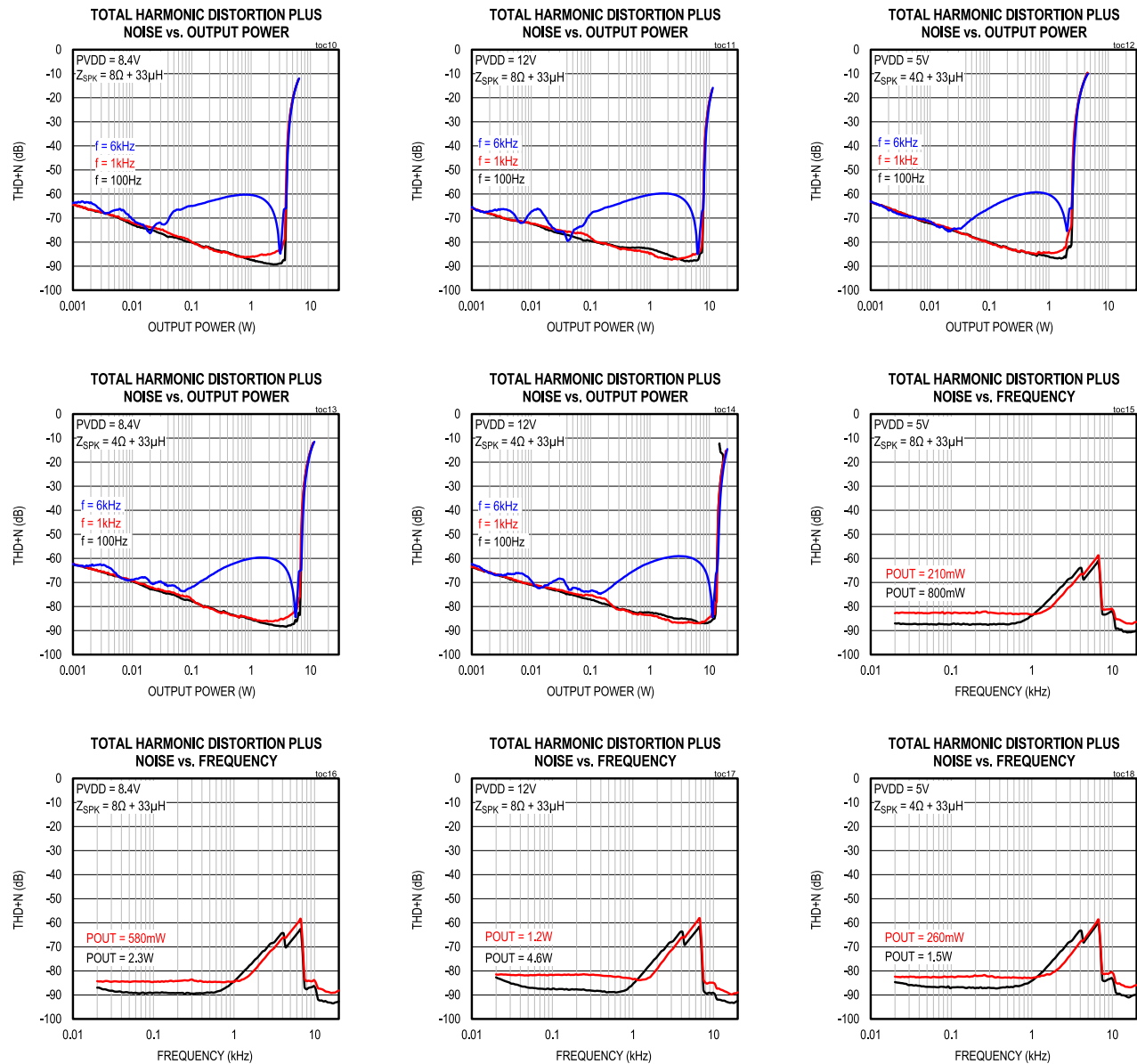
Typical Operating Characteristics

( $V_{PVDD} = 12V$ ,  $V_{DD} = 1.8V$ ,  $V_{GND} = 0V$ ; Gain = 21.5dB,  $Z_{SPK} = \infty$  between OUP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $f_S = 48kHz$ , 24-bit data,  $f_{BCLK} = 3.072MHz$ . Typical values are at  $T_A = +25^\circ C$ )



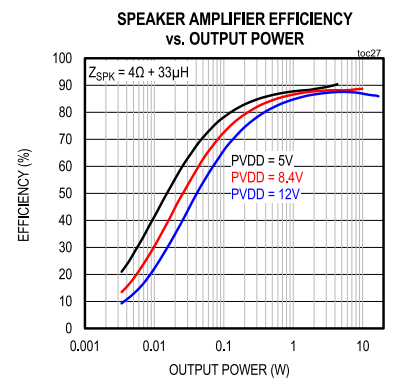
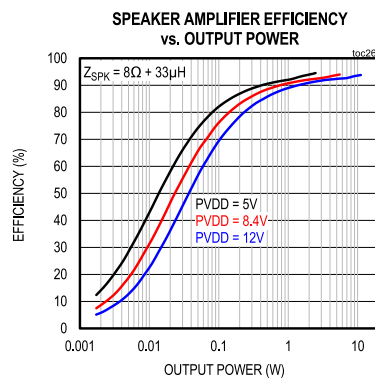
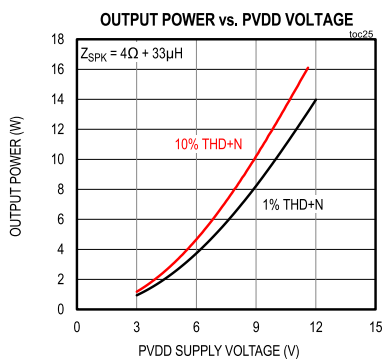
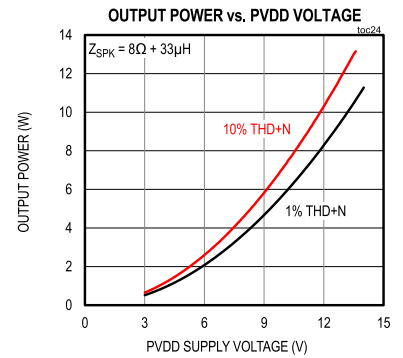
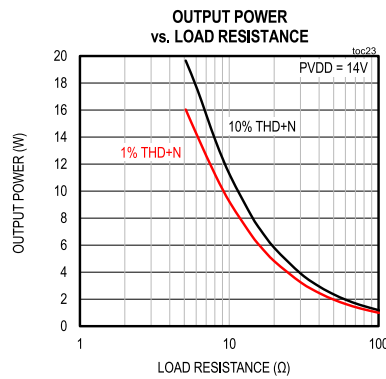
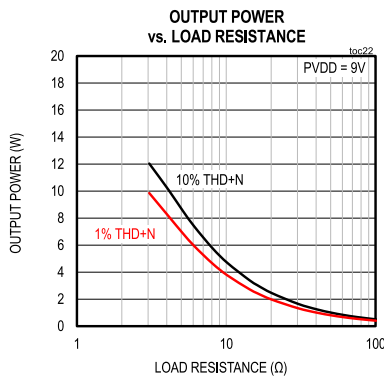
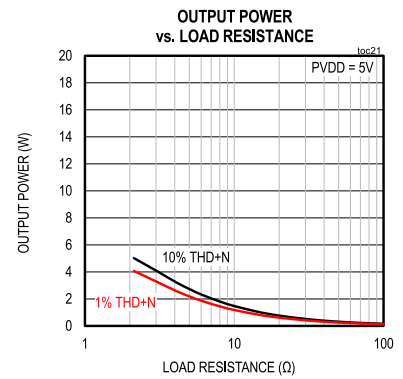
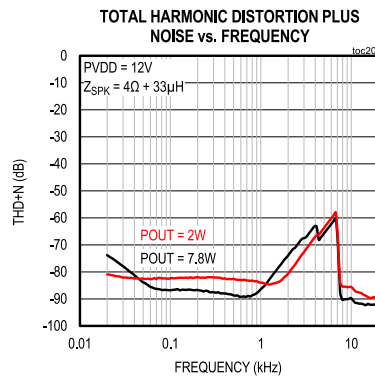
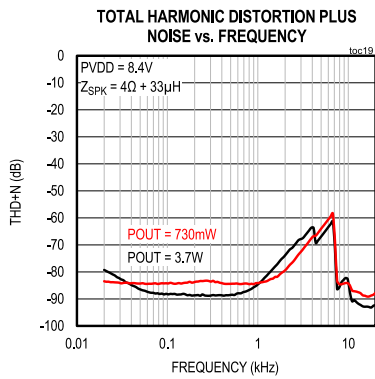
Typical Operating Characteristics (continued)

( $V_{PVDD} = 12V$ ,  $V_{DD} = 1.8V$ ,  $V_{GND} = 0V$ ; Gain = 21.5dB,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $f_S = 48kHz$ , 24-bit data,  $f_{CLK} = 3.072MHz$ . Typical values are at  $T_A = +25^\circ C$ )



Typical Operating Characteristics (continued)

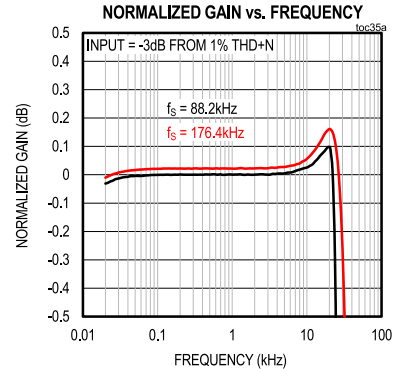
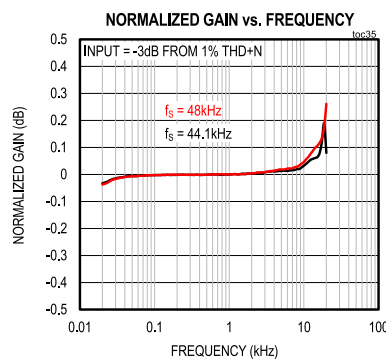
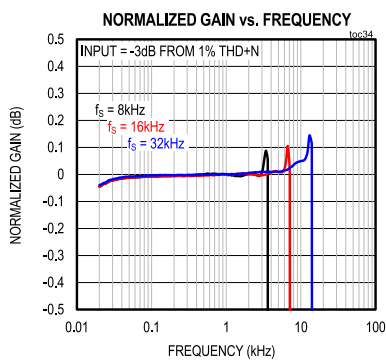
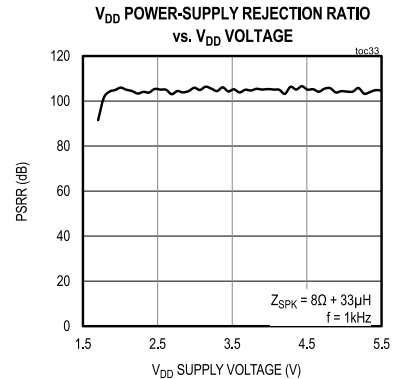
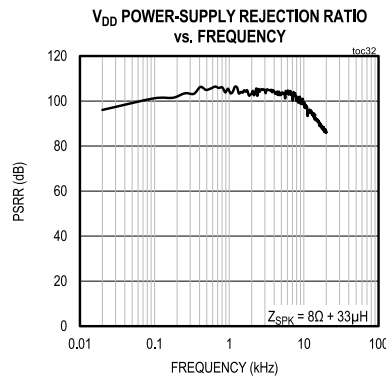
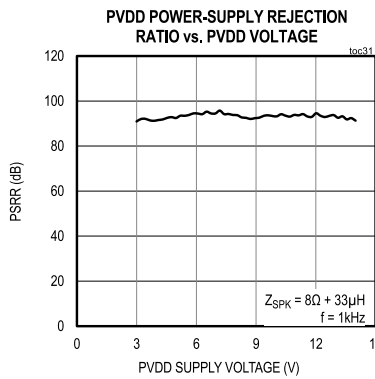
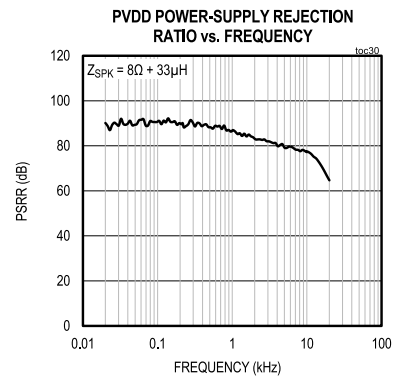
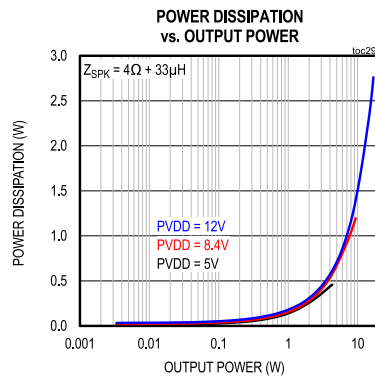
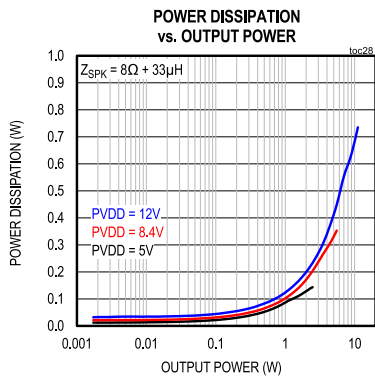
( $V_{PVDD} = 12V$ ,  $V_{DD} = 1.8V$ ,  $V_{GND} = 0V$ ; Gain = 21.5dB,  $Z_{SPK} = \infty$  between OUP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $f_S = 48kHz$ , 24-bit data,  $f_{CLK} = 3.072MHz$ . Typical values are at  $T_A = +25^\circ C$ )





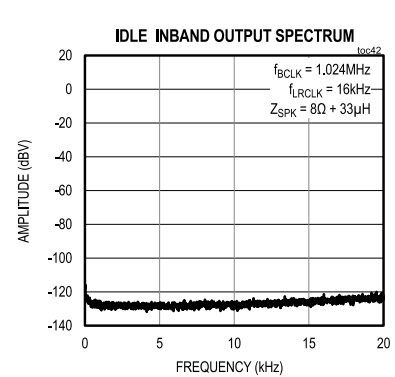
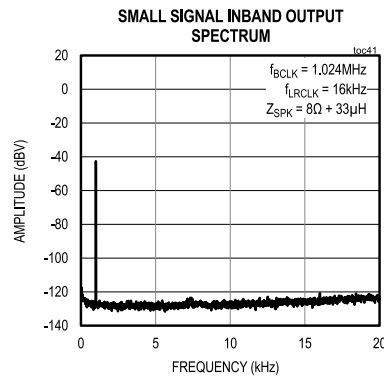
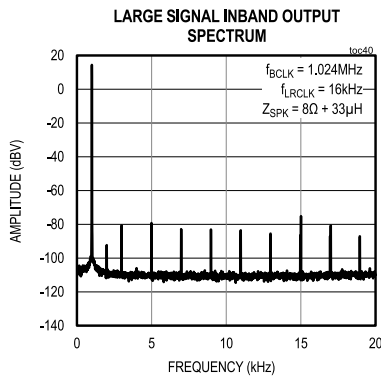
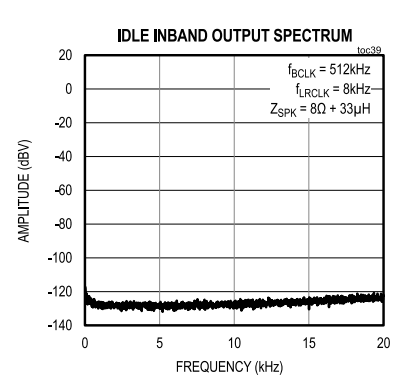
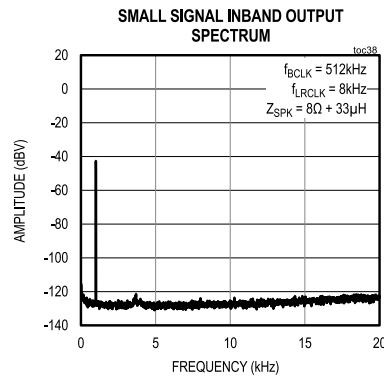
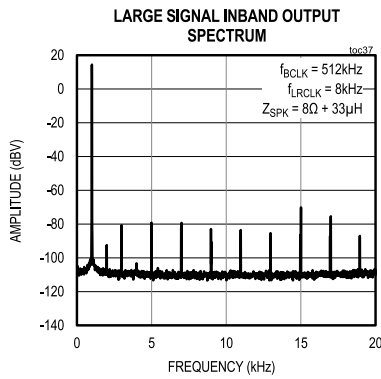
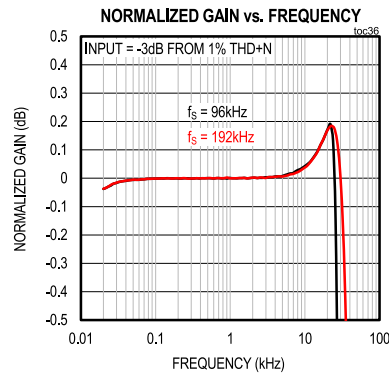
Typical Operating Characteristics (continued)

( $V_{PVDD} = 12V$ ,  $V_{DD} = 1.8V$ ,  $V_{GND} = 0V$ ; Gain = 21.5dB,  $Z_{SPK} = \infty$  between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $f_s = 48kHz$ , 24-bit data,  $f_{BCLK} = 3.072MHz$ . Typical values are at  $T_A = +25^\circ C$ )



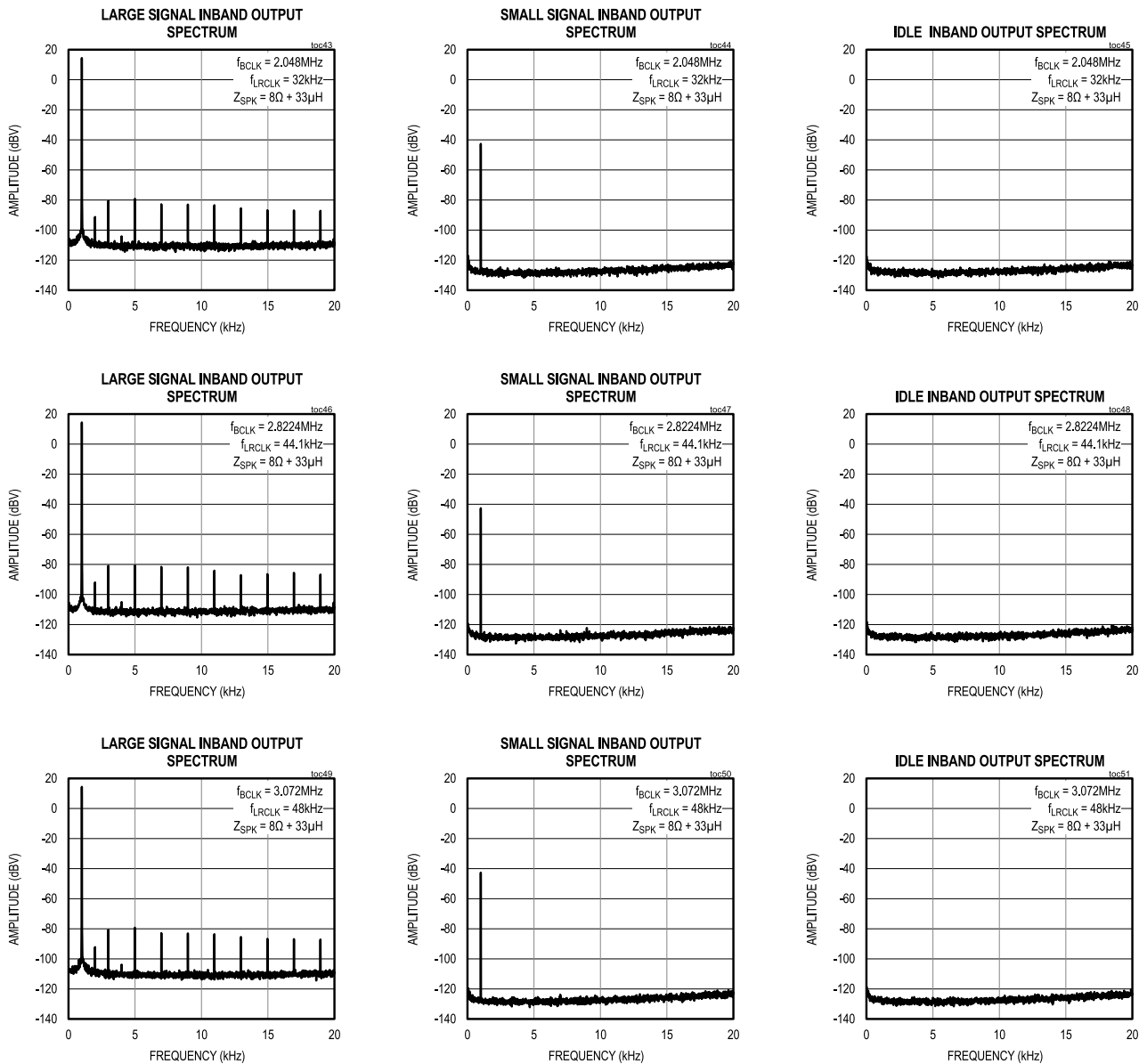
Typical Operating Characteristics (continued)

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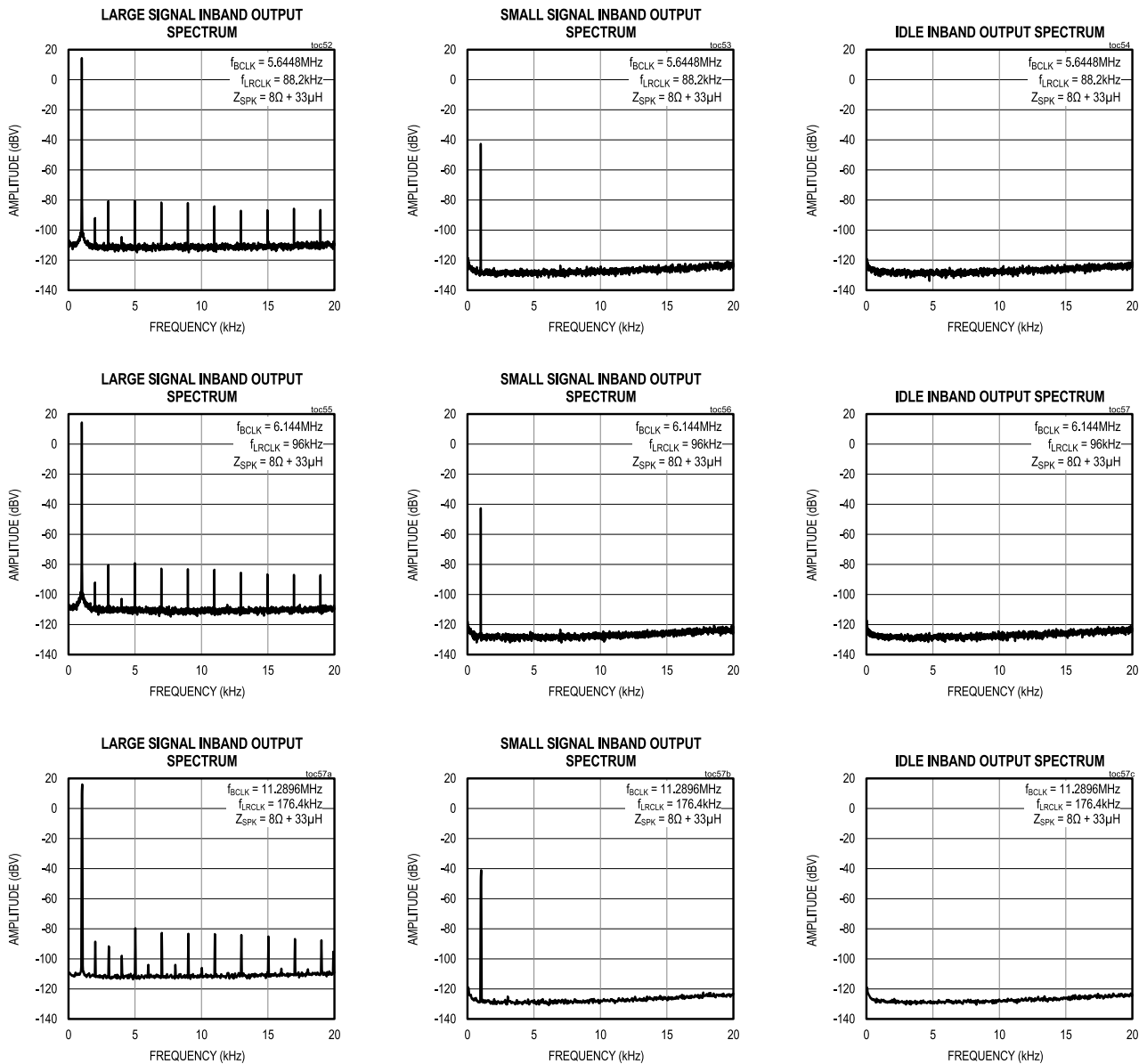
Typical Operating Characteristics (continued)

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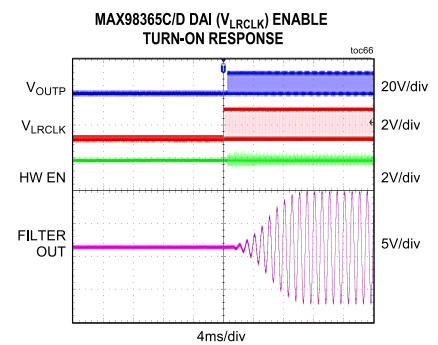
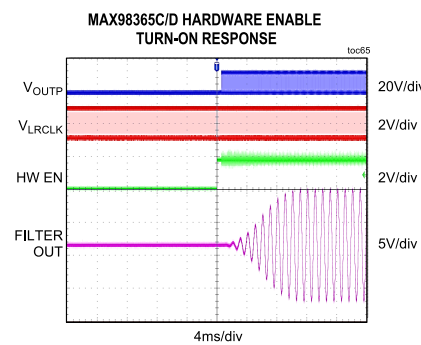
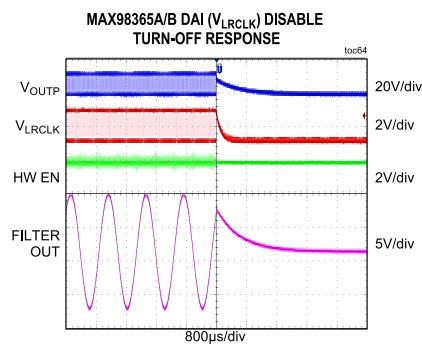
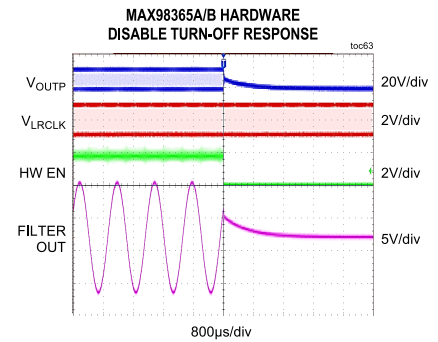
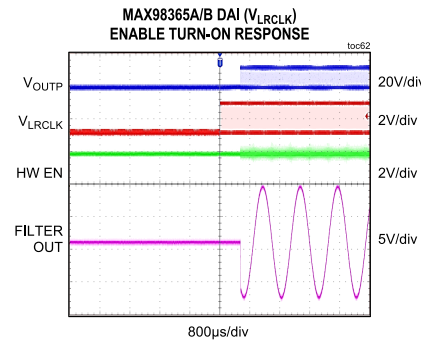
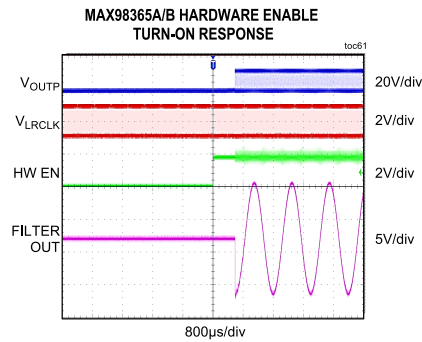
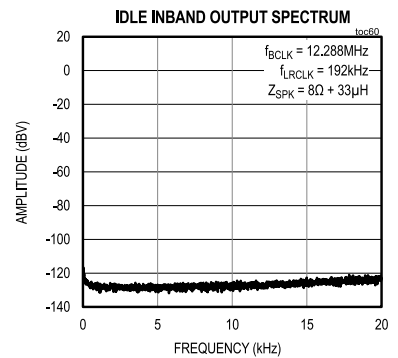
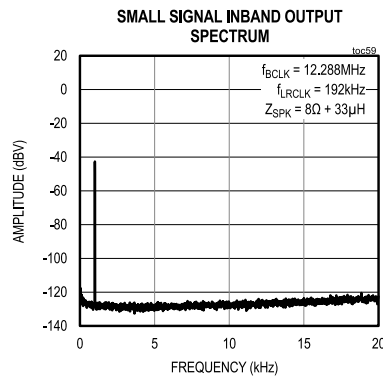
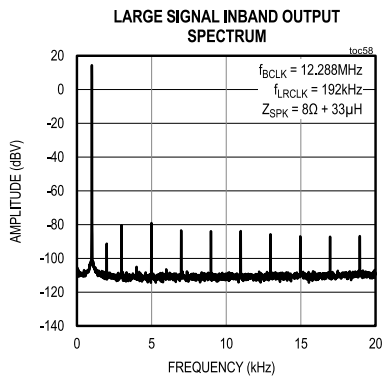
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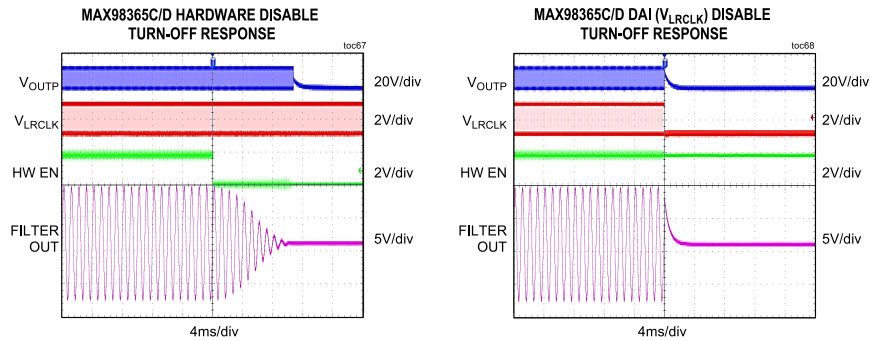
Typical Operating Characteristics (continued)

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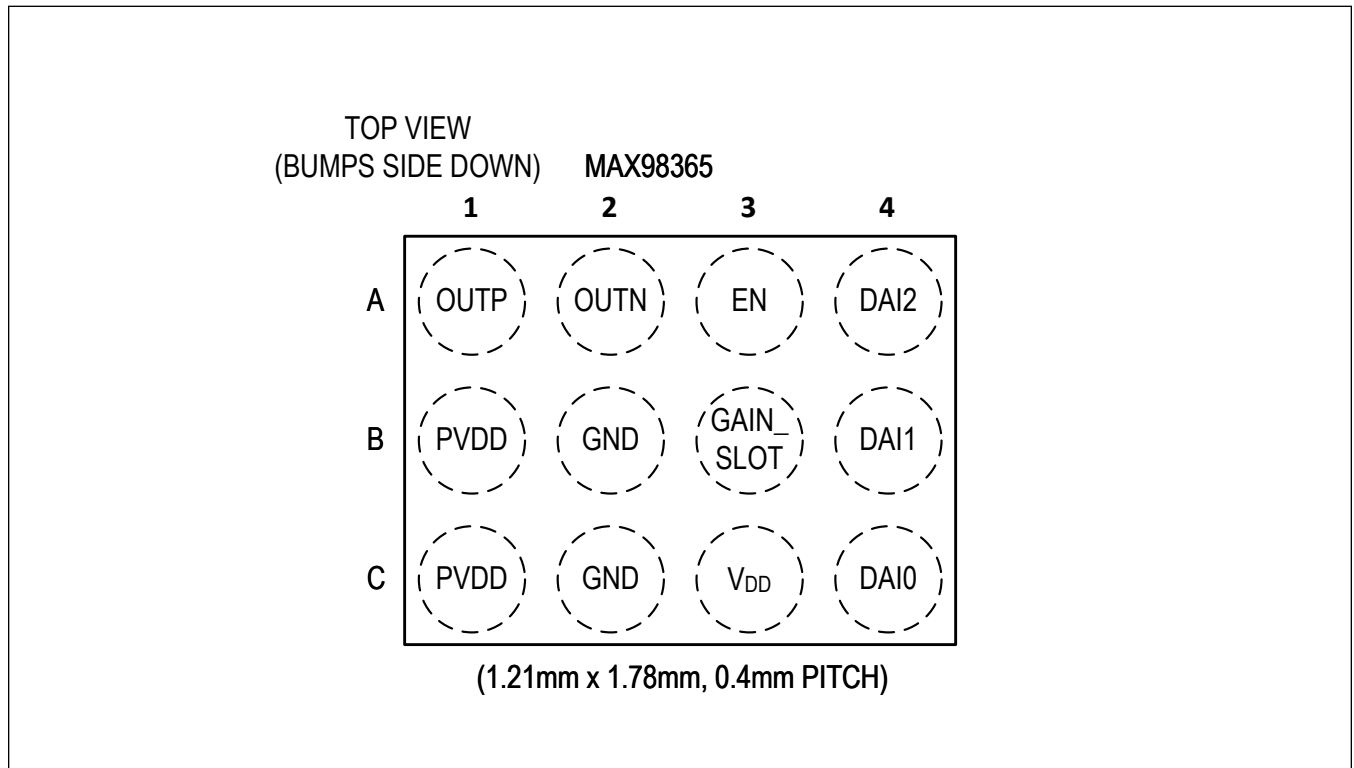
**Typical Operating Characteristics (continued)**

( $V_{PVDD} = 12V$ ,  $V_{DD} = 1.8V$ ,  $V_{GND} = 0V$ ; Gain = 21.5dB,  $Z_{SPK} = \infty$  between OUP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz,  $f_S = 48kHz$ , 24-bit data,  $f_{BCLK} = 3.072MHz$ . Typical values are at  $T_A = +25^\circ C$ )



**Pin Configuration**

**WLP**



## Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A3	EN	Hardware Enable Pin. Pull EN low, to place the the device in Shutdown mode.	—	Digital Input
B1, C1	PVDD	Amplifier Power Supply Input. Bypass to GND with a 1 $\mu$ F and 10 $\mu$ F capacitor placed as close as possible.	—	Supply
C3	V <sub>DD</sub>	Power Supply Input. Bypass to GND with a 1 $\mu$ F capacitor placed as close as possible.	—	Supply
A1	OUP	Positive Class-D Amplifier Output	PVDD	Analog Output
A4	DAI2	Digital Audio Interface Pin 2. Internally pulled down to GND through a 3M $\Omega$ resistor.	—	Digital Input
B3	GAIN_SLOT	Gain and Channel Selection. Determines amplifier output voltage in I <sup>2</sup> S and left-justified modes ( <a href="#">Gain Selection</a> ). Used for channel selection along with DAI Configuration in TDM mode ( <a href="#">Table 8</a> ). In TDM mode, full-scale output voltage is fixed at 21.5dBV.	V <sub>DD</sub>	Digital Input
A2	OUTN	Negative Class-D Amplifier Output	PVDD	Analog Output
C4	DAI0	Digital Audio Interface Pin 0. Internally pulled down to GND through a 3M $\Omega$ resistor.	—	Digital Input
B2, C2	GND	Ground	—	Supply
B4	DAI1	Digital Audio Interface Pin 1. Internally pulled down to GND through a 3M $\Omega$ resistor.	—	Digital Input

## Detailed Description

The MAX98365A/B/C/D are digital PCM input Class-D power amplifiers. When the LRCLK duty cycle is 50%, the MAX98365A and MAX98365C accept standard I<sup>2</sup>S data while the MAX98365B and MAX98365D accept left-justified data. When LRCLK is a frame sync pulse (LRCLK is high for 3 BCLK periods or less), the device accepts 16-bit or 32-bit TDM data with eight channels. The digital audio interface eliminates the need for an external MCLK signal that is typically required for I<sup>2</sup>S data transmission.

The MAX98365A and MAX98365B have a fast 1ms turn-on time. The MAX98365C and MAX98365D ramp the audio volume over 13ms upon EN going high or low.

**Table 1. MAX98365 Versions**

	TURN-ON AND TURN-OFF VOLUME RAMP	TURN-ON TIME (ms)	DATA FORMAT WHEN LRCLK DUTY CYCLE IS 50%	DATA FORMAT WHEN LRCLK IS A SYNC PULSE
<b>MAX98365A</b>	Disabled	1	I <sup>2</sup> S data valid on BCLK rising edge	TDM data valid on BCLK rising edge
<b>MAX98365B</b>	Disabled	1	Left-justified data valid on BCLK rising edge	TDM data valid on BCLK falling edge
<b>MAX98365C</b>	Enabled	13	I <sup>2</sup> S data valid on BCLK rising edge	TDM data valid on BCLK rising edge
<b>MAX98365D</b>	Enabled	13	Left-justified data valid on BCLK rising edge	TDM data valid on BCLK falling edge

Gain and channel selection are configured by a combination of GAIN\_SLOT pin settings and connecting digital audio source signals to different DAI<sub>n</sub> pins.

The MAX98365A/B/C/D features low quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The amplifier offers Class-AB audio performance with Class-D efficiency in a minimal board-space solution. The Class-D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients during turn-on and turn-off. The amplifier includes thermal-overload and short-circuit protection.

## EN and Shutdown Mode

The device features a low-power shutdown mode, drawing I<sub>SHDN</sub> current. During shutdown, all internal blocks are turned off including setting the amplifier output stage to a Hi-Z state. Drive EN low to put the device into shutdown.

The device exits the shutdown mode when the EN pin is asserted high and transitions into UVLO mode.

## Standby Mode

When the PVDD and V<sub>DD</sub> supplies are above their respective UVLO thresholds and EN pin is high and there is no toggling on the DAI<sub>n</sub> pins, the device automatically enters Standby mode. In Standby mode, the Class-D amplifier is off and the outputs are in a Hi-Z state. Standby mode has reduced current consumption from normal operation (I<sub>STNDBY</sub>), but not as low as full shutdown when the EN pin is low (I<sub>SHDN</sub>). Standby mode can be used to reduce power consumption when no host GPIO is available to control the EN pin.

Note that volume is not ramped down when entering standby. For optimal click-and-pop performance on MAX98365A and MAX98365B, ramp down the digital audio amplitude on data presented to DIN before removing clocks. For optimal click-and-pop performance on MAX98365C and MAX98365D, either ramp down the digital audio amplitude on data presented to DIN before removing clocks or keep clocks valid for at least 13ms after pulling EN low to allow time for turn-off volume ramping.

While in standby, any toggling of the DAI<sub>n</sub> pins causes the part to exit Standby mode and enter DAI Configuration.



### Digital Audio Interface (DAI) Configuration (Patent Pending)

Different operating modes can be selected by connecting the digital audio bit clock (BCLK), the digital audio frame clock (LRCLK), and the digital audio data (DIN) to different DAI pins.

The DAI detects BCLK by monitoring the switching frequencies at the DAI pins. Detection starts when EN is toggled from low to high, when  $V_{DD}$  rises from UVLO to operating range while EN is held high, and when exiting Standby mode by applying clocks. The DAI pin with the highest frequency is selected as the BCLK input. Once the BCLK input pin is identified, the LRCLK and DIN pin locations are assumed, as shown in [Table 2](#).

If the clocks are valid for four consecutive LRCLK periods, the DAI Configuration is latched and the amplifier turn on sequence is allowed to proceed. Otherwise, if there is still toggling on the DAI pins, the detection routine is restarted; if there is no toggling on the DAI pins, the device enters Standby mode.

Once a DAI Configuration has been latched, it does not change unless EN is toggled,  $V_{DD}$  falls below  $V_{UVLO}$ , DAI Configuration restarts due to invalid clocks, or the DAI pins stop toggling and the part goes into Standby mode. Shutdowns due to thermal protection or Class-D Current Limit do not trigger a new round of BCLK detection.

While the amplifier is on, clock validity is continually checked. If clocks become invalid, the Class-D amplifier is immediately turned off (no volume ramping) and the outputs go into a Hi-Z state. If there is still toggling on the DAI pins, the detection routine is restarted; if there is no toggling on the DAI pins, the device enters Standby mode.

DAI Configurations other than those shown in [Table 2](#) are not valid.

**Table 2. DAI Configurations**

DAI CONFIGURATION	BCLK CONNECTION	LRCLK CONNECTION	DIN CONNECTION
A	DAI0	DAI1	DAI2
B	DAI1	DAI2	DAI0
C	DAI2	DAI0	DAI1

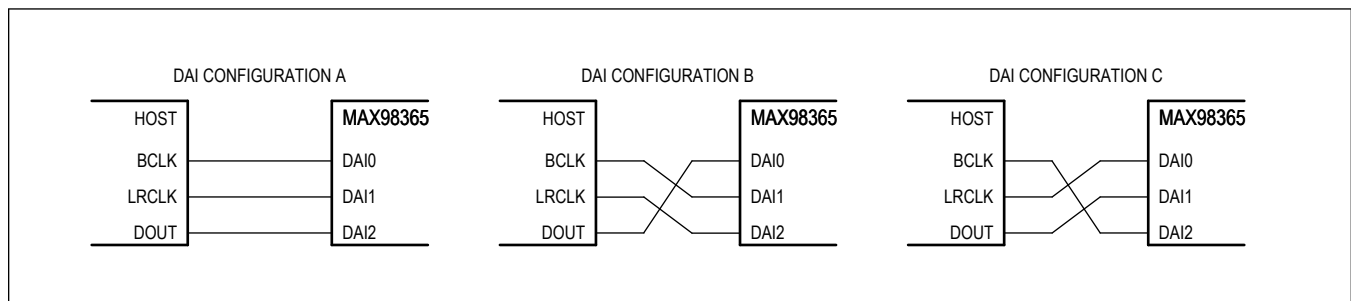


Figure 1. DAI Connections

### Valid Clock Frequencies

When LRCLK has a 50% duty cycle, MAX98365A and MAX98365C are automatically configured for I<sup>2</sup>S mode, while MAX98365B and MAX98365D are automatically configured for left-justified mode. When a frame sync pulse is used for LRCLK (LRCLK is high for 3 BCLK periods or less), the device is automatically configured for TDM mode.

Valid sample rates are 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz. (LRCLK clocks at 11.025kHz, 12kHz, 22.05kHz and 24kHz are **NOT** supported.)

In I<sup>2</sup>S/left-justified mode, valid resolutions are 16-, 24-, and 32-bits per channel. There are 2 channels per LRCLK period. Therefore, the valid numbers of BCLK periods per LRCLK period in I<sup>2</sup>S/left-justified mode are exactly 32 BCLK periods per LRCLK period, 48 BCLK periods per LRCLK period, and 64 BCLK periods per LRCLK period.

In TDM mode, valid resolutions are 16-bits per channel and 32-bits per channel. The valid numbers of BCLK periods per LRCLK period in TDM mode are 125, 128, 250, and 256, so there are 8 channels per LRCLK period when the BCLK periods per LRCLK period is 128 or 256. When there are 125 or 250 BCLK periods per LRCLK period, there are 7 channels per LRCLK period.

An invalid number of BCLKs per LRCLK other than those shown in [Table 3](#) results in an unpredictable output waveform.

**Table 3. Valid Resolutions and Frame Widths**

SAMPLE RESOLUTION (BITS)	BCLK PERIODS PER LRCLK IN I <sup>2</sup> S/LEFT-JUSTIFIED MODE	BCLK PERIODS PER LRCLK IN TDM MODE
16	32	125, 128
24	48	NOT VALID
32	64	250, 256

**Table 4. Valid BCLK Frequencies (kHz)**

	I <sup>2</sup> S/LEFT-JUSTIFIED MODE			TDM MODE			
	32 BCLKs PER LRCLK	48 BCLKs PER LRCLK	64 BCLKs PER LRCLK	125 BCLKs PER LRCLK	128 BCLKs PER LRCLK	250 BCLKs PER LRCLK	256 BCLKs PER LRCLK
LRCLK = 8kHz	256	384	512	N/A	1024	N/A	2048
LRCLK = 16kHz	512	768	1024	N/A	2048	N/A	4096
LRCLK = 32kHz	1024	1536	2048	N/A	4096	N/A	8192
LRCLK = 44.1kHz	1411.2	2116.8	2822.4	N/A	5644.8	N/A	11289.6
LRCLK = 48kHz	1536	2304	3072	6000	6144	12000	12288
LRCLK = 88.2kHz	2822.4	4233.6	5644.8	N/A	11289.6	N/A	22579.2
LRCLK = 96kHz	3072	4608	6144	12000	12288	24000	24576
LRCLK = 176.4kHz	5644.8	8467.2	11289.6	22579.2	N/A	N/A	N/A
LRCLK = 192kHz	6144	9216	12288	24000	24576	N/A	N/A

### MCLK Elimination

The MAX98365 eliminates the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin-count.

### BCLK Jitter Tolerance

The MAX98365 features a high BCLK jitter tolerance while maintaining a high dynamic range (see the [Electrical Characteristics](#) table).

### BCLK Polarity

In I<sup>2</sup>S and left-justified mode, incoming serial data is always clocked-in on the rising-edge of BCLK. In TDM mode, the MAX98365A and MAX98365C clock-in serial data on the rising edge of BCLK while the MAX98365B and MAX98365D clock in serial data on the falling edge of BCLK ([Table 5](#)).

**Table 5. BCLK Polarity**

MODE	PART NUMBERS	BCLK POLARITY
I <sup>2</sup> S	MAX98365A/C	Rising edge
Left-justified	MAX98365B/D	Rising edge
TDM	MAX98365A/C	Rising edge

**Table 5. BCLK Polarity (continued)**

MODE	PART NUMBERS	BCLK POLARITY
TDM	MAX98365B/D	Falling edge

**LRCLK Polarity in I<sup>2</sup>S/Left-Justified Mode**

In I<sup>2</sup>S and left-justified mode, LRCLK specifies whether left-channel data or right-channel data is currently being read by the digital audio interface. The MAX98365A and MAX98365C indicate the left-channel word when LRCLK is low, and the MAX98365B and MAX98365D indicate the left-channel word when LRCLK is high ([Table 6](#)).

**Table 6. LRCLK Polarity in I<sup>2</sup>S/Left-Justified Mode**

PART NUMBER	LRCLK POLARITY (LEFT CHANNEL)
MAX98365A/C	Low
MAX98365B/D	High

**I<sup>2</sup>S and Left-Justified Mode**

When the LRCLK duty cycle is 50%, the MAX98365A and MAX98365C follow standard I<sup>2</sup>S timing by allowing a delay of one BCLK cycle after the LRCLK transition before the beginning of a new data word ([Figure 2](#) and [Figure 3](#)). The MAX98365B and MAX98365D follow the left-justified timing specification by aligning the LRCLK transitions with the beginning of a new data word ([Figure 4](#) and [Figure 5](#)).

In I<sup>2</sup>S and left-justified modes, the audio channel that is sent to the amplifier output is chosen by the DAI Configuration (see [Table 2](#)). Use DAI Configuration A to select the left word of the stereo input data. Use DAI Configuration B to select the right word of the stereo input data. Use DAI Configuration C to select both the left and right words of the stereo input data (left/2 + right/2).

**Table 7. Channel Selection in I<sup>2</sup>S and Left-Justified Modes**

DAI CONFIGURATION	CHANNEL
A	Left
B	Right
C	Left/2 + Right/2

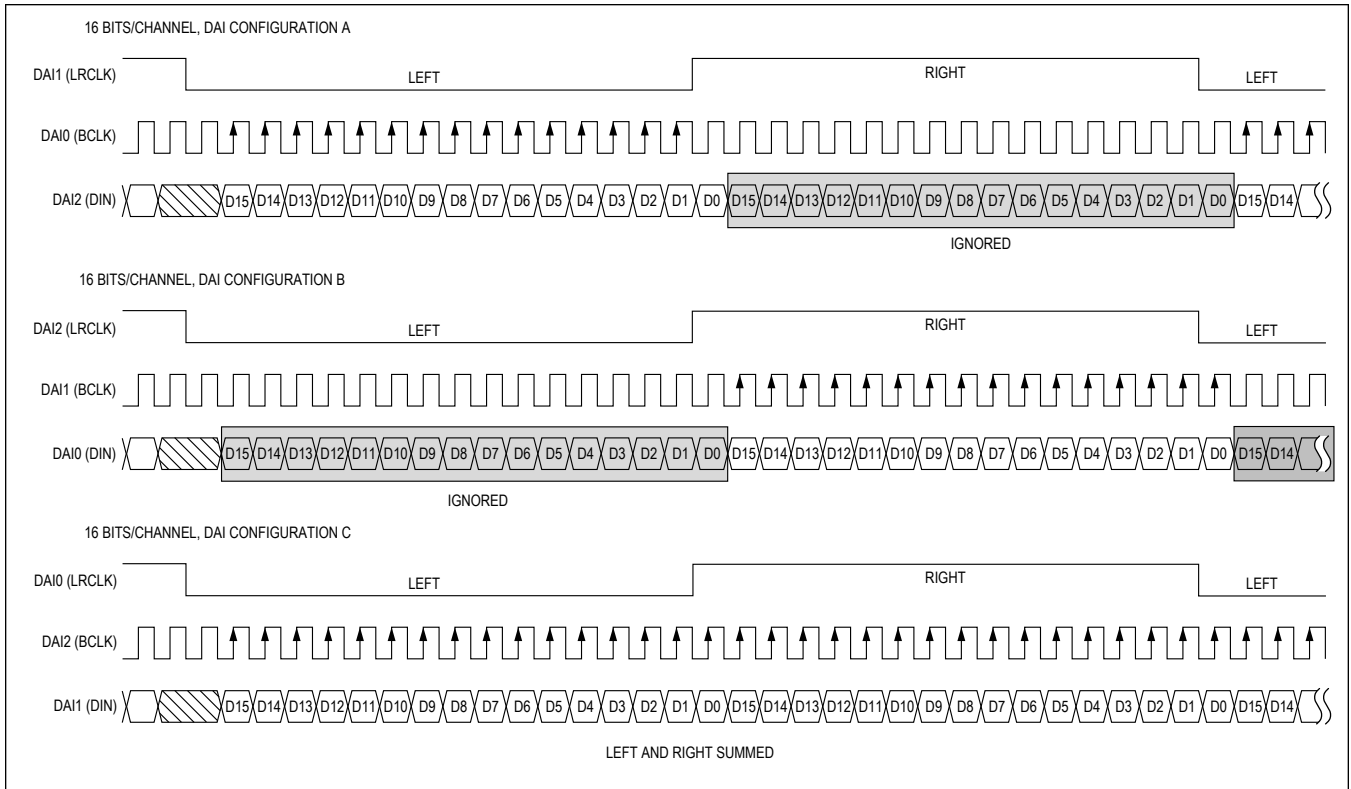


Figure 2. MAX98365A and MAX98365C I<sup>2</sup>S Protocol, 16-Bit Resolution

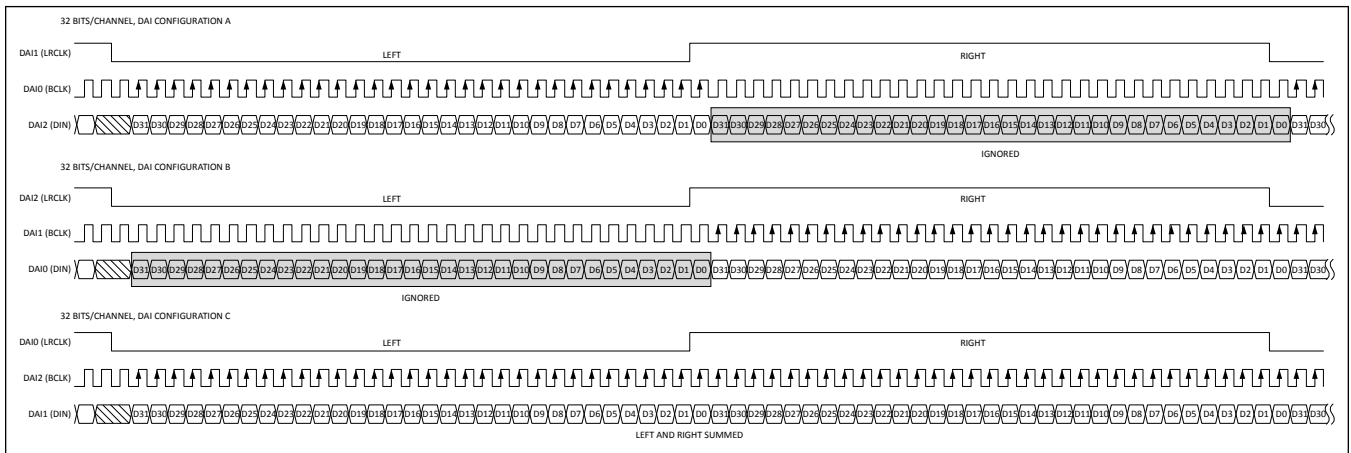


Figure 3. MAX98365A and MAX98365C I<sup>2</sup>S Protocol, 32-Bit Resolution

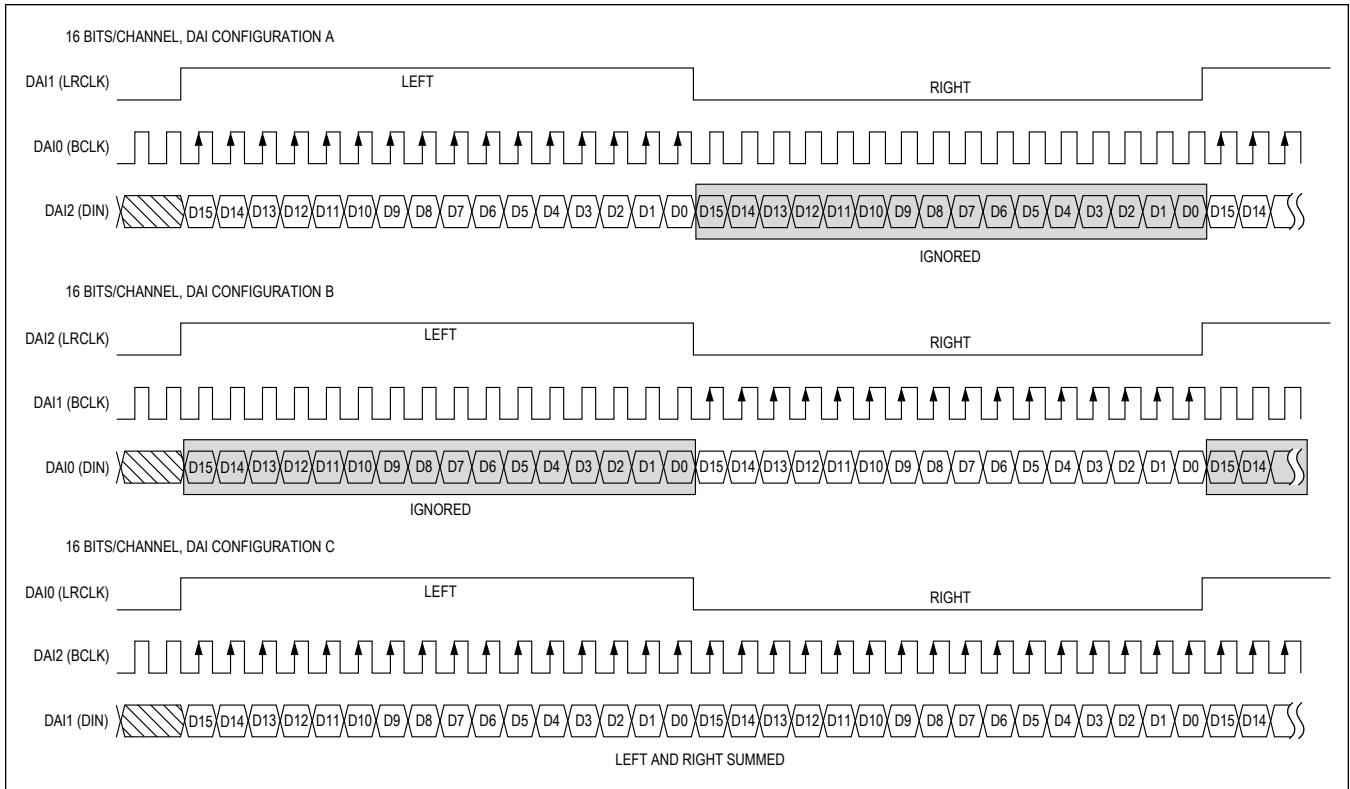


Figure 4. MAX98365B and MAX98365D Left-Justified Protocol, 16-Bit Resolution

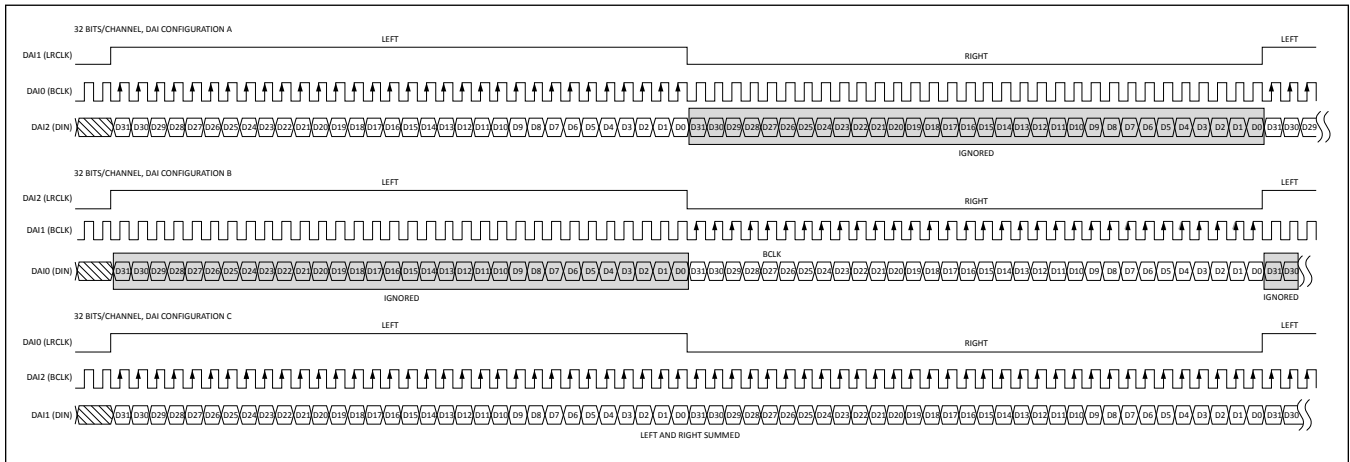


Figure 5. MAX98365B and MAX98365D Left-Justified Protocol, 32-Bit Resolution

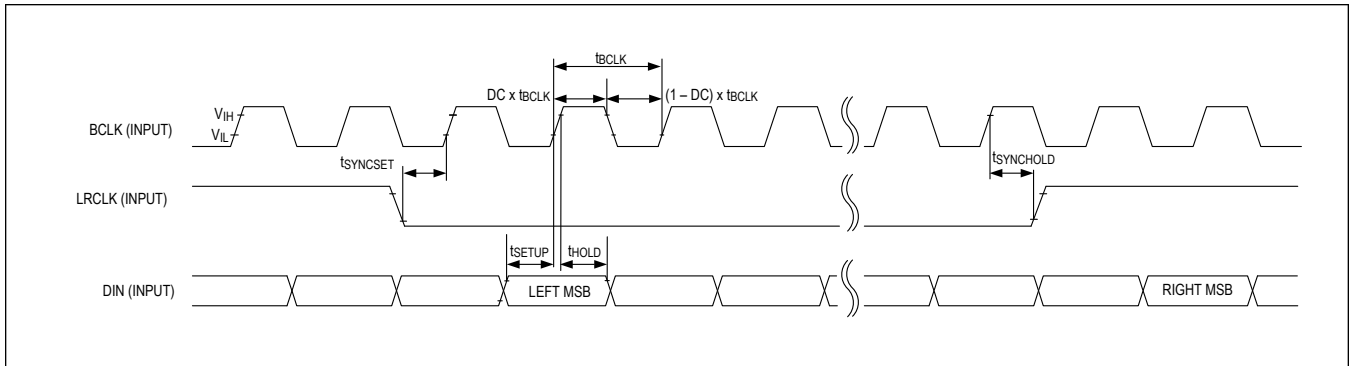


Figure 6. I<sup>2</sup>S Timing Diagram (MAX98365A and MAX98365C)

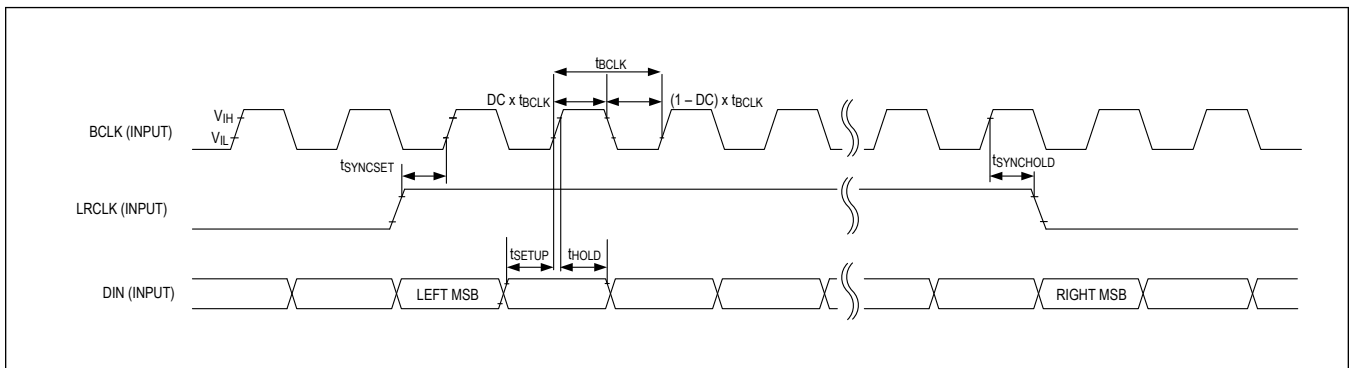


Figure 7. Left-Justified Timing Diagram (MAX98365B and MAX98365D)

**TDM Mode**

When a frame sync pulse is used for LRCLK (LRCLK is high for 3 BCLK periods or less), the device is automatically configured for TDM mode.

In TDM mode, the device accepts 7 or 8 channels of 16-bit or 32-bit formatted data. When there are 125 (16-bit mode) or 250 (32-bit mode) BCLK cycles per frame, the device accepts 7 channels. When BCLK cycles per frame is 128 (16-bit mode) or 256 (32-bit mode), the device accepts 8 channels of data.

DAI Configuration and GAIN\_SLOT are used to select which channel is sent to the amplifier (see [Table 8](#) and [Table 2](#)).

On the MAX98365A and MAX98365C, data is valid on the BCLK rising edge (see [Figure 8](#) and [Figure 9](#)). On the MAX98365B and MAX98365D, data is valid on the BCLK falling edge (see [Figure 10](#) and [Figure 11](#)).

**Table 8. TDM Mode Channel Selection**

CHANNEL SELECTION	DAI CONFIGURATION	GAIN_SLOT CONNECTION
0	A	GND
1	A	V <sub>DD</sub>
2	A	Unconnected
3	B	V <sub>DD</sub>
4	B	GND
5	C	GND
6	C	Unconnected
7	C	V <sub>DD</sub>

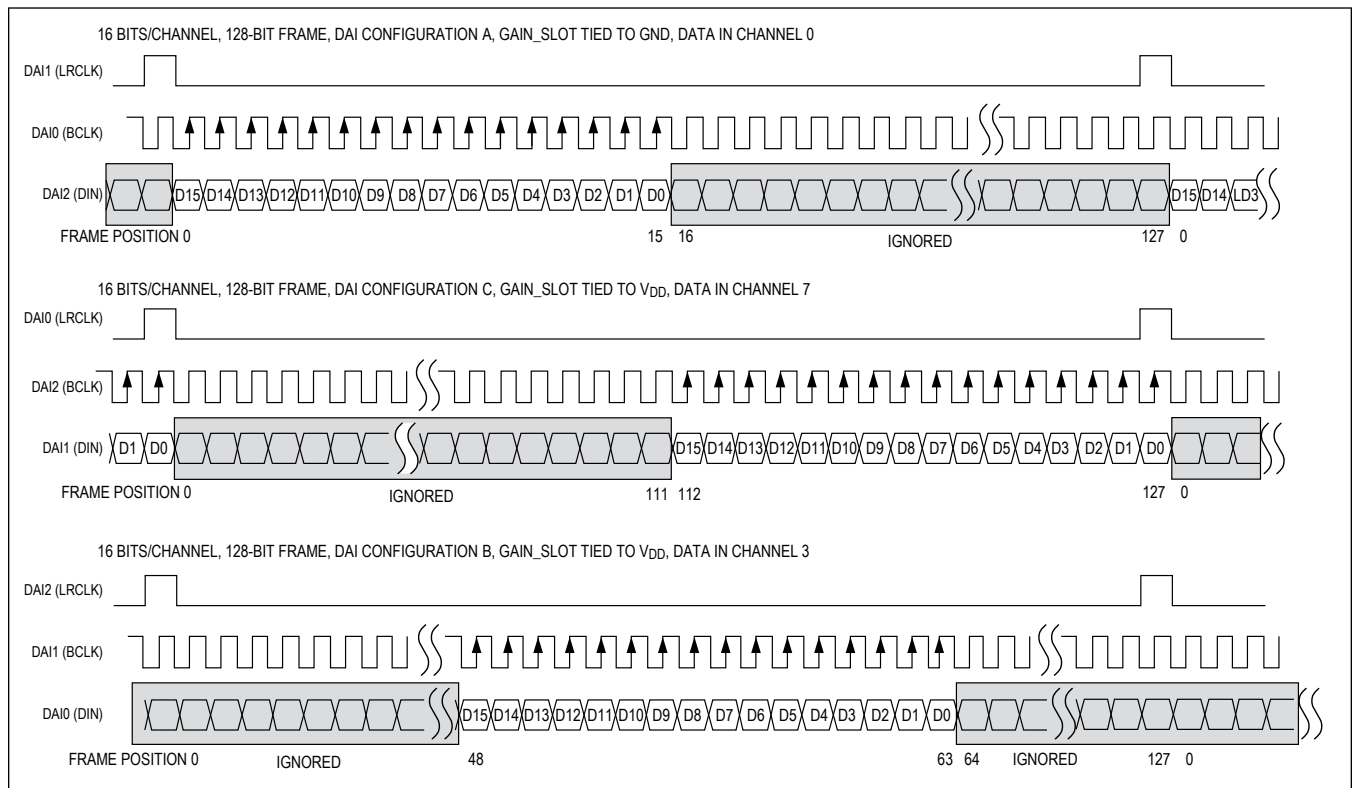


Figure 8. MAX98365A and MAX98365C TDM Protocol, 16-Bit Resolution

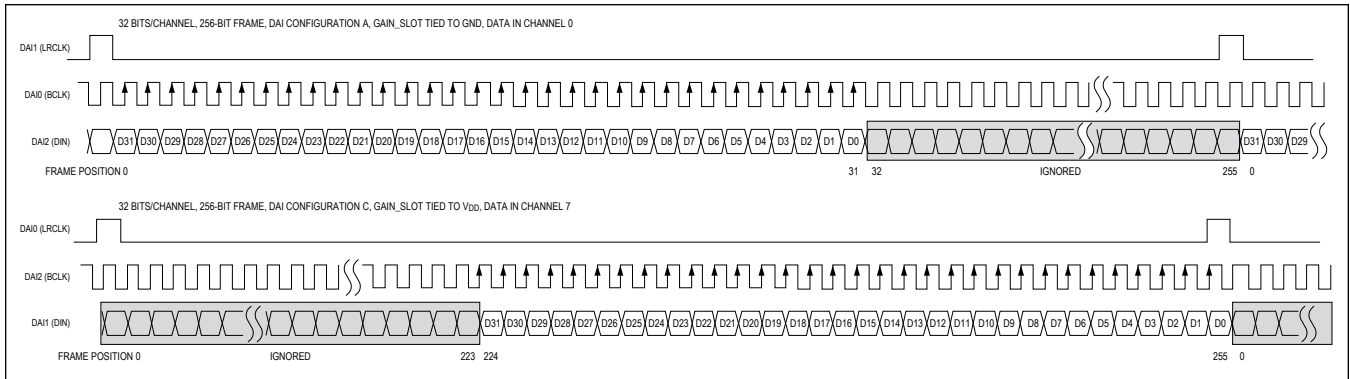


Figure 9. MAX98365A and MAX98365C TDM Protocol, 32-Bit Resolution

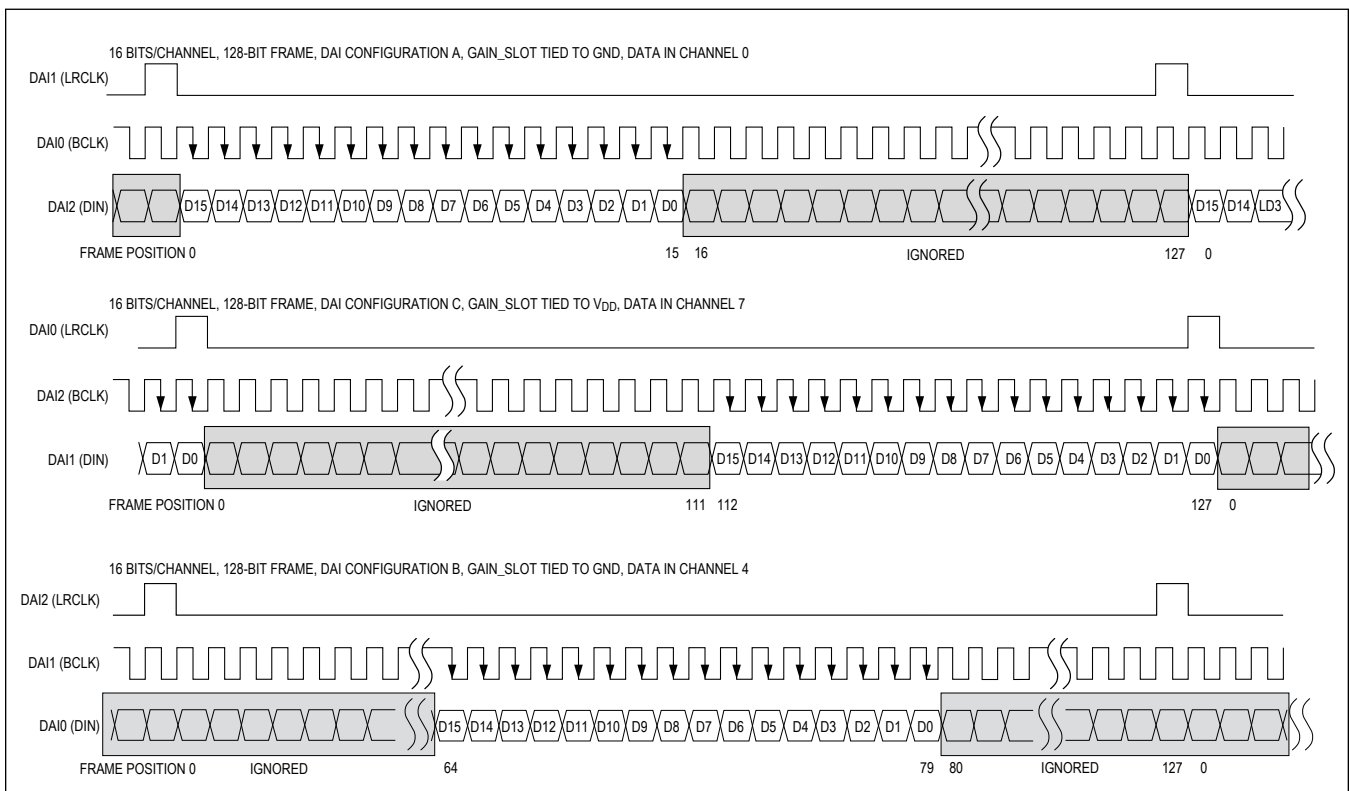


Figure 10. MAX98365B and MAX98365D TDM Protocol, 16-Bit Resolution



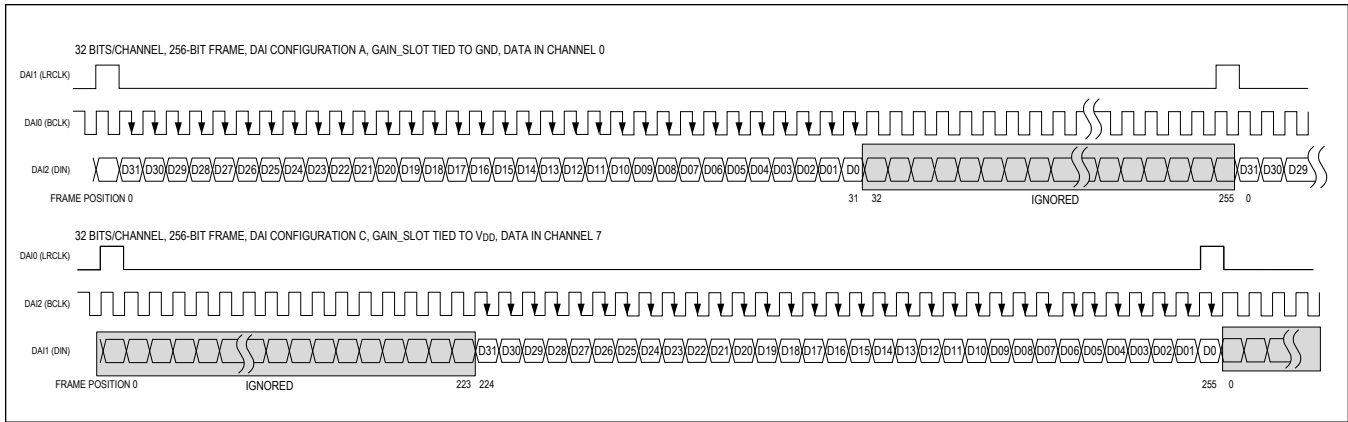


Figure 11. MAX98365B and MAX98365D TDM Protocol, 32-Bit Resolution

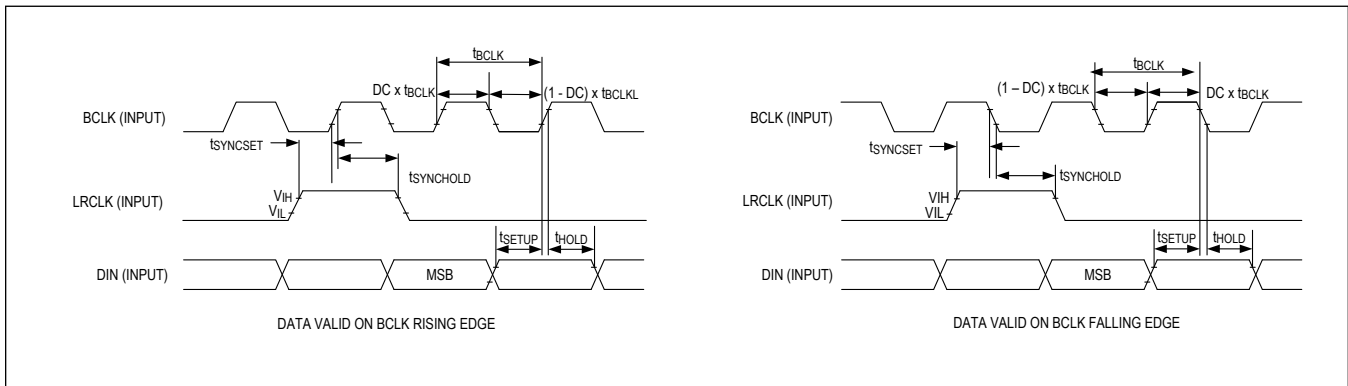


Figure 12. TDM Timing Diagrams—BCLK Rising Edge (MAX98365A/C) and BCLK Falling Edge (MAX98365B/D)

**Gain Selection**

In I<sup>2</sup>S and left-justified modes, use the information in [Table 9](#) to connect the GAIN\_SLOT pin for the desired maximum output voltage level (dBV). In TDM mode, the gain is automatically set at a fixed output voltage level of 21.5dBV.

**Table 9. Gain Selection for I<sup>2</sup>S/Left-Justified Mode**

FULL SCALE OUTPUT VOLTAGE LEVEL (dBV)	GAIN_SLOT CONNECTION
21.5	Connect to GND
18.5	Unconnected
15.5	Connect to V <sub>DD</sub>
12.5	Connect to V <sub>DD</sub> through 100kΩ ±5% resistor
9.5	Connect to GND through 100kΩ ±5% resistor

**DC Blocking Filter**

The digital audio interface includes a DC blocking filter with a -3dB cutoff at f<sub>c</sub> (see the [Electrical Characteristics](#) table).

**DAC Digital Filters**

The DAC features a digital lowpass filter that is automatically configured based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. See the [DAC Digital Filters](#) section of the [Electrical Characteristics](#) table.

### Class-D Amplifier

The filterless Class-D amplifier offers much higher efficiency than Class-AB amplifiers. The high efficiency of a Class-D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class-D output stage is mostly due to the  $I^2R$  loss of the MOSFET on-resistance and quiescent current overhead.

### Class-D Output Short-Circuit Protection

If the output current limit of the Class-D amplifier ( $I_{LIM}$ ) is exceeded (see the [Electrical Characteristics](#) table), the outputs are disabled for approximately 27ms. At the end of the 27ms, the outputs are re-enabled. If the fault condition still exists, the outputs continue to disable and reenable until the fault condition is removed.

### Turn-On and Turn-Off Volume Ramping

The MAX98365A and MAX98365B have a fast 1ms turn-on time. For optimal click-and-pop performance, ramp down the digital audio amplitude on data presented to DIN before shutting down, removing clocks, or removing power.

The MAX98365C and MAX98365D ramp the audio signal from mute to full-scale over 13ms after DAI Configuration. When turned off by pulling EN low, gain is ramped down to mute over 13ms. Turn-off ramping only occurs if BCLK and LRCLK remain valid and  $V_{PVDD}$  and  $V_{DD}$  supplies remain within their operating ranges for at least 13ms after EN goes low. If either clock becomes invalid or if  $V_{PVDD}$  or  $V_{DD}$  falls below their respective UVLO thresholds, audio stops immediately without ramping.

### Click-and-Pop Suppression

The speaker amplifier features Analog Devices' comprehensive click-and-pop suppression. During turn-on, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. When entering shutdown or standby, the differential speaker outputs simultaneously go to Hi-Z.

The comprehensive click-and-pop suppression of the MAX98365 is unaffected by power-up or power-down sequencing. Applying or removing the clocks before or after the transition of EN yields the same click-and-pop performance. However, note that for MAX98365C and MAX98365D clocks and  $V_{DD}$  must remain valid for 13ms after EN goes low to allow for volume ramping to complete for best click-and-pop performance.

### Ultra-Low EMI Filterless Output Stage

Traditional Class-D amplifiers require the use of external LC filters or shielding to meet EN55022B electromagnetic interference (EMI) regulation standards. Analog Devices' active emissions-limiting, edge-rate control circuitry, and spread-spectrum modulation reduce EMI emissions while maintaining high efficiency.

Analog Devices' spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The device's spread-spectrum modulator randomly varies the switching frequency by  $f_{SSM}$  around the center frequency ( $f_{SW}$ ). Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

## Applications Information

### Filterless Class-D Operation

Traditional Class-D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, size, and decreases efficiency and THD+N performance. The amplifier's filterless modulation scheme does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output.

Because the switching frequency of the amplifier is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance  $> 10\mu\text{H}$ . Typical  $8\Omega$  speakers exhibit series inductances in the  $20\mu\text{H}$  to  $100\mu\text{H}$  range.

### Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

For best EMI and audio performance, it is essential that the  $V_{\text{PVDD}}$  decoupling capacitor be placed as close as possible to the MAX98365 to minimize the supply loop inductance.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a  $4\Omega$  load through  $100\text{m}\Omega$  of total speaker trace, 1.95W is being delivered to the speaker. If power is delivered through  $10\text{m}\Omega$  of total speaker trace, 1.99W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

Parasitic capacitance on the output traces cause higher quiescent current by  $V_{\text{PVDD}} \times f_{\text{SW}} \times C_{\text{PARASITIC}}$ . For example, at  $V_{\text{PVDD}} = 12\text{V}$  and a total parasitic capacitance of  $100\text{pF}$  ( $50\text{pF}$  on each output trace), the increase in quiescent current is  $12\text{V} \times 300\text{kHz} \times 100\text{pF} = 360\mu\text{A}$ .

The device is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

In many applications, only three capacitors are required, which results in a small solution size of  $7.84\text{mm}^2$ .



Figure 13. Solution Size

### WLP GAIN\_SLOT Routing

The intended use for the GAIN\_SLOT pin is to either fix the desired gain in I<sup>2</sup>S and left-justified modes or to select the channel in TDM mode. GAIN\_SLOT should not be changed during audio playback as it could result in audible clicks or pops.

Most modes are selectable without using a via or routing out the center bump of the WLP. This simplifies the layout and allows for inexpensive PCB fabrication.

In I<sup>2</sup>S and left-justified modes, 15.5dBV, 18.5dBV, and 21.5dBV gain settings do not require GAIN\_SLOT to be routed out (see [Gain Selection](#)). In TDM mode, all channels can be selected without routing out GAIN\_SLOT (see [Table 8](#)). This is possible because of the GAIN\_SLOT pin's placement in relation to the V<sub>DD</sub> and GND pins.

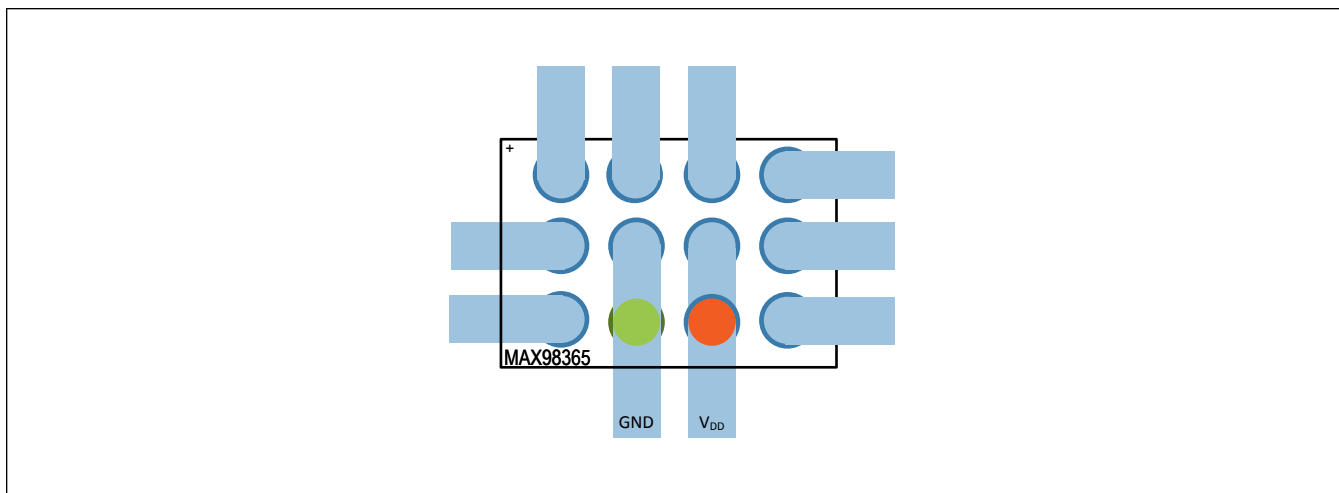


Figure 14. GAIN\_SLOT Connected to  $V_{DD}$  (Output is 15.5dBV in  $I^2S$  and Left-Justified Modes)

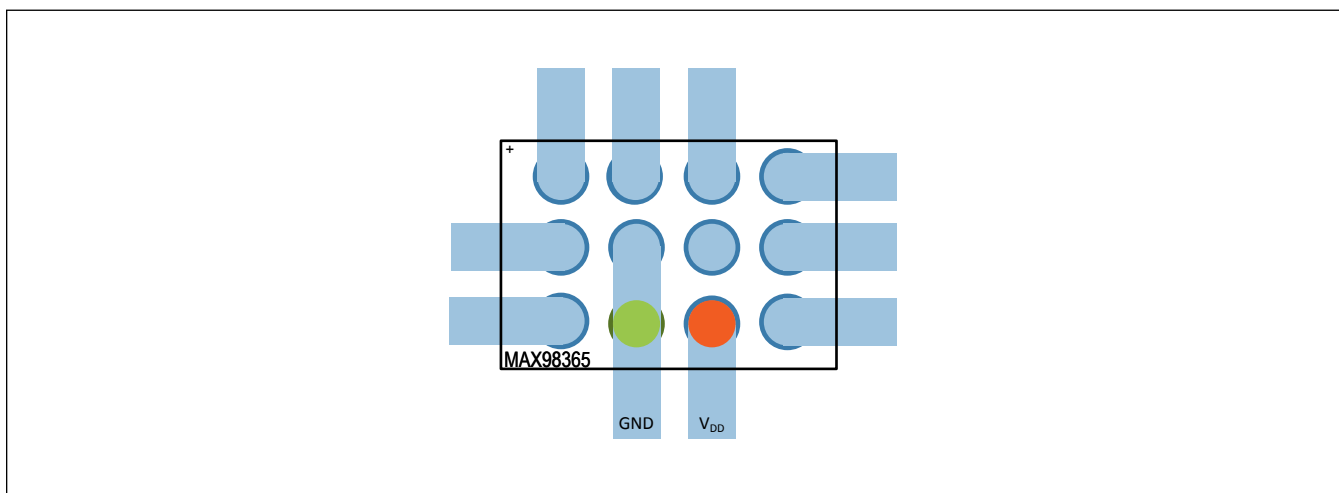


Figure 15. GAIN\_SLOT Unconnected (Output is 18.5dBV in  $I^2S$  and Left-Justified Modes)

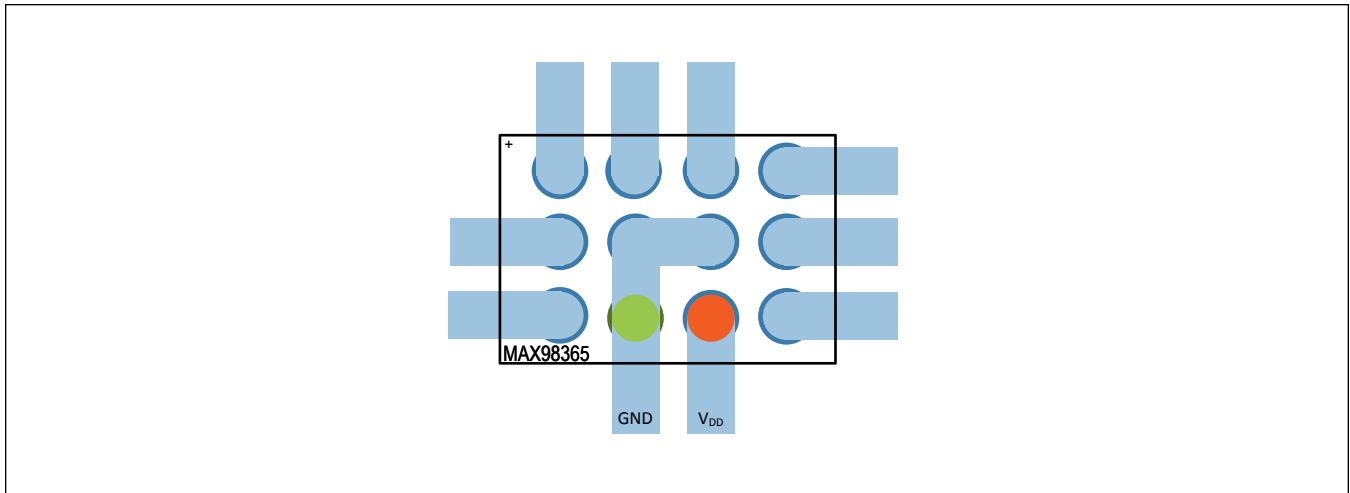


Figure 16. GAIN\_SLOT Connected to GND (Output is 21.5dBV in I<sup>2</sup>S and Left-Justified Modes)

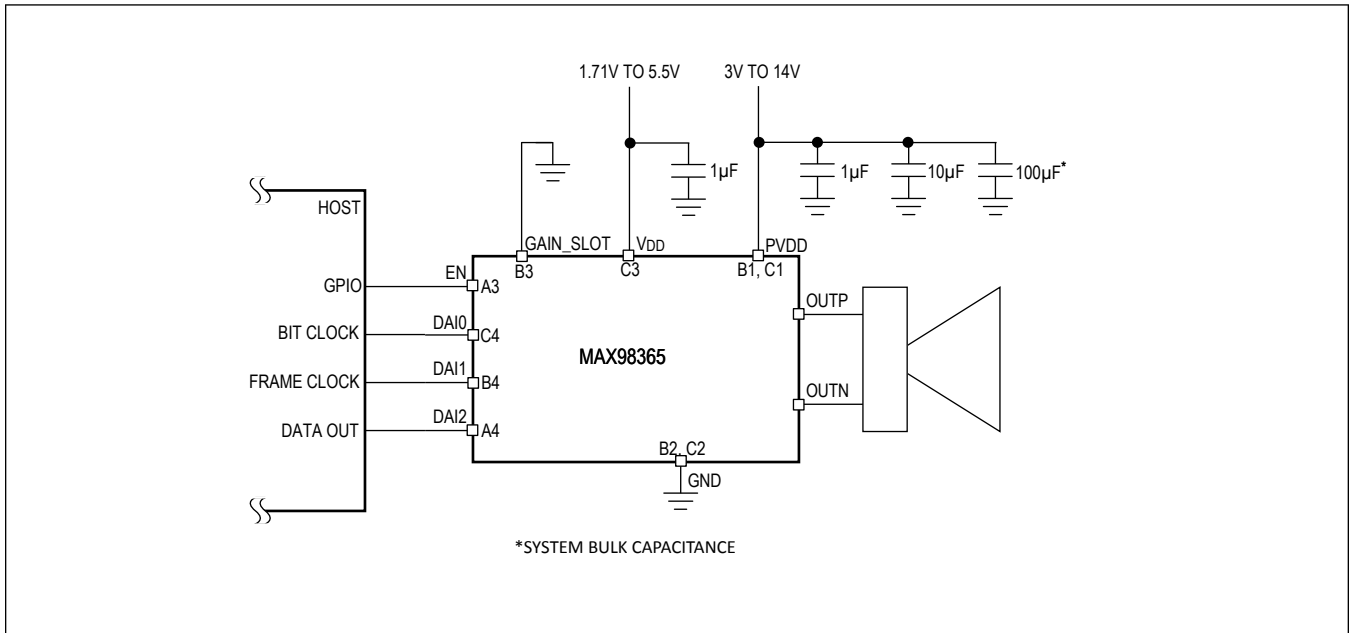
If using I<sup>2</sup>S or left-justified modes and a 12.5dBV or 9.5dBV gain setting is required, the GAIN\_SLOT pin must be routed to a 100k $\Omega$  resistor that is connected to either V<sub>DD</sub> or GND (See [Gain Selection](#)). Some routing options are:

- Mechanically drilled via: cheaper if PCB volumes are low
- Laser-drilled alternative: cheaper if PCB volumes are high
- Blind and buried vias with dog-boning
- Trace on the top layer: this must be a minimal pitch trace

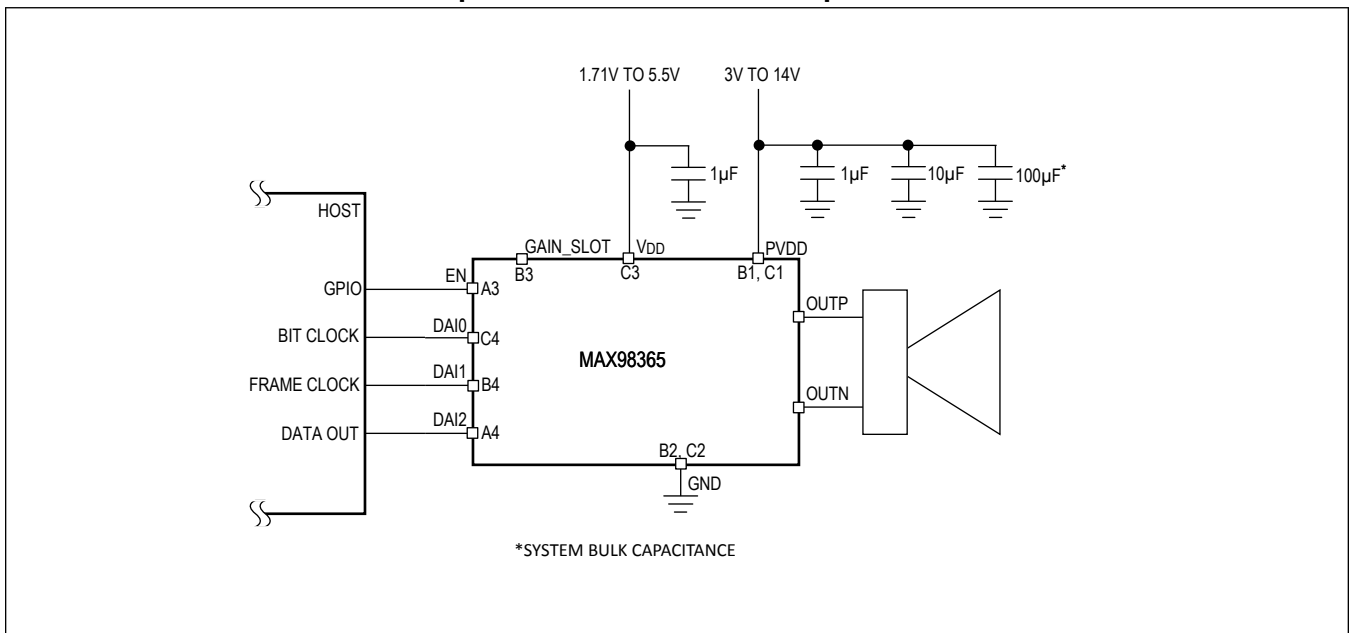
PCB fabrication technology is constantly evolving, so check with your PCB manufacturer to see what option can work best for your design.

Typical Application Circuits

I<sup>2</sup>S/Left-Justified Left-Channel Operation with 21.5 dBV Output

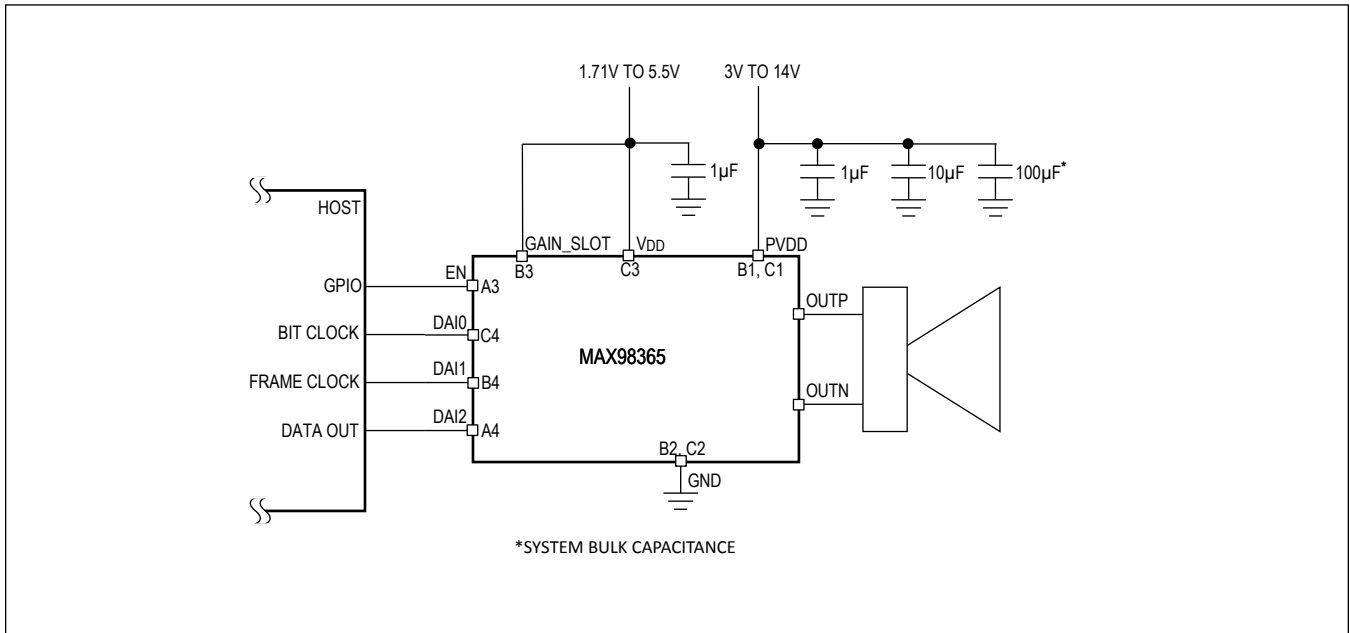


I<sup>2</sup>S/Left-Justified Left-Channel Operation with 18.5dBV Output

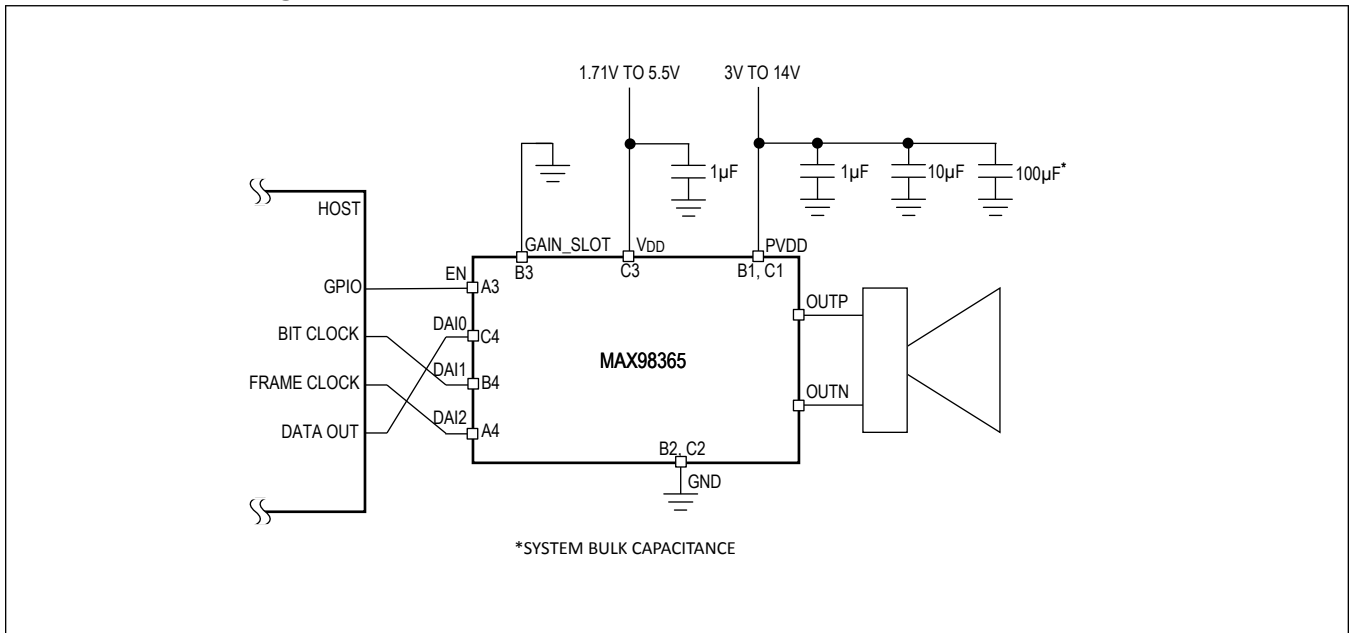


Typical Application Circuits (continued)

I<sup>2</sup>S/Left-Justified Left-Channel Operation with 15.5dBV Output



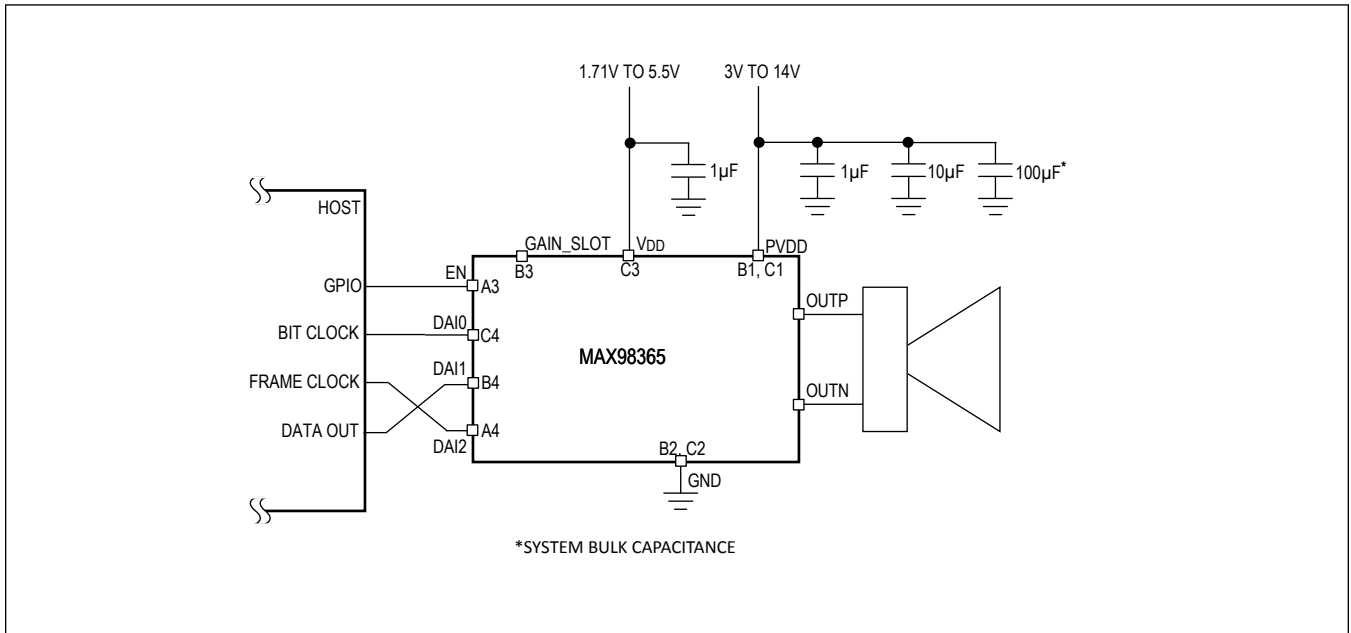
I<sup>2</sup>S/Left-Justified Right-Channel Operation with 21.5dBV Output





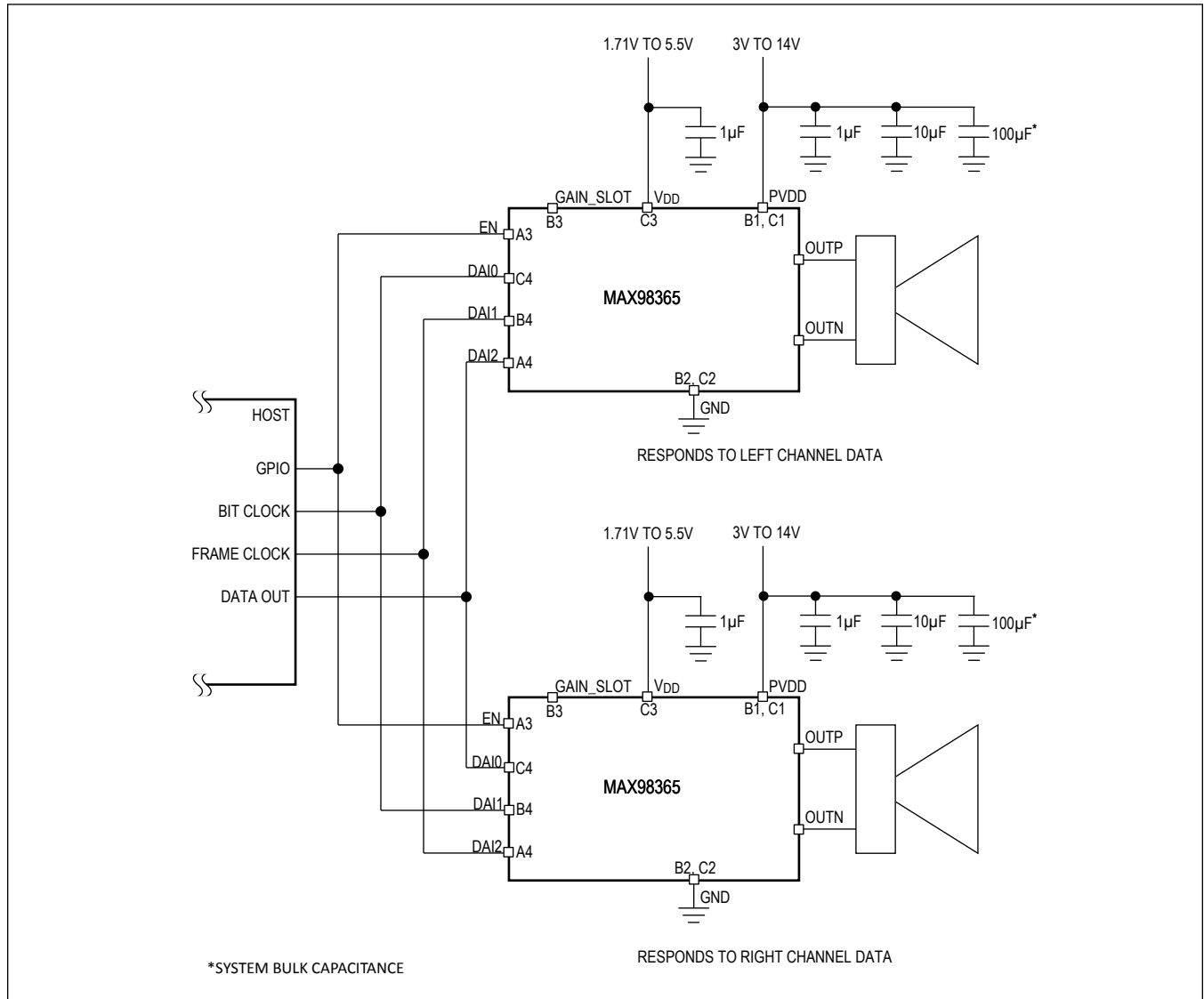
Typical Application Circuits (continued)

I<sup>2</sup>S/Left-Justified Left/2 + Right/2 Operation with 18.5dBV Output



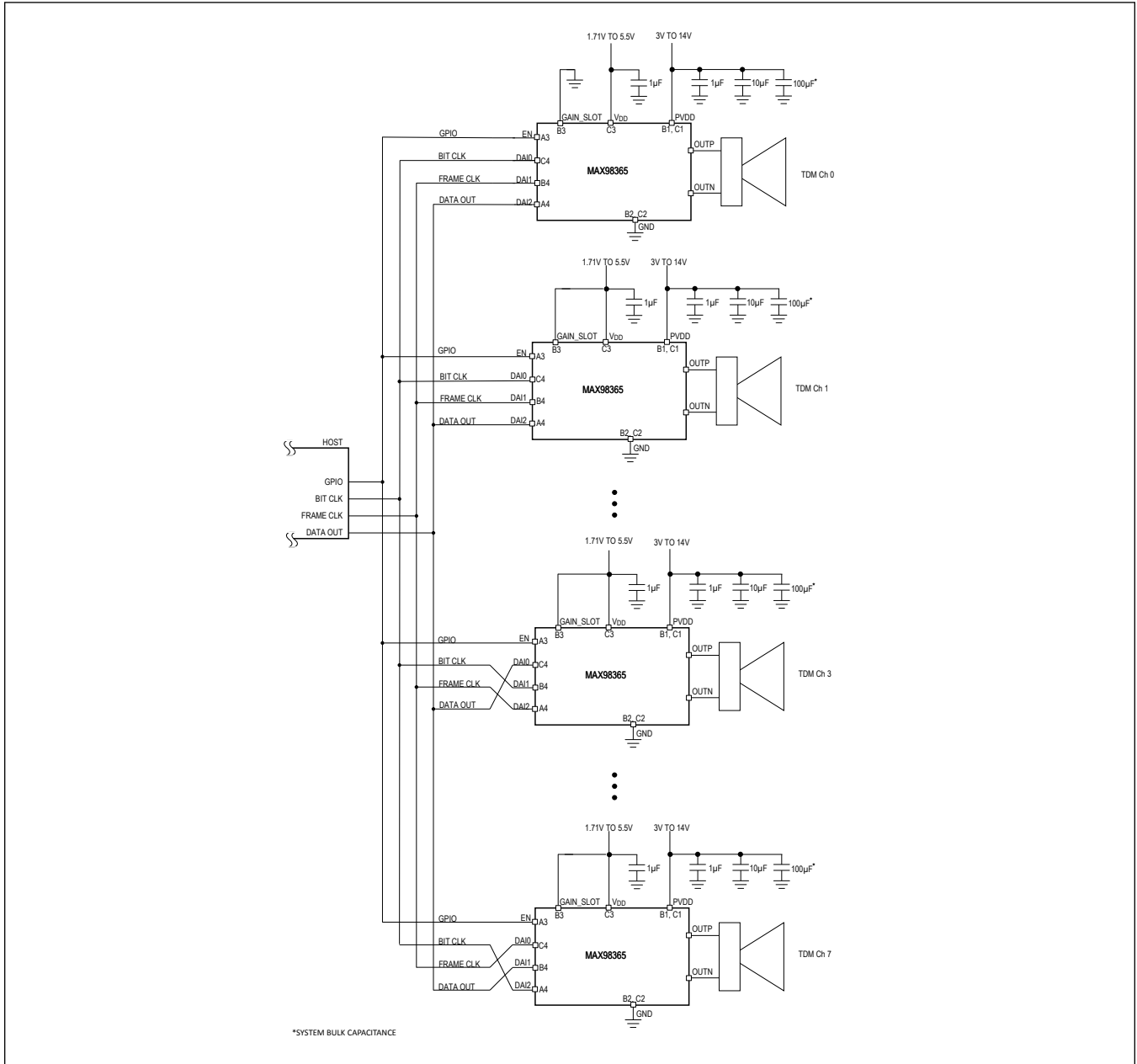
Typical Application Circuits (continued)

I<sup>2</sup>S/Left-Justified Stereo Operation with 18.5dBV Output



Typical Application Circuits (continued)

TDM Operation (Gain Fixed at 21.5dB)



**Ordering Information**

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX98365AEWC+	-40°C to +85°C	12 WLP	AEQ
MAX98365AEWC+T	-40°C to +85°C	12 WLP	AEQ
MAX98365BEWC+	-40°C to +85°C	12 WLP	AER
MAX98365BEWC+T	-40°C to +85°C	12 WLP	AER
MAX98365CEWC+	-40°C to +85°C	12 WLP	AES
MAX98365CEWC+T	-40°C to +85°C	12 WLP	AES
MAX98365DEWC+	-40°C to +85°C	12 WLP	AET
MAX98365DEWC+T	-40°C to +85°C	12 WLP	AET

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Initial release	—
1	1/22	Updated <i>General Description, Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics</i> table, <i>Typical Operating Characteristics, Valid Clock Frequencies, Table 4, Layout and Grounding, and Ordering Information</i> table	1, 8, 11, 12, 17, 18, 20, 24, 25, 34, 43