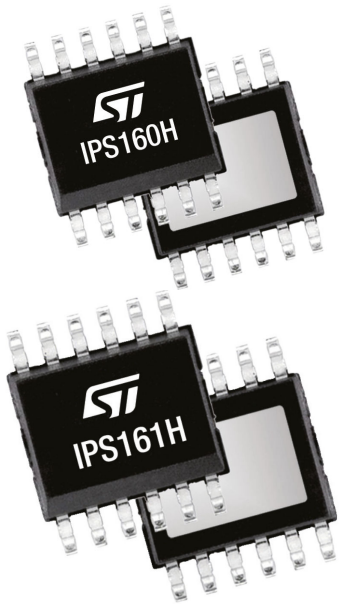
life.augmented

IPS160H, IPS161H

Datasheet

60 V, 60 mΩ single high-side switches



IPS

Product status
IPS160H
IPS161H

Product label
SUSTAINABLE TECHNOLOGY

Features

- 8 V to 60 V operating voltage range
- Minimum output current limitation: 0.7 A (IPS161H) or 2.5 A (IPS160H)
- Fast demagnetization of inductive load
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Ground disconnection protection
- V_{CC} disconnection protection
- Thermal shutdown protection
- Undervoltage lock-out
- Diagnostic signalization for: open load in off-state, cut-off and junction thermal shutdown
- Designed to meet IEC 61131-2
- PowerSSO12 package

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Domotics
- Generic power supply switch

Description

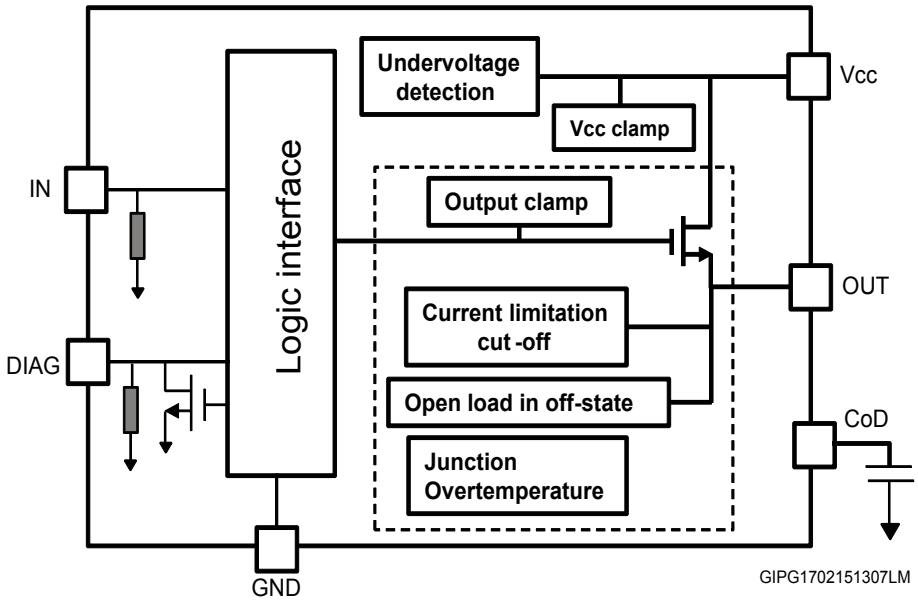
The IPS160H (I_{OUT} < 2.5 A) and IPS161H (I_{OUT} < 0.7 A) are monolithic devices which can drive capacitive, resistive or inductive loads with one side connected to ground.

The 60 V operating range and Ron = 60 mΩ, combined with the extended diagnostic (Open Load, Over Load, Overtemperature) make the IC suitable for applications implementing the proper architectures to address higher SIL levels.
The built-in overload and thermal shutdown protections guarantee the ICs, the application and the load against electrical and thermal overstress. Furthermore, in order to minimize the power dissipation when the output is shorted, a low-dissipative short-circuit protection (cut-off) is implemented to limit the output average current value and consequent device overheating.Cut-off delay time can be set by soldering an external capacitor or disabled by a resistor on pin 4 (CoD).

The DIAG common diagnostic open drain pin reports the open load in off-state, cutoff (overload) and thermal shutdown.

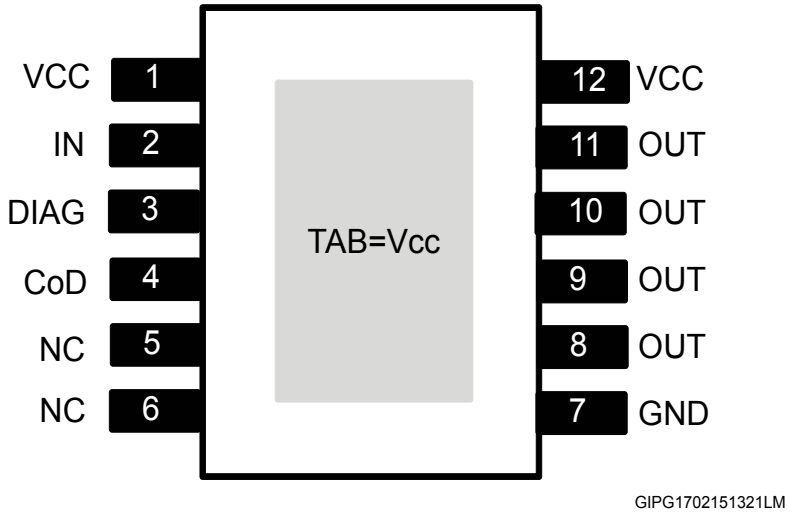
1 Block diagram

Figure 1. **Block diagram**



2 Pin description

Figure 2. **Pin connection (top view)**



GIPG1702151321LM

Table 1. **Pin configuration**

Number	Name	Function	Type
1, 12, TAB	VCC	Device supply voltage	Supply
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin both for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Cut-off delay pin, cannot be left floating. Connected to GND by 1 kΩ resistor to disable the cut-off function. Connect to a C_{CoD} capacitor to set the cut-off delay see Table 8. Protection and diagnostic	Input
5, 6	NC	Not connected	
7	GND	Device ground	Ground
8, 9, 10, 11	OUT	Channel power stage output	Output

2.1 IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see Table 7. Logic inputs.

2.2 OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

2.3 DIAG

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

2.4 CoD

This pin cannot be left floating and can be used to program the cut-off delay time t_{coff}, see Table 8. Protection and diagnostic through an external capacitor (C_{CoD}). The cut-off function can be completely disabled connecting the CoD pin to GND through 1 kΩ resistor: in this condition the output channel remains in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered.

2.5 GND

IC ground.

2.6 VCC

IC supply voltage.

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 65	V
V_{OUT}	Output channel voltage	V_{cc}-V_{clamp} to V_{cc}+0.3	V
I_{IN}	Input current	-10 to +10	mA
V_{IN}	IN voltage	V_{CC}	V
V_{COD}	Output cut-off voltage pin	5.5	V
I_{COD}	Input current on cut-off pin	-1 to +10	mA
V_{DIAG}	Fault voltage	V_{CC}	V
I_{DIAG}	Fault current	-5 to +10	mA
I_{CC} (1)	Maximum DC reverse current flowing through the IC from GND to V_{CC}	-250	mA
I_{OUT}	Output stage current	Internally limited	A
$-I_{OUT}$ (1)	Maximum DC reverse current flowing through the IC from OUT to V_{CC}	5	
E_{AS} (1)	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{load} = 0.5 A)	3000	mJ
	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{load} = 1.0 A)	1000	mJ
P_{TOT}	Power dissipation at T_C = 25 °C (2)	Internally limited	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature	-40 to 150	

1. *Verified on STEVAL-IFP028V1 and STEVAL-IFP034V1 application board*
2. *$(T_{JSD(MAX)}$-$T_C)$/ $R_{th(JA)}$*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		1s	2s2p	2s2p (with 4 thermal vias)	
$R_{th(JC)}$	Thermal resistance junction-case	0.4	0.9	0.5	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	117	57	29	

Note: $R_{th(JC)}$ is intended between the die and the bottom case surface measured by cold plate as per JESD51.
$R_{th(JA)}$ according JESD51-3 (1s) JESD51-5 (2s2p) and JESD51-7 (2s2p and thermal vias).
Maximum power dissipation (T_{AMB} = 85 °C, T_J < 150 °C):

- *P_{MAX} = 0.5 W ($R_{th(JA)}$ = 117 °C/W)*
- *P_{MAX} = 1.1 W ($R_{th(JA)}$ = 57 °C/W)*
- *P_{MAX} = 2.2 W ($R_{th(JA)}$ = 29 °C/W)*

4 Electrical characteristics

(8 V < V_{CC} < 60 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		V_{UVON}		60	V
V_{UVON}	Undervoltage on threshold		6.9		8	V
V_{UVOFF}	Undervoltage off threshold		6.5		7.8	V
V_{UVH}	Undervoltage hysteresis		0.15	0.5		V
I_S	Supply current in off-state	V_{CC} = 24 V		300	500	µA
		V_{CC} = 60 V		350	600	
	Supply current in on-state	V_{CC} = 24 V		1	1.4	mA
		V_{CC} = 60 V		1.4	2.1	
I_{LGND}	GND disconnection output current	V_{GND} = V_{IN} = V_{CC}, V_{OUT} = 0 V; T_J = 25 °C			0.5	mA
		V_{GND} = V_{IN} = V_{CC}, V_{OUT} = 0 V; T_J = 125 °C			0.55	

Table 5. Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	On-state resistance	V_{CC} = 24 V I_{OUT} =0.5 A (IPS161H), 1 A (IPS160H) @ T_J = 25 °C		60	80	mΩ
		V_{CC} = 24 V I_{OUT} =0.5 A (IPS161H), 1 A (IPS160H) @ T_J = 125 °C			120	
$V_{OUT(OFF)}$	Off-state output voltage	V_{IN} = 0 V and I_{OUT} = 0 A			2	V
$I_{OUT(OFF)}$	Off-state output current	V_{CC} = 24 V, V_{IN} = 0 V, V_{OUT} = 0 V			3	µA
		V_{CC} = 60 V, V_{IN} = 0 V, V_{OUT} = 0 V			10	
$I_{OUT(OFF-min)}$	Off-state output current	V_{IN} = 0 V, V_{OUT} = 4 V	-35		0	

Table 6. Switching (V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 48 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time	I_{OUT} = 0.5 A, (see Figure 3. Timing in normal operation)		10	20	µs
t_f	Fall time			10	20	
$t_{PD(H-L)}$	Propagation delay time off			20	35	
$t_{PD(L-H)}$	Propagation delay time on			20	35	
$t_{D(VCC-ON)}$	Power-on delay time from V_{CC} rising edge	I_{OUT} = 0.5 A, (see Figure 4. Propagation delay at start-up)		600	1200	

Figure 3. Timing in normal operation

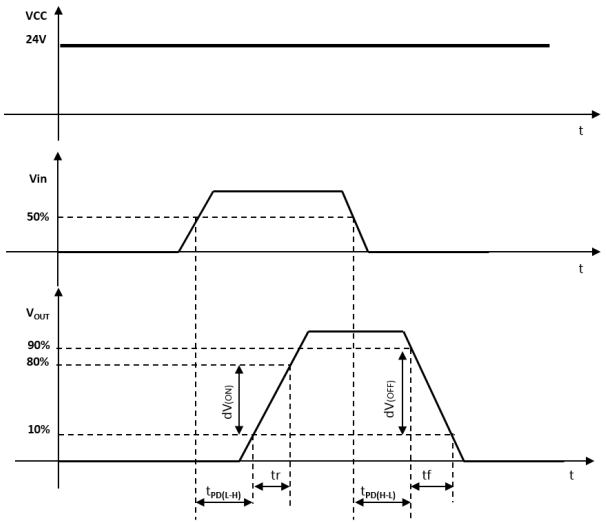


Figure 4. Propagation delay at start-up

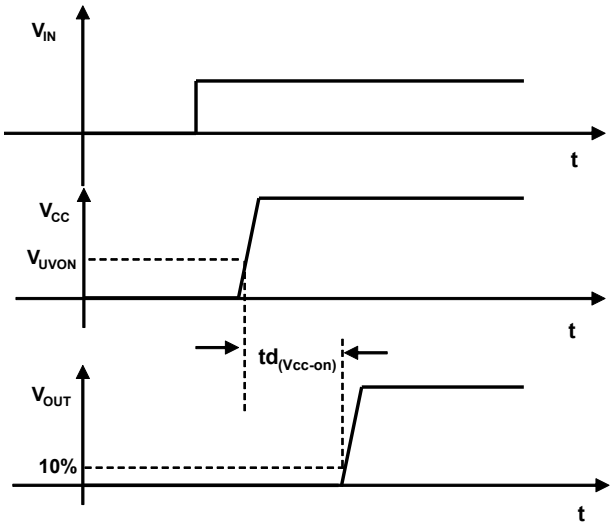


Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.2			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
I_{IN}	Input current	V_{CC} = V_{IN} = 36 V			200	µA
		V_{CC} = V_{IN} = 60 V			550	

Table 8. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} active clamp	I_{CC} = 10 mA	65.5	68.5	71.5	V
V_{demag}	Demagnetization voltage	I_{OUT} = 0.5 A; load =1 mH	V_{CC}-71.5	V_{CC}-68.5	V_{CC}-65.5	
V_{OLoff}	Open load (off-state) or short to V_{CC} detection threshold		2		4	
t_{BKT}	Open load blanking time				200	µs
V_{DIAG}	Voltage drop on DIAG	I_{DIAG} = 4 mA			1	V
I_{DIAG}	DIAG pin leakage current	V_{CC} ≤ 36 V			110	µA
		36 V < V_{CC} ≤ 60 V			180	
I_{PK}	IPS161H Output current limitation activation threshold	VCC ≤ 24 V, R_{LOAD} ≤ 10 mΩ	1.3		2.1	A
	IPS160H Output current limitation activation threshold		3.0		4.6	
I_{LIM}	IPS161H Output current limitation		0.7		1.7	
	IPS160H Output current limitation		2.5		4.2	
t_{coff}	Cut-off current delay time	Programmable by the external capacitor on CoD pin. Cut-off is disabled when CoD pin is connected to GND through 1 kΩ resistor. T_J< T_{JSD}	50xC_{COD}[nf] ± 35%(1)			µs
t_{res}	Output stage restart delay time	T_J< T_{JSD}	32xt_{coff} [µs]± 40%			
T_{JSD}	Junction temperature shutdown		150	170	190	°C
T_{JHYST}	Junction temperature thermal hysteresis			15		

1. *The formula is guaranteed in the range 10 nF ≤ C_{COD} ≤ 100 nF.*

5 Output logic

Table 9. Output stage truth table

Operation	IN	OUT	DIAG
Normal	L	L	H
	H	H	H
Cut-off	L	L	L
	H	L	L
Overtemperature	L	L	L
	H	L	L
Open load	L	H (external pull-up resistor is used)	L (external pull-up resistor is used)
	H	H	H
UVLO	X	L	X
	X	L	X

6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ($V_{UV(off)}$). Normal operation restarts after V_{CC} exceeds the turn-on threshold ($V_{UV(on)}$). Turn-on and turn-off thresholds are defined in Table 4. Supply.

6.2 Overtemperature

The output stage turns off when its internal junction temperature (T_J) exceeds the shutdown threshold T_{JSD}. Normal operation restarts when T_J comes back below the reset threshold (T_{JSD} - T_{JHYST}), see Table 8. Protection and diagnostic. The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is reported on DIAG pin.

6.3 Cut-off

The IC can limit the output current at the power stage by its embedded output current limitation circuit.

This circuit continuously monitor the output current and, when load is increasing, at the triggering of its activation threshold (3.8A TYP) it starts limiting to I_{LIM} limitation level (See Protection and diagnostic): while current limitation is active the IC enters an high dissipation status.

The IC implements the cut-off feature which limits the duration of the current limitation condition.

The duration of the current limitation condition (T_{coff}) can be set by a capacitor (C_{CoD}) placed between CoD and GND pins. The design rule for C_{CoD} is:

t_{coff}[us] +/- 35% = 50 x C_{cod}[nF]

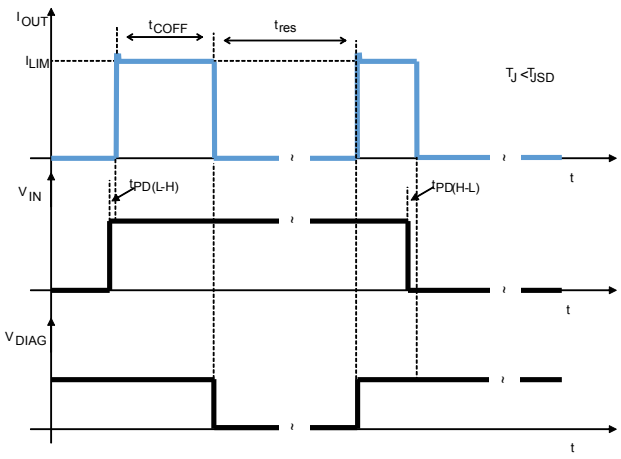
The drift of +/-35% is guaranteed in the range of 10 nF < C_{cod} < 100 nF; lower capacitance than 10 nF can be used.

If I_{LIM} threshold is triggered, the output stage remains in the current limitation condition (I_{OUT} = I_{LIM}) no longer than t_{coff}. If t_{coff} elapses, the output stage turns off and restarts after the t_{res} restart time.

Thermal shutdown protection has higher priority than cut-off:

- IC is forced off if T_{JSD} is triggered before t_{coff} elapses
- if T_{JSD} is triggered, IC is maintained off even after the t_{res} has elapsed and until the T_J decreases below T_{JSD}-T_{JHYST}

Figure 5. Current limitation and cut-off



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time t_{res}, the same behavior is reported on DIAG pin.

The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 1 kΩ resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

In case of low ambient temperature conditions (T_{AMB} < -20 °C) and high supply voltage (V_{CC} > 36 V) the cut-off function needs activating in order to avoid IC permanent damages. The following table reports the suggested cut-off delay for the different operating voltage.

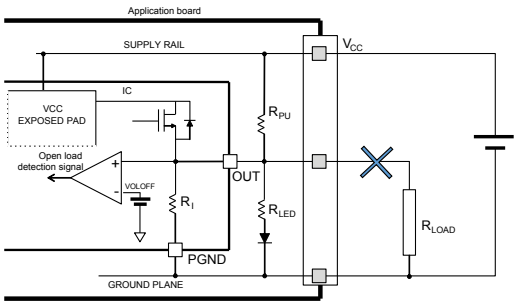
Table 10. Minimum cut-off delay for T_{AMB} less than -20 °C

V_{CC} [V]	Cut-off delay [µs]	Cut-off capacitance [nF]
36-48	100	2.2
48-60	50	1

6.4 Open load in off-state

The IC provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor (R_{PU}) between OUT and VCC pins.

Figure 6. Open load off-state



In case of wire break and during the OFF state (IN = low), the output voltage V_{OUT} rises according to the the partitioning between the external pull-up resistor and the internal impedence of the IC (130 kΩ < RI < 360 kΩ).

The effect of the LED (if any) on the output pin has to be considered as well. In case of wire break and during the ON state (IN = high), the output voltage V_{OUT} is pulled up to V_{CC} by the low resistive integrated switch. If the load is not connected, in order to guarantee the correct open load signalization it must result:

$V_{OUT} > V_{OLoff(max.)}$

Referring to the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times (I_{RI} + I_{LED} + I_{RL}) \quad (1)$$

therefore:

$$R_{PU} < \frac{V_{CC(min)} - V_{OLoff(max)}}{\left(\frac{V_{OLoff(max)}}{RI(\min)} + \frac{V_{OLoff(max)} - V_{LED}}{R_{LED}}\right)} \quad (2)$$

If the load is connected, in order to avoid any false signalization of the open load, it must result as follows:

$V_{OUT} < V_{OLoff(min)}$

By taking into account the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times \left(\frac{V_{OUT}}{R_I} + \frac{V_{OUT} - V_{LED}}{R_{LED}} + \frac{V_{OUT}}{R_L}\right) \quad (3)$$

so:

$$R_{PU} > \frac{V_{CC(max)} - V_{OLoff(min)}}{\left(\frac{V_{OLoff(min)}}{RI(\max)} + \frac{V_{OLoff(min)} - V_{LED}}{R_{LED}} + \frac{V_{OLoff(min)}}{R_L}\right)} \quad (4)$$

The fault condition is reported on the DIAG pin and the fault reset occurs when load is reconnected.

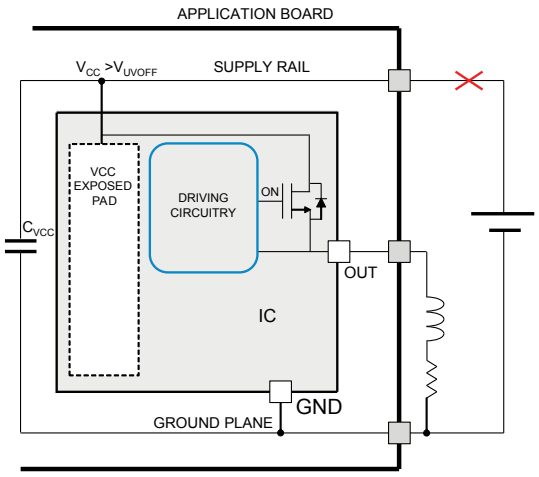
If the channel is switched on by IN pin, the fault condition is no longer detected.

When inductive load is driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when I_{LOAD} = 0 A and the OUT pin remains floating until next turn-on. In order to avoid a fake signalization of the open load event driving inductive loads, the open load signal is masked for t_{BKT}. So, the open load is reported on the DIAG pin with a delay of t_{BKT} and if the open load event is triggered for more than t_{BKT}.

6.5 VCC disconnection protection

The IC is protected despite the V_{CC} disconnection event. This event is intended as the disconnection of the V_{CC} wire from the application board, see figure below. When this condition happens, the IC continues working normally until the voltage on the V_{CC} pin is ≥ V_{UVOFF}. Once the V_{UVOFF} is triggered, the output channel is turned off independently on the input status. In case of inductive load, if the V_{CC} is disconnected while the output channel is still active, the IC allows the discharge of the energy still stored in the inductor through the integrated power switch.

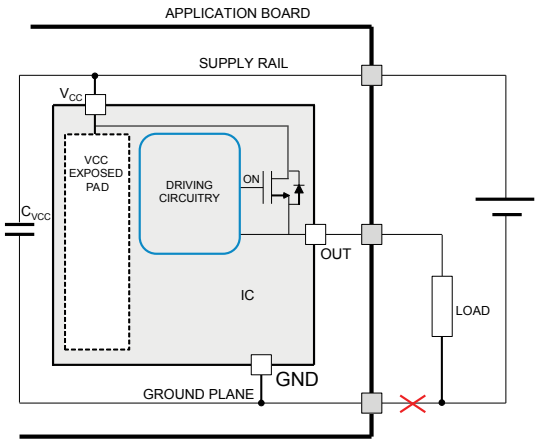
Figure 7. **VCC disconnection**



6.6 GND disconnection protection

GND disconnection is intended as the disconnection event of the application ground, see figure below. When this event happens, the IC continues working normally until the voltage between V_{CC} and GND pins of the IC results ≥ V_{UVOFF}. The voltage on GND pin of the IC rises up to the supply rail voltage level. In case of GND disconnection event, a current (I_{LGND}) flows through OUT pin. Table 7. Logic inputs reports I_{OUT} = I_{LGND} for the worst case of GND disconnection event in case of output shorted to ground.

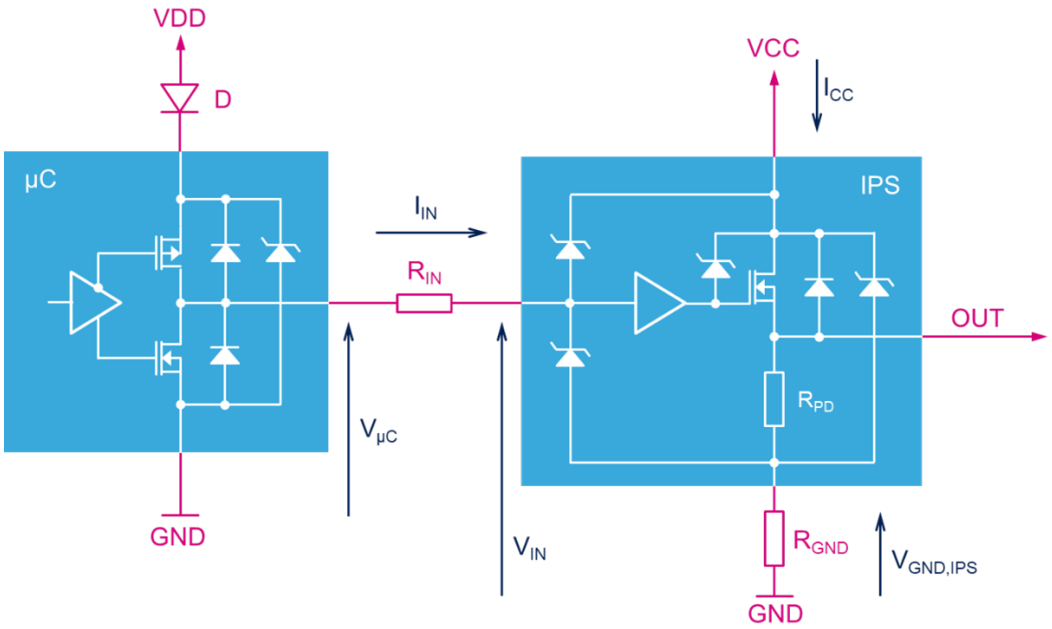
Figure 8. **GND disconnection**



6.7 Input pin protection

When used as Digital Output the IC is driven by a digital device (microcontroller or an ASIC) which can be either galvanically coupled or there can be a galvanic isolation (optocoupler, digital isolator) in between. A typical scheme is shown in Figure 9. Digital Output IC connection.

Figure 9. **Digital Output IC connection**



The input pin is protected against EMC by dedicated circuitries that might be activated in some non- operative circumstances, like Vcc disconnection, reverse polarity etc.

For this reason is a good practice to decouple the microcontroller and IPS ICs using series resistors to limit parasitic currents in case of faults and to limit EMC disturbance signals from the Process side affecting the microcontroller.

The value of the resistor must ensure proper operation in the full operating range and prevent damage in case of fault events.

Consider the microcontroller supply voltage VDD = 3.3 V and output voltage in logic H state $V_{µC,H}$ = VDD, under normal operating conditions, we calculate the resistance as:

$V_{IN,\,H} = V_{µC,\,H} - R_{IN} \times I_{IN} - V_{GND,\,IPS,\,max} \geq V_{IN,\,H,\,min} = 2.2$ V

$R_{IN} \times I_{IN} \leq V_{µC,\,H} - V_{GND,\,IPS,\,max} - V_{IN,\,H,\,min}$

$R_{IN} \times I_{IN} \leq 3.3 - 0.252 - 2.2 = 0.848$ V

$R_{IN} \leq V_{RIN} / I_{IN} = 0.848 / 0.2 = 4.24$ kΩ

For current limitation in case of reverse polarity:

$R_{IN} \geq (ABS(-VCC,max) - 2 \times V_F) / I_{IN,max} = (28.8 - 0.6) / 10 = 2.82$ kΩ

Therefore:

$2.82\ kΩ \leq R_{IN} \leq 4.24\ kΩ$

We use the highest resistance value is selected for maximum protection: $R_{IN} = 4.2$ kΩ

Note: The reverse polarity condition has the greatest impact on R_{IN} dimensioning, so other common fault scenarios where VCC supply is disconnected or shorted to GND while VDD is present do not need to be analyzed.

6.8 Reverse polarity

The IC can be protected against reverse polarity using two different solutions:

1. Placing a resistor R_{GND} between IC GND pin and load connection point to GND (R_{GND} > VCC/ICC, see Table 2. Absolute maximum ratings).

Note that power dissipated by R_{GND} during reverse polarity condition is Vcc^2/R_{GND}.

2. Placing a diode in parallel to R_{GND}

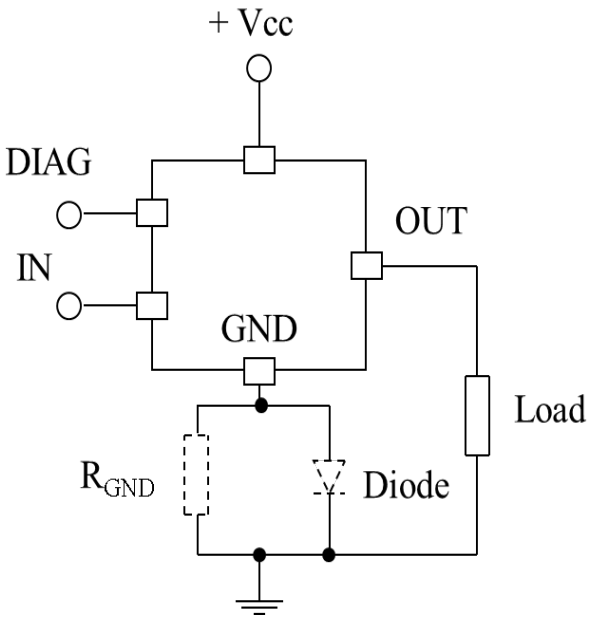
The diode must be selected such that its VRRM > |VCC| and power dissipation capability is higher than VF*I_S (see Table 4. Supply).

In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the module.

Using option 1, ΔV = R_{GND} * I_{CC}.

Using option 2, ΔV = VF@(I_S).

Figure 10. Reverse polarity protection schematic



7 Active VDS clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to V_{demag}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in IC internal switch and in load resistance.

Figure 11. Active clamp equivalent principle schematic

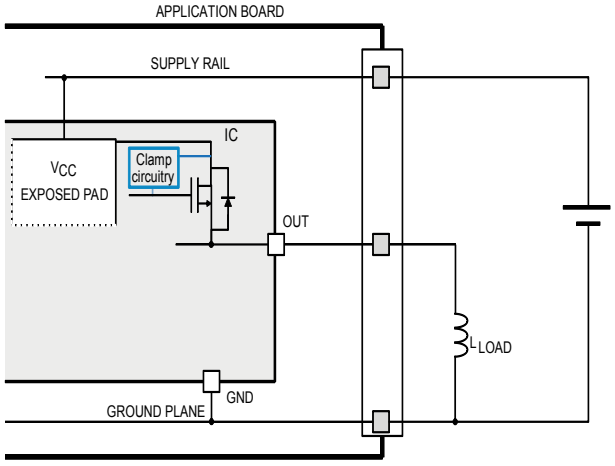
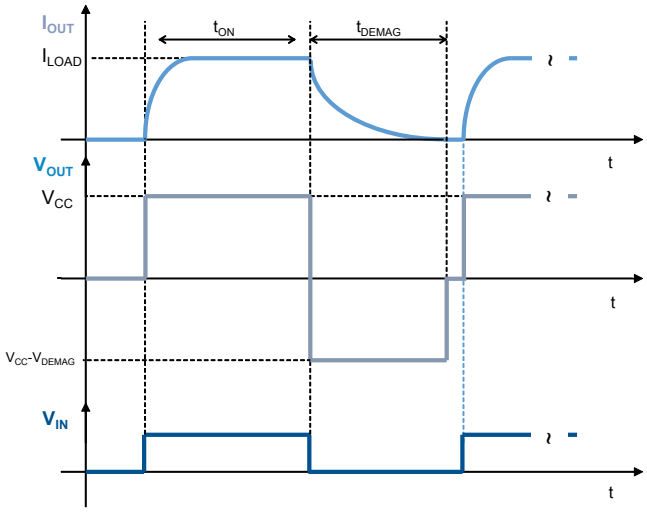


Figure 12. Fast demag waveforms



The demagnetization of inductive load causes a huge electrical and thermal stress to the IC. The curves plotted below show the maximum demagnetization energy (and the corresponding value of inductance) that the IC can support in a single demagnetization pulse with V_{CC} = 24 V and T_{AMB} = 125 °C. If higher demagnetization energy is required then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 13. Typical single pulse demagnetization: E_{OFF} vs I_{OUT} (VCC = 24 V, T_{AMB} = 125 °C)

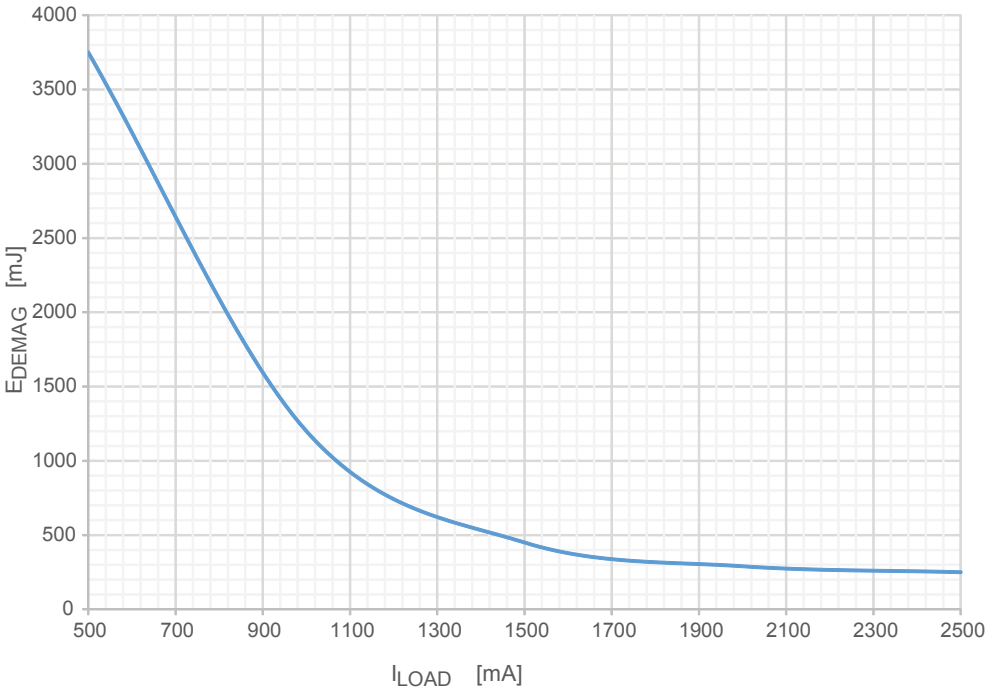
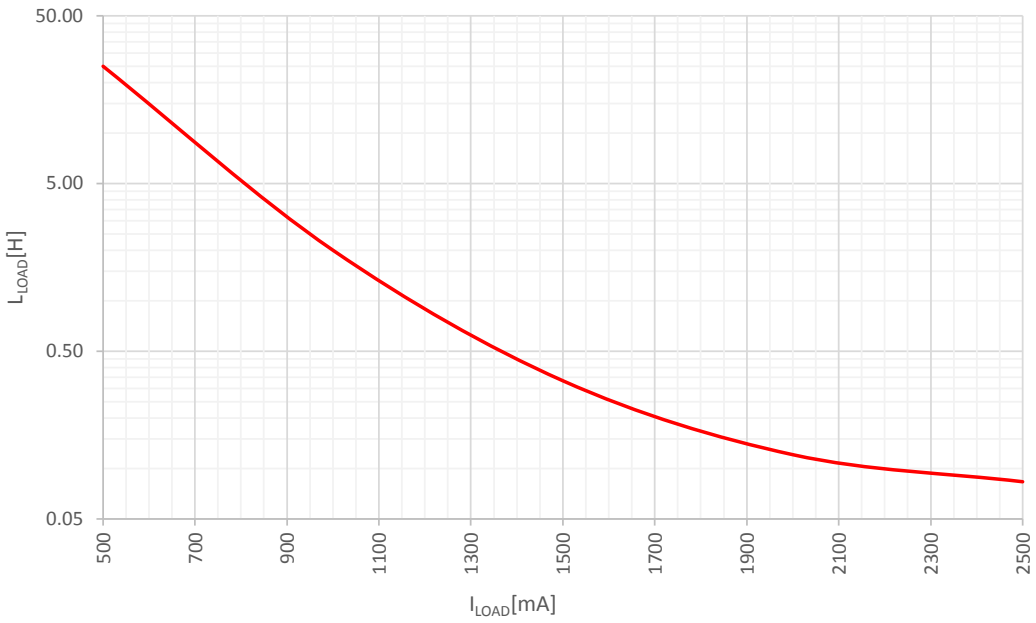


Figure 14. Typical single pulse demagnetization: L_{LOAD} vs I_{OUT} (VCC = 24 V, T_{AMB} = 125 °C)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 PowerSSO12 package information

Figure 15. PowerSSO12 package outline

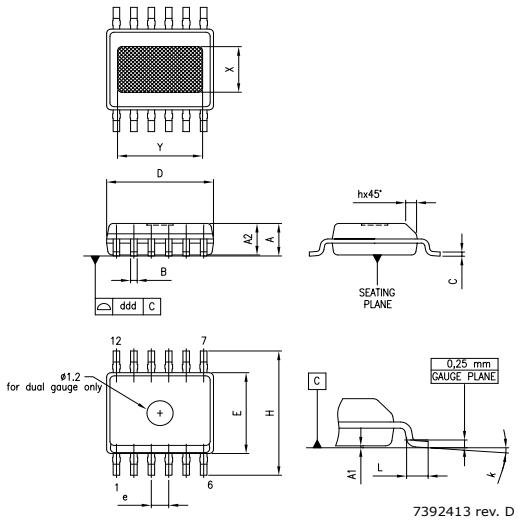


Table 11. PowerSSO12 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.55
L	0.400		1.270
k	0d		8d
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Note: Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

Figure 16. PowerSSO12 recommended footprint

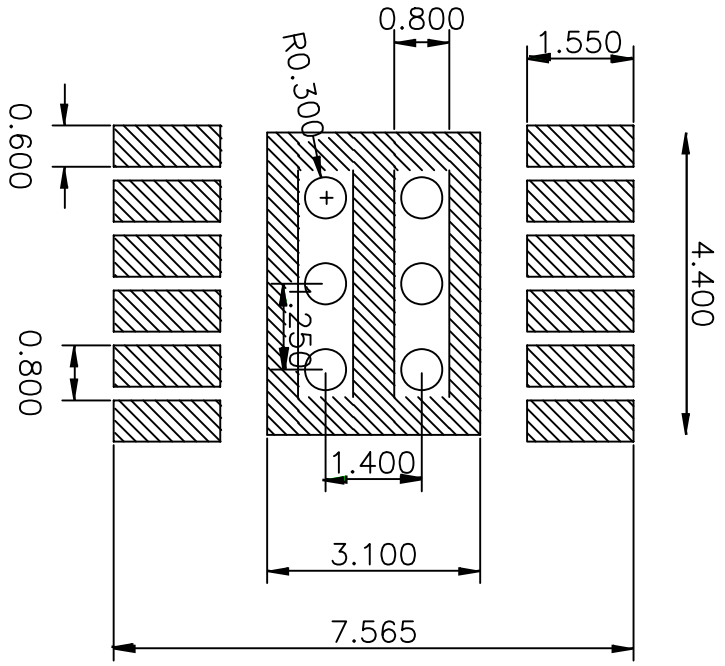
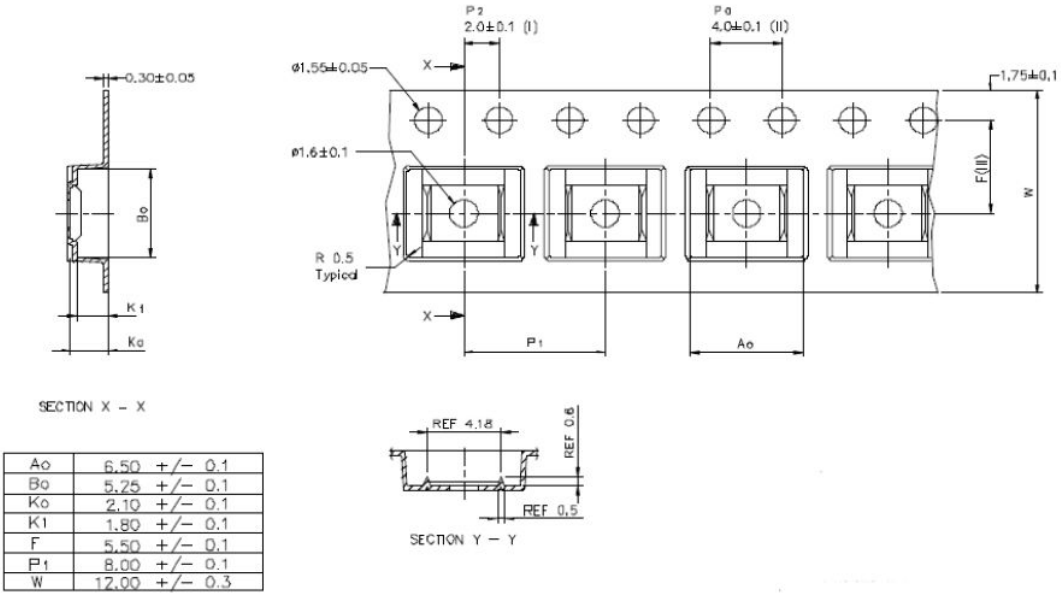
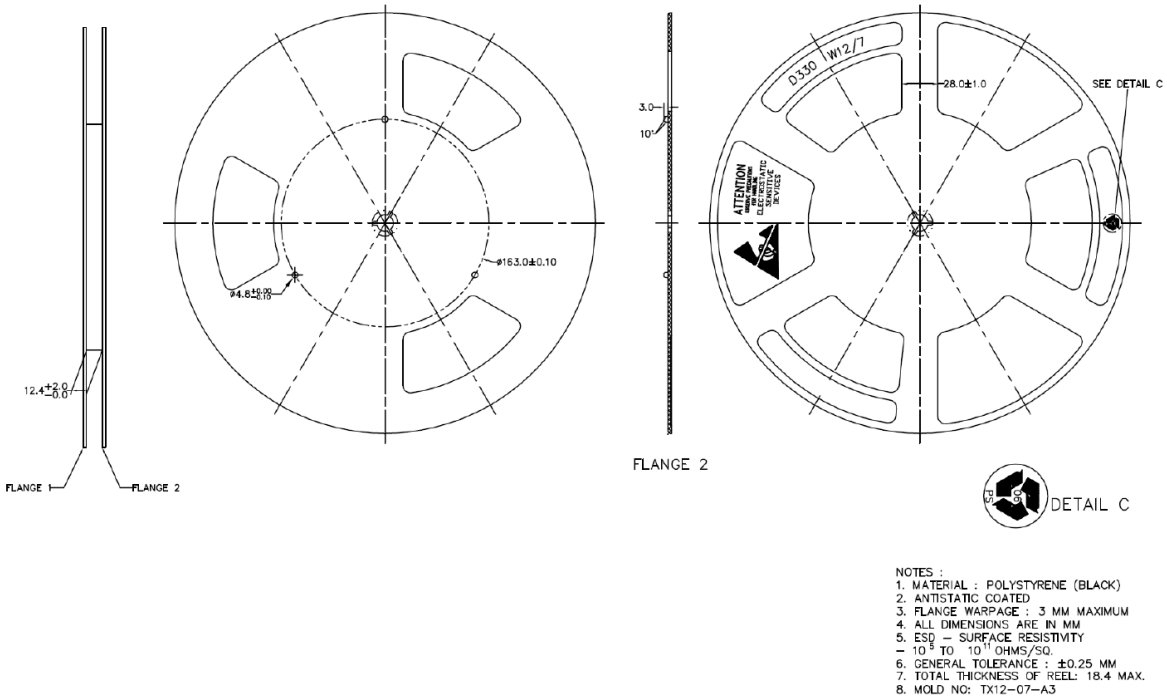


Figure 17. PowerSSO12 tape packing information [mm]



Ao	6.50 +/– 0.1
Bo	5.25 +/– 0.1
Ko	2.10 +/– 0.1
K1	1.80 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 18. PowerSS012 reel packing information [mm]



NOTES :
1. MATERIAL : POLYSTYRENE (BLACK)
2. ANTISTATIC COATED
3. FLANGE WARPAGE : 3 MM MAXIMUM
4. ALL DIMENSIONS ARE IN MM
5. ESD – SURFACE RESISTIVITY
– 10^{9} TO 10^{11} OHMS/SQ.
6. GENERAL TOLERANCE : ±0.25 MM
7. TOTAL THICKNESS OF REEL: 18.4 MAX.
8. MOLD NO: TX12–07–A3

9 Ordering information

Table 12. **Ordering information**

Order code	Package	Packing
IPS160H	PowerSSO12	Tube
IPS160HTR		Tape and reel
IPS161H		Tube
IPS161HTR		Tape and reel

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
19-Mar-2015	1	Initial release.
04-Nov-2015	2	Minor text changes throughout the document. Added figure 7 titled "V_{CC} disconnection", figure 10 titled: "Fast demag waveforms" and figure 11 titled "Typical demagnetization energy (single pulse) at V_{CC} = 24 V and T_{AMB} = 125 °C.
11-May-2016	3	Updated tables titled: "Supply", "Switching (V_{CC} = 24 V; 125 °C > T_J > -40 °C, R_{LOAD} = 48 Ω)" and "Protection diagnostic". Changed figures titled: "$t_{PD(L-H)}$ and $t_{PD(H-L)}$" and "Current limitation and cut-off".
20-May-2016	4	Document status promoted from preliminary to production data.
08-Mar-2018	5	Updated E_{AS} value in Table 2. Absolute maximum ratings.
14-Dec-2018	6	Added reel packaging information in Section 8.1 PowerSSO12 package information
02-Dec-2019	7	Updated value in Table 4. Supply. Text change in Section 2.4 CoD. Change to Figure 18 title.
03-Mar-2021	8	Merged IPS160H and IPS161H datasheets. Updated Section Description and Section Applications target.
29-Mar-2021	9	Updated I_{LGND} max value in Table 4.
30-Jul-2021	10	Reviewed the feature list order in front page. Updated thermal data in Table 3 according to Jedec conditions.
06-Dec-2022	11	Updated Table Table 6. Switching (V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 48 Ω): filled column Max, added $t_{D(VCC-ON)}$ parameter. Added figure Figure 4. Propagation delay at start-up. Added parameter I_{PK} (activation threshold of current activation feature) in table Table 8. Protection and diagnostic. Reduced minimum and maximum values of I_{LIM} for IPS160H in table Table 8. Protection and diagnostic.
15-Jan-2024	12	Added note (maximum power dissipation) in Table 3. Thermal data; added Section 6.7 Input pin protection; moved Reverse Polarity paragraph to Section 6 Protection and diagnostic; added Figure 14. Typical single pulse demagnetization: L_{LOAD} vs I_{OUT} (VCC = 24 V, T_{AMB} = 125 °C); added Section 9 Ordering information; some minor changes.

Contents

List of tables

List of figures