- **Nine Single-Ended SCSI Transceiver Channels With Active Termination**
- **Programmable Drivers Provide Active Negation (Totem Pole) or Wired-OR (Open Drain) Outputs**
- **24-mA Current-Mode Active Termination With Common Nine-Channel Bus Enable**
- **Low Output Capacitance Presented to SCSI Bus, 13.5 pF Typ**
- **3.3 V Compatible Logic Inputs Provide Bridge from 3 V Controllers to 5 V SCSI Bus**
- **Designed to Operate at 10-Million Data Transfers Per Second (Fast-SCSI)**
- **Controlled Driver Rise and Fall Times 5 ns Min**
- **High-Receiver Input-Voltage Hysteresis 500 mV Typ**
- **Receiver Input-Noise Pulse Filter 5 ns Typ**
- **Each Driver and Receiver Meets ANSI X3.131-1994 (SCSI-2) and the Proposed SCSI-3 Standards**
- **Power-Up/Power-Down Glitch Protection**
- **High Impedance Driver With V_{CC} at 0 V**

DL PACKAGE
(TOP VIEW)

GND	1	56	8B
TE	2	55	GND
GND	3	54	CE
1A	4	53	NC
1DE/$\overline{RE}$	5	52	NC
2A	6	51	NC
2DE/$\overline{RE}$	7	50	7B
3A	8	49	NC
3DE/$\overline{RE}$	9	48	6B
4A	10	47	NC
4DE/$\overline{RE}$	11	46	5B
V_{CC1}	12	45	V_{CC}
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V_{CC}	18	39	V_{CC}
5A	19	38	NC
5DE/$\overline{RE}$	20	37	4B
6A	21	36	NC
6DE/$\overline{RE}$	22	35	3B
7A	23	34	NC
7DE/$\overline{RE}$	24	33	2B
8A	25	32	NC
8DE/$\overline{RE}$	26	31	1B
9A	27	30	NC
9DE/$\overline{RE}$	28	29	9B

NC − No internal connection

description

The SN75LBC968 is a nine-channel transceiver with active termination that drives and receives the signals from the single-ended, parallel data buses such as the Small Computer-Systems Interface (SCSI) bus. The features of the line drivers, receivers, and active-termination circuits provide the optimum signal-to-noise ratios for reliable data transmission. Integration of the termination and transceivers in the LinBiCMOS™ process provides the necessary analog-circuit performance, has low quiescent power, and reduces the capacitance presented to the bus over separate termination and I/O circuits.

The transceivers of the SN75LBC968 can be enabled to function as totem-pole or open-drain outputs. The open-drain mode drives the wired-OR lines of SCSI (BSY, SEL, and RST) by inputting the data to the direction control input DE/RE instead of the A input. When driving the data through the A input, the outputs become totem poles and provide active signal negation for a higher voltage level on low-to-high signal transitions on heavily loaded buses. In either mode, the turnon and turnoff output transition times are limited to minimize crosstalk through capacitive coupling to adjacent lines and RF emissions from the cable. The receivers are also designed for optimum analog performance by precisely controlling the input-voltage thresholds, providing wide input-voltage hysteresis and including an input-noise filter. These features significantly increase the likelihood of detecting only the desired data signal and rejecting noise.

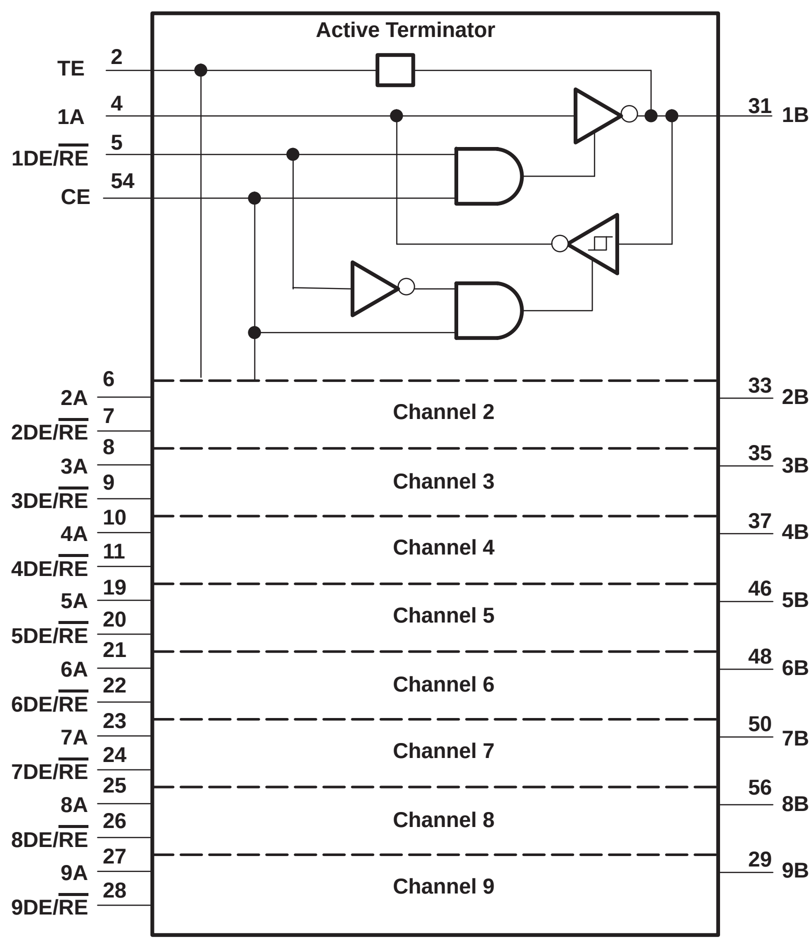
description (continued)

The communication between the SN75LBC968 and the controller can be accomplished at 3.3-V logic levels provided that the V_{CC1} input connects to the same supply rail as the controller. This provides a bridge from the lower-voltage circuit and the 5-V SCSI bus. The SN75LBC968 also removes the need for special I/O buffers (and associated power dissipation) on the controller itself. The SN75LBC968 must be used with a SCSI controller with support for Differential SCSI.

The integrated, current-mode, active termination supplies a constant 24 mA of current (TERMPWR) to the bus when the bus voltage falls below 2.5 V. This makes the next low-to-high (negation) signal transition independent of the low-level (asserted) bus voltage, unlike voltage-mode terminators. The termination current is provided through the TE input and from TERMPWR and can be disabled by letting the TE input float or by connecting it to ground. The termination circuitry is independent from the line drivers and receivers and V_{CC} or V_{CC1}. Operational termination is present as long as TERMPWR is applied.

The switching speeds of the SN75LBC968 are sufficient to transfer data over the data bus at ten million transfers per second (Fast-SCSI). The specification, $t_{sk(lim)}$, is for system skew budgeting and maintenance of bus set-up and hold times. The device is available in the space-efficient shrink-small-outline package (SSOP) with 25-mil lead pitch. The SN75LBC968 meets or exceeds the requirements of ANSI X3.131−1994 (SCSI-2) and the proposed SPI (SCSI-3) standards, and is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

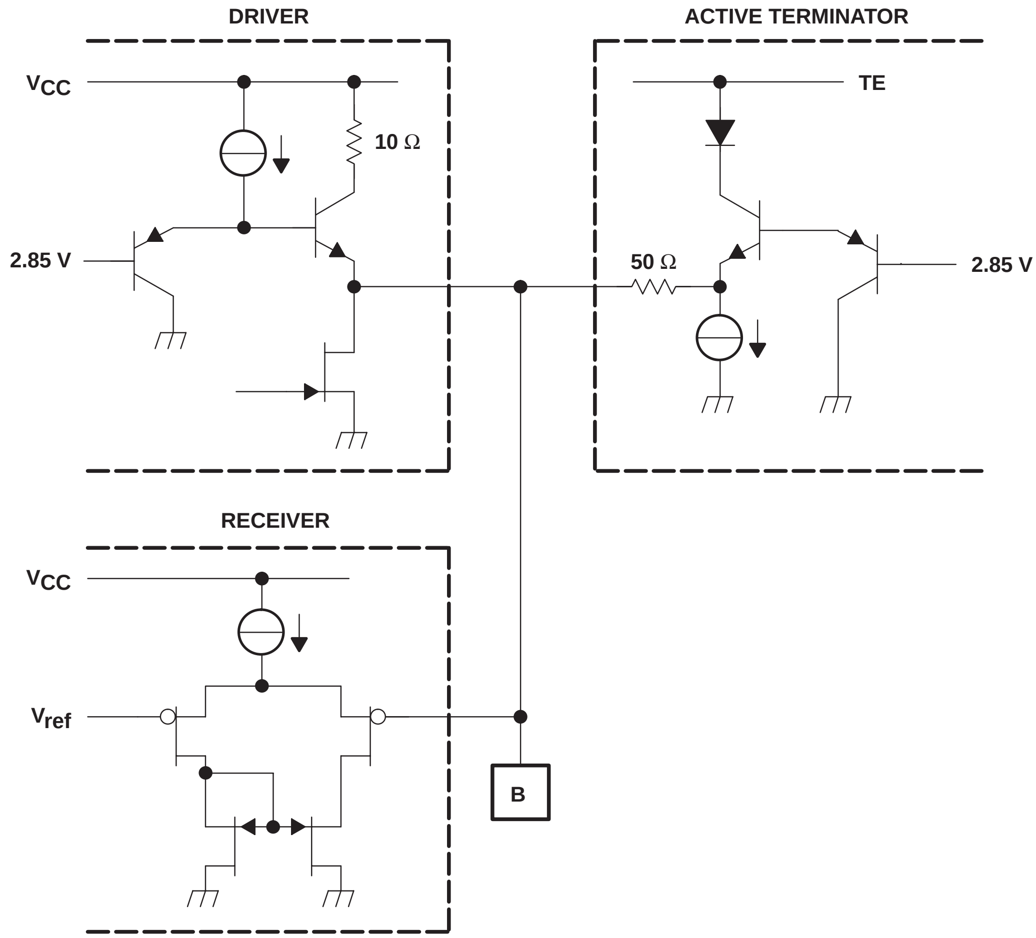


FUNCTION TABLE

	INPUTS					OUTPUTS	
	CE	**DE/RE_n**	**A**	**B**	**TE**	**A**	**B**
Terminator	L	X	X	X	GND	Z	Z
	L	X	X	X	Open	Z	Z
	L	X	X	X	V_{TE}	Z	−24 mA
Driver	H	H	L	NA	GND	Z	H
	H	H	L	NA	Open	Z	Z
	H	H	L	NA	V_{TE}	Z	−24 mA
	H	H	H	NA	GND	Z	L
	H	H	H	NA	Open	Z	L
	H	H	H	NA	V_{TE}	Z	L
Receiver	H	L	NA	L	GND	H	Z
	H	L	NA	L	Open	H	Z
	H	L	NA	L	V_{TE}	H	−24 mA
	H	L	NA	H	GND	L	Z
	H	L	NA	H	Open	L	Z
	H	L	NA	H	V_{TE}	L	−24 mA

NOTE: Input A defaults to a high-level and input B a low-level if left open circuited.
−24 mA = current-mode termination
GND = Ground
H = High L = Low
NA = Not applicable
Open = Open circuit
V_{TE} = Termination power
X = Don’t care
Z = High-impedance

schematics



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, V_{CC1}, V_{TE} (see Note 1)	−0.5 V to 7 V
Input voltage range, V_I (A-side)	V_{CC1} + 0.3 V
Bus voltage range (B-side)	−0.5 V to 7 V
Data I/O and control (A-side) voltage range	−0.5 V to 7 V
Continuous power dissipation (see Note 2)	Internally Limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating-junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

† Derating factors are the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{CC1} (see Note 3)		3		5.25	V
Termination voltage, V_{TE}		4.25		5.25	V
High-level input voltage, V_{IH}	DE/$\overline{RE}$, CE, A, B	2			V
Low-level input voltage, V_{IL}	DE/$\overline{RE}$, CE, A, B			0.8	V
High-level output current, I_{OH}	A			−8	mA
Low-level output current, I_{OL}	B			48	mA
	A			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: All electrical characteristics are measured with $V_{CC1} = V_{CC}$ unless otherwise noted.

driver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -20$ mA		2		V
V_{OL}	Low-level output voltage	$I_{OL} = 48$ mA			0.5	V
I_{IH}	High-level input current	$V_{IH} = 2$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	µA
I_{IL}	Low-level input current, A	$V_{IL} = 0.5$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	µA
I_{OZ}	High-impedance-state output current	$V_O = 5.25$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	µA
		$V_O = 0$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	

termination electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(OC)}$	Open-circuit output voltage	$I_O = 0$ mA,	$V_{CC} = V_{CC1} = 0$ V	2.5	2.85	3.24	V
I_O	Output current	$V_O = 0$ V,	$V_{CC} = V_{CC1} = 0$ V			−24	mA
		$V_O = 0.5$ V,	$V_{CC} = V_{CC1} = 0$ V	−20		−24	mA
		$V_O = 3$ V,	$V_{CC} = V_{CC1} = 0$ V			100	µA
		$V_O = 4$ V,	$V_{CC} = V_{CC1} = 0$ V	2		12	mA

receiver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −8 mA	2	2.5		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.8	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = V_{CC1}$	1.2	1.6	2	V
V_{IT-}	Negative-going input threshold voltage		0.8	1.1	1.4	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)		0.2	0.5		V
I_{IH}	High-level input current	V_{IH} = 2 V			100	µA
I_{IL}	Low-level input current	V_{IL} = 0.5 V			100	µA
I_{OZ}	High-impedance-state output current	V_O = 0 V			−100	µA
		V_O = 5.25 V			−100	

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current to V_{CC} and V_{CC1}	All drivers, receivers, and terminator disabled	All inputs at 0 V		1.3	3	mA
		All receivers enabled, termination and drivers disabled, No load	CE at V_{CC}, DE/$\overline{RE}$ at 0 V, TE at 0 V		14	21	
		All drivers enabled, termination and receivers disabled, No load	DE/$\overline{RE}$ and CE at V_{CC}, A and TE at 0 V		33	45	
			DE/$\overline{RE}$ and CE at V_{CC}, V_{TE} = 0 V, A at V_{CC1}		15	21	
I_{CC}	Supply current to TE	Termination and receivers enabled, No load	TE at V_{TE}, DE/$\overline{RE}$ at 0 V		33	45	
C_o	Bus port capacitance (see Note 4)				13.5	16.5	pF
I_{IH}	High-level input current	DE/$\overline{RE}$, CE	$V_{IH} = V_{CC}$ or 2 V			100	µA
I_{IL}	Low-level input current	DE/$\overline{RE}$, CE	V_{IL} = 0.5 V			100	µA

† All typical values are at $V_{CC} = V_{CC1}$ = 5 V, T_A = 25°C.
NOTE 4: Tested in accordance with Annex G X3T9.2/855D, revision 14

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output (see Figure 4)	C_L = 15 pF		10		35	ns
t_{PLH}	Propagation delay time, low- to high-level output (see Figure 4)	C_L = 15 pF		15		45	ns
$t_{sk(lim)}$	Skew limit‡, the maximum delay time − minimum delay time	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, C_L = 15 pF				14	ns
		V_{CC} = V_{CC1} = 5 V, T_A = 70°C, C_L = 15 pF				14	ns
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	V_{CC} = V_{CC1} = 5 V, T_A = 25°C			8		ns
t_t	Output transition time, 10% to 90% or 90% to 10% of the steady-state output	15 pF < C_L < 100 pF		5		20	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output (see Figure 5)	From CE,	C_L = 15 pF	5		150	ns
		From DE/$\overline{RE}$,	C_L = 15 pF			45	
t_{PZL}	Propagation delay time, high-impedance to low-level output (see Figure 5)	From CE,	C_L = 15 pF	5		150	ns
		From DE/$\overline{RE}$,	C_L = 15 pF			45	

† All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.
‡ The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

receiver switching characteristics over recommended of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6		5		20	ns
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6		5		25	ns
$t_{sk(lim)}$	Skew limit‡, the maximum delay time − minimum delay time	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, See Figure 6				8.5	ns
		V_{CC} = V_{CC1} = 5 V, T_A = 70°C, See Figure 6				8.5	ns
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, See Figure 6			6		ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output	From CE,	See Figure 7	5		150	ns
		From DE/$\overline{RE}$,	See Figure 7			45	
t_{PZL}	Propagation delay time, high-impedance to low-level output	From CE,	See Figure 7	5		150	ns
		From DE/$\overline{RE}$,	See Figure 7			80	
t_{PHZ}	Propagation delay time, high-level to high-impedance output	From CE,	See Figure 8	5		150	ns
		From DE/$\overline{RE}$,	See Figure 8			45	
t_{PZH}	Propagation delay time, high-impedance to high-level output	From CE,	See Figure 8	5		150	ns
		From DE/$\overline{RE}$,	See Figure 8			80	

† All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.
‡ The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W
T_{JS}	Junction-shutdown temperature			180		°C

PARAMETER MEASUREMENT INFORMATION

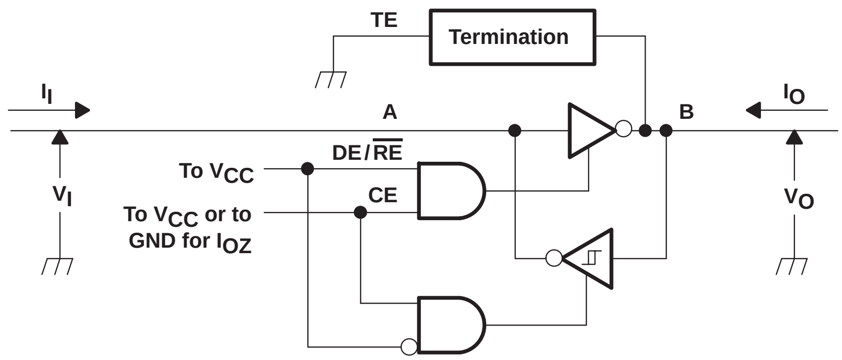


Figure 1. Driver Test Circuit Currents and Voltages.

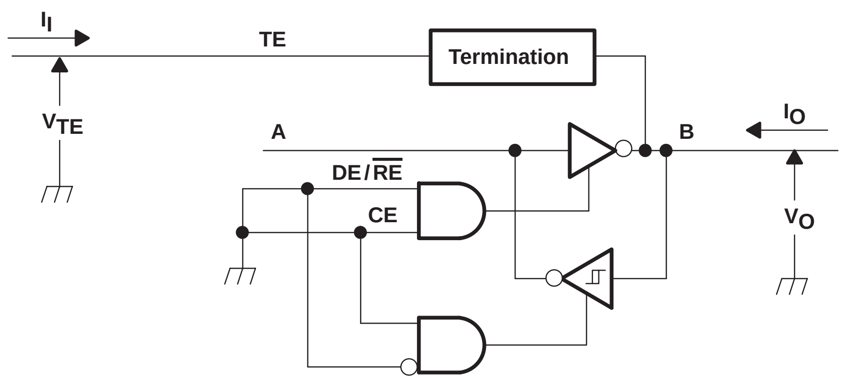


Figure 2. Active Termination Voltages, Currents, and Test Circuit.

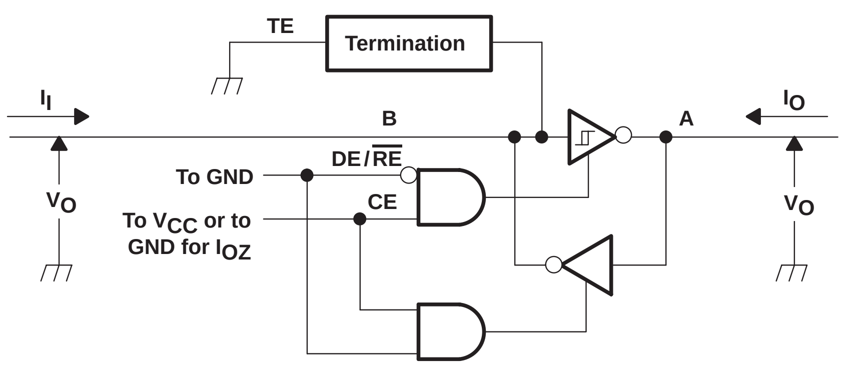
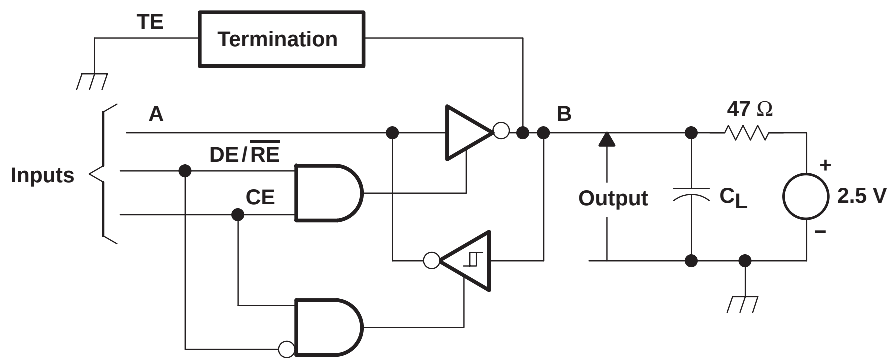
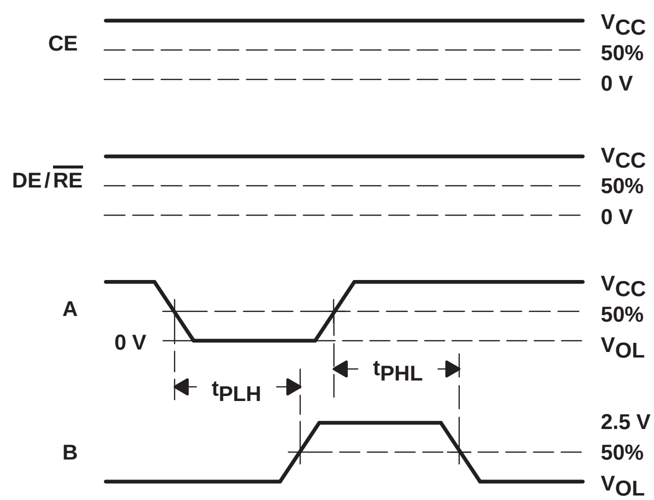


Figure 3. Receiver Voltages, Currents, and Test Circuit

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

PARAMETER MEASUREMENT INFORMATION

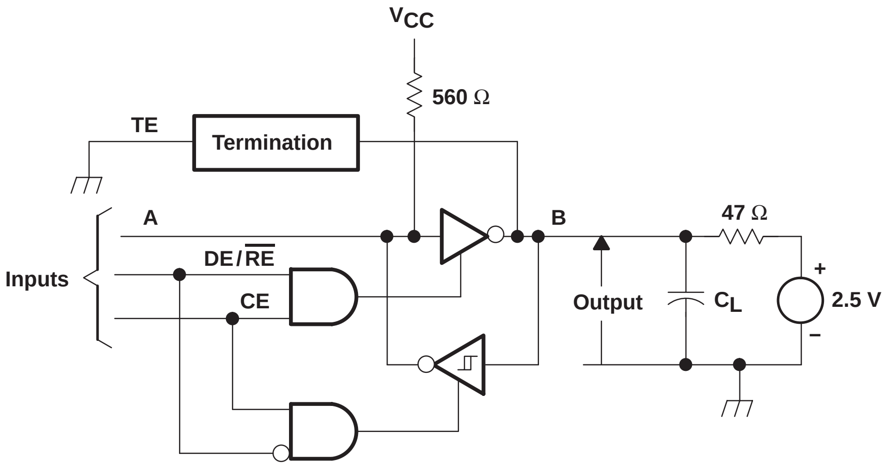


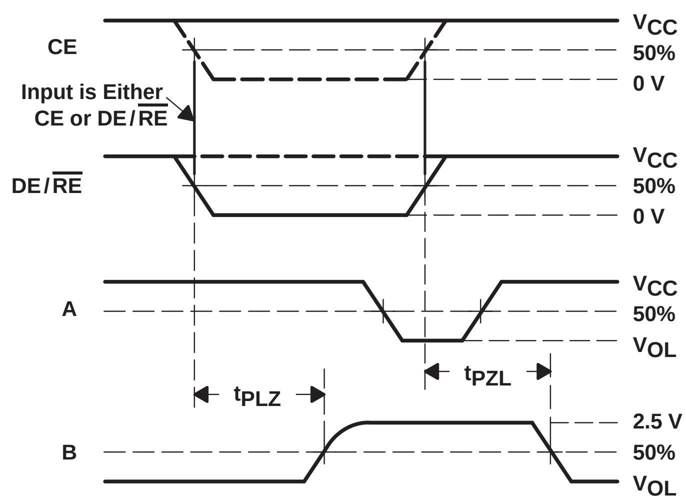


NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

Figure 4. Driver Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

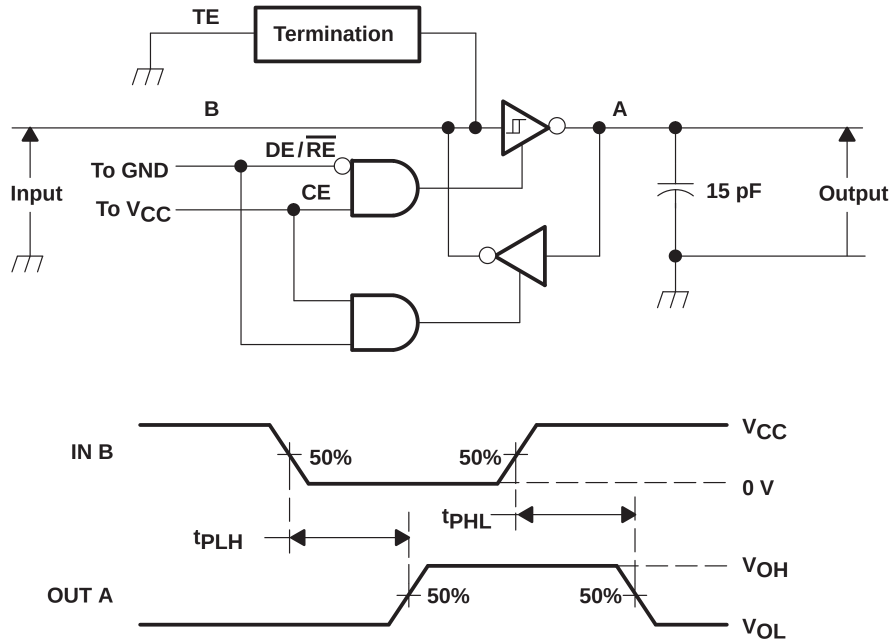




NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, PRR $\leq$ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

Figure 5. Driver Delay Time Test Circuit and Waveforms

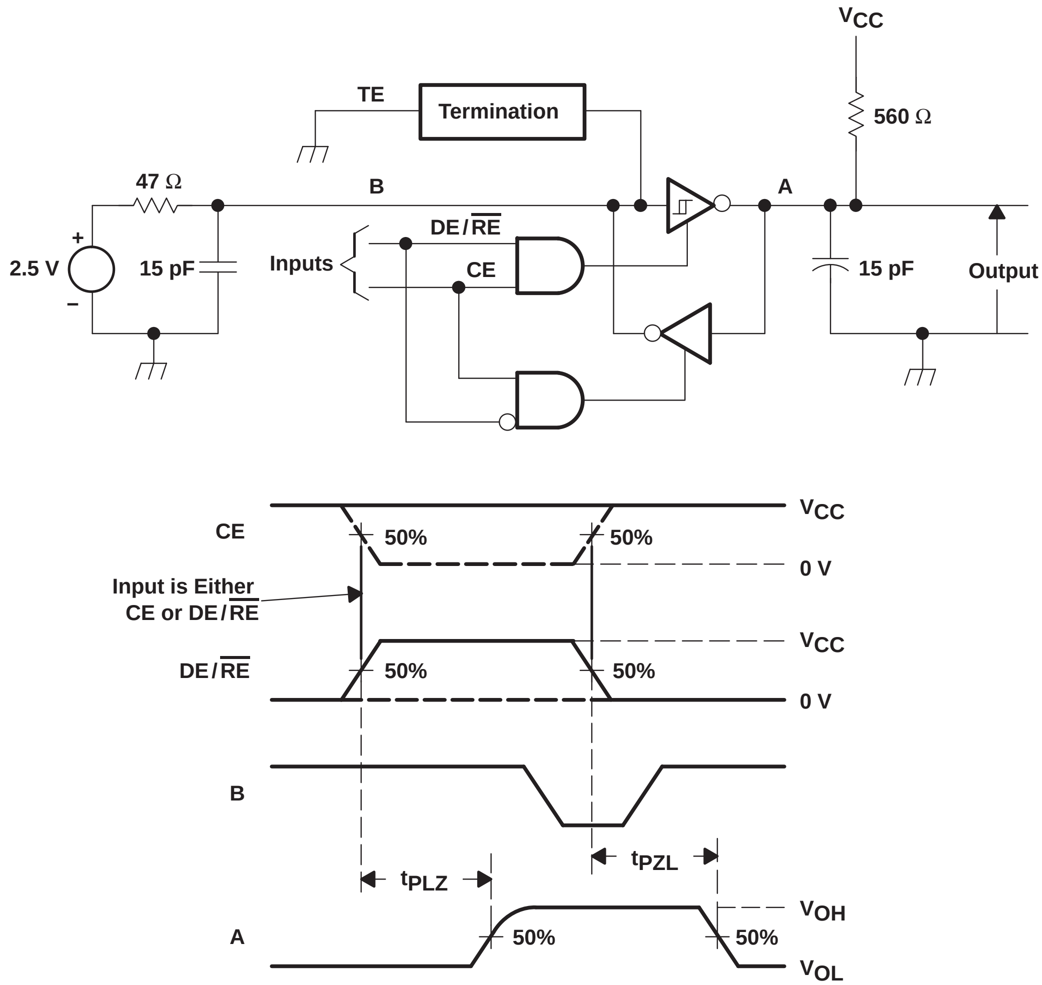
PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

Figure 6. Receiver Propagation Delay Time Test Circuit and Waveforms

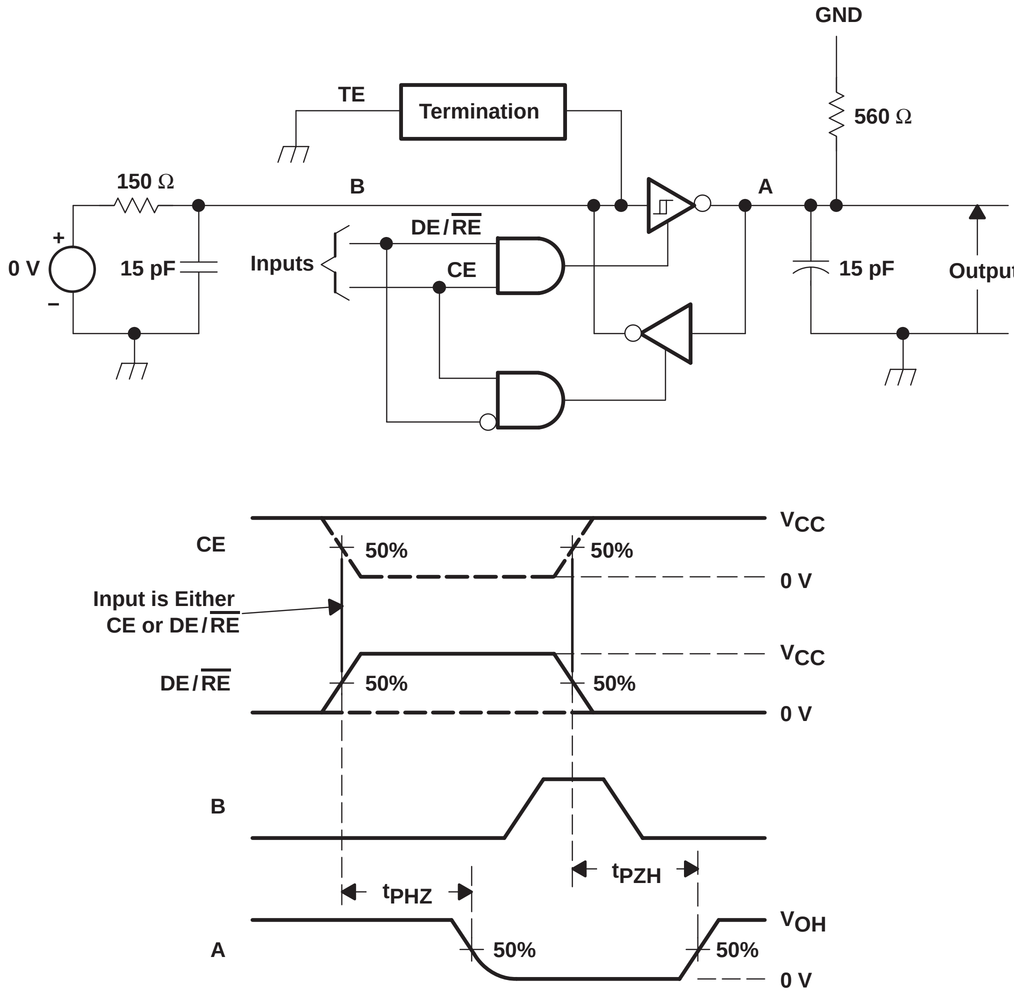
PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

Figure 7. Receiver Enable and Disable Times to and From Low-Level Output Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.

B. All resistances are in ohms and ±5%, unless otherwise indicated.

C. All capacitances are in picofarads and ±10%, unless otherwise indicated.

D. All indicated voltages are ±10 mV.

Figure 8. Receiver Enable and Disable Times to and From High-Level Output Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DRIVER AND TERMINATION
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

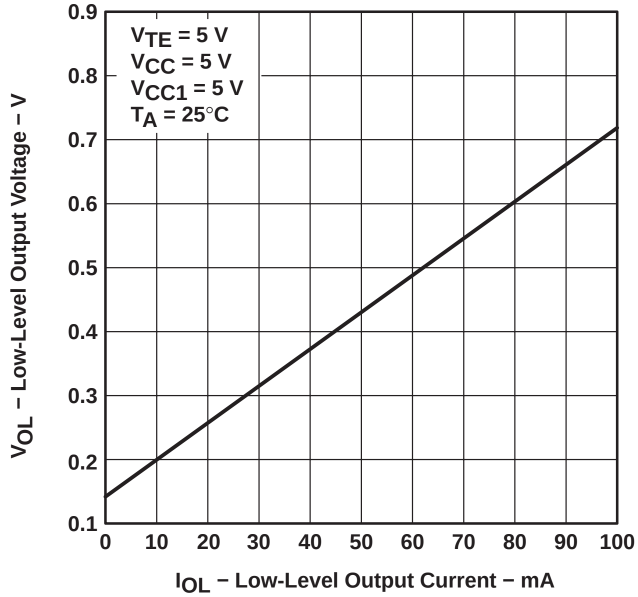


Figure 9

TERMINATION
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

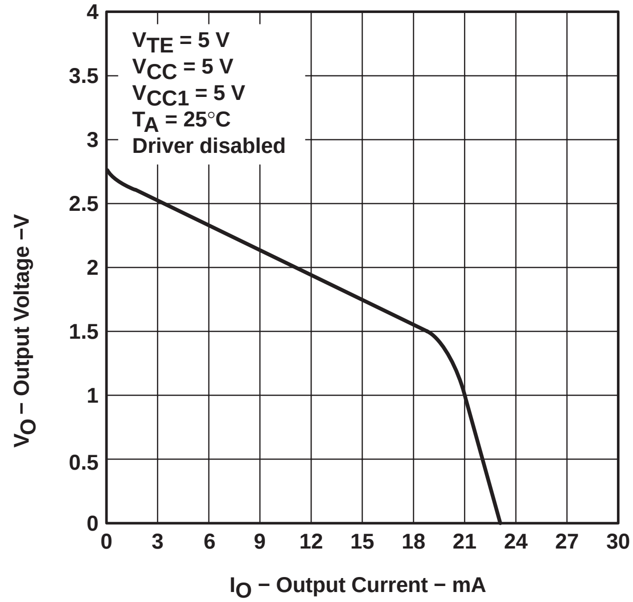


Figure 10

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

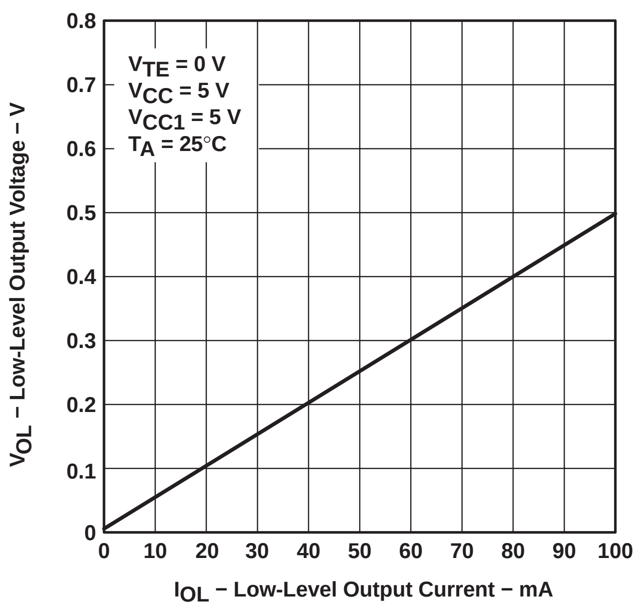


Figure 11

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

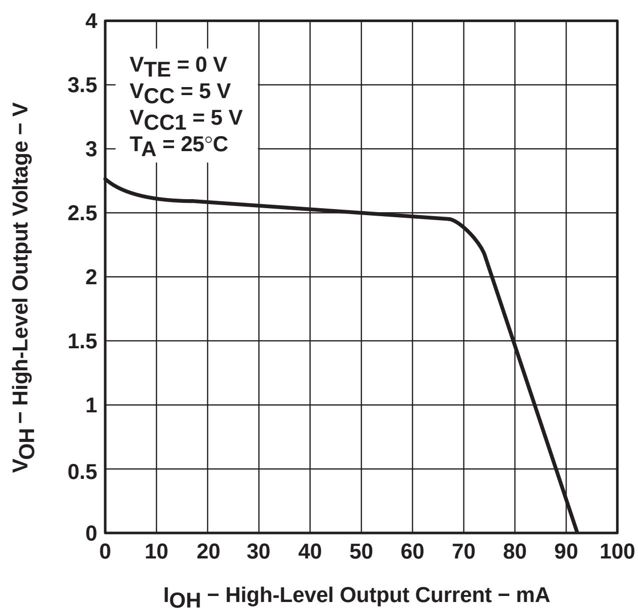


Figure 12

TYPICAL CHARACTERISTICS

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

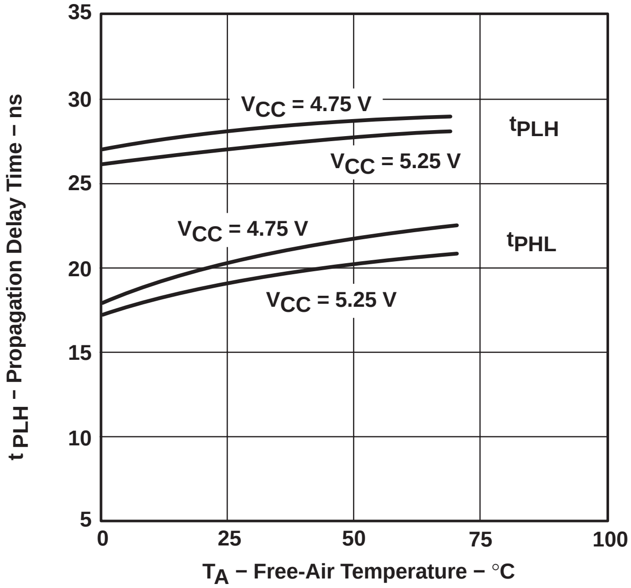


Figure 13

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

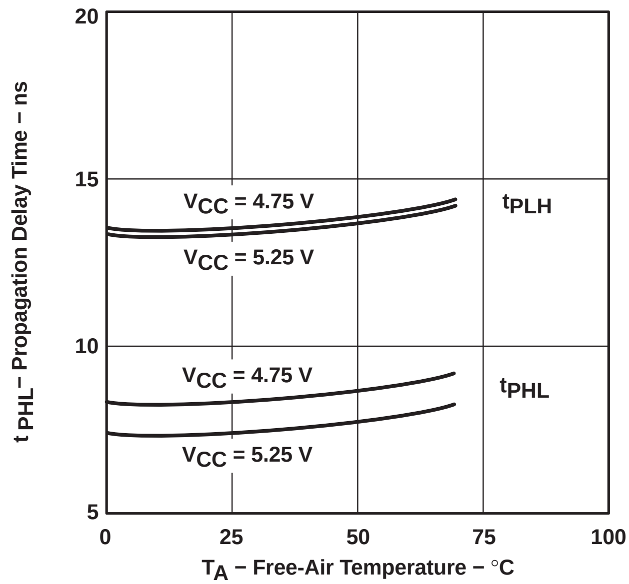


Figure 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75LBC968DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC968DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC968DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC968DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

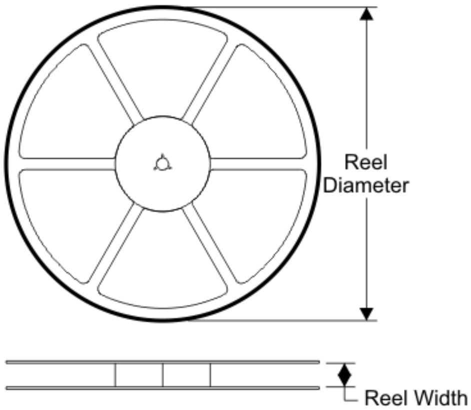
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

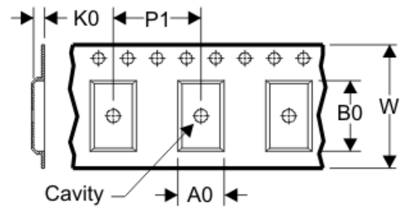
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

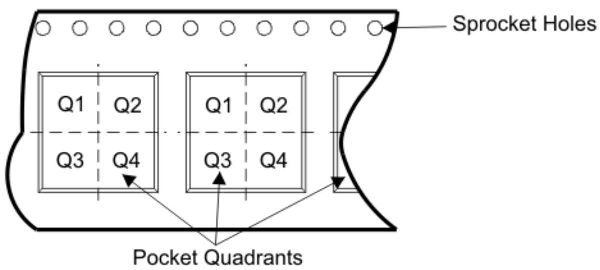


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

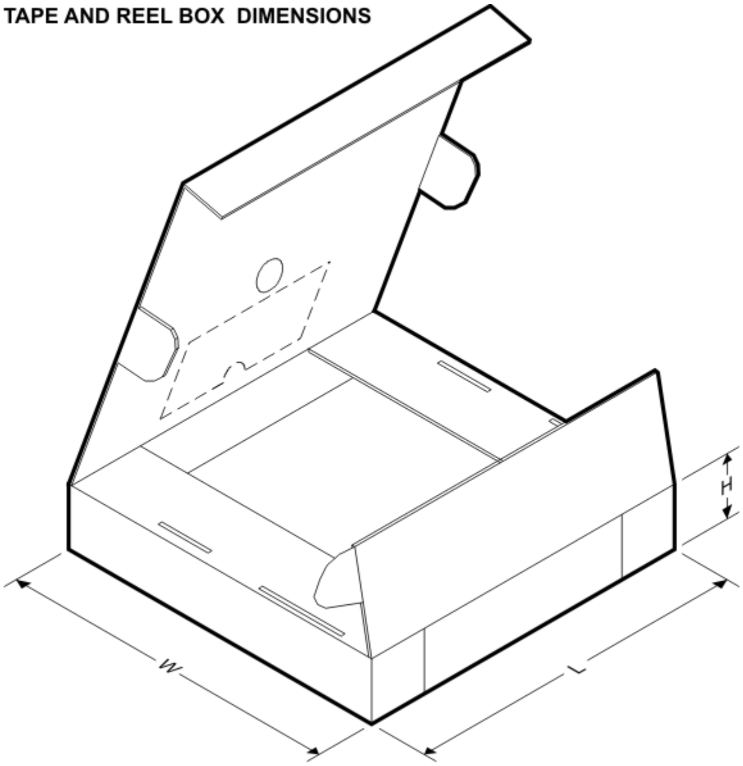
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC968DLR	DL	56	SITE 41	330	32	11.35	18.67	3.1	16	32	Q1

PACKAGE MATERIALS INFORMATION

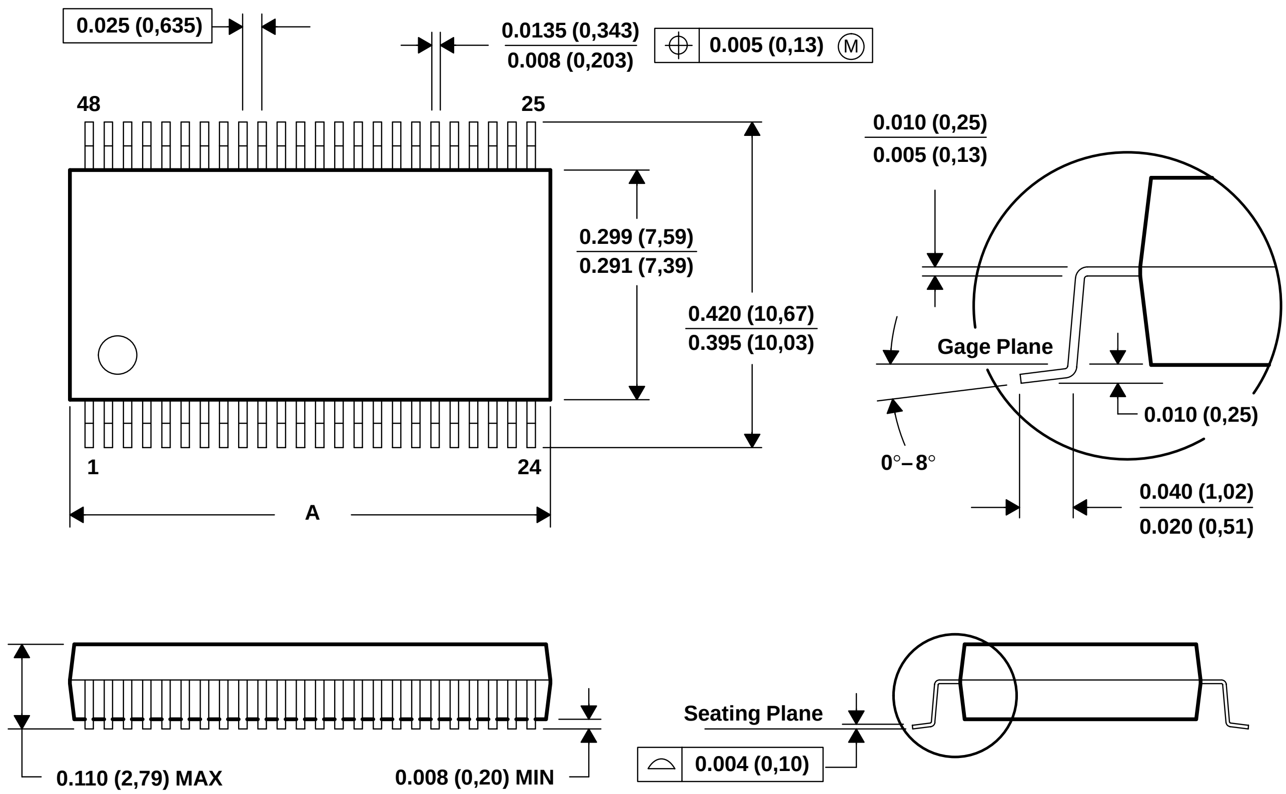
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN75LBC968DLR	DL	56	SITE 41	346.0	346.0	49.0

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118