

# DS90CR285-86ATQEVM User's Guide

## User's Guide



Literature Number: SNLU218  
September 2016

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## DS90CR285-86ATQEVM Evaluation Boards

### 1 Overview

The DS90CR285-86ATQEVM contains a Transmitter (Tx) board, a Receiver (Rx) board, and interfacing cables. This kit allows users to interface from test equipment or a graphics controller through Low Voltage Differential Signaling (LVDS) to a receiver board. The DS90CR285-86ATQEVM can be used for performance evaluation and initial system prototyping for multiple display applications.



**Figure 1. DS90CR285-86ATQEVM**

## 2 Features

- Operates with 20-66 MHz Parallel Clock
- Tx (DS90CR285) Board
  - Strokes on Incoming Data Rising Clock Edge
  - 30 x 2 LVCMOS Parallel Input Header Connectors with 0.08" (2-mm) Pitch
  - 10 x 2 LVDS Serial Output Header Connectors with 0.1" (2.54-mm) Pitch
- Rx (DS90CR286AT-Q1) Board
  - Strokes on Outgoing Data Rising Clock Edge
  - 30 x 2 LVCMOS Parallel Output Header Connectors with 0.08" (2-mm) Pitch
  - 10 x 2 LVDS Serial Input Header Connectors with 0.1" (2.54-mm) Pitch

## 3 Applications

- Video Displays
- Printers and Imaging
- Digital Video Transport
- Machine Vision
- RGB-to-OpenLDI or Open LDI-to RGB Bridge

## 4 Ordering Information

**Table 1. DS90CR285 and DS90CR286AT-Q1 Ordering Information**

EVM ID	DEVICE ID	DEVICE PACKAGE
DS90CR285	DS90CR285MTD/NOPB	DGG0056A
DS90CR286AT-Q1	DS90CR286ATDGGQ1	DGG0056A

## 5 Setup

This section describes the jumpers and connectors on the EVM as well as how to connect, set up, and use the DS90CR285-86ATQEVM. When operating the DS90CR285-86ATQEVM, signal inputs and outputs can be connected as shown in [Figure 2](#).

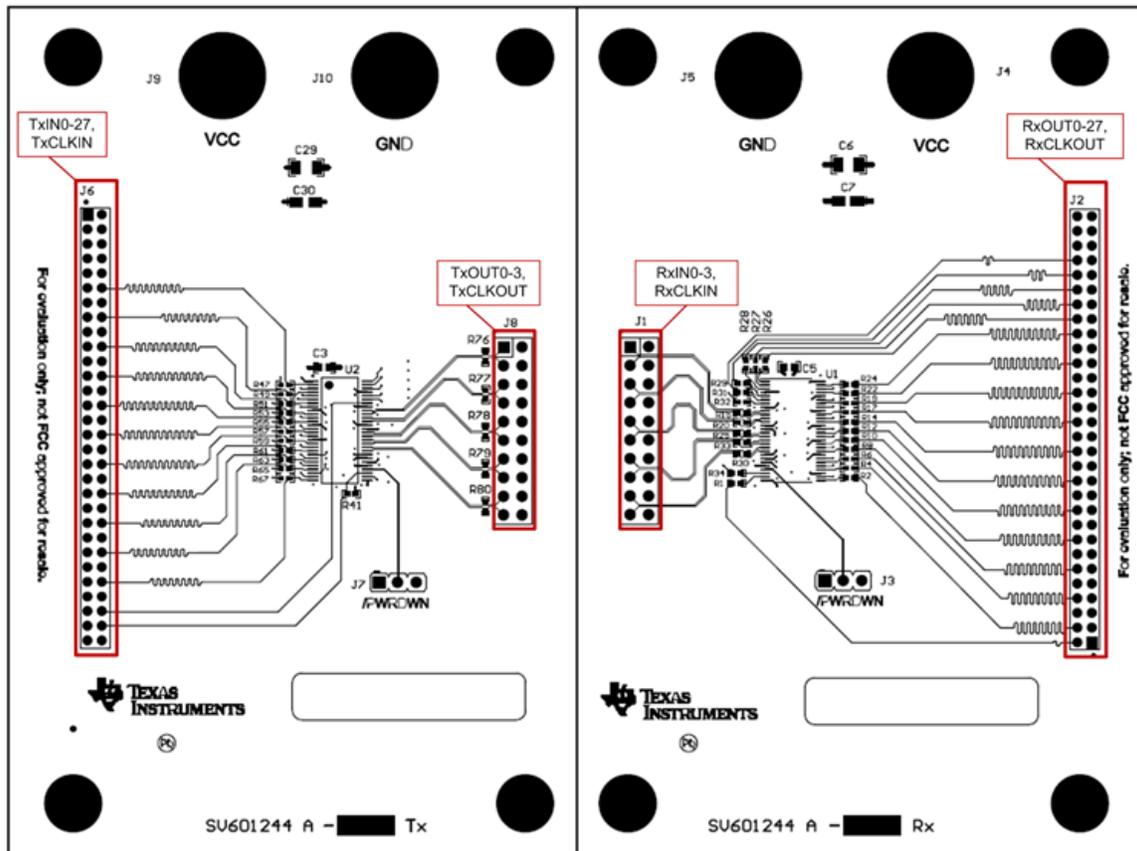


Figure 2. DS90CR285-86ATQEVM Input and Output Pins

On both Tx and Rx boards, the ICs can be enabled or disabled by the /PWRDWN pin setting on J7 and J3, respectively, as shown in [Figure 2](#). Jumpers on both devices should be placed in the “ON” state by default.



Figure 3. /PWRDWN Pin Settings

## 5.1 Tx Board Connections

### 5.1.1 Pin Mapping for IDC Connectors

Table 2 and Table 3 illustrate how the Tx inputs and outputs are mapped to the IDC connectors (J6, J8). Note that the inputs and outputs are also labeled on the back of the Tx board.

**Table 2. 60-Pin 0.08" Pitch IDC Connector (J6)**

<b>GND</b>	TxIN0
GND	TxIN1
GND	TxIN2
GND	TxIN3
GND	TxIN4
GND	TxIN5
GND	TxIN6
GND	TxIN7
GND	TxIN8
GND	TxIN9
GND	TxIN10
GND	TxIN11
GND	TxIN12
GND	TxIN13
GND	TxIN14
GND	TxIN15
GND	TxIN16
GND	TxIN17
GND	TxIN18
GND	TxIN19
GND	TxIN20
GND	TxIN21
GND	TxIN22
GND	TxIN23
GND	TxIN24
GND	TxIN25
GND	TxIN26
GND	TxIN27
GND	TxCLKIN
GND	GND

**Table 3. 20-Pin 0.1" Pitch IDC Connector (J8)**

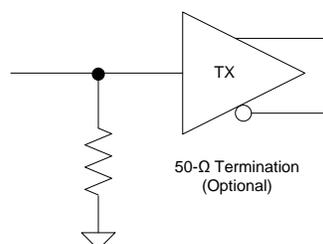
<b>TxOUT0-</b>	GND
TxOUT0+	GND
TxOUT1-	GND
TxOUT1+	GND
TxOUT2-	GND
TxOUT2+	GND
TxCLKOUT-	GND
TxCLKOUT+	GND
TxOUT3-	GND
TxOUT3+	GND

### 5.1.2 Tx Board Optional: 50-Ω Termination for TxIN

On the Tx demo board, the 29 inputs have an option for 50-Ω terminations. There are 0402 pads for this purpose. One side is connected to the signal line, and the other side is tied to ground. These pads are unpopulated from the factory but are provided if the user needs to install a 50-Ω termination for some test equipment. Mapping of transmitter inputs for the optional termination resistors is shown in [Table 4](#), and a schematic of the termination is shown in [Figure 4](#).

**Table 4. Tx Pin and Optional Termination Resistor Mapping**

Tx PIN NAMES	Tx PIN NUMBER	TERMINATION RESISTOR
TxIN0	51	R41
TxIN1	52	R42
TxIN2	54	R43
TxIN3	55	R44
TxIN4	56	R45
TxIN5	2	R46
TxIN6	3	R47
TxIN7	4	R48
TxIN8	6	R49
TxIN9	7	R50
TxIN10	8	R51
TxIN11	10	R52
TxIN12	11	R53
TxIN13	12	R54
TxIN14	14	R55
TxIN15	15	R56
TxIN16	16	R57
TxIN17	18	R58
TxIN18	19	R59
TxIN19	20	R60
TxIN20	22	R61
TxIN21	23	R62
TxIN22	24	R63
TxIN23	25	R64
TxIN24	27	R65
TxIN25	28	R66
TxIN26	30	R67
TxIN27	50	R68
TxCLKIN	31	R69



**Figure 4. Schematic of Optional Parallel Input 50-Ω Termination to GND**

## 5.2 Rx Board Connections

### 5.2.1 Pin Mapping for IDC Connectors

Table 5 and Table 6 illustrate how the Rx inputs and outputs are mapped to the IDC connectors (J1, J2). Note that the inputs and outputs are also labeled on the back of the Rx board.

**Table 5. 20-Pin 0.1" Pitch IDC Connector (J1)**

<b>RxIN0-</b>	GND
RxIN0+	GND
RxIN1-	GND
RxIN1+	GND
RxIN2-	GND
RxIN2+	GND
RxCLKIN-	GND
RxCLKIN+	GND
RxIN0-	GND
RxIN3+	GND

**Table 6. 60-Pin 0.08" Pitch IDC Connector (J2)**

GND	GND
RxCLKOUT	GND
RxOUT27	GND
RxOUT26	GND
RxOUT25	GND
RxOUT24	GND
RxOUT23	GND
RxOUT22	GND
RxOUT21	GND
RxOUT20	GND
RxOUT19	GND
RxOUT18	GND
RxOUT17	GND
RxOUT16	GND
RxOUT15	GND
RxOUT14	GND
RxOUT13	GND
RxOUT12	GND
RxOUT11	GND
RxOUT10	GND
RxOUT9	GND
RxOUT8	GND
RxOUT7	GND
RxOUT6	GND
RxOUT4	GND
RxOUT3	GND
RxOUT2	GND
RxOUT1	GND
RxOUT0	<b>GND</b>

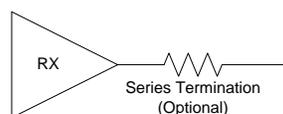
### 5.2.2 Rx Board Optional: Termination for RxOUT

On the Rx demo board, there are 29 outputs that have an 0402 pad in series. These pads are populated from the factory with 0-Ω resistors, and they can be replaced with 450-Ω series resistors if necessary. This is required if directly connecting to 50-Ω inputs on a scope. R1 to R28 are associated with the DATA output lines. R29 is associated with CLKOUT. The total load presented to the receiver output is 500 Ω (450 Ω + 50 Ω). The waveform on the scope is 1/10 of the signal due to the resulting voltage divider (50 / (450 + 50)).

Optional series termination resistor mapping is shown in [Table 7](#), and a schematic of the series resistance is shown in [Figure 5](#).

**Table 7. Tx Pin and Optional Termination Resistor Mapping**

Rx PIN NAMES	Rx PIN NUMBER	TERMINATION RESISTOR
RxOUT0	27	R1
RxOUT1	29	R2
RxOUT2	30	R3
RxOUT3	32	R4
RxOUT4	33	R5
RxOUT5	34	R6
RxOUT6	35	R7
RxOUT7	37	R8
RxOUT8	38	R9
RxOUT9	39	R10
RxOUT10	41	R11
RxOUT11	42	R12
RxOUT12	43	R13
RxOUT13	45	R14
RxOUT14	46	R15
RxOUT15	47	R16
RxOUT16	49	R17
RxOUT17	50	R18
RxOUT18	51	R19
RxOUT19	53	R20
RxOUT20	54	R21
RxOUT21	55	R22
RxOUT22	1	R23
RxOUT23	2	R24
RxOUT24	3	R25
RxOUT25	5	R26
RxOUT26	6	R27
RxOUT27	7	R28
RxCLKOUT	26	R29



**Figure 5. Schematic of Optional Series Output 450-Ω Termination**

## 6 Typical Connection Setup

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from a 60-pin IDC connector with 0.08" (2-mm) pitch. The TxOUT and RxIN interface uses a 20-pin IDC connector with 0.1" (2.54-mm) pitch through a IDC ribbon cable. Please follow these steps to set up the evaluation kit for bench testing and performance measurements with a graphics card source and display panel:

1. Connect one end of the 20-pin IDC cable to the Tx board and the other end to the Rx board. Longer lengths than the IDC cable provided with the EVM can be used.
2. Jumpers have been pre-configured by factory default. They should not require any changes for operation of the chipset. Reference [Figure 6](#) for default jumper settings.

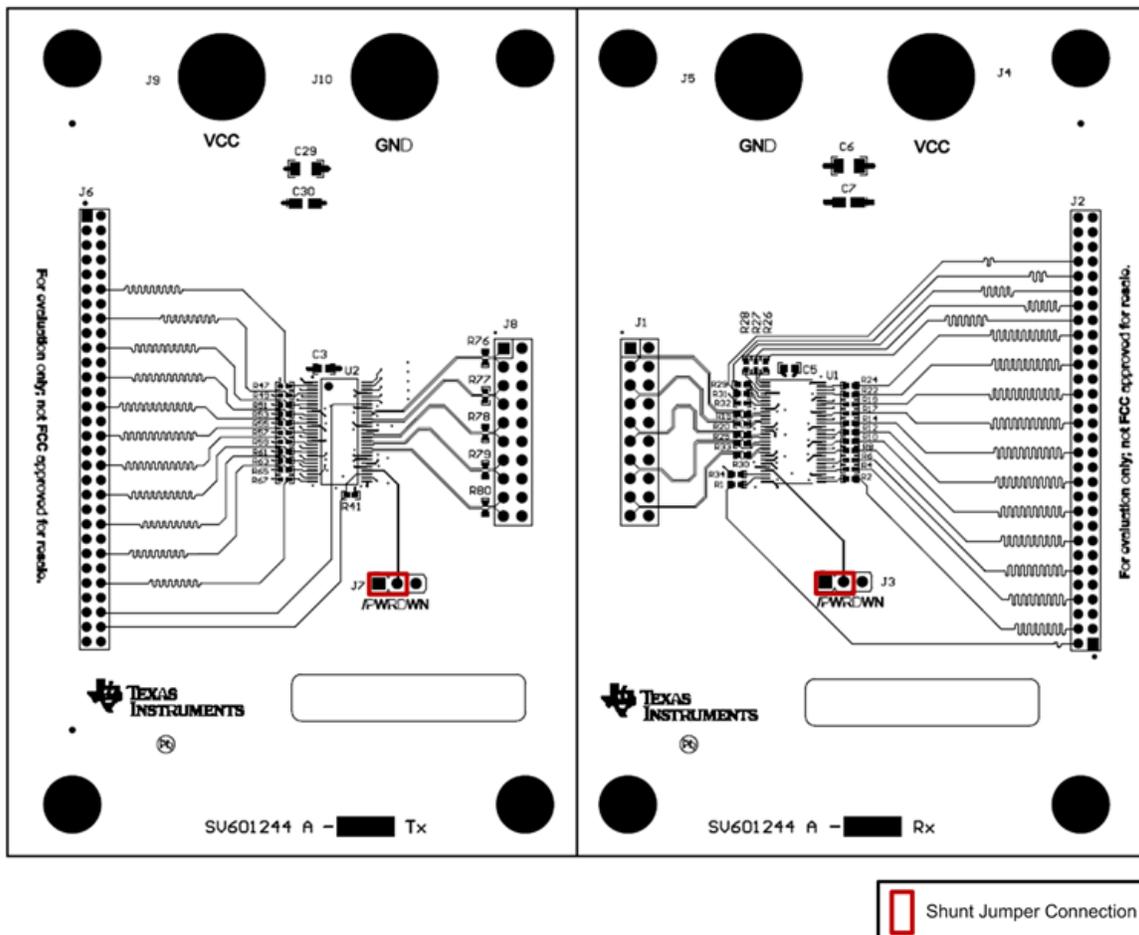


Figure 6. DS90CR285-86ATQEVm Default Jumper Pin Settings

3. From a graphics card or other video source, connect a flat (ribbon) cable to the Tx board and connect another flat cable from the Rx board to the display panel. Note that pin 1 on the connector should be connected to pin 1 of the cable. A scramble cable may be required.
4. Power for the Tx and Rx boards must be supplied externally by applying a 3.3-V Vcc supply to J9 and J5. GND should be applied to J10 and J4.

## 7 Typical Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Tx inputs (similar equipment can be used):

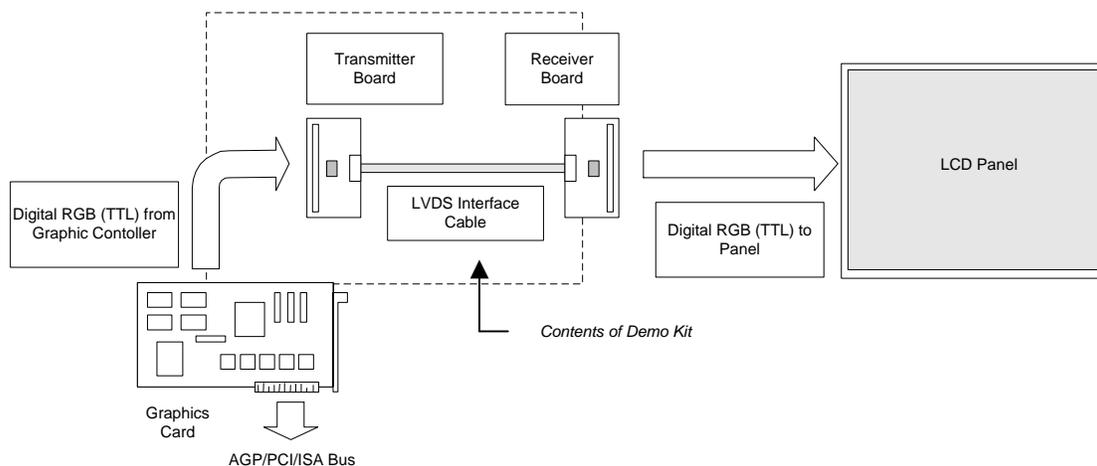
1. Graphics card or GUI controller with digital RGB (LVTTTL) output.
2. TEK HFS9009 - This pattern generator along with 9DG2 Cards may be used to generate input signals and also the clock signal.
3. TEK DG2020 - This generator may also be used to generate data and clock signals.
4. TEK MB100 BERT - This bit error rate tester may be used for both signal source and receiver.
5. Any other signal / pattern generator that generates the correct input levels as specified in the DS90CR285 datasheet.

The following is a list of typically test equipment that may be used to monitor the output signals from the Rx outputs (similar equipment can be used):

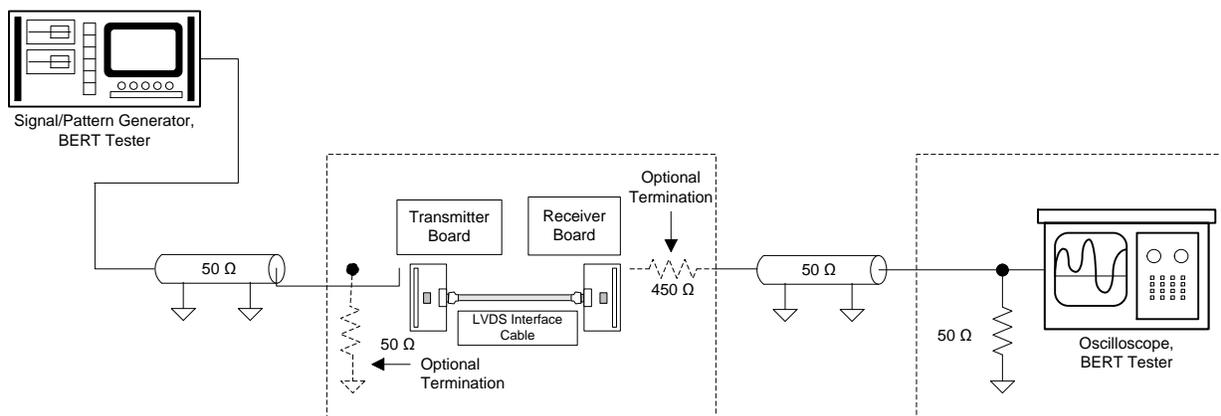
1. LCD Display Panel which supports digital RGB (LVTTTL) inputs.
2. TEK MB100 BERT - Receiver.
3. Any SCOPE with 50- $\Omega$  inputs or high impedance probes.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes. Ensure that, when measuring LVDS signals that the measurement is taken across a 100- $\Omega$  differential termination resistor.

Figure 7 and Figure 8 show typical applications to use the DS90CR285-86ATQEVM demo boards.



**Figure 7. Typical Channel-Link I Setup for Graphics Card and LCD Panel Application**



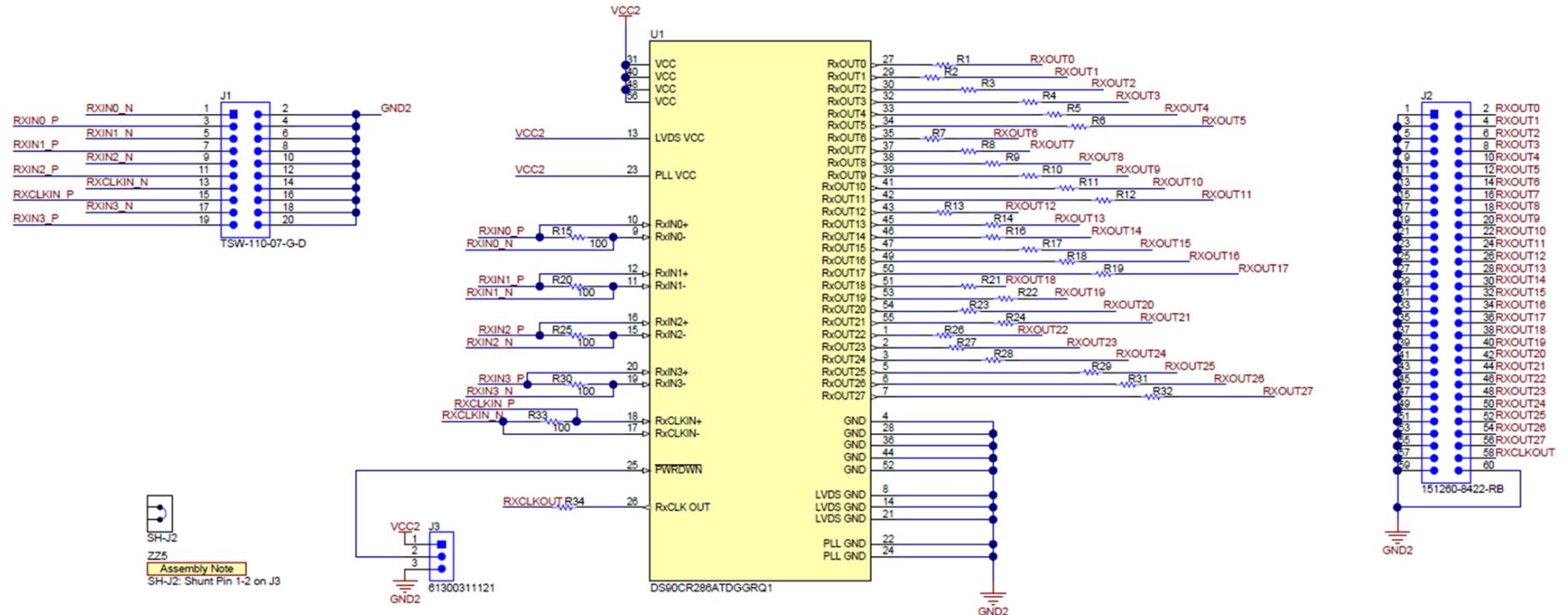
**Figure 8. Typical Test Setup With Generator and Scope**

## 8 Bill of Materials

Rx	Tx	DESIGNATOR	VALUE	DESCRIPTION	PART NUMBER
1	0	C1	1000 pF	CAP, CERM, 1000 pF, 50 V, ±5%, C0G/NP0, 0805	GRM2165C1H102JA01D
3	0	C2, C9, C13	0.01 µF	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0402	C1005X7R1C103K050BA
1	0	C5	22 µF	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603	C1608X5R0J226M080AC
0	1	C3			
4	0	C4, C6, C10, C14	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 5%, X7R, 1206	C1206C104J5RACTU
0	1	C29			
1	0	C7	10 µF	CAP, TA, 10 µF, 63 V, +/- 10%, 1 Ω, SMD	293D106X9063E2TE3
0	1	C30			
2	0	C8, C12	1000 pF	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0805	08055A102FAT2A
0	3	C17, C21, C25			
0	3	C18, C22, C26	0.01 µF	CAP, CERM, 0.01 µF, 250 V, +/- 10%, X7R, 0805	GRM21BR72E103KW03L
0	3	C19, C23, C27	0.1 µF	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X7R, 0402	GRM155R70J104KA01D
4	0	H3, H4, H13, H14		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH
0	4	H1, H2, H15, H16			
4	0	H5, H6, H7, H8			
0	4	H9, H10, H11, H12			
1	0	J1	10x2	Header, 100mil, 10x2, Gold, TH	TSW-110-07-G-D
0	1	J8			
1	0	J2	30x2	Header, 2mm, 30x2, Gold, TH	151260-8422-RB
0	1	J6			
1	0	J3	3x1	Header, 2.54 mm, 3x1, Gold, TH	61300311121
0	1	J7			
2	0	J4, J5		Standard Banana Jack, Uninsulated, 15 A	108-0740-001
0	2	J9, J10			
29	0	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R16, R17, R18, R19, R21, R22, R23, R24, R26, R27, R28, R29, R31, R32, R34	0 Ω	RES, 0, 5%, 0.063 W, 0402	ERJ-2GE0R00X
5	0	R15, R20, R25, R30, R33	100 Ω	RES, 100, 1%, 0.063 W, 0402	CRCW0402100RFKED
1	0	SH-J2	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN
0	1	SH-J1			
1	0	U1		3.3-V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link 66 MHz, DGG0056A	DS90CR286ATDGGRQ1
0	1	U2		+3.3-V Rising Edge Data Strobe LVDS 28-Bit Channel - 66 MHz, 56-pin TSSOP, Pb-Free	DS90CR285MTD/NOPB
0	0	FID1, FID2, FID3		Fiducial mark. There is nothing to buy or mount.	N/A
0	0	R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69	49.9 Ω	RES, 49.9, 1%, 0.063 W, 0402	CRCW040249R9FKED
0	0	R76, R77, R78, R79, R80	100 Ω	RES, 100, 1%, 0.063 W, 0402	CRCW0402100RFKED

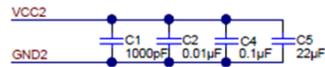


## 9.2 Rx Board Schematic

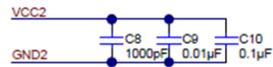


SH-J2  
Z25  
**Assembly Note**  
SH-J2: Shunt Pin 1-2 on J3

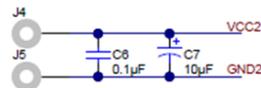
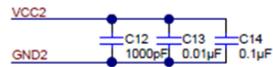
Place one cap near each of the DS90CR286AT-Q1 VCC pins. Larger value caps can be farther away from pins if space is limited.



Place one cap near each of the DS90CR286AT-Q1 LVDS VCC pins. Larger value caps can be farther away from pins if space is limited.



Place caps near each of the DS90CR286AT-Q1 PLL VCC pins. Larger value caps can be farther away from pins if space is limited.



## 10 EVM Layout

Figure 9 and Figure 10 show the Tx and Rx Board layout for the DS90CR285-86ATQEV. The DS90CR285-86ATQEV uses 0.08" (2-mm) IDC header pins to connect to parallel inputs of the DS90CR285 and parallel outputs of the DS90CR286AT-Q1. For the serial LVDS bit stream between boards, 0.1" (2.54-mm) IDC pin headers are used.

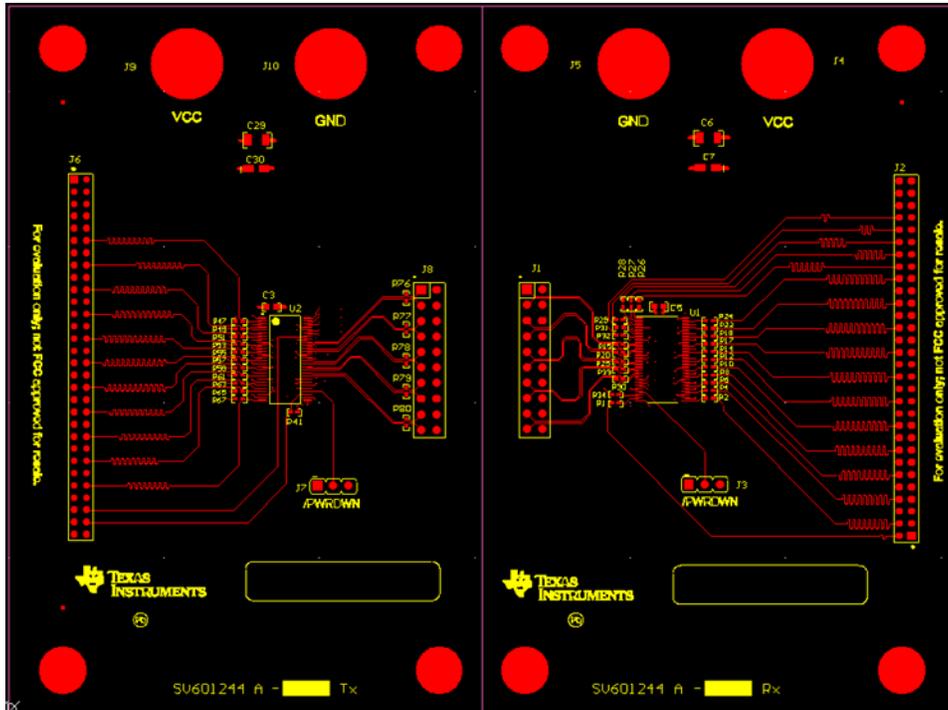


Figure 9. DS90CR285-86ATQEV Top Layer

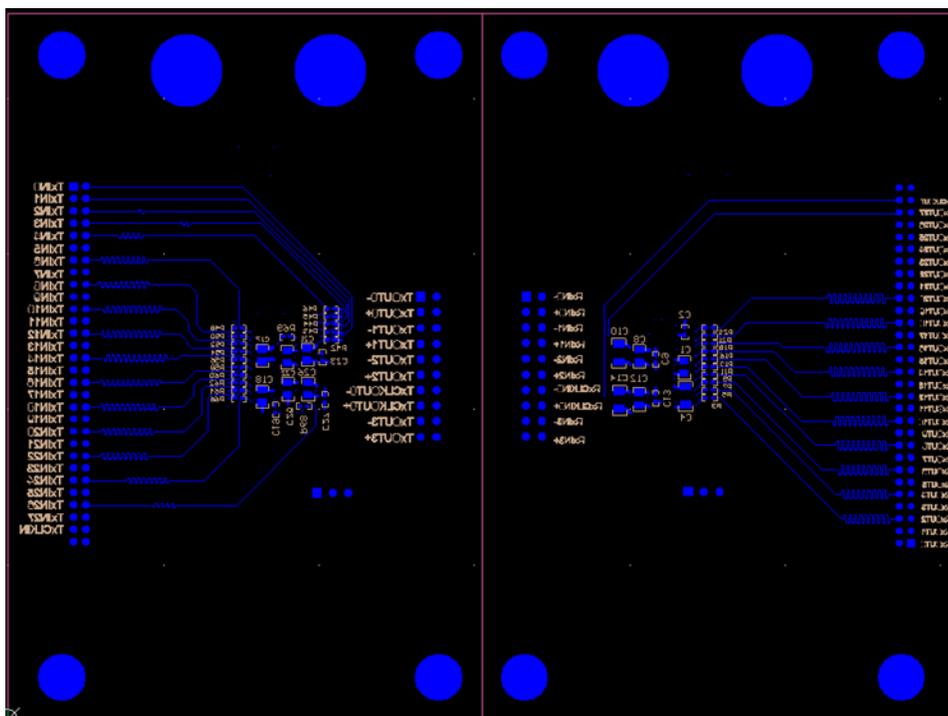


Figure 10. DS90CR285-86ATQEV Bottom Layer

**11 Document Revision History**

REVISION	COMMENTS	DATE
*	Initial creation of EVM User's Guide	September 2016

## STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.
  - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software
  - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
  - 2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
  - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.
  - 2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
  - 3.1 *United States*
    - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
    - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

### CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### FCC Interference Statement for Class A EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

## FCC Interference Statement for Class B EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

#### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

### 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。  
[http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page)

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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#### 4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

#### 4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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