User's Guide
SLVU973–September 2013

# Evaluation Module for the TPS54540-Q1 Step-Down Converter

This user's guide contains information for the TPS54540-Q1EVM-593 evaluation module (PWR593) including the performance specifications, schematic, and the bill of materials.

**Contents**



**List of Figures**



**List of Tables**

Eco-mode is a trademark of Texas Instruments.

# 1 Introduction

This user's guide contains background information for the TPS54540-Q1 as well as support documentation for the TPS54540-Q1EVM-593 evaluation module (PWR593). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54540-Q1EVM-593.

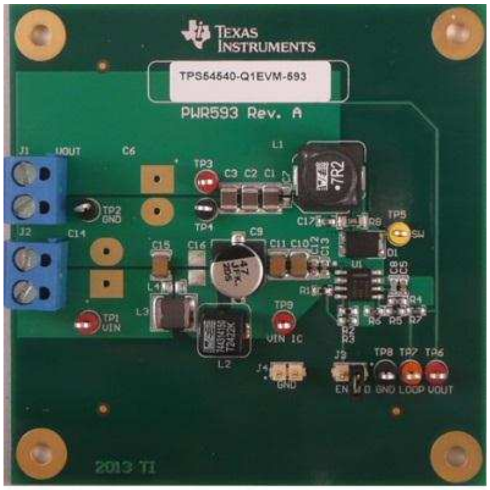



**Figure 1. TPS54540-Q1EVM-593 Board**

## 1.1 Background

The TPS54540-Q1 DC-DC converter is designed to provide up to a 5-A output from an input voltage source of 4.5 V to 42 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board (PCB) areas that may be achieved when designing with the TPS54540-Q1 regulator. The switching frequency is externally set at a nominal 400 kHz. This frequency was chosen to help with Electromagnetic Compatibility (EMC) by keeping the fundamental frequency out of the typical medium wave (MW) frequency range. The high-side MOSFET is incorporated inside the TPS54540-Q1 package along with the gate-drive circuitry. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS54540-Q1 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider. Lastly, the TPS54540-Q1EVM-593 includes additional input filtering and a snubber circuit to reduce emissions. The absolute maximum input voltage for the TPS54540-Q1EVM-593 is 42 V.

**Table 1. Input Voltage and Output Current Summary**

| EVM | Input Voltage Range | Output Current Range |
|---|---|---|
| TPS54540-Q1EVM-593 | $V_{IN}$ = 7.0 V to 42 V | $I_{OUT}$ = 0 A to 5 A |

## 1.2 Performance Specification Summary

A summary of the TPS54540-Q1EVM-593 (EVM) performance specifications is provided in Table 2. Specifications are given for an input voltage of $V_{IN}$ = 12 V and an output voltage of 5.0 V, unless otherwise specified. This EVM is designed and tested for $V_{IN}$ = 7.0 V to 42 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. TPS54540-Q1EVM-593 Performance Specification Summary**

| Specification | Test Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ voltage range | | | 7.0 | 12 | 42 | V |
| Output voltage set point | | | | 5.0 | | V |
| Output current range | $V_{IN}$ = 7.0 V to 42 V | | 0 | | 5 | A |
| Line regulation | $I_{OUT}$ = 5 A, $V_{IN}$ = 7.0 V to 42 V | | | ±0.02% | | |
| Load regulation | $V_{IN}$ = 12 V, $I_{OUT}$ = 0.001 A to 5 A | | | ±0.2% | | |
| Load transient response | $I_{OUT}$ = 1.3 A to 3.8 A | Voltage change | | -150 | | mV |
| | | Recovery time | | 200 | | µs |
| | $I_{OUT}$ = 3.8 A to 1.3 A | Voltage change | | 170 | | mV |
| | | Recovery time | | 300 | | µs |
| Loop bandwidth | $V_{IN}$ = 12 V, $I_{OUT}$ = 5 A | | | 18 | | kHz |
| Phase margin | $V_{IN}$ = 12 V, $I_{OUT}$ = 5 A | | | 72 | | ° |
| Input voltage ripple | $I_{OUT}$ = 5 A, 20 MHz BWL | | | 20 | | mVpp |
| Output voltage ripple | $I_{OUT}$ = 5 A, 20 MHz BWL | | | 5 | | mVpp |
| Output rise time | | | | 2.6 | | ms |
| Operating frequency | | | | 400 | | kHz |
| Maximum efficiency | TPS54540-Q1EVM-593, $V_{IN}$ = 12 V, $I_{OUT}$ = 1.3 A | | | 92.0% | | |
| DCM threshold | $V_{IN}$ = 12 V | | | 400 | | mA |
| Pulse skipping threshold | $V_{IN}$ = 12 V | | | 25 | | mA |
| No load input current | $V_{IN}$ = 12 V | | | 280 | | µA |
| UVLO start threshold | | | | 6.5 | | V |
| UVLO stop threshold | | | | 5.0 | | V |

## 1.3 Schematic

Figure 2 is the schematic for the EVM.

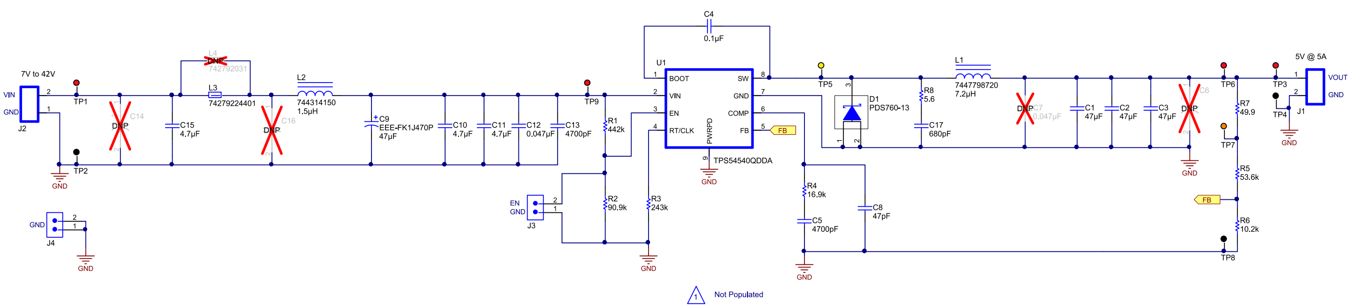



**Figure 2. TPS54540-Q1EVM-593 Schematic**

## *1.4 Modifications*

These evaluation modules are designed to provide access to the features of the TPS54540-Q1. Some modifications can be made to this module. Component selection for modifications can be done with the aid of WEBENCH or the excel spreadsheet (SLVC452) located on the product page.

### 1.4.1 Output Voltage Set Point

To change the output voltage of the EVM, the value of resistor R5 ($R_{HS}$) should be changed while keeping R6 ($R_{LS}$) fixed. The output voltage can be adjusted to a minimum of the 0.8 V internal reference. The value of R5 for a specific output voltage can be calculated using Equation 1:

$$R_{HS} = R_{LS} \times \left( \frac{Vout - 0.8V}{0.8\ V} \right) \tag{1}$$

Table 3 lists the R5 values for some common output voltages, assuming R6 = 10.2 kΩ. Note $V_{IN}$ must be in a range to keep the on time greater than the minimum on-time. The values given in Table 3 are standard 1% values, not the exact value calculated using Equation 1.

**Table 3. R5 Values for Common Output Voltages**

| Output Voltage (V) | R5 Value (kΩ) |
|---|---|
| 1.8 | 12.7 |
| 2.5 | 21.5 |
| 5.0 | 31.6 |
| 5.0 | 53.6 |

Be aware, changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. Please see the TPS54540-Q1 data sheet (SLVSC56) for details.

### 1.4.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 ($R_{UVLO1}$) and R2 ($R_{UVLO2}$). The EVM is set for a start voltage of 6.5 V and stop voltage of 5.0 V, using R1 = 442 kΩ and R2 = 90.9 kΩ. Use Equation 2 and Equation 3 to calculate the required resistor values for R1 and R2, respectively, for different start and stop voltages. The typical values of the constants in the two equations are as follows: $I_{HYS}$ = 3.4 µA, $V_{ENA}$ = 1.2 V, and $I_1$ = 1.2 µA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{2}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \tag{3}$$

# 2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up, and shutdown.

## 2.1 I/O Connections

This EVM includes I/O connectors and test points as shown in Table 4. A power supply capable of supplying at least 5 A must be connected to J2 through a pair of 20-AWG wires. The load must be connected to J1 through a pair of 20-AWG wires. The maximum load-current capability must be 5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the $V_{IN}$ input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

**Table 4. EVM Connectors and Test points**

| Reference Designator | Function |
|---|---|
| J1 | $V_{OUT}$, 5.0 V at 5-A maximum |
| J2 | $V_{IN}$ (see Table 1 for $V_{IN}$ range) |
| J3 | EN jumper. Connect EN to ground to disable, open to enable. |
| J4 | GND jumper for additional ground connections |
| TP1 | $V_{IN}$ test point at $V_{IN}$ connector |
| TP2 | GND test point at $V_{IN}$ |
| TP3 | Output voltage test point at $V_{OUT}$ connector |
| TP4 | GND test point at $V_{OUT}$ connector |
| TP5 | SW test point |
| TP6 | $V_{OUT}$ test point used for loop response measurements |
| TP7 | Test point between voltage divider network and output. Used for loop response measurements. |
| TP8 | GND test point |
| TP9 | $V_{IN}$ test point at the TPS54540-Q1 VIN pin |

## 2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 1.3 A with $V_{IN}$ = 12 V, and then decreases as the load current increases towards full load. Figure 3 shows the efficiency for the EVM. Figure 4 shows the light-load efficiency for the EVM using a semi-log scale. Measurements are taken at an ambient temperature of 25°C. The efficiency may be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the internal MOSFET.

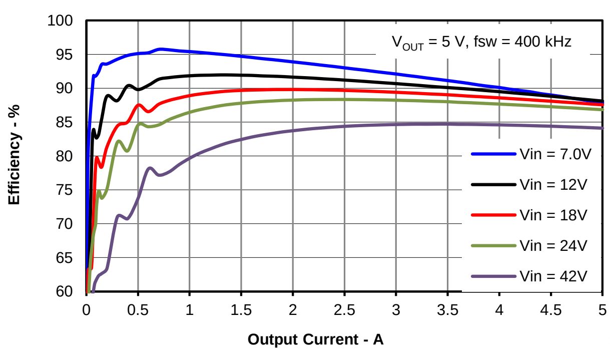



Figure 3. Efficiency versus Load Current

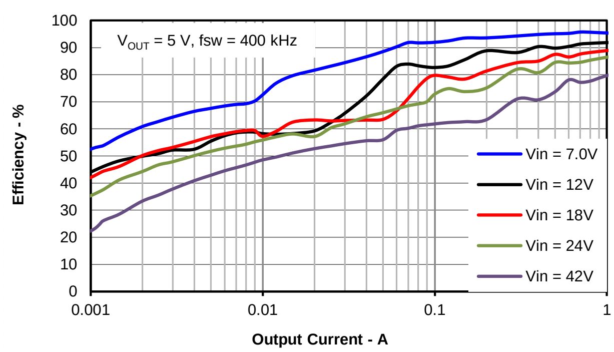



Figure 4. Light-Load Efficiency

## 2.3 Output Voltage Regulation

The load regulation for the EVM is shown in Figure 5. The line regulation for the EVM is shown in Figure 6. Measurements are given for an ambient temperature of 25°C.

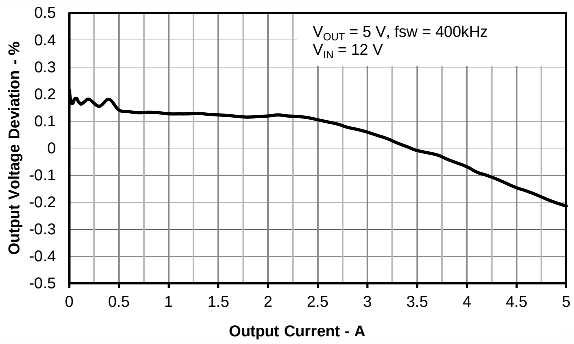



Figure 5. Regulation versus Output Current

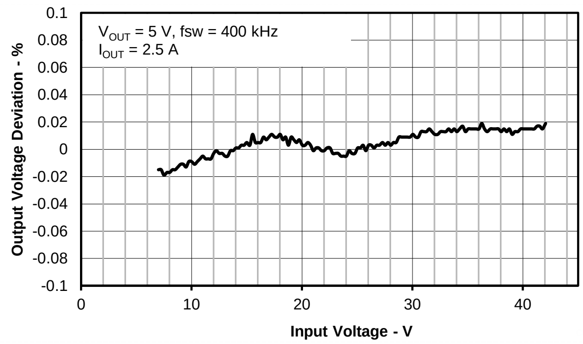



Figure 6. Regulation versus Input Voltage

## 2.4 Load Transients and Loop Response

The EVM response to load transients is shown in Figure 7. The current step is from 25% to 75% of the maximum rated load at 12-V input. The current step slew rate is 100 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

The EVM loop-response characteristics are shown in Figure 8. Gain and phase plots are shown for $V_{IN}$ voltage of 12 V. Load current for the measurement is 5 A.

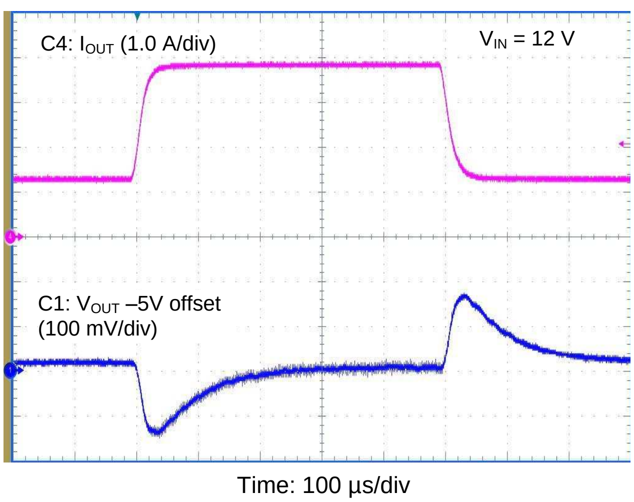



Figure 7. Load Transient Response

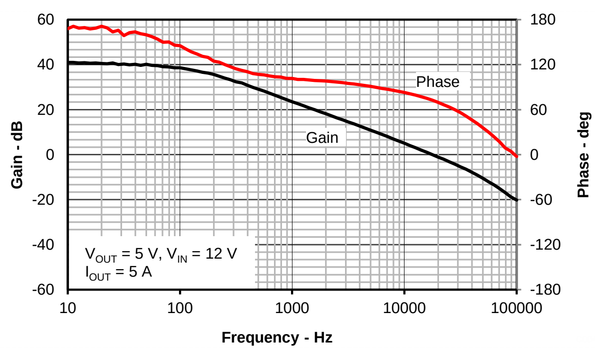



Figure 8. Loop Response

### 2.5 Line Transients

The EVM response to line transients is shown in Figure 9. The input voltage step is from 8.0 V to 40 V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

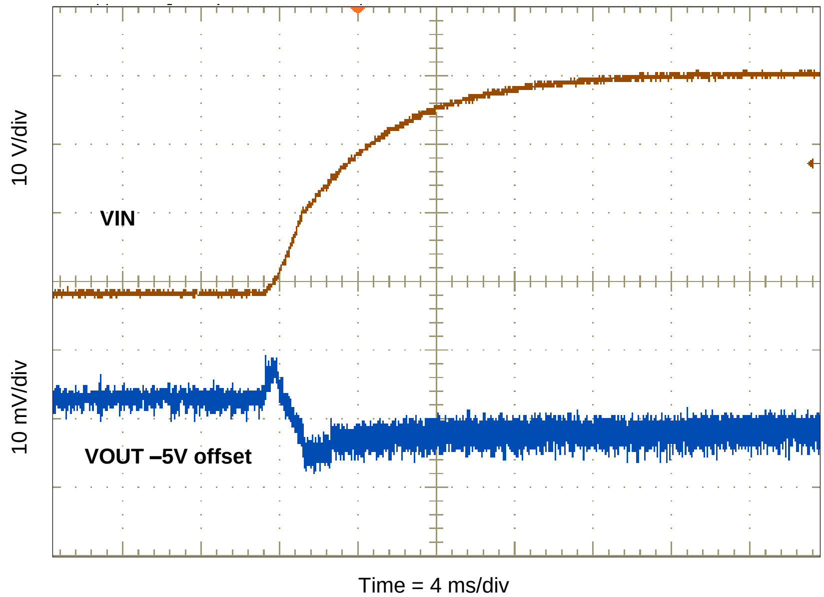



**Figure 9. Line Transient Response**

### 2.6 Input Voltage Ripple

The EVM CCM input voltage ripple is shown in Figure 10. The output current is the rated full load of 5 A and $V_{IN}$ = 12 V. The voltage ripple is measured directly across the capacitors located at the VIN pin of the IC (C9–C13) and at the input to the board (C15) showing the attenuation of the input filter. A 150-MHz BW is used for this measurement.

The DCM input voltage ripple is shown in Figure 11. The output current is 0.1 A and $V_{IN}$ = 12 V.

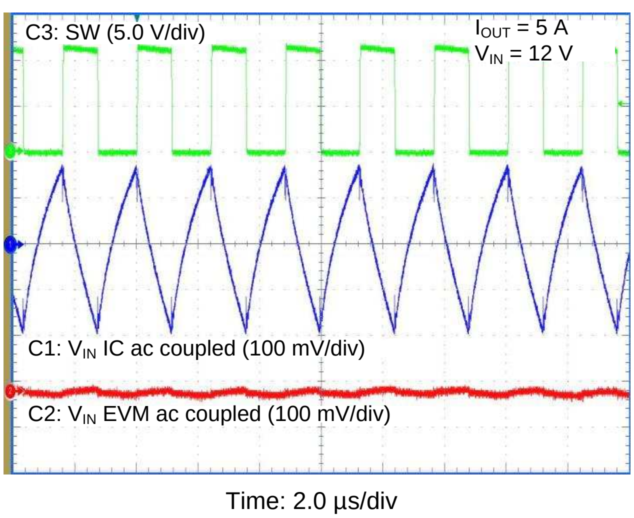



**Figure 10. Input Voltage Ripple CCM**

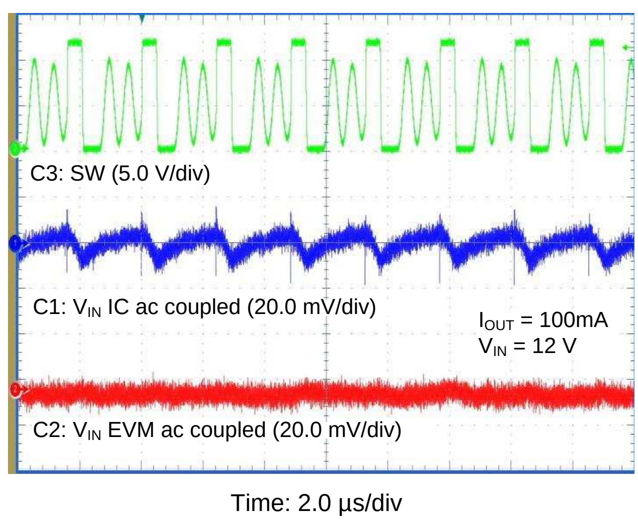



**Figure 11. Input Voltage Ripple DCM**

### 2.7 Output Voltage Ripple

The EVM CCM output voltage ripple is shown in Figure 12. The output current is the rated full load of 5 A and $V_{IN}$ = 12 V. The voltage ripple is measured directly across the output capacitors.

The DCM output voltage ripple is shown in Figure 13. The output current is 0.1 A and $V_{IN}$ = 12 V.

The Pulse Skip Eco-mode™ output voltage ripple is shown in Figure 14. There is no external load on the output and $V_{IN}$ = 12 V.

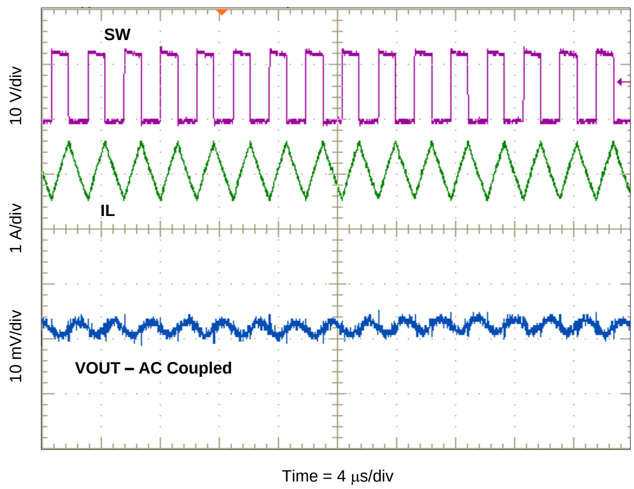



**Figure 12. Output Voltage Ripple CCM**

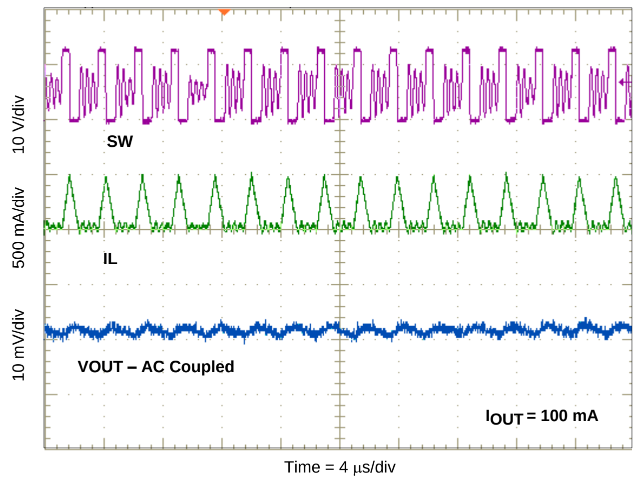



**Figure 13. Output Voltage Ripple DCM**

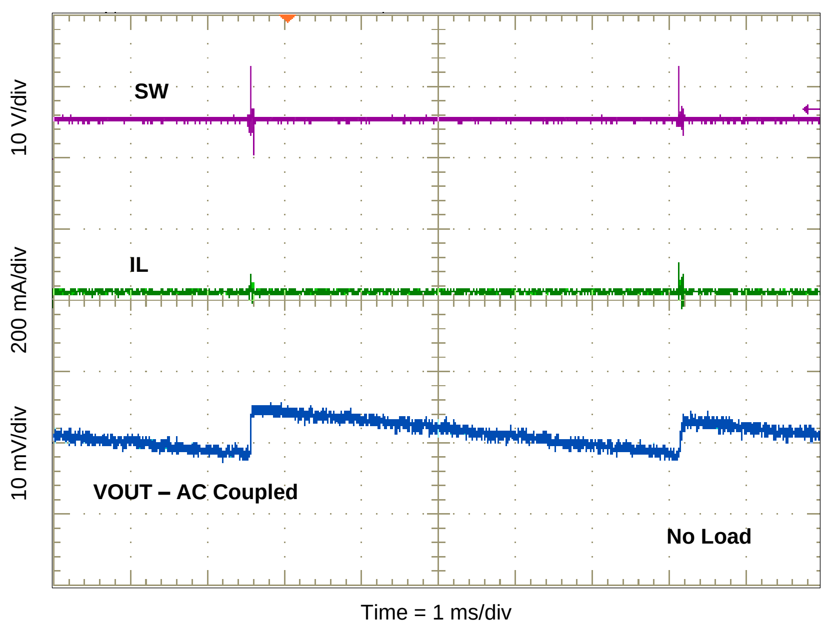



**Figure 14. Output Voltage Ripple Eco-mode**

## 2.8 SW Voltage

This design uses a snubber to reduce ringing at the SW node, lowering the emissions of the EVM. Figure 15 shows the ringing and rise time at the SW pin before the snubber is added. Figure 16 shows the performance with the snubber. The input voltage for these plots is 12 V with a 5.0-A resistive load.

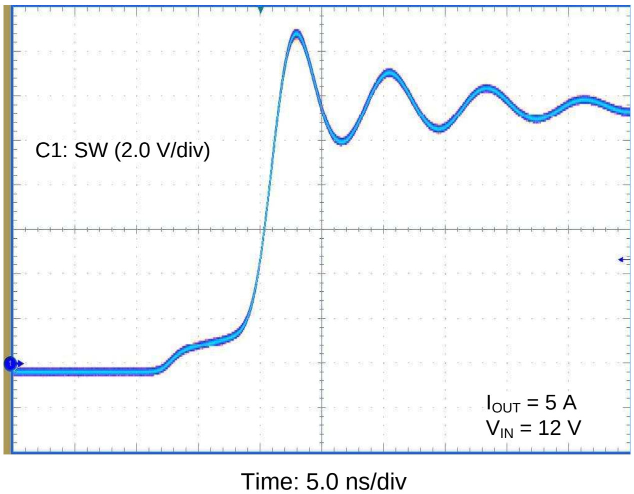



**Figure 15. SW Voltage Without Snubber**

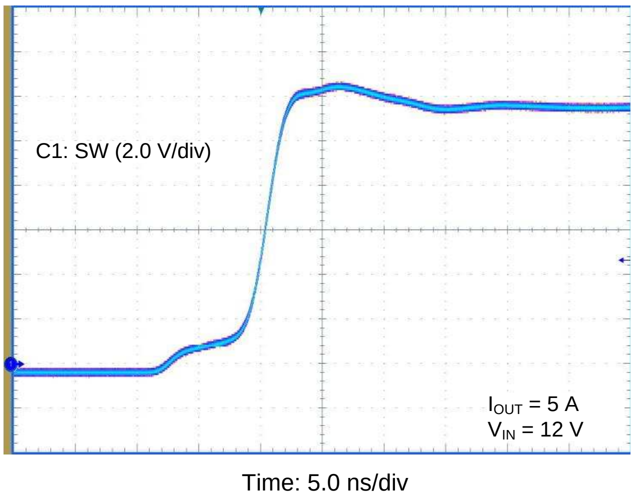



**Figure 16. SW Voltage With Snubber**

## 2.9 Start Up

The start up waveforms are shown in Figure 17, Figure 18, and Figure 19. The input voltage for these plots is 12 V with a 5-A resistive load. In Figure 17 the top trace shows $V_{IN}$, the middle trace shows EN, and the bottom trace shows $V_{OUT}$. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start up sequence begins and the output ramps up toward the set value of 5.0 V.

In Figure 18 the input voltage is initially applied with EN held low. When EN is released, the start up sequence begins and the output ramps up toward the set value of 5.0 V.

In Figure 19 the input voltage is initially applied with EN held low. An external voltage of 3.3 V is supplied to $V_{OUT}$. When EN is released, the start up sequence begins and the internal reference ramps up from 0 V with the internal soft-start. When the internal reference reaches the FB voltage the output begins ramping toward the set value of 5.0 V.

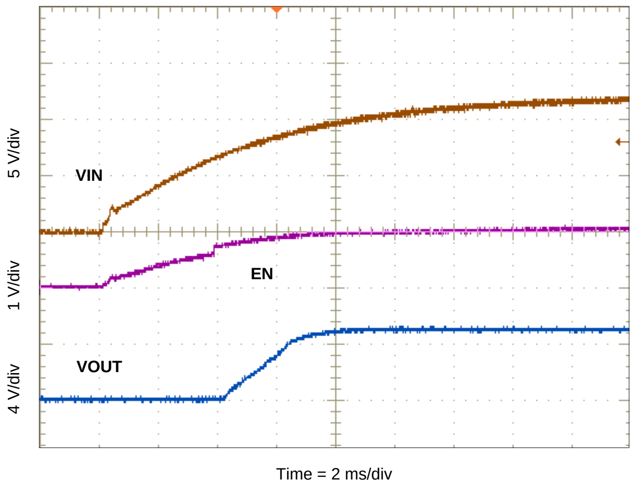



**Figure 17. Start Up Relative to $V_{IN}$ Ramping Up**

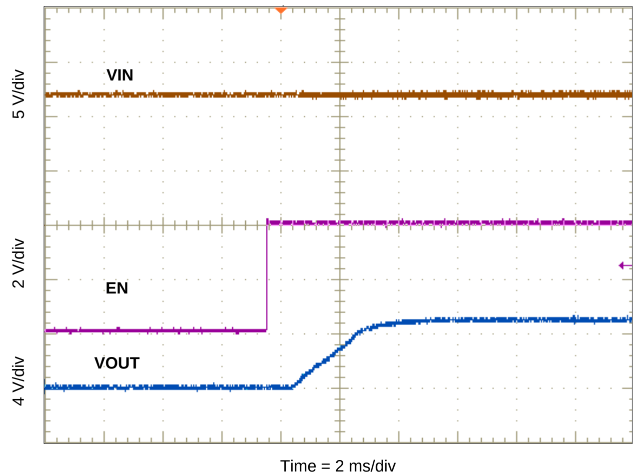



**Figure 18. Start Up Using EN**

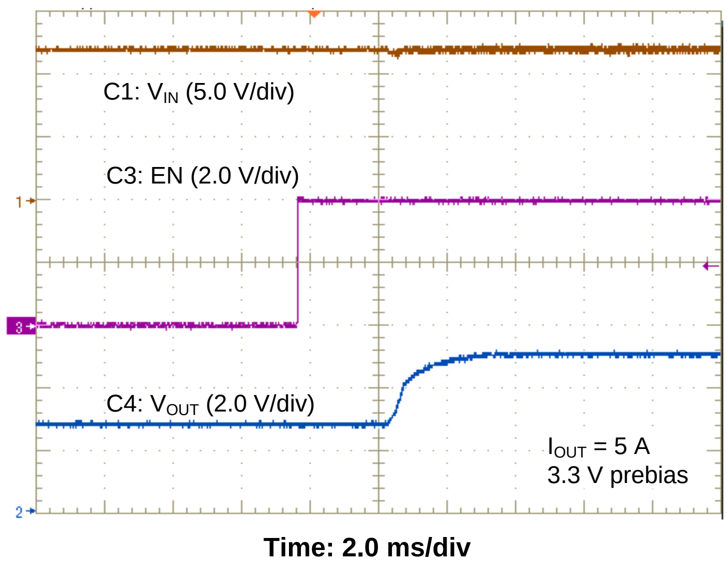
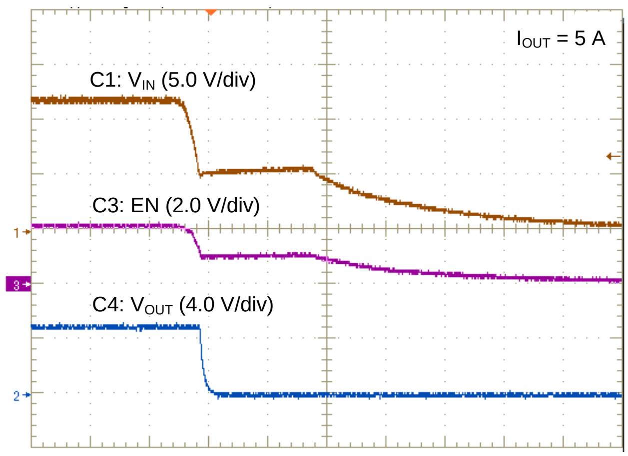



**Figure 19. Prebias Start Up Using EN**

## 2.10 Shutdown

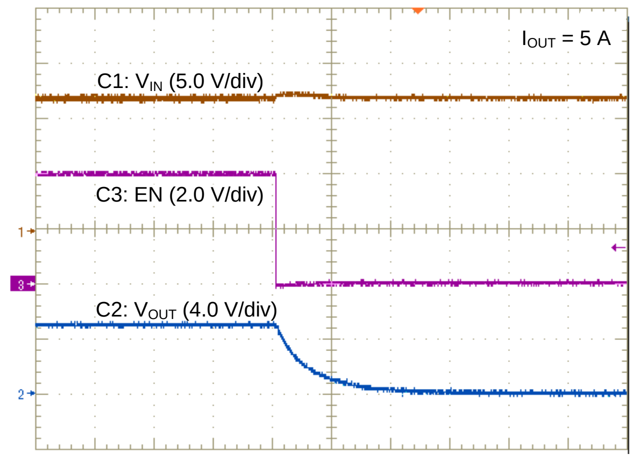
The shutdown waveforms are shown in Figure 20 and Figure 21. The input voltage for these plots is 12 V with a 5-A resistive load. The top trace shows $V_{IN}$, the middle trace shows EN, and the bottom trace shows $V_{OUT}$. In Figure 20 the input voltage is removed, and when the input falls below the undervoltage lockout threshold, the TPS54540-Q1 shuts down and the output falls to ground.

In Figure 21, the input voltage is held at 12 V, and EN is shorted to ground. When EN is grounded, the TPS54540-Q1 is disabled, and the output voltage discharges to ground.




Time: 2.0 ms/div

Figure 20. Shutdown Relative to $V_{IN}$

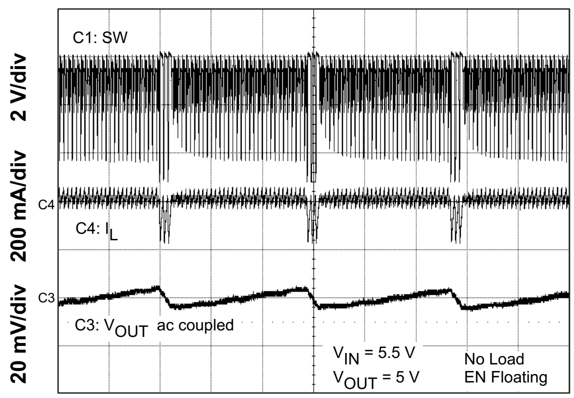



Time: 200 µs/div

Figure 21. Shutdown Relative to EN

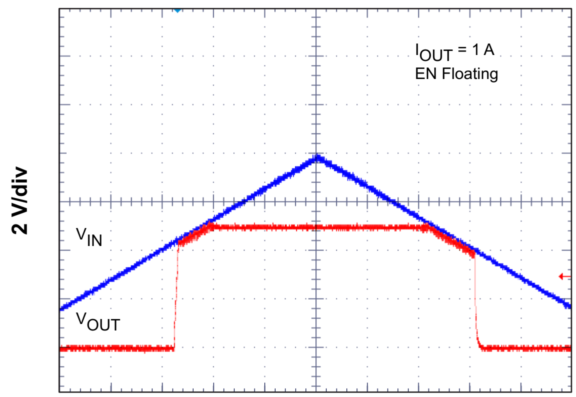
## 2.11 Low Dropout Operation

For improved low dropout operation, the TPS54540-Q1 includes a small integrated low-side MOSFET to pull SW to GND when the BOOT to SW voltage drops below 2.1 V. This recharges the BOOT capacitor for driving the high-side MOSFET. Figure 22 shows the steady state operation and Figure 23 shows the start up and shutdown in a low dropout condition. Both measurements are taken with a 5-V output.




Time = 20 µs/div

Figure 22. Low Dropout Operation




Time = 40 µs/div

Figure 23. Low Dropout Start Up and Shutdown

# 3 Board Layout

This section provides a description of the EVM, board layout, and layer illustrations.

## 3.1 Layout

The board layout for the EVM is shown in Figure 24 through Figure 27. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for $V_{IN}$, $V_{OUT}$, and SW. Also on the top layer are connections for the remaining pins of the TPS54540-Q1 and a large area filled with ground. The bottom layer contains ground and a signal route for the bootstrap capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54540-Q1 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane. Multiple vias are also placed near the Schottky diode (D1) to provide a nearby thermal path to improve its thermal performance.

The input decoupling capacitors (C10–C13), bootstrap capacitor (C4), and frequency set resistor (R3) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC, especially the bottom resistor (R6). The voltage divider network ties to the output voltage at the point of regulation, the copper $V_{OUT}$ trace past the output connector (J1). For the TPS54540-Q1EVM-593, an additional input bulk capacitor may be required (C14), depending on the EVM connection to the input supply.

Layout considerations to reduce emissions are as follows. The bootstrap capacitor (C4) is placed on the bottom side of the board so the Schottky diode (D1) can be placed directly next to the IC. The diode should be as close as possible to the SW pin and GND of the input decoupling capacitors. The smaller sized input decoupling capacitors (C12 and C13) are located closest to the IC to reduce any board parasitics to improve their effectiveness of filtering high frequency noise. The snubber (R8 and C17) is located directly next to the diode to improve its performance. Lastly, the SW copper area is kept as small as possible because it is a high dv/dt node which can radiate noise.

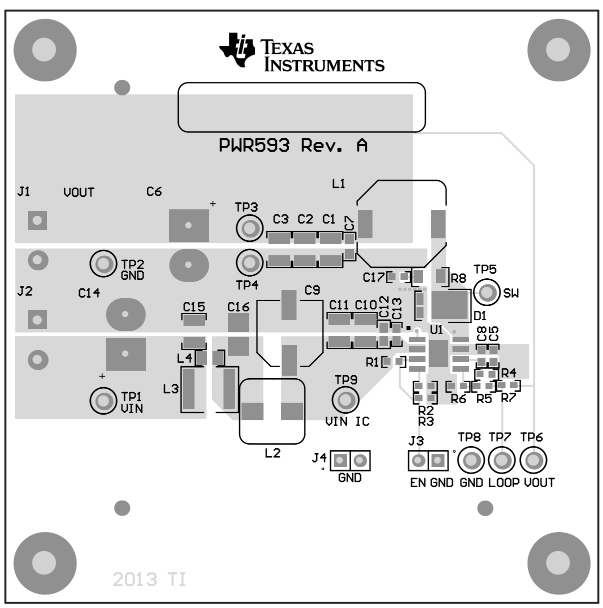



**Figure 24. TPS54540-Q1EVM-593 Top Assembly and Silkscreen**

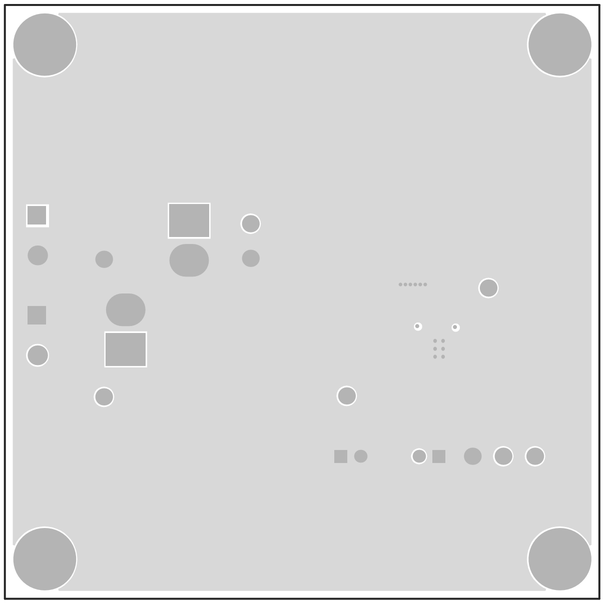


Figure 25. TPS54540-Q1EVM-593 Layer 2 Layout

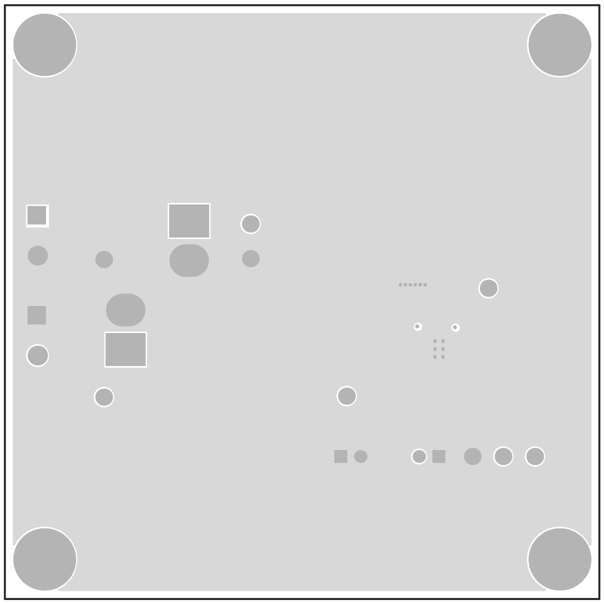


Figure 26. TPS54540-Q1EVM-593 Layer 3 Layout

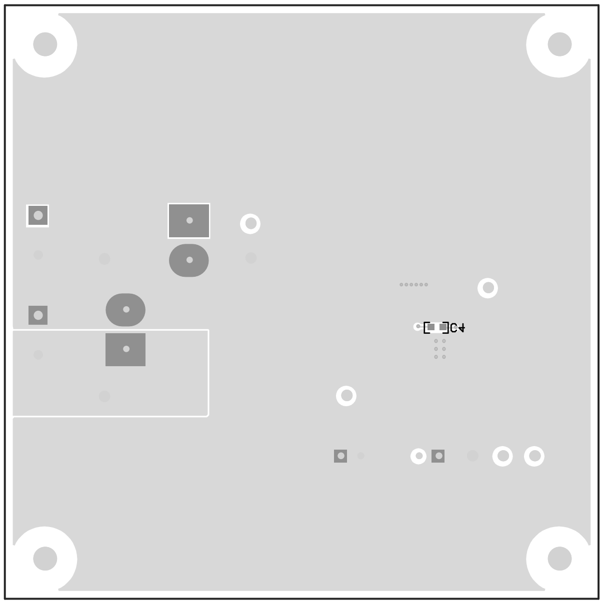


**Figure 27. TPS54540-Q1EVM-593 Bottom-Side Assembly and Silkscreen (Viewed From Top)**

## *3.2 Estimated Circuit Area*

The estimated printed-circuit-board area in this design by simply boxing in the components on the top layer is 1.43 $in^2$ (923 $mm^2$). This area does not include test points or connectors. This design uses 0603 components for easy modifications. The area can be reduced by using smaller-sized components.

# 4 Bill of Materials

Table 5 presents the bill of materials for the EVM.

**Table 5. TPS54540-Q1EVM-593 Bill of Materials**

| Designator | Quantity | Value | Description | Package | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| C1, C2, C3 | 3 | 47uF | CAP, CERM, 47uF, 16V, ±20%, X5R, 1210 | 1210 | GRM32ER61C476ME15L | MuRata |
| C4 | 1 | 0.1uF | CAP, CERM, 0.1uF, 10V, ±10%, X7R, 0603 | 0603 | STD | STD |
| C5, C13 | 2 | 4700pF | CAP, CERM, 4700pF, 50V, ±10%, X7R, 0603 | 0603 | STD | STD |
| C8 | 1 | 47pF | CAP, CERM, 47pF, 50V, ±5%, C0G/NP0, 0603 | 0603 | STD | STD |
| C9 | 1 | 47uF | CAP, AL, 47uF, 63V, ±20%, 0.65 ohm, SMD | SMT Radial F | EEE-FK1J470P | Panasonic |
| C10, C11, C15 | 3 | 4.7uF | CAP, CERM, 4.7uF, 50V, ±10%, X7R, 1210 | 1210 | STD | STD |
| C12 | 1 | 0.047uF | CAP, CERM, 0.047uF, 50V, ±10%, X7R, 0603 | 0603 | STD | STD |
| C17 | 1 | 680pF | CAP, CERM, 680pF, 50V, ±10%, X7R, 0603 | 0603 | STD | STD |
| D1 | 1 | 0.52V | Diode, Schottky, 60V, 7A, PowerDI5 | PowerDI5 | PDS760-13 | Diodes Inc. |
| J1, J2 | 2 | ED120/2DS | Terminal Block, 2-pin, 15-A, 5.1mm | 0.40 x 0.35 inch | ED120/2DS | OST |
| J3, J4 | 2 | | Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator | TSW-102-07-G-S | TSW-102-07-G-S | Samtec, Inc. |
| L1 | 1 | 7.2uH | Inductor, Shielded Flat Iron, Ferrite, 7.2uH, 6.0A, 0.01 ohm, SMD | WE-PDF | 7447798720 | Wurth Elektronik eiSos |
| L2 | 1 | 1.5uH | Inductor, Shielded Drum Core, Superflux, 1.5uH, 11A, 0.0046 ohm, SMD | WE-HC3 | 744314150 | Wurth Elektronik eiSos |
| L3 | 1 | 400 ohm | 4500mA Ferrite Bead, 400 ohm @ 100MHz, SMD | 2220 | 74279224401 | Wurth Elektronik eiSos |
| R1 | 1 | 442k | RES, 442k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R2 | 1 | 90.9k | RES, 90.9k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R3 | 1 | 243k | RES, 243k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R4 | 1 | 16.9k | RES, 16.9k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R5 | 1 | 53.6k | RES, 53.6k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R6 | 1 | 10.2k | RES, 10.2k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R7 | 1 | 49.9 | RES, 49.9 ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R8 | 1 | 5.6 | RES, 5.6 ohm, 5%, 0.25W, 1206 | 1206 | STD | STD |
| SH-J3 | 1 | 1x2 | Shunt, 100mil, Gold plated, Black | Shunt | SNT-100-BK-G | Samtec |
| TP1, TP3, TP6, TP9 | 4 | Red | Test Point, TH, Multipurpose, Red | Keystone5010 | 5010 | Keystone |
| TP2, TP4, TP8 | 3 | Black | Test Point, TH, Multipurpose, Black | Keystone5011 | 5011 | Keystone |
| TP5 | 1 | Yellow | Test Point, TH Multipurpose, Yellow | Keystone5014 | 5014 | Keystone |
| TP7 | 1 | Orange | Test Point, TH, Multipurpose, Orange | Keystone5013 | 5013 | Keystone |
| U1 | 1 | TPS54540QDDA | IC, 42V, 5A, Low Iq, Current Mode, Non-Synchronous Monolithic Buck, AEC-Q100 Qualified | SON | TPS54540QDDA | TI |
| C6, C14 | 0 | Open | Capacitor, Aluminum, vvV, 20% | Multi sizes | Engineering Only | |
| C7 | 0 | 0.047uF | CAP, CERM, 0.047uF, 50V, ±10%, X7R, 0603 | 0603 | GRM188R71H473KA61D | MuRata |
| C16 | 0 | Open | Capacitor, Ceramic, 500V, X7R, ±10 % | Multi sizes | Engineering Only | |
| L4 | 0 | 300 ohm | 3000mA Ferrite Bead, 300 ohm @ 100MHz, SMD | 0805 | 742792031 | Wurth Elektronik eiSos |

## EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

## REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations*: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

**For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

**Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concerning EVMs including detachable antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

**Concernant les EVMs avec appareils radio**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 【Important Notice for Users of EVMs for RF Products in Japan】

**This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

**Texas Instruments Japan Limited**
**(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan**

http://www.tij.co.jp

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス･インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

## EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

**Certain Instructions**. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265