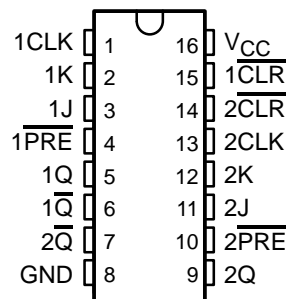


CD54AC112, CD74AC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCHS325 – JANUARY 2003

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **± 24 -mA Output Drive Current**
– Fanout to 15 F Devices
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC112 . . . F PACKAGE
CD74AC112 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'AC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC112E	CD74AC112E
	SOIC – M	Tube	CD74AC112M	AC112M
		Tape and reel	CD74AC112M96	
	CDIP – F	Tube	CD54AC112F3A	CD54AC112F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54AC112, CD74AC112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

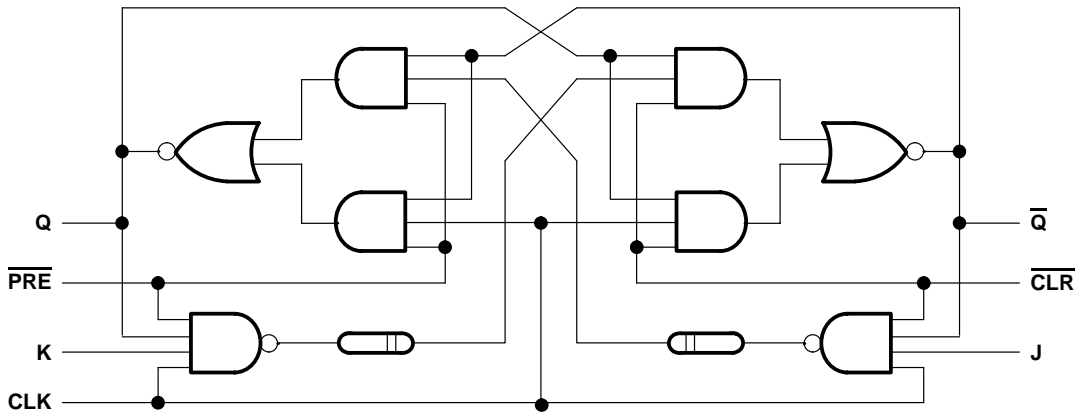
SCHS325 – JANUARY 2003

FUNCTION TABLE
 (each flip-flop)

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q ₀	$\overline{\text{Q}}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	Toggle
H	H	H	X	X	Q ₀	$\overline{\text{Q}}_0$

[†] Output states are unpredictable if $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ go high simultaneously after both being low at the same time.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.



CD54AC112, CD74AC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCHS325 – JANUARY 2003

recommended operating conditions (see Note 3)

		T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.5 V	1.2		1.2		1.2	V
		V _{CC} = 3 V	2.1		2.1		2.1	
		V _{CC} = 5.5 V	3.85		3.85		3.85	
V _{IL}	Low-level input voltage	V _{CC} = 1.5 V		0.3		0.3		V
		V _{CC} = 3 V		0.9		0.9		
		V _{CC} = 5.5 V		1.65		1.65		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		-24		-24		mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		24		24		mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.5 V to 3 V		50		50		ns/V
		V _{CC} = 3.6 V to 5.5 V		20		20		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.5 V	1.4		1.4		1.4	V	
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I _{OH} = -4 mA	3 V	2.58		2.4		2.48		
		I _{OH} = -24 mA	4.5 V	3.94		3.7		3.8		
		I _{OH} = -50 mA [†]	5.5 V			3.85				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V		0.1		0.1		V	
			3 V		0.1		0.1			
			4.5 V		0.1		0.1			
		I _{OL} = 12 mA	3 V		0.36		0.5			0.44
		I _{OL} = 24 mA	4.5 V		0.36		0.5			0.44
		I _{OL} = 50 mA [†]	5.5 V				1.65			
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		80		40	μA	
C _i				10		10		10	pF	

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



CD54AC112, CD74AC112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SCHS325 – JANUARY 2003

timing requirements over recommended operating free-air temperature range, $V_{CC} = 1.5\text{ V}$ (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	8		9		MHz
t_w	Pulse duration	CLK high or low		55		ns
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low		49		
t_{su}	Setup time, before CLK↓	J or K		44		ns
t_h	Hold time, after CLK↓	J or K		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{\text{CLR}}\uparrow$ or $\overline{\text{PRE}}\uparrow$		27		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	71		81		MHz
t_w	Pulse duration	CLK high or low		6		ns
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low		5.5		
t_{su}	Setup time, before CLK↓	J or K		4.9		ns
t_h	Hold time, after CLK↓	J or K		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{\text{CLR}}\uparrow$ or $\overline{\text{PRE}}\uparrow$		3.1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	100		114		MHz
t_w	Pulse duration	CLK high or low		4.4		ns
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low		3.9		
t_{su}	Setup time, before CLK↓	J or K		3.5		ns
t_h	Hold time, after CLK↓	J or K		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{\text{CLR}}\uparrow$ or $\overline{\text{PRE}}\uparrow$		2.2		ns



CD54AC112, CD74AC112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SCHS325 – JANUARY 2003

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 1.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Q or \bar{Q}		129		117	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$			153		139	
t_{PHL}	CLK	Q or \bar{Q}		129		117	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$			153		139	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			71		81		MHz
t_{PLH}	CLK	Q or \bar{Q}	3.6	14.4	3.7	13.1	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		4.3	17.1	4.4	15.5	
t_{PHL}	CLK	Q or \bar{Q}	3.6	14.4	3.7	13.1	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		4.3	17.1	4.4	15.5	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100		114		MHz
t_{PLH}	CLK	Q or \bar{Q}	2.6	10.3	2.7	9.4	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		3.1	12.2	3.2	11.1	
t_{PHL}	CLK	Q or \bar{Q}	2.6	10.3	2.7	9.4	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		3.1	12.2	3.2	11.1	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	56	pF

CD54AC112, CD74AC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCHS325 – JANUARY 2003

PARAMETER MEASUREMENT INFORMATION



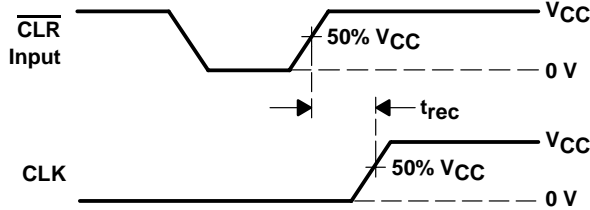
† When $V_{CC} = 1.5\text{ V}$, $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC112F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC112F3A	Samples
CD74AC112E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC112E	Samples
CD74AC112M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC112M	Samples
CD74AC112M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC112M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC112, CD74AC112 :

- Catalog: [CD74AC112](#)
- Military: [CD54AC112](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC112M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC112M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated