TPAD8606ARZ

10MHz, Low Power, CMOS,Rail to Rail Operational Amplifier

Features

- General Purpose, Low Cost
- Gain Bandwidth Product: 10MHz
- Low Input Bias Current: 10pA (Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 800μA per Amplifier (Typ.)
- Unity Gain Stable
- Rail-to-Rail Input and Output
- Supply Voltage Range: 2.2V to 5.5V
- Operating Temperature: -40°C ~ +125°C
- Type Package:SOP-8

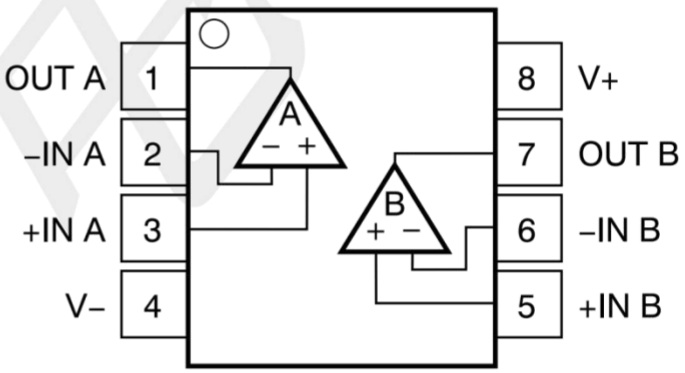
General Description

The is wide band, low-noise, low-dis tortio n dual operational amplifier, that offer rail-to-rail inputs / outputs and single supply operation down to 2.2V.They draw 1.6mA of quiescent supply current while featuring ultra-low distortion(0.0002% THD+N), as well as low input voltage noise density (15nV/Hz) and low input currentnoise density(0.5fA/Hz).These features make the devices an ideal choicef or applications that require low distortion and/or low noise. These amplifiers have inputs and outputs which swing rail-to rail and their input common mode voltage range includes ground. The maximum input offset of these amplifiers is less than 5mV.

Applications

- Temperature Sensors
- Battery-Powered Instruments
- Smoke/Gas/Environment Sensors
- Medical Equipment
- Portable Instruments and Mobile Device
- Active Filters
- Piezo Electrical Transducer Amplifier
- Sensor Interface
- Handheld Test Equipment

Pinout (top view)



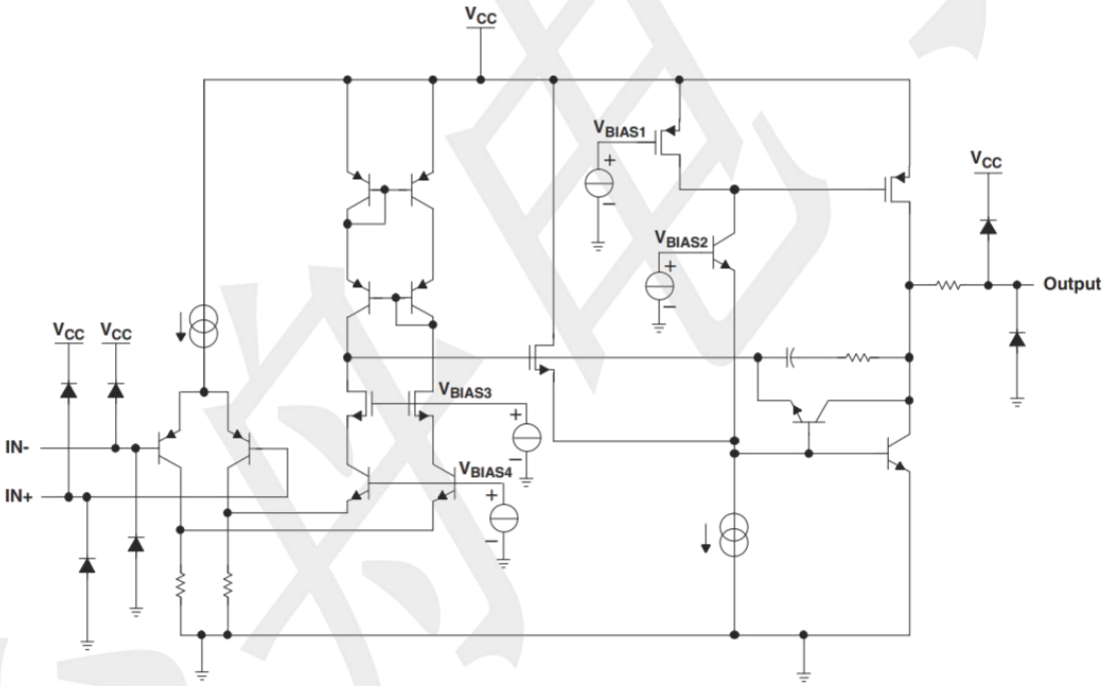
Pin Configurations

Pin Number	Pin Name	Pin Function
1	OUT A	Output A
2	-IN A	Reverse input A
3	+IN A	In-phase input A
4	-V	Chip Supply Voltage(Negative)/GND
5	+IN B	In-phase input B
6	-IN B	Reverse input B
7	OUT B	Output B
8	+V	Chip Supply Voltage(Positive)/VCC

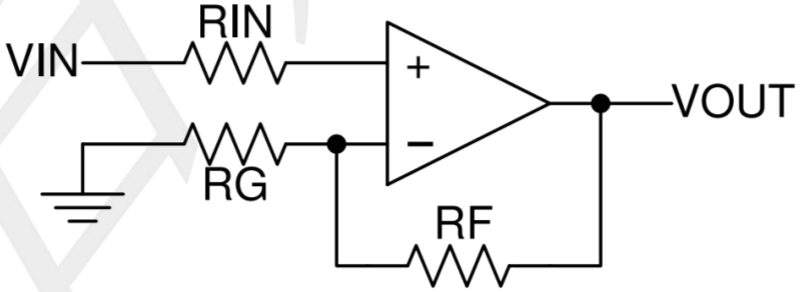
Absolute Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Condition		Rating		UNIT
VDD to GND	Power Supply Voltage	7V		V
IN+ or IN-	Signal Input Terminals Voltage	GND-0.3V~VDD+0.3V		V
OUT to GND	Output Short-Circuit	Continuous		mA
TJ	Junction Temperature	150		°C
LT	Lead Temperature (Soldering, 10 sec.)	260		°C
TA	Operating Temperature Range	-40	125	°C
Tstg	Storage Temperature Range	-65	150	°C

BLOCK DIAGRAM



Power Supply Bypassing



Electrical Characteristics (unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply-Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.2	--	5.5	V
Quiescent Supply Current (per Amplifier)	I_{DD}	V_{DD} = 3V	--	0.8	--	mA
		V_{DD} = 5V	--	0.8	1.2	
Input Offset Voltage	V_{OS}	T_A = +25°C	--	--	5	mV
		T_A = -40°C to +85°C	--	--	--	
		T_A = -40°C to +125°C	--	--	1.5	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		--	0.3	6	μV/°C
Input Bias Current	I_B	(Note 3)	--	1	100	pA
Input Offset Current	I_{OS}	(Note 3)	--	1	100	pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the T_A = 25°C	-0.2	--	V_{DD}+0.2	V
		CMRR test T_A = -40 C to +125 C	0	--	V_{DD}0	
Common-Mode Rejection Ratio	CMRR	Vss-0.2V V_{CM} V_{DD}+0.2V, +25°C	--	75	--	dB
		Vss≤V_{CM}≤5V T_A = +25°C	65	80	--	
		Vss-0.2V V_{CM} V_{DD}+0.2V T_A = -40°C to +125°C	--	65	--	
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.2V to +5.5V	75	90	--	dB
Open-Loop Voltage Gain	A_V	R_L=100k to V_{DD}/2, 100mV≤V_O≤V_{DD} -125mV	90	100	--	dB
		RL=1k to VDD/2, 200mV≤VO≤VDD -250mV	75	85	--	
		RL=500 to VDD/2, 350mV≤VO≤VDD -500mV	55	65	--	
Output Voltage Swing	V_{OUT}	|VIN+-VIN-| 10mV VDD-VOH	--	10	35	mV
		RL = 10k to VDD/2 VOL-VSS	--	10	30	
		|V_{IN+}-V_{IN-}| 10mV V_{DD}-V_{OH}	--	80	200	
		R_L = 1k to V_{DD}/2 V_{OL}-V_{SS}	--	50	150	
		|V_{IN+}-V_{IN-}| 10mV V_{DD}-V_{OH}	--	100	350	
		R_L = 500 to V_{DD}/2 V_{OL}-V_{SS}	--	80	260	

Electrical Characteristics (unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	--	50	--	mA
PDB Logic Low	V_{IL}		--	-	0.8	V
PDB Logic High	V_{IH}		2	-	--	V
Turn-On Time	T_{ON}		--	2.2	--	μs
Turn-Off Time	T_{OFF}		--	0.8	--	μs
Output Leakage Current	I_{LEAK}	Shutdown Mode (PDB = V_{SS}), V_{OUT} = V_{SS} to V_{DD}	--	0.001	1.0	μA
Input Capacitance	C_{IN}		--	10	--	pF
Gain Bandwidth Product	GBW	A_V = +1V/V	--	10	--	MHz
Slew Rate	SR	A_V = +1V/V	--	4.5	--	V/μs
Full Power Bandwidth		Av = +1V/V	--	0.4	--	MHz
Phase Margin	m	Av = +1V/V	--	55	--	deg
Gain Margin	G_m	Av = +1V/V	--	12	--	dB
Settling Time	ts	To 0.01%, V_{OUT} = 2V step A_V = +1V/V	--	1	--	μs
Capacitive-Load Stability	C_{LOAD}	No sustained oscillations. Av = +1V/V	--	200	--	pF
Peak-to-Peak Input Noise Voltage	e_n(p-p)	f = 0.1Hz to 10Hz	--	5	--	Vp-p
Input Voltage Noise Density	e_n	f = 10Hz f = 1kHz f = 30kHz	-- -- --	60 30 15	-- -- --	nV/Hz
Input Current Noise Density	i_n	f = 1kHz				fA/ Hz
Total Harmonic Distortion plus Noise	THD+N	V_{OUT} = 2Vp-p, Av = +1V/V, f = 1kHz RL = 10k to GND f = 20kHz V_{OUT} = 2Vp-p, Av = +1V/V, f = 1kHz RL = 1k to GND f = 20kHz	-- -- -- --	0.0001 0.002 0.0002 0.004	-- -- -- --	%

Note :

1: All devices are 100% production tested at TA = +25°C .

2: Parameter is guaranteed by design.

3: Peak-to-peak input noise voltage is defined as six times RMS value of input noise voltage.

Typical Application Circuit

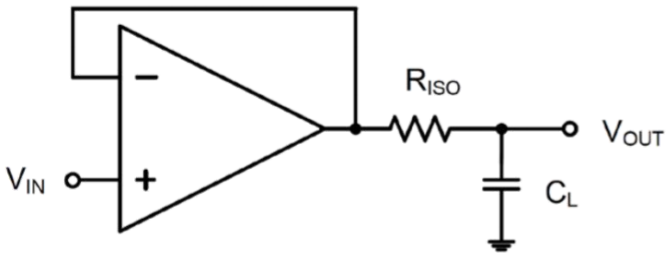


Figure 1. Indirectly Driving Heavy Capacitive Load

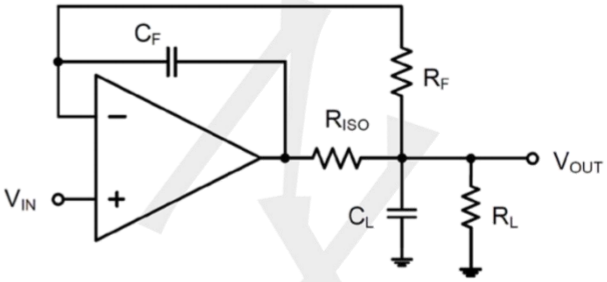


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

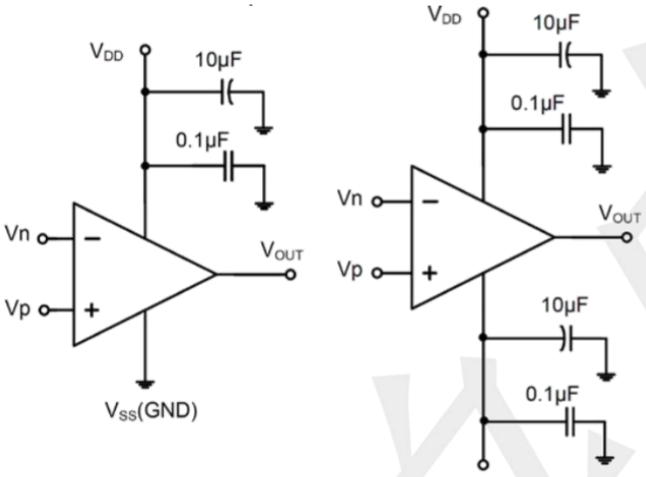


Figure 3. Amplifier with Bypass Capacitors

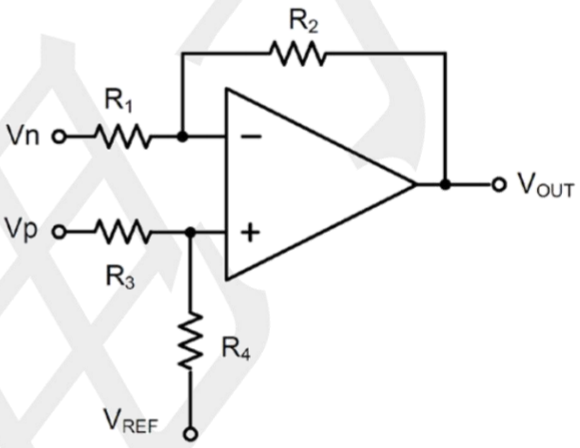


Figure 4. Differential Amplifier

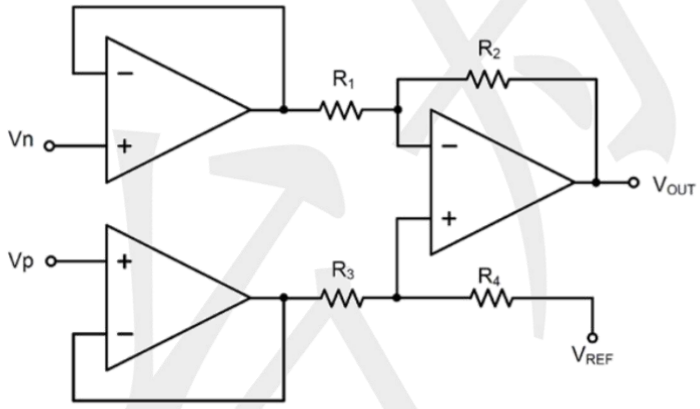


Figure 5. Instrumentation Amplifier

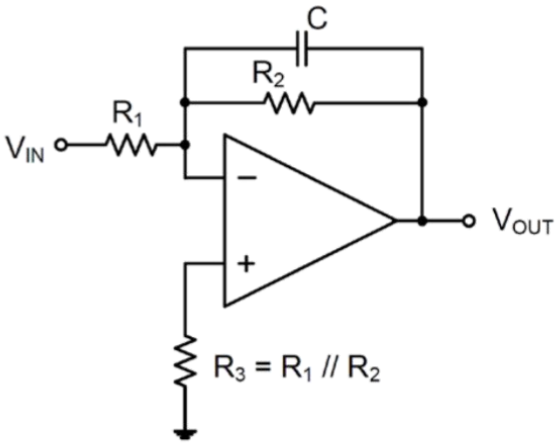
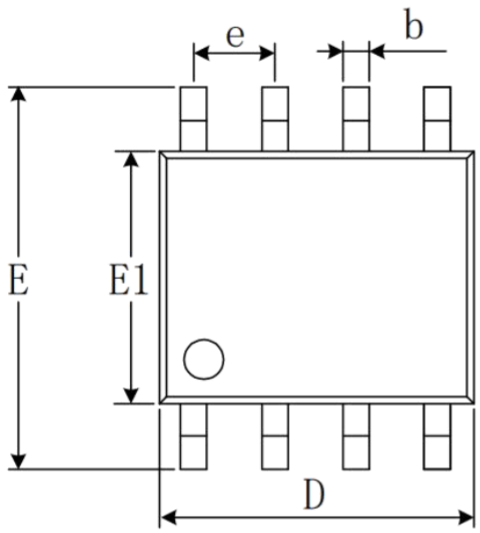
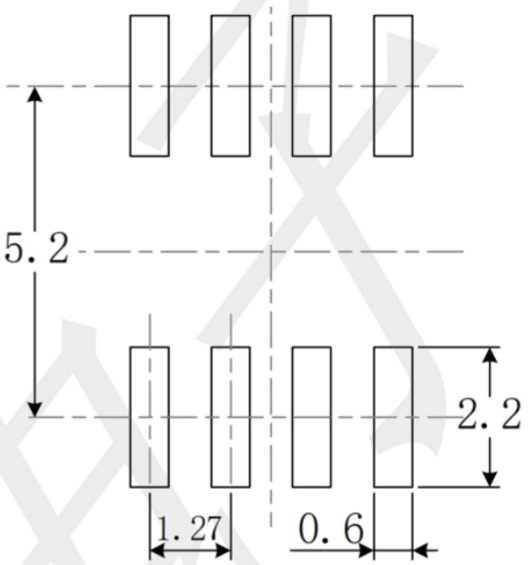


Figure 6. Low Pass Active Filter

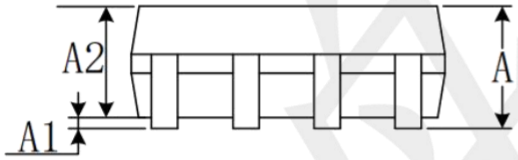
Package information

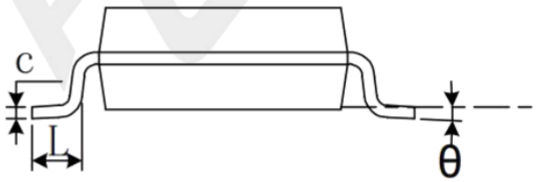
SOP-8





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°