4Mb
ZBT® SRAM

MT55L256L18P1, MT55L256V18P1,
MT55L128L32P1, MT55L128V32P1,
MT55L128L36P1, MT55L128V36P1

3.3V VDD, 3.3V or 2.5V I/O

FEATURES

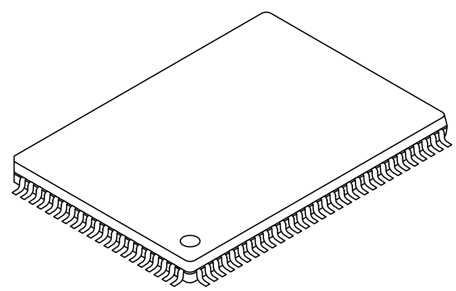
- High frequency and 100 percent bus utilization
- Fast cycle times: 6ns, 7.5ns and 10ns
- Single +3.3V ±5% power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer supply (VDDQ)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or interleaved burst modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 8Mb, and 16Mb ZBT SRAM family
- Automatic power-down
- 165-pin FBGA package
- 100-pin TQFP package

OPTIONS	MARKING
• Timing (Access/Cycle/MHz)	
3.5ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V I/O	
256K x 18	MT55L256L18P1
128K x 32	MT55L128L32P1
128K x 36	MT55L128L36P1
2.5V I/O	
256K x 18	MT55L256V18P1
128K x 32	MT55L128V32P1
128K x 36	MT55L128V36P1
• Package	
100-pin TQFP	T
165-pin FBGA	F*
• Operating Temperature Range	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)**	IT

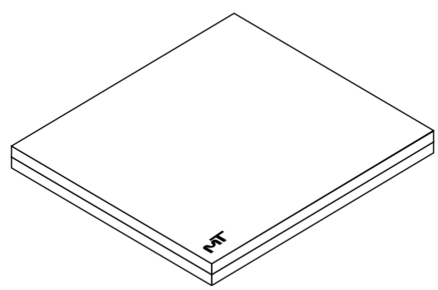
Part Number Example:

MT55L256L18P1T-10

100-Pin TQFP[1]



165-Pin FBGA



NOTE: 1. JEDEC-standard MS-026 BHA (LQFP).

* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/support/index.html.

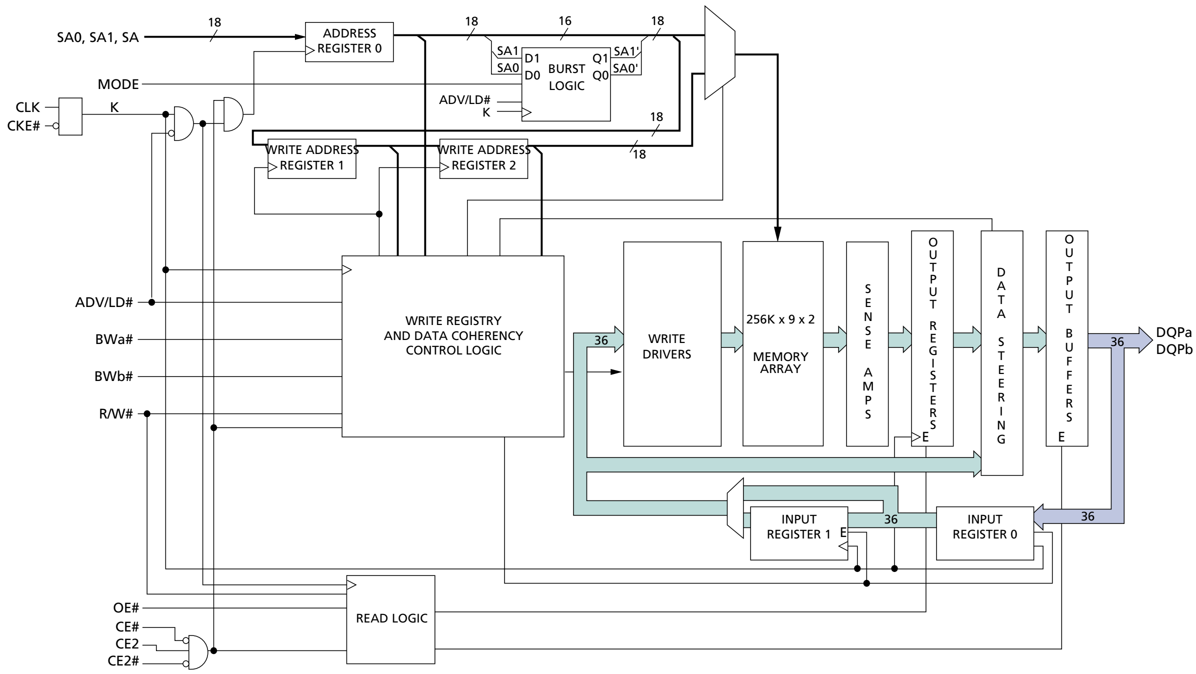
** Industrial temperature range offered in specific speed grades and configurations. Contact factory for more information.

GENERAL DESCRIPTION

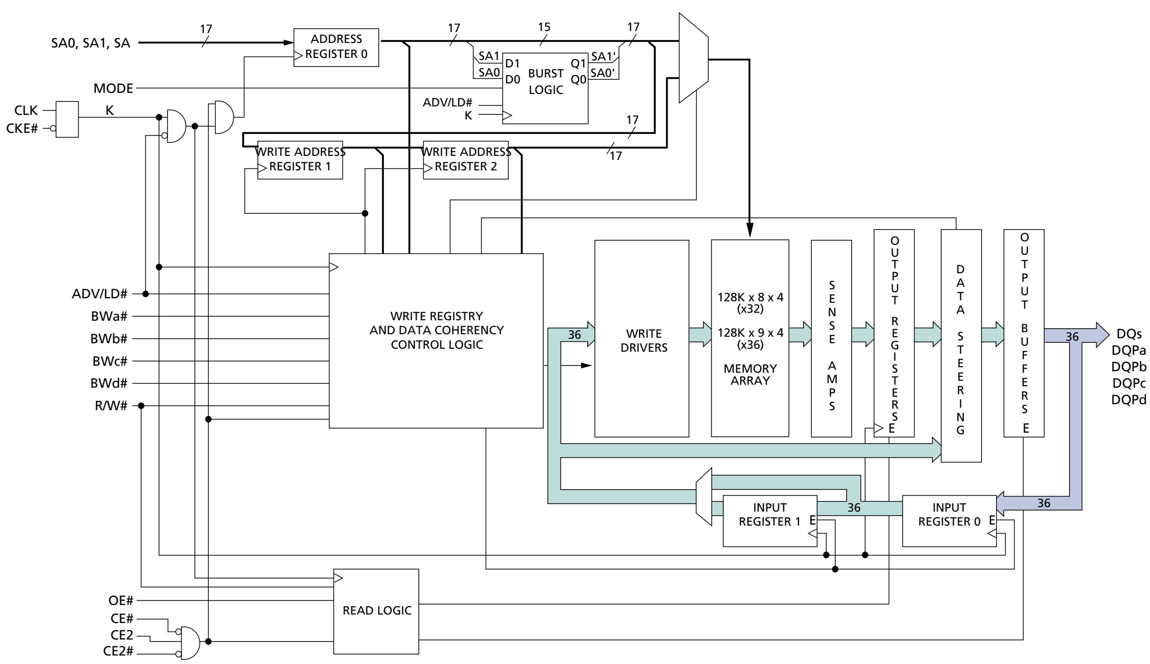
The Micron® Zero Bus Turnaround™ (ZBT®) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 4Mb ZBT SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK).

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 32/36



NOTE: Functional block diagrams illustrate simplified device operation. See truth tables, pin descriptions, and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc#, and BWd#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The data-out (Q), enabled by OE#, is registered by the rising edge of CLK. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the pipelined ZBT SRAM uses a LATE LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The data associated with the address is required two cycles later, or on the rising edge of clock cycle three.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 4Mb ZBT SRAMs operate from a +3.3V V_{DD} power supply, and all inputs and outputs are LVTTL-compatible. Users can choose either a 2.5V or 3.3V I/O version. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

PIN#	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	VSS		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	VSS		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	VDD		
15	VDD		
16	VDD		
17	VSS		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	VSS		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

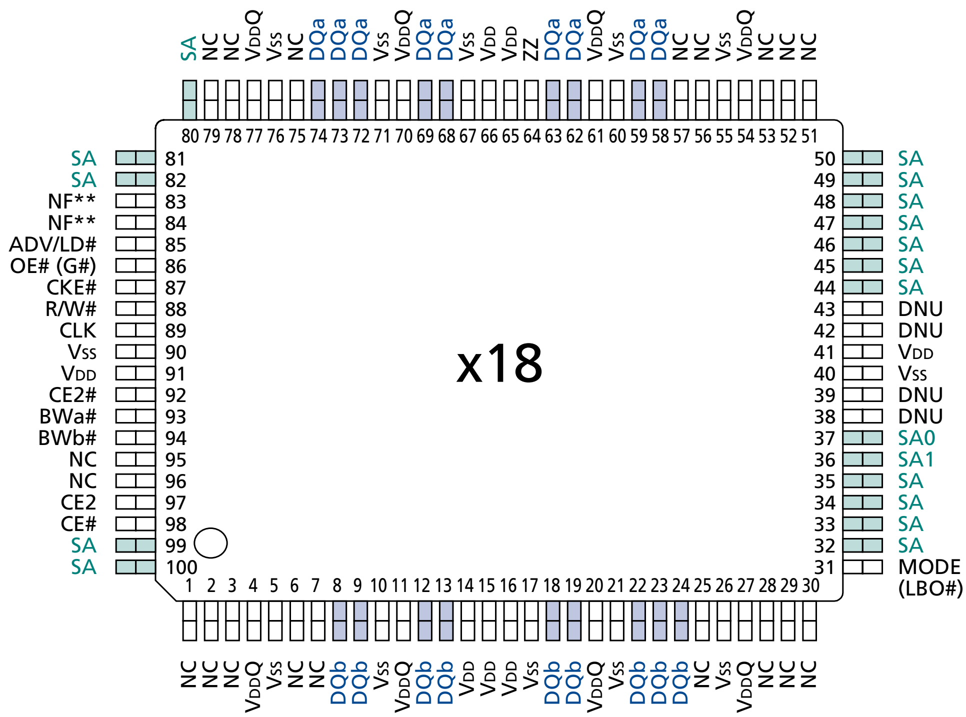
PIN#	x18	x32	x36
26	VSS		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	VSS		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		

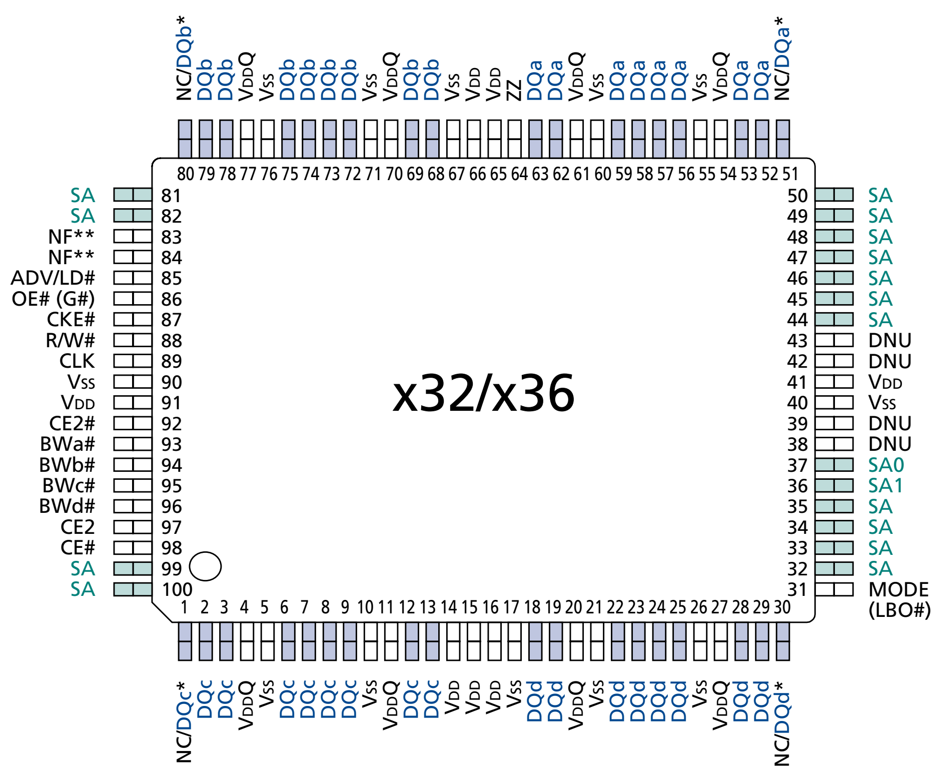
PIN#	x18	x32	x36
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	VSS		
56	NC	DQa	DQa
57	NC	DQa	DQa
58	DQa		
59	DQa		
60	VSS		
61	VDDQ		
62	DQa		
63	DQa		
64	ZZ		
65	VDD		
66	VDD		
67	VSS		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	VSS		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN#	x18	x32	x36
76	VSS		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81	SA		
82	SA		
83	NF*		
84	NF*		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	VSS		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

* Pins 83 and 84 are reserved for address expansion, 8Mb and 16Mb respectively.

Pin Assignment (Top View)
100-Pin TQFP





*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.
**Pins 83 and 84 are reserved for address expansion, 8Mb and 16Mb respectively.

TQFP PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
37 36 32–35, 44–50, 80–82, 99, 100	37 36 32–35, 44–50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 83 and 84 are reserved as address bits for higher-density 8Mb and 16Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

(continued on next page)

TQFP PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
(a) 58, 59, 62, 63, 68, 69, 72–74 (b) 8, 9, 12, 13, 18, 19, 22–24	(a) 52, 53, 56–59, 62, 63 (b) 68, 69, 72–75, 78, 79 (c) 2, 3, 6–9, 12, 13 (d) 18, 19, 22–25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28–30, 51–53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
83, 84	83, 84	NF	–	No Function: These are internally connected to the die and will have the capacitance of input pins. It is allowable to leave these pins unconnected or driven by signals. Reserved for address expansion, pin 83 becomes an SA at 8Mb density and pin 84 becomes an SA at 16Mb density.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
14, 15, 16, 41, 65, 66, 91	14, 15, 16, 41, 65, 66, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.

PIN LAYOUT (Top View)
165-Pin FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	CKE#	ADV/LD#	NC	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	R/W#	OE# (G#)	NC	SA	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	VDD	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	NC	VDD	VSS	VDDQ	NC	NC
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	CKE#	ADV/LD#	NC	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	R/W#	OE# (G#)	NC	SA	NC
C	NC/DQPc*	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	NC/DQPb*
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	VDD	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	NC/DQPd*	NC	VDDQ	VSS	NC	NC	VDD	VSS	VDDQ	NC	NC/DQPa*
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

NOTE: 1. Pins 9A, and 9B reserved for address pin expansion; 8Mb, and 16Mb respectively.

FBGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11A, 11R	6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5B 4A – –	5B 5A 4A 4B	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQas and DQPa; BWb# controls DQbs and DQPb. For the x32 and x36 versions, BWa# controls DQas and DQPa; BWb# controls DQbs and DQPb; BWc# controls DQcs and DQPc; BWd# controls DQds and DQPd. Parity is only available on the x18 and x36 versions.
6B	6B	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3A	3A	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded.
6A	6A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
7A	7A	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
11H	11H	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
7B	7B	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
3B	3B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
8B	8B	OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.

(continued on next page)

FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
8A	8A	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
1R	1R	MODE (LB0#)	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
(a) 10J, 10K, 10L, 10M, 11D, 11E, 11F, 11G (b) 1J, 1K, 1L, 1M, 2D, 2E, 2F, 2G	(a) 10J, 10K, 10L, 10M, 11J, 11K, 11L, 11M (b) 10D, 10E, 10F, 10G, 11D, 11E, 11F, 11G (c) 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G (d) 1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated DQa's; Byte "b" is associated with DQb's. For the x32 and x36 versions, Byte "a" is associated with DQa's; Byte "b" is associated with DQb's; Byte "c" is associated with DQc's; Byte "d" is associated with DQd's. Input data must meet setup and hold times around the rising edge of CLK.
11C 1N – –	11N 11C 1C 1N	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/ I/O	No Connect/Parity Data I/Os: On the x32 version, these are No Connect (NC). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
1H, 2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 7N, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	1H, 2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 7N, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

(continued on next page)

FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 8C, 8N	4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 8C, 8N	V_{SS}	Supply	Ground: GND.
5P, 5R, 7P, 7R	5P, 5R, 7P, 7R	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1A, 1B, 1C, 1D, 1E, 1F, 1G, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 2R, 3H, 4B, 5A, 5N, 6N, 9A, 9B, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N, 11P	1A, 1B, 1P, 2C, 2N, 2P, 2R, 3H, 5N, 6N, 9A, 9B, 9H, 10C, 10H, 10N, 11A, 11B, 11P	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. Pins 9A, and 9B reserved for address pin expansion; 8Mb, and 16Mb respectively.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x18)

FUNCTION	R/W#	BWa#	BWb#
READ	H	X	X
WRITE Byte “a”	L	L	H
WRITE Byte “b”	L	H	L
WRITE All Bytes	L	L	L
WRITE ABORT/NOP	L	H	H

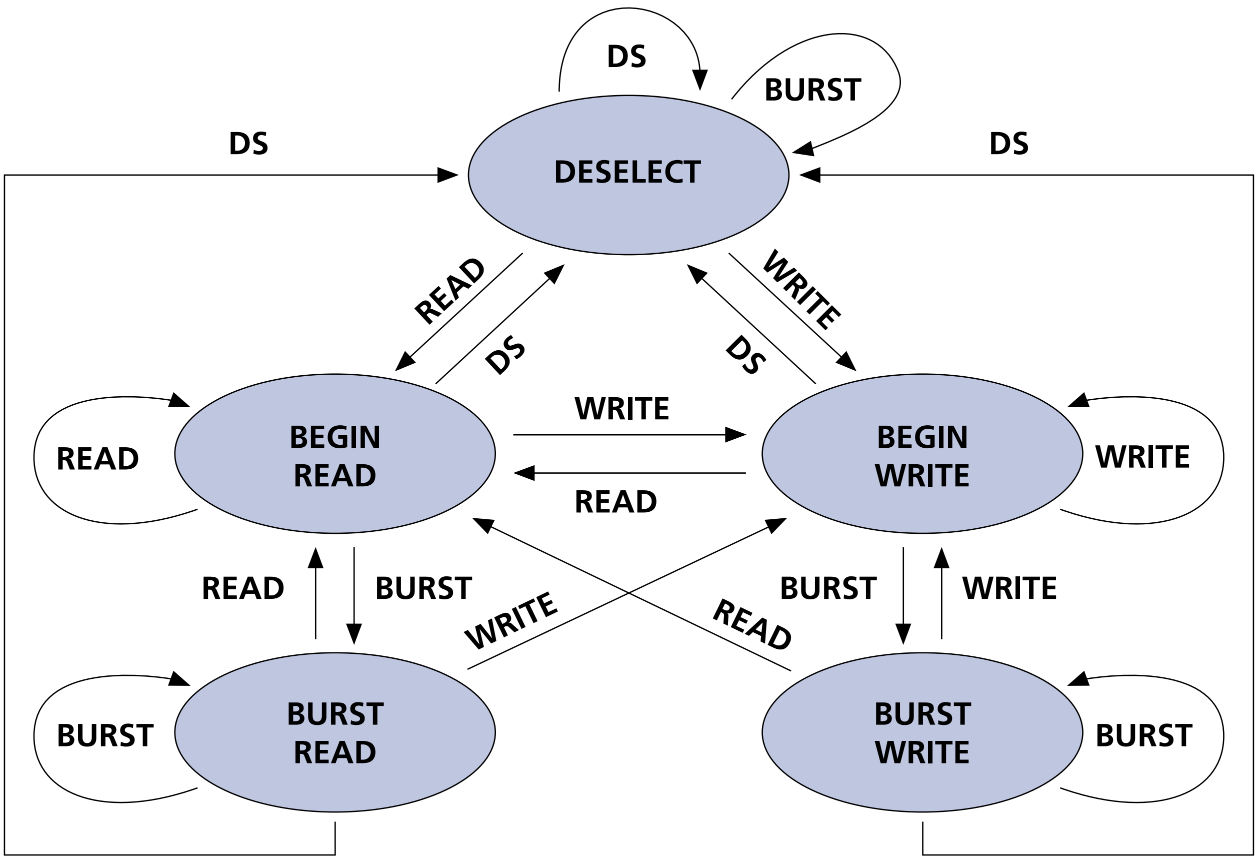
NOTE: Using R/W# and BYTE WRITE(s), any one or more bytes may be written.

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x32/x36)

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
READ	H	X	X	X	X
WRITE Byte “a”	L	L	H	H	H
WRITE Byte “b”	L	H	L	H	H
WRITE Byte “c”	L	H	H	L	H
WRITE Byte “d”	L	H	H	H	L
WRITE All Bytes	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

NOTE: Using R/W# and BYTE WRITE(s), any one or more bytes may be written.

State Diagram for ZBT SRAM



KEY:

COMMAND	OPERATION
DS	DESELECT
READ	New READ
WRITE	New WRITE
BURST	BURST READ, BURST WRITE, or CONTINUE DESELECT

NOTE: 1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK).

TRUTH TABLE

(Notes 5–10)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADV/ LD#	R/W#	BWx	OE#	CKE#	CLK	DQ	NOTES
DESELECT Cycle	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
CONTINUE DESELECT Cycle	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	1
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	1, 11
NOP/DUMMY READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	2
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	1, 2, 11
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	3
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	1, 3, 11
NOP/WRITE ABORT (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	2, 3
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	1, 2, 3, 11
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	–	4
SNOOZE MODE	None	X	X	X	H	X	X	X	X	X	X	High-Z	

NOTE:
1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. Some users may use OE# when the bus turn-on and turn-off times do not meet their requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWa#, BWb#, BWc# and BWd#) are HIGH. BWx = L means one or more byte write signals are LOW.
6. BWa# enables WRITEs to Byte "a" (DQas); BWb# enables WRITEs to Byte "b" (DQbs); BWc# enables WRITEs to Byte "c" (DQcs); BWd# enables WRITEs to Byte "d" (DQds).
7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE# HIGH.
9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth burst cycle.
11. The address counter is incremented for all CONTINUE BURST cycles.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} .... -0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} .... -0.5V to V_{DD}
V_{IN} .... -0.5V to $V_{DD}Q$ + 0.5V
Storage Temperature (plastic) .... -55°C to +150°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD}, $V_{DD}Q$ = 3.3V ±0.165 unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input High (Logic 1) Voltage	DQ pins	V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ V_{DD}	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 4
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	V_{DD}	V	1, 5

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ $^tKHKH/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ $^tKHKH/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.465V and V_{DD} ≤ 3.135V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be externally wired together to the same power supply for 3.3V I/O operation.

2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = +2.5V +0.4V/-0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.9	V	1

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz V_{DD} = 3.3V	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	4	5	pF	4
Address Capacitance		C_A	3	3.5	pF	4
Clock Capacitance		C_{CK}	3	3.5	pF	4

FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	2.5	3.5	pF	4
Output Capacitance (Q)		C_O	4	5	pF	4
Clock Capacitance		C_{CK}	2.5	3.5	pF	4

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ $^tKHKH/2$ for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ $^tKHKH/2$ for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.465V and V_{DD} ≤ 3.135V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. This parameter is sampled.

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note 1) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V unless otherwise noted)

				MAX				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	200	500	400	300	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; CKE# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	10	25	25	20	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	0.5	10	10	10	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	6	25	25	25	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADV/LD# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	45	120	75	60	mA	3, 4
SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}	0.5	10	10	10	mA	4

NOTE:
1. $V_{DD}Q$ = +3.3V ±0.165V for 3.3V I/O configuration; $V_{DD}Q$ = +2.5V +0.4V/-0.125V for 2.5V I/O configuration.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in a deselected cycle as defined in the truth table. "Device selected" means device is active (not in deselected mode).
4. Typical values are measured at 3.3V, 25°C and 10ns cycle time.

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	46	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	2.8	°C/W	1

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1, 2
Junction to Case (Top)		θ_{JC}	9	°C/W	1, 2
Junction to Pins (Bottom)		θ_{JB}	17	°C/W	1, 2

NOTE: 1. This parameter is sampled.
2. Preliminary package data.

AC ELECTRICAL CHARACTERISTICS

(Notes 6, 8, 9) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V; ZBT mode)

DESCRIPTION	SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS	NOTES
Clock									
Clock cycle time	^{t}KHKH	6.0		7.5		10		ns	
Clock frequency	^{f}KF		166		133		100	MHz	
Clock HIGH time	^{t}KHKL	1.7		2.0		3.2		ns	1
Clock LOW time	^{t}KLKH	1.7		2.0		3.2		ns	1
Output Times									
Clock to output valid	^{t}KHQV		3.5		4.2		5.0	ns	
Clock to output invalid	^{t}KHQX	1.5		1.5		1.5		ns	2
Clock to output in Low-Z	^{t}KHQX1	1.5		1.5		1.5		ns	2, 3, 4, 5
Clock to output in High-Z	^{t}KHQZ	1.5	3.5	1.5	3.5	1.5	3.5	ns	2, 3, 4, 5
OE# to output valid	^{t}GLQV		3.5		4.2		5.0	ns	6
OE# to output in Low-Z	^{t}GLQX	0		0		0		ns	2, 3, 4, 5
OE# to output in High-Z	^{t}GHQZ		3.5		4.2		5.0	ns	2, 3, 4, 5
Setup Times									
Address	^{t}AVKH	1.5		1.7		2.0		ns	7
Clock enable (CKE#)	^{t}EVKH	1.5		1.7		2.0		ns	7
Control signals	^{t}CVKH	1.5		1.7		2.0		ns	7
Data-in	^{t}DVKH	1.5		1.7		2.0		ns	7
Hold Times									
Address	^{t}KHAX	0.5		0.5		0.5		ns	7
Clock enable (CKE#)	^{t}KHEX	0.5		0.5		0.5		ns	7
Control signals	^{t}KHCX	0.5		0.5		0.5		ns	7
Data-in	^{t}KHDX	0.5		0.5		0.5		ns	7

NOTE:
1. This parameter is sampled.
2. Measured as HIGH above V_{IH} and LOW below V_{IL}.
3. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion on these parameters.
4. This parameter is sampled.
5. This parameter is measured with output loading as shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
6. Transition is measured ±200mV from steady state voltage.
7. OE# can be considered a "Don't Care" during WRITEs; however, controlling OE# can help fine-tune a system for turnaround timing.
8. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW to remain enabled.
9. Test conditions as specified with output loading shown in Figure 1 for 3.3V I/O ($V_{DD}Q$ = +3.3V ±0.165V) and Figure 3 for 2.5V I/O ($V_{DD}Q$ = +2.5V +0.4V/-0.125V).
10. A WRITE cycle is defined by R/W# LOW having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.

3.3V I/O AC TEST CONDITIONS

Input pulse levels	Vss to 3.3V
Input rise and fall times	1ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Input pulse levels	Vss to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Output load	See Figures 3 and 4

3.3V I/O Output Load Equivalents

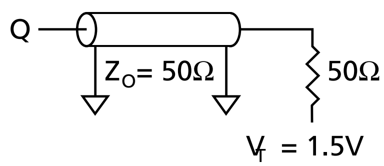


Figure 1

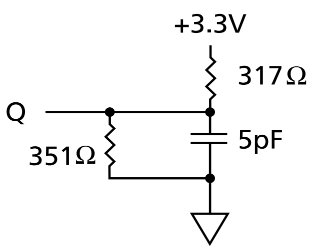


Figure 2

2.5V I/O Output Load Equivalents

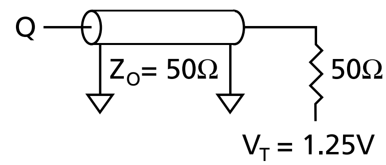


Figure 3

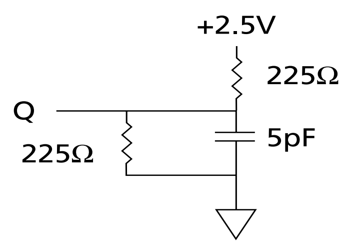


Figure 4

LOAD DERATING CURVES

The Micron 256K x 18, 128K x 32, and 128K x 36 ZBT SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

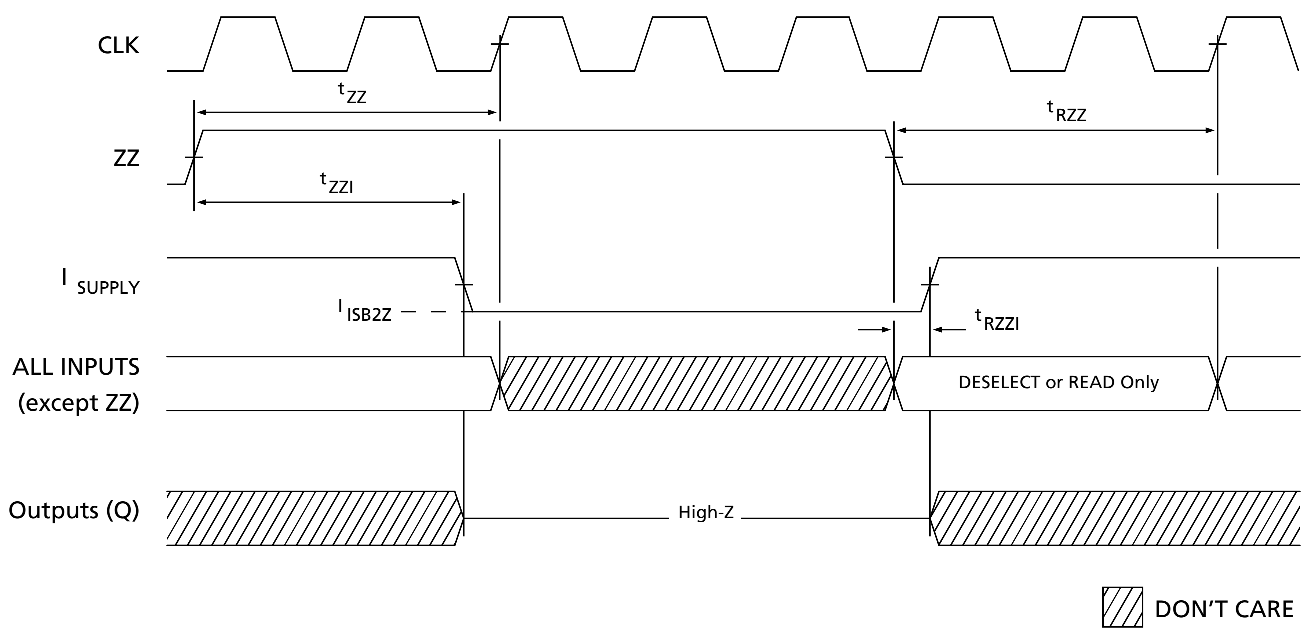
The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the time ${}^tZZI$ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during ${}^tRZZ$, only a DESELECT or READ cycle should be given.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

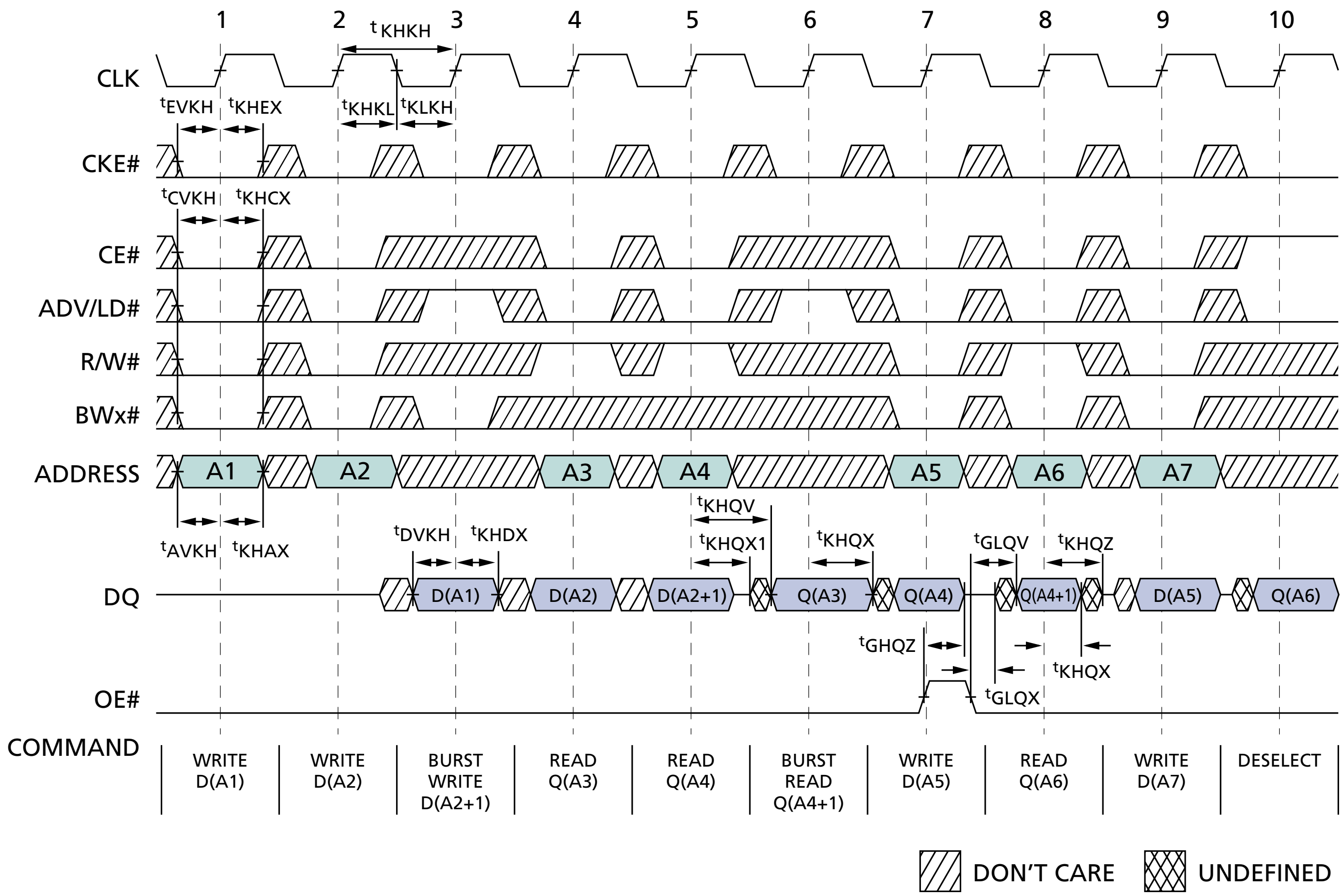
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		10	mA	
Current during SNOOZE MODE (P Version)	ZZ ≥ V_{IH}	I_{SB2ZP}		1	mA	
ZZ active to input ignored		${}^tZZ$	0	2(${}^tKHKH$)	ns	1
ZZ inactive to input sampled		${}^tRZZ$	0	2(${}^tKHKH$)	ns	1
ZZ active to snooze current		${}^tZZI$		2(${}^tKHKH$)	ns	1
ZZ inactive to exit snooze current		${}^tRZZI$	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



READ/WRITE TIMING



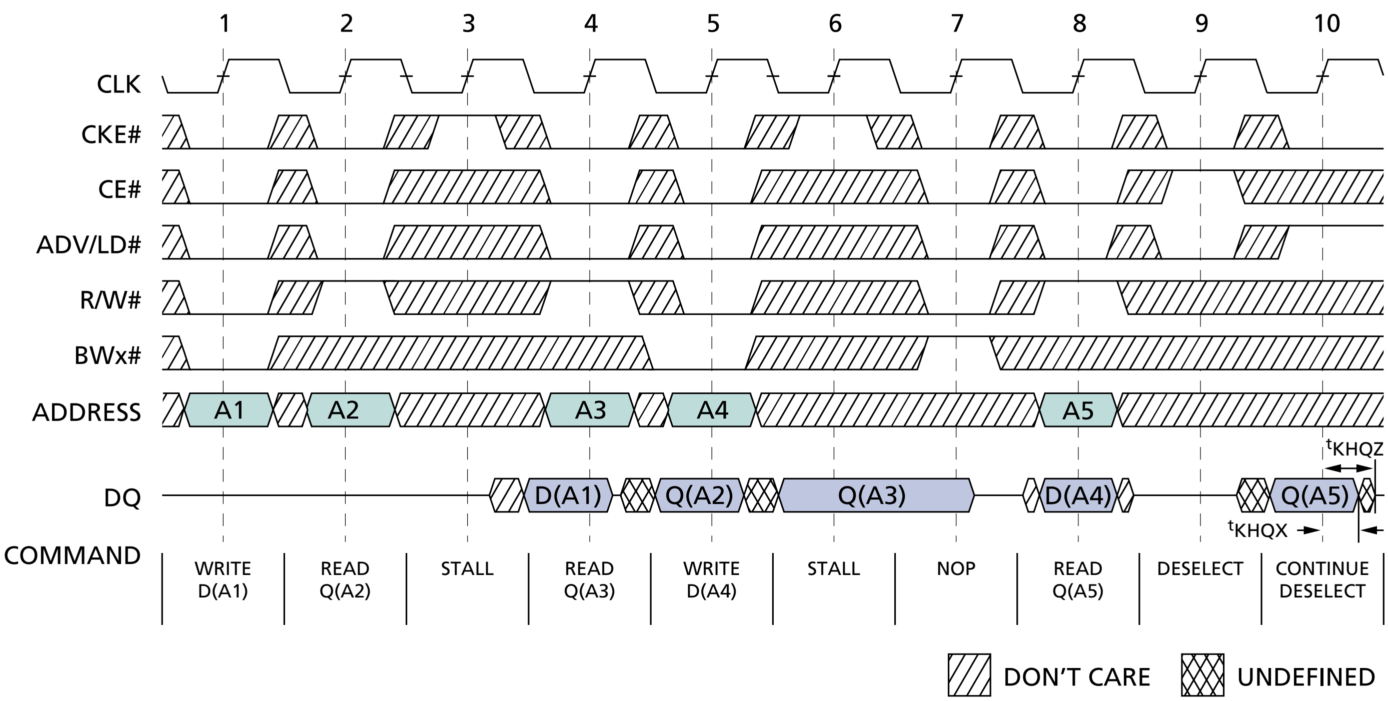
READ/WRITE TIMING PARAMETERS

SYM	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tKHKH	6.0		7.5		10		ns
fKF		166		133		100	MHz
tKHKL	1.7		2.0		3.2		ns
tKLKH	1.7		2.0		3.2		ns
tKHQV		3.5		4.2		5.0	ns
tKHQX	1.5		1.5		1.5		ns
tKHQX1	1.5		1.5		1.5		ns
tKHQZ	1.5	3.5	1.5	3.5	1.5	3.5	ns
tGLQV		3.5		4.2		5.0	ns
tGLQX	0		0		0		ns

SYM	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
tGHQZ		3.5		4.2		5.0	ns
tAVKH	1.5		1.7		2.0		ns
tEVKH	1.5		1.7		2.0		ns
tCVKH	1.5		1.7		2.0		ns
tDVKH	1.5		1.7		2.0		ns
tKHAX	0.5		0.5		0.5		ns
tKHEX	0.5		0.5		0.5		ns
tKHCX	0.5		0.5		0.5		ns
tKHDX	0.5		0.5		0.5		ns

NOTE:
1. For this waveform, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

NOP, STALL, AND DESELECT CYCLES

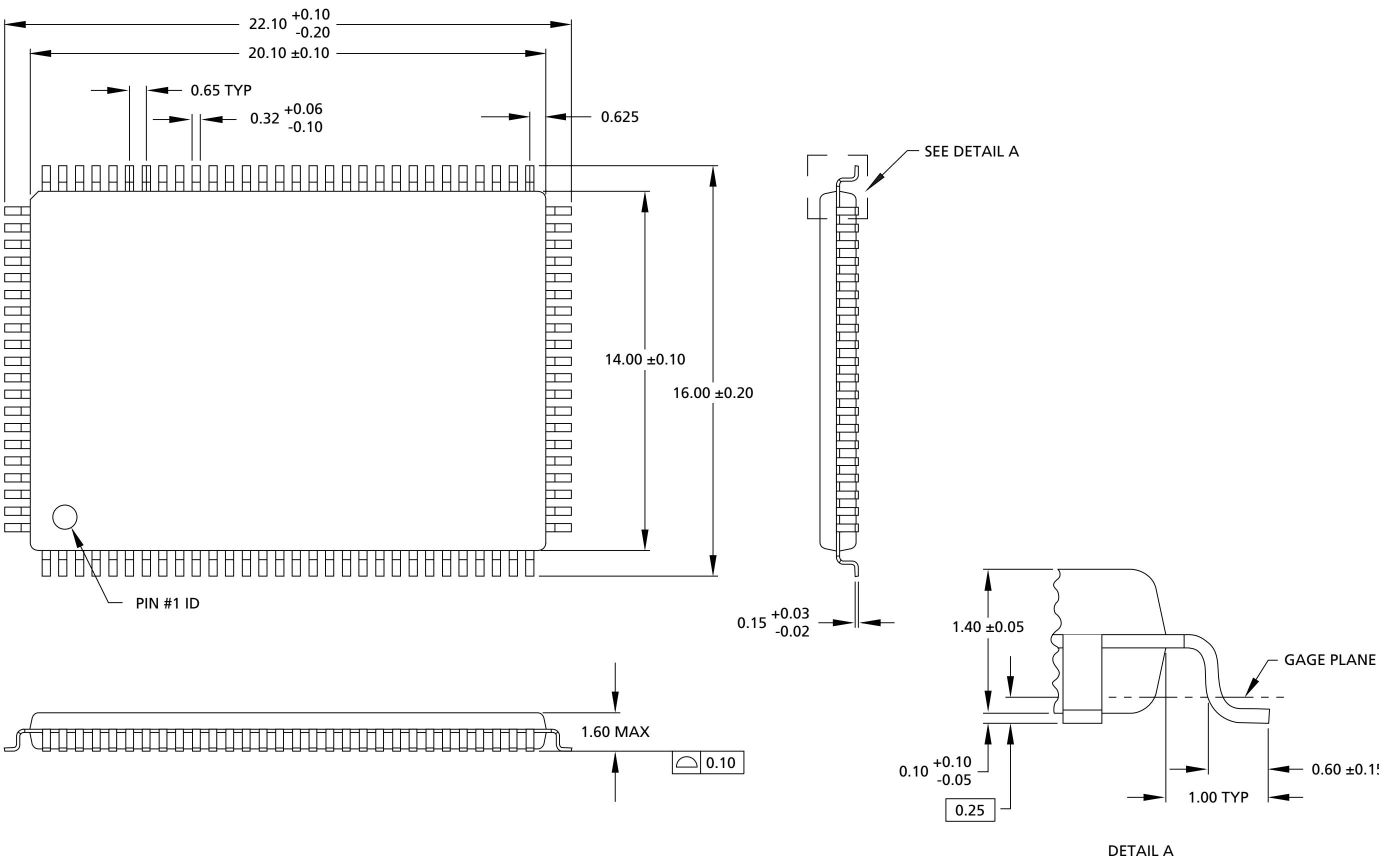


NOP, STALL, AND DESELECT TIMING PARAMETERS

SYM	-6		-7.5		-10		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^tKHQX	1.5		1.5		1.5		ns
^tKHQZ	1.5	3.5	1.5	3.5	1.5	3.5	ns

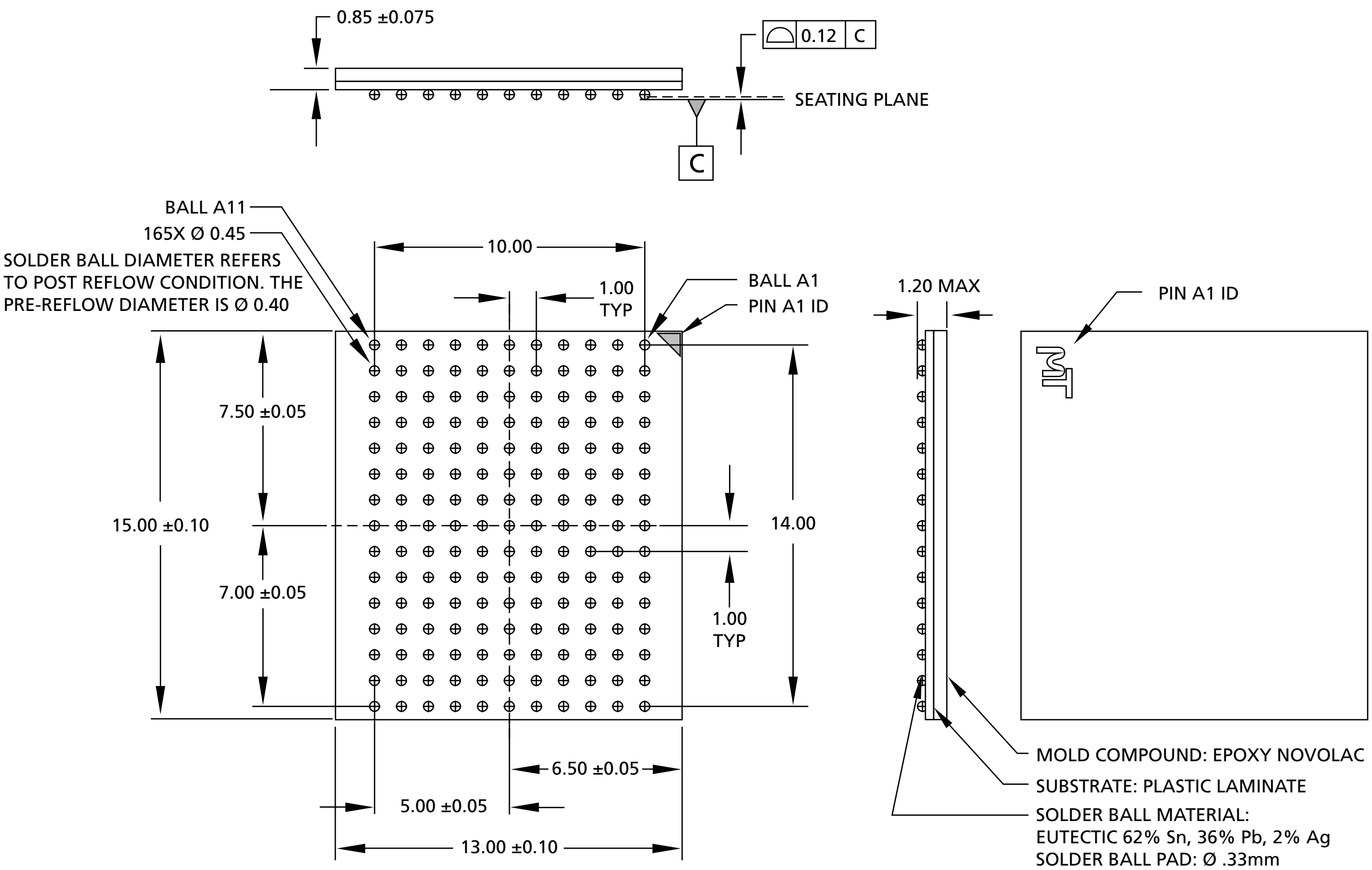
NOTE:
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
2. For this waveform, ZZ and OE# are tied LOW.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

100-PIN PLASTIC TQFP (JEDEC LQFP)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

165-PIN FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATIONS

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micronsemi.com, Customer Comment Line: 800-932-4992

REVISION HISTORY

Updated package drawings .... January 9/03

Removed "Preliminary Package Data" from front page .... February 22/02

Removed 119-pin PBGA package and references .... February 14/02

Removed note "Not Recommended for New Designs," Rev. 6/01 .... June 7/01

Added Industrial Temperature note and references, Rev. 3/01, FINAL .... March 6/01

Added 119-pin PBGA package, Rev. 1/01, FINAL .... January 10/01

Removed FBGA Part Marking Guide, REV 8/00-A, FINAL .... August 22/00

Changed FBGA capacitance values, REV 8/00, FINAL .... August 7/00
C_I; TYP 2.5pF from 4pF; MAX. 3.5pF from 5pF
C_O; TYP 4pF from 6pF; MAX. 5pF from 7pF
C_{CK}; TYP 2.5pF from 5pF; MAX. 3.5pF from 6pF

Added FBGA Part Marking Guide, Rev. 7/00, Preliminary .... July 13/00
Removed 119-pin PBGA package and references

Added 165-pin FBGA package, Rev. 6/00, Preliminary .... May 23/00
Removed all "Smart ZBT" references