SC560

Dual Output Low Noise LDO Linear Regulator

POWER MANAGEMENT

Features

- Input voltage range — 2.5V to 5.5V
- Output voltage ranges — 1.2V to 5.0V (each LDO)
- Maximum output current — 300mA (both LDOs)
- Dropout at 200mA load — 200mV max.
- Quiescent supply current — 100µA (both LDOs enabled)
- Shutdown current — 100nA (typ)
- Output noise < 50µV_{RMS} (SC560A and fixed output versions)
- PSRR < -65dB at 1kHz (SC560A and fixed output versions)
- Over-temperature protection
- Short-circuit protection
- Under-voltage lockout
- Power good monitor for output A (SC560C and fixed output versions)
- Independent enable/disable for LDOB (SC560B and fixed output versions)
- MLPQ-UT8, 1.5mm x 1.5mm x 0.6mm package
- Lead-free and halogen-free

Applications

- PDAs and cellular phones
- GPS devices
- Palmtop computers and handheld instruments
- TFT/LCD applications
- Wireless handsets
- Digital cordless phones and PCS phones
- Personal communicators
- Wireless LAN

Description

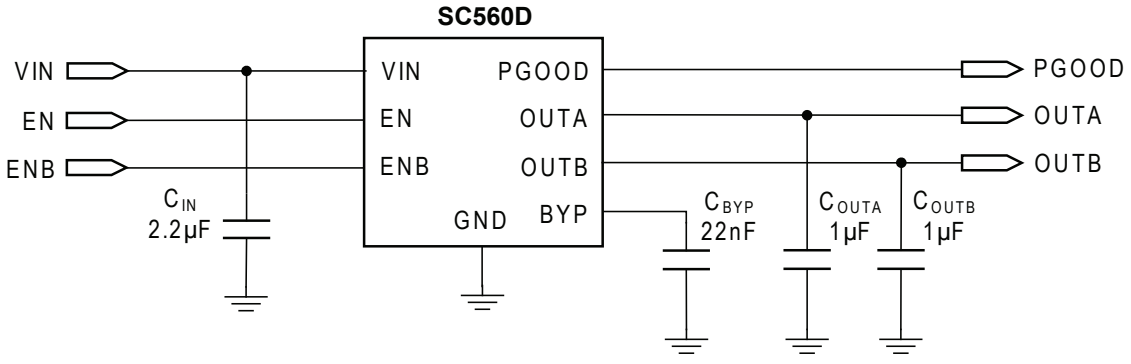
The SC560 is a family of dual output, ultra-low dropout linear voltage regulators designed for use in battery powered wireless applications. The SC560A, SC560B, and SC560C provide adjustable output voltages that can be set using two external resistors. Fixed output voltages are also available (see ordering information for available combinations). Fixed output devices provide the power-good monitor, independent enable pins, and a bypass pin for low-noise operation

All members of the SC560 family require an input voltage level between 2.5V and 5.5V. Output voltages for the adjustable versions can vary between 1.2V and 5.0V. Fixed output voltage options are also chosen from this range.

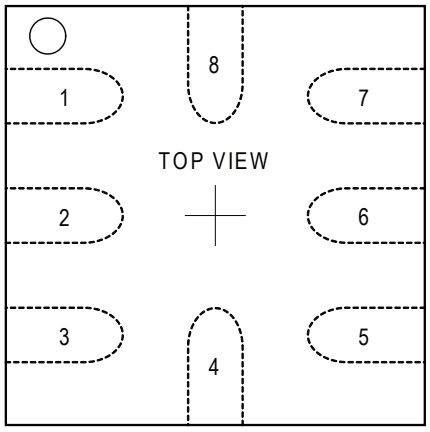
The SC560A provides superior low-noise performance by using an external bypass capacitor connected to pin 7 to filter the bandgap reference. The SC560B uses pin 7 as a separate enable pin for the second regulator output so the two outputs can be controlled independently. The SC560C uses this pin to provide a PGOOD output to hold a processor in reset when the voltage on OUTA is not in regulation. All other versions provide all three functions with fixed output voltages (no feedback pins are provided).

The device also provides protection circuitry such as current limiting, under-voltage lockout, and thermal protection to prevent device failures. Stability is maintained by using 1µF capacitors on the output pins. The MLPQ-UT8 package and 0402 ceramic capacitors minimize the required PCB area.

Typical Application Circuit



Pin Configuration



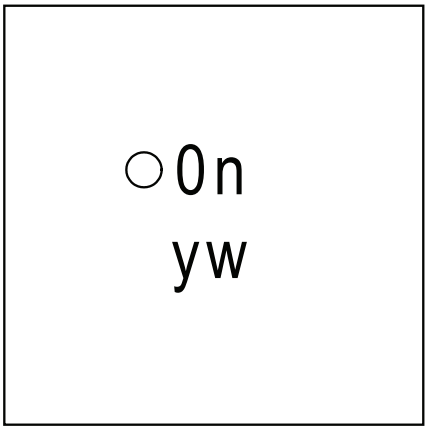
MLPQ-UT-8; 1.5x1.5, 8 LEAD
θ_{JA} = 157°C/W

Ordering Information

Device	Package
SC560xULTRT[1][2][3]	MLPQ-UT8 1.5×1.5
SC560xEVB[3]	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant and halogen-free.
(3) The device variant is denoted by the x.

Marking Information



0n = Part No. Code
See Pinout and Voltage Options Table for details
yw = Datecode

Pinout and Voltage Options

Device	Pin Options			Output Voltage Options		Part No. Code
	Pin 4	Pin7	Pin 8	V_{LDOA}	V_{LDOB}	
SC560A	FBA	BYP	FBB	ADJ	ADJ	0A
SC560B	FBA	ENB	FBB	ADJ	ADJ	0B
SC560C	FBA	PGOOD	FBB	ADJ	ADJ	0C
SC560D	ENB	BYP	PGOOD	2.8V	1.8V	0D
SC560E	ENB	BYP	PGOOD	2.85V	2.85V	0K
SC560F	ENB	BYP	PGOOD	2.5V	1.8V	0L
SC560G	ENB	BYP	PGOOD	2.8V	1.5V	0U
SC560H	ENB	BYP	PGOOD	3.3V	3.3V	0S
SC560L	ENB	BYP	PGOOD	3.3V	1.8V	0Z

Absolute Maximum Ratings

VIN (V) ..... -0.3 to +6.5
EN, ENB (V) ..... -0.3 to (V_{IN} + 0.3)
PGOOD (V) ..... -0.3 to (V_{IN} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUTA, OUTB Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
V_{IN} (V) ..... $2.5 \le V_{IN} \le 5.5$
V_{OUTA}, V_{OUTB} (V) ..... $1.2 \le V_{OUT} \le 5.0$

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) ... 157
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 3.6V, C_{IN} = 2.2µF, C_{OUTA} = C_{OUTB} = 1µF, V_{EN} = V_{ENB} = V_{IN}, T_A = -40 to +85°C. Typical values are at T_A = 25°C. All specifications apply to both LDOs unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply Voltage Range	V_{IN}		2.5		5.5	V
Output Voltage	V_{OUTx}	$V_{IN} > V_{OUTx} + 0.3V$	1.2		5.0	V
Output Voltage Accuracy	ΔV_{OUTx}	V_{IN} = 2.5V to 5.5V, I_{OUTx} = 0 to 300mA, $V_{IN} > V_{OUTx} + 0.3V$	-3		3	%
Maximum Output Current	I_{MAX}		300			mA
Dropout Voltage[1]	V_D	I_{OUTx} = 200mA, V_{OUTx} = 2.5V		180	215	mV
		I_{OUTx} = 200mA, V_{OUTx} = 3.3V to 5.0V		100		mV
Shutdown Current	I_{SD}	T_A = 25°C		0.1	1	µA
Quiescent Current	I_Q	I_{OUTA} = I_{OUTB} = 0mA, T_A = 25°C		100		µA
Load Regulation	ΔV_{LOAD}	I_{OUTx} = 1mA to I_{MAX}			20	mV
Line Regulation	ΔV_{LINE}	I_{OUTx} = 1mA	-6		6	mV
Feedback Regulation Voltage[2]	V_{FB}		0.985	1	1.015	V
Current Limit	I_{LIM}		350		850	mA

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Noise[3]	e_N	V_{IN} = 3.7V, I_{OUTx} = 50mA , 10Hz < f < 100kHz, C_{BYP} = 22nF		50		μV_{RMS}
		V_{IN} = 3.7V, I_{OUTx} = 50mA , 10Hz < f < 100kHz		300		μV_{RMS}
Power Supply Rejection Ratio [3]	PSRR	V_{IN} = 3.7V, I_{OUTx} = 50mA, f = 1kHz, C_{BYP} = 22nF		65		dB
		V_{IN} = 3.7V, I_{OUTx} = 50mA, f = 1kHz		40		
PGOOD Delay[4]	t_{DELAY}		160	200	240	ms
PGOOD Threshold[4]	$V_{TH-PGOOD}$	Percentage of nominal output, V_{OUTA} falling	82	87	92	%
Start-Up Time	t_{SU}	From OFF to 87% V_{OUTx}, I_{OUTx} = 50mA, C_{BYP} = 22nF[2]		1		ms
Power Up Delay Between LDOA and LDOB[5]	t_{DELAY}	Delay between V_{OUTA} and V_{OUTB} start-ups		128		µs
Under Voltage Lockout	V_{UVLO}	V_{IN} Rising	2.15	2.25	2.35	V
UVLO Hysteresis	$V_{UVLO-HYS}$			100		mV
Over Temperature Protection Threshold	T_{OT}	Temperature Rising		160		°C
Over Temperature Hysteresis	T_{OT-HYS}			20		°C
Digital Inputs						
Logic Input High Threshold	V_{IH}	V_{IN} = 5.5V	1.25			V
Logic Input Low Threshold	V_{IL}	V_{IN} = 2.5V			0.4	V
Logic Input High Current	I_{IH}	V_{IN} = 5.5V			1	µA
Logic Input Low Current	I_{IL}	V_{IN} = 5.5V			1	µA
Digital Outputs						
PGOOD Output voltage Low	V_{OL}	I_{SINK} = 500µA,V_{IN}=3.7V	7		20	mV

Notes:

(1) Dropout voltage is defined as V_{IN} - V_{OUTx} , when V_{OUTx} is 100mV below the value of V_{OUTx} at V_{IN} = V_{OUTx} + 0.5V.

(2) SC560A, SC560B and SC560C only

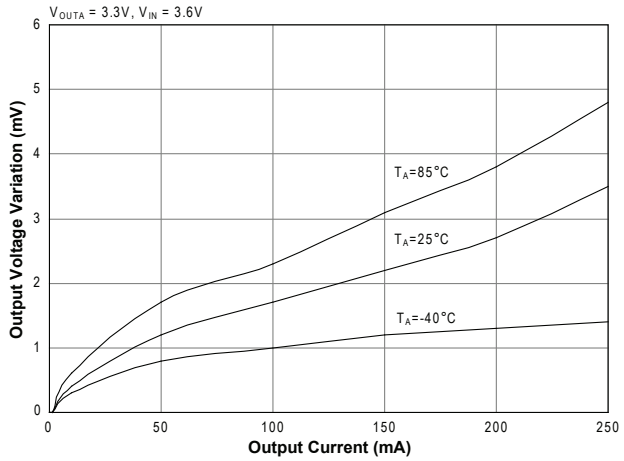
(3) Except SC560B and fixed output versions

(4) Except SC560A and SC560B

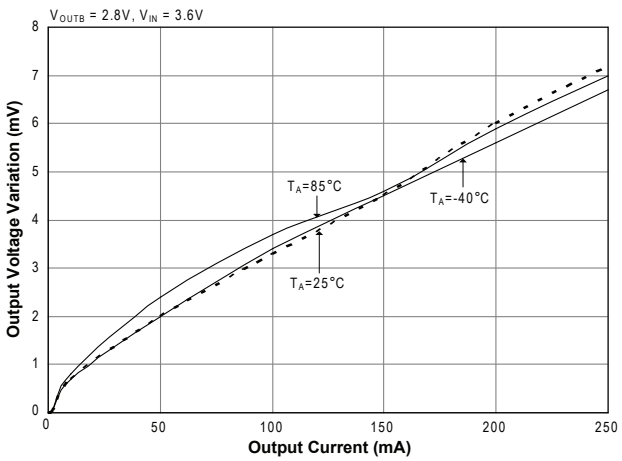
(5) SC560A and SC560C only

Typical Characteristics

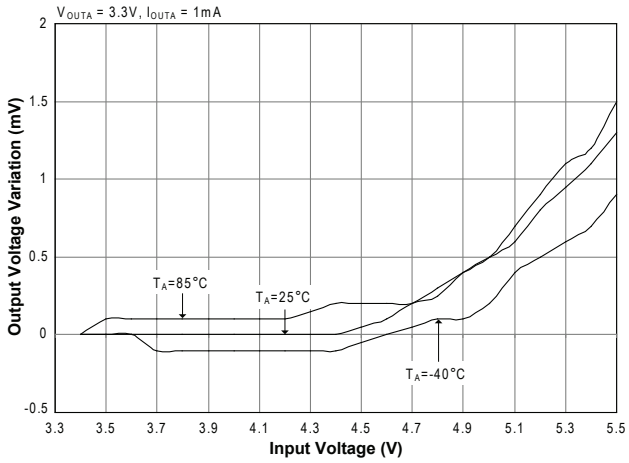
Load Regulation — LDOA



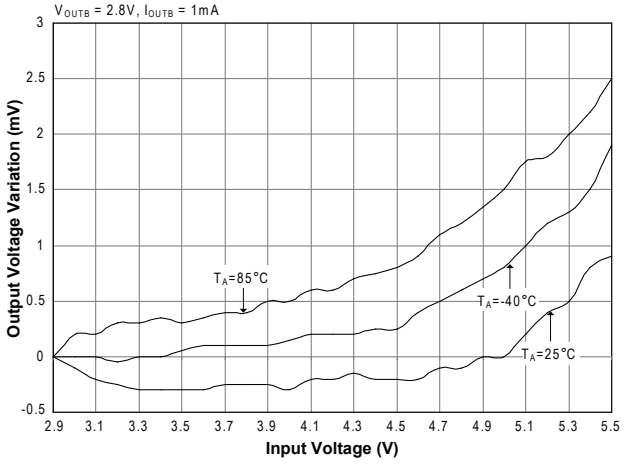
Load Regulation — LDOB



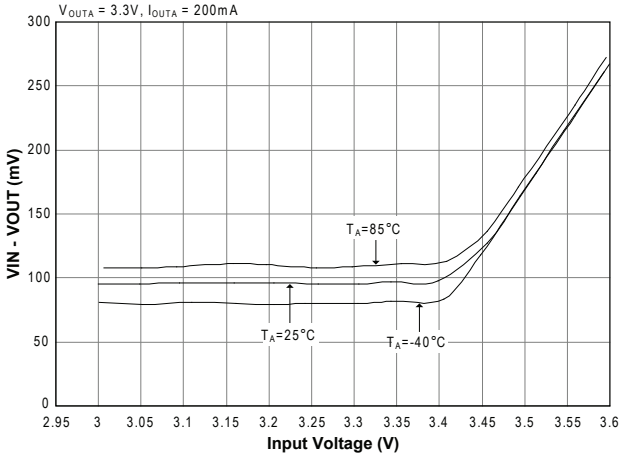
Line Regulation — LDOA



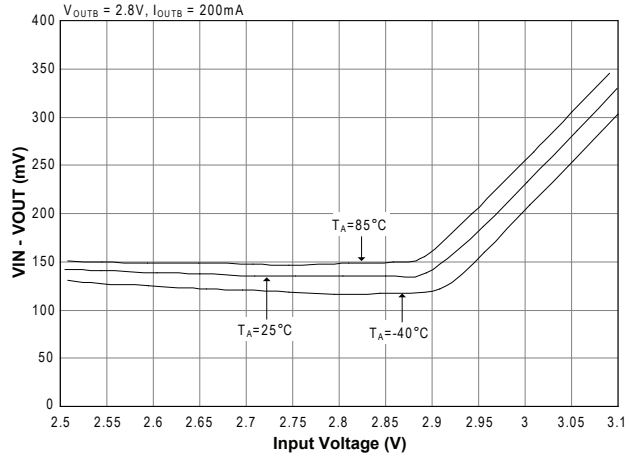
Line Regulation — LDOB



Dropout Voltage LDOA

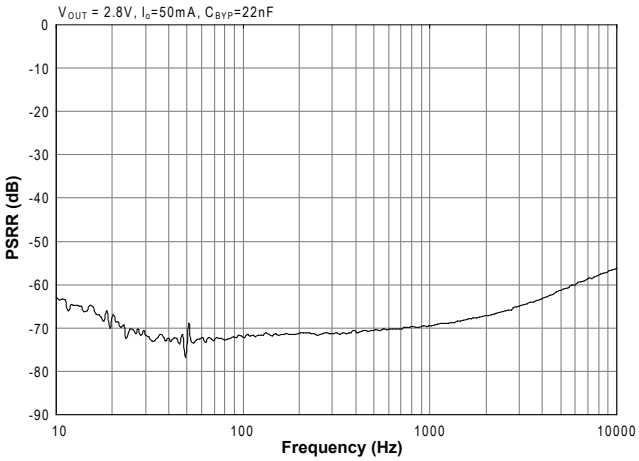


Dropout Voltage LDOB

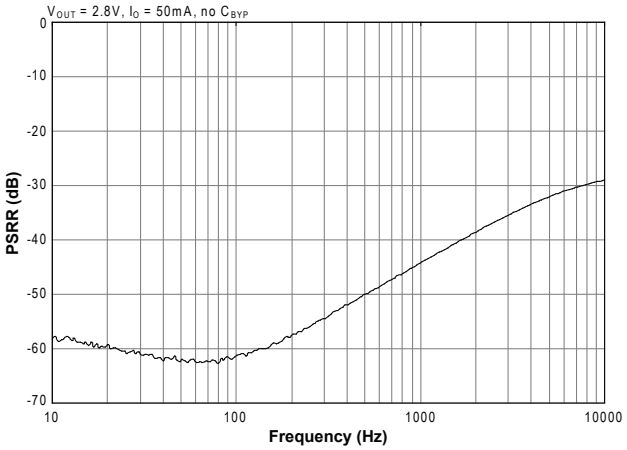


Typical Characteristics (continued)

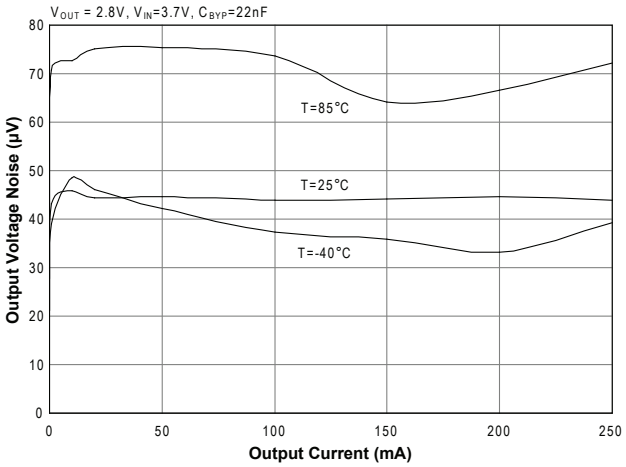
PSRR vs. Frequency (Both LDOs)



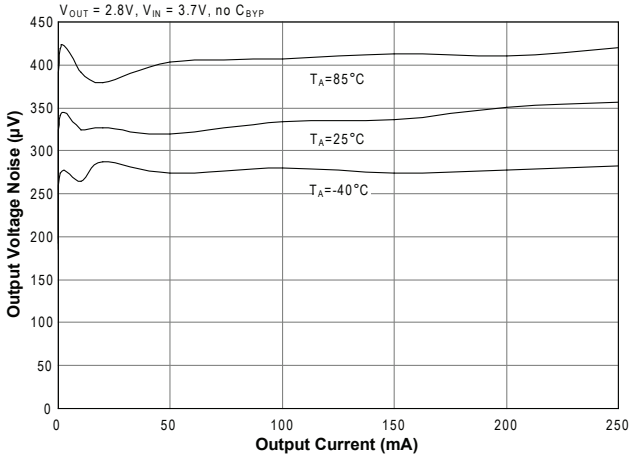
PSRR vs. Frequency (Both LDOs)



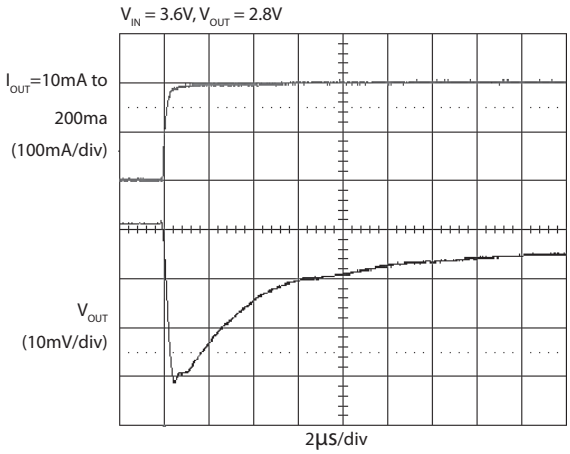
Output Noise vs. Load Current (Both LDOs)



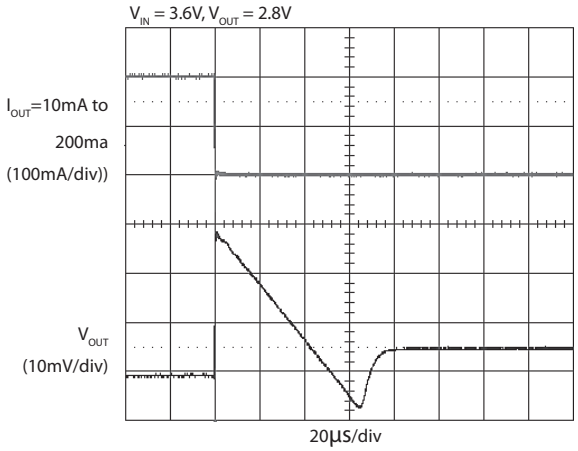
Output Noise vs. Load Current (Both LDOs)



Load Transient Response Rising Edge (Both LDOs)

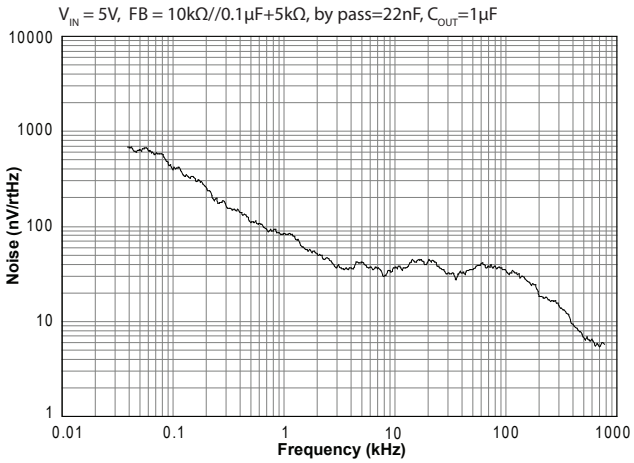


Load Transient Response Falling Edge (Both LDOs)

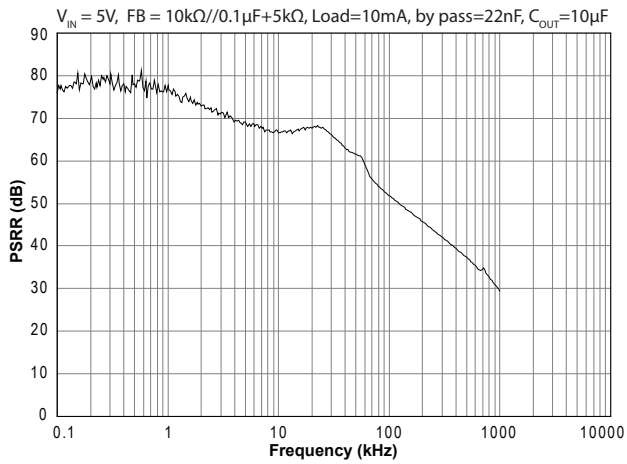


Typical Characteristics (continued)

SC560A Noise Spectrum



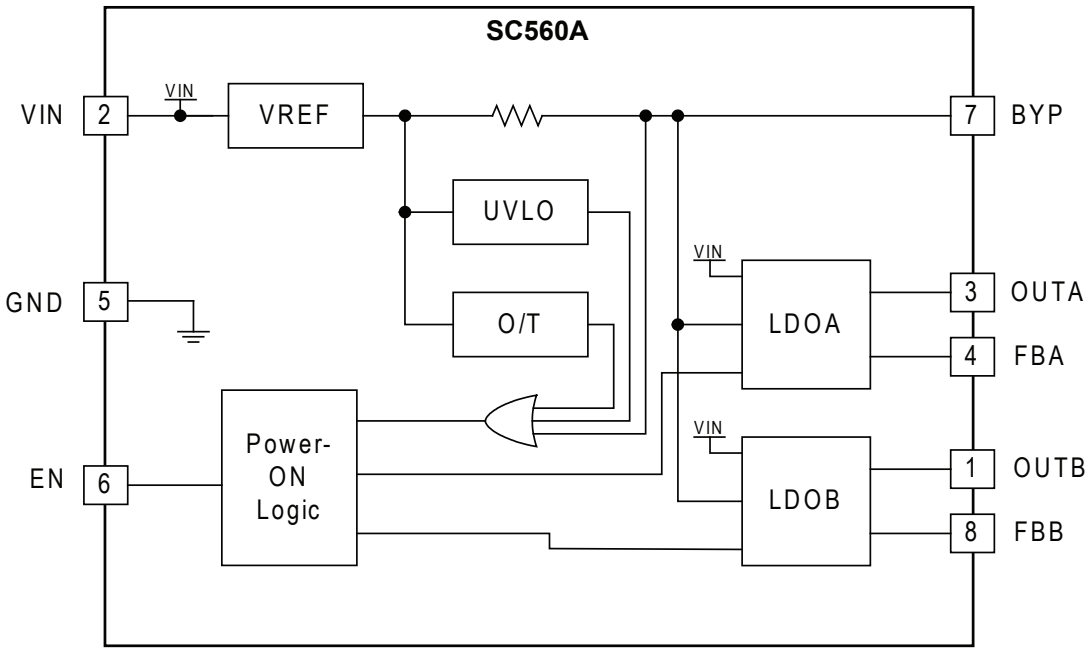
SC560A PSRR vs. Frequency (Both LDOs)

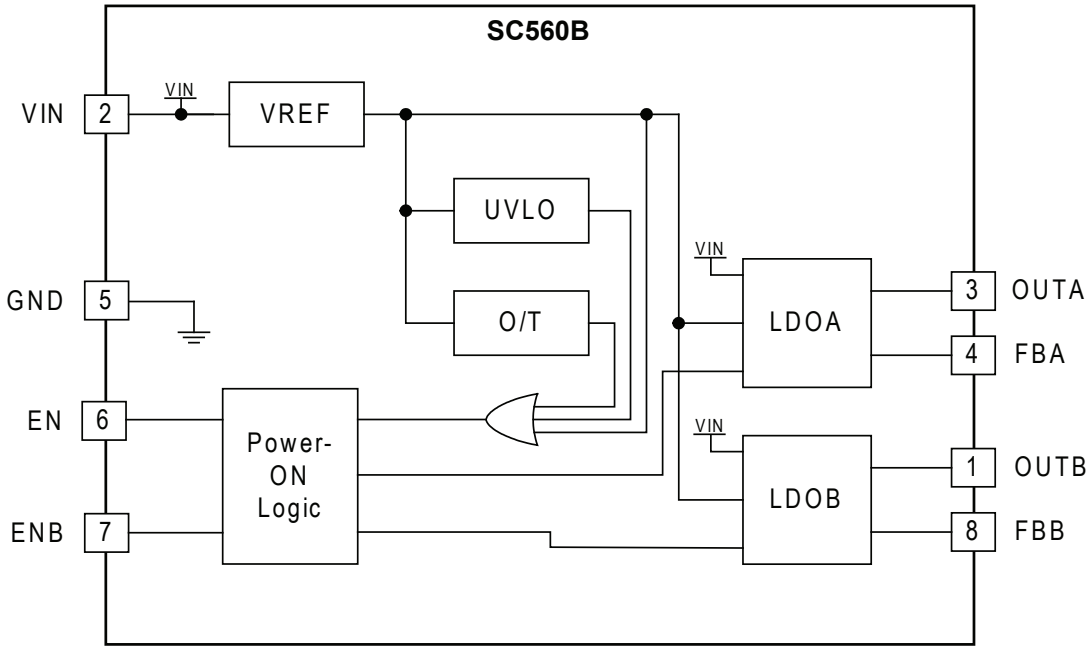


Pin Configurations and Descriptions

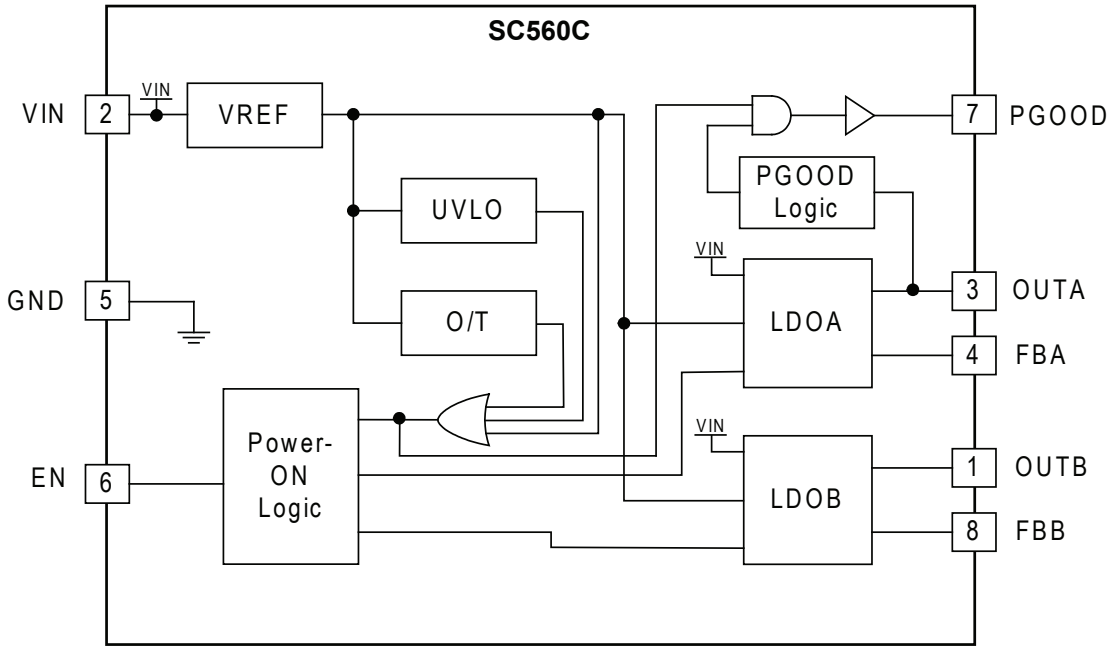
Pin #				Pin Name	Pin Function
SC560A	SC560B	SC560C	SC560 Fixed Output		
1	1	1	1	OUTB	Output for LDOB
2	2	2	2	VIN	Input supply voltage terminal
3	3	3	3	OUTA	Output for LDOA
4	4	4		FBA	Feedback sense pin for LDOA — Connect this pin to an external resistor divider to set V_{OUTA}
5	5	5	5	GND	Analog and digital ground
6	6	6	6	EN	Logic input — active HIGH enables both LDOs for the SC560A and SC560C, or LDOA for all other variants. EN must be active in the SC560B and the fixed output variants before ENB can be activated.
7			7	BYP	LDO bypass output — Bypass with a 22nF capacitor
	7		4	ENB	Logic input — active HIGH enables LDOB for SC560B and the fixed voltage variants.
		7	8	PGOOD	Power Good output — monitors the level of LDOA, switches low when the output drops out of regulation (PGOOD is open drain).
8	8	8		FBB	Feedback sense pin for LDOB — Connect this pin to an external resistor divider to set V_{OUTB}

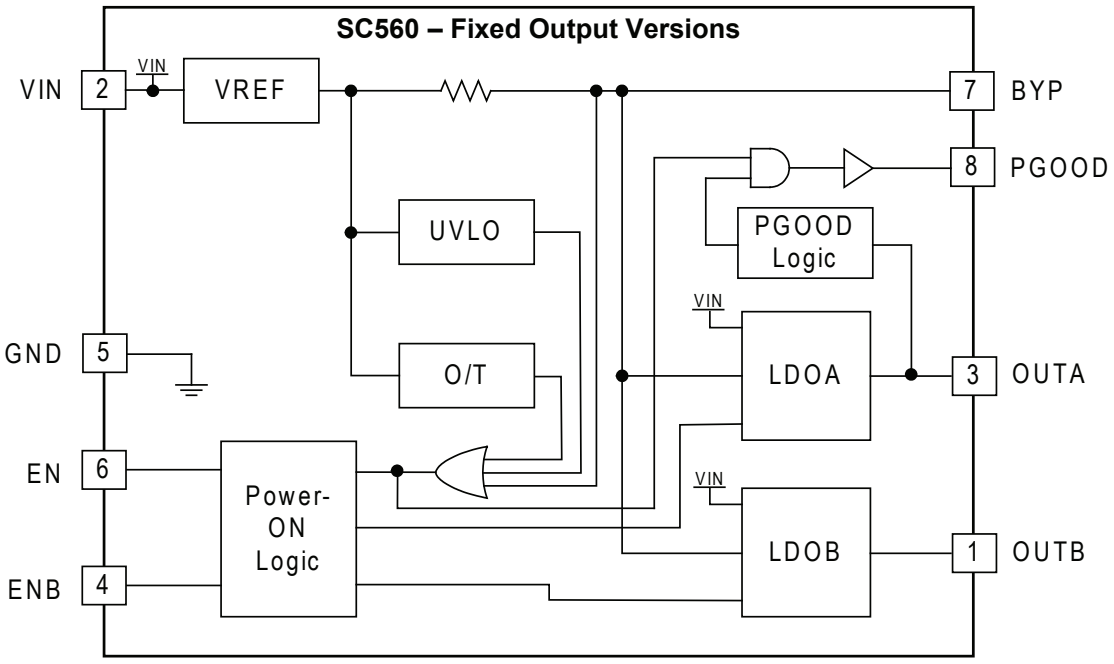
Block Diagrams



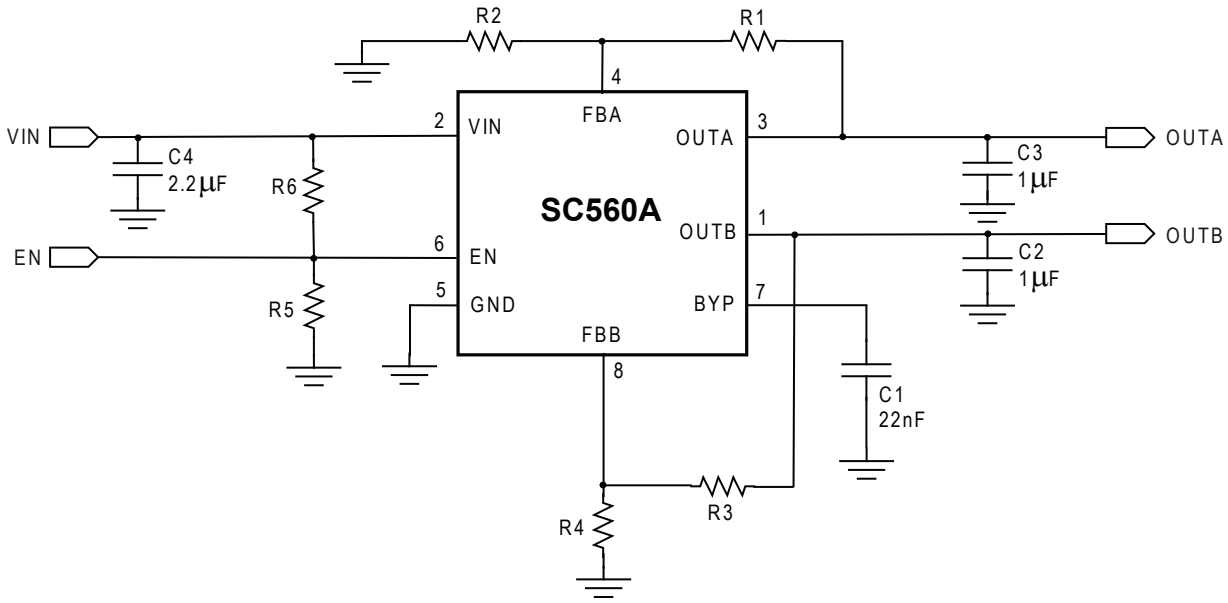


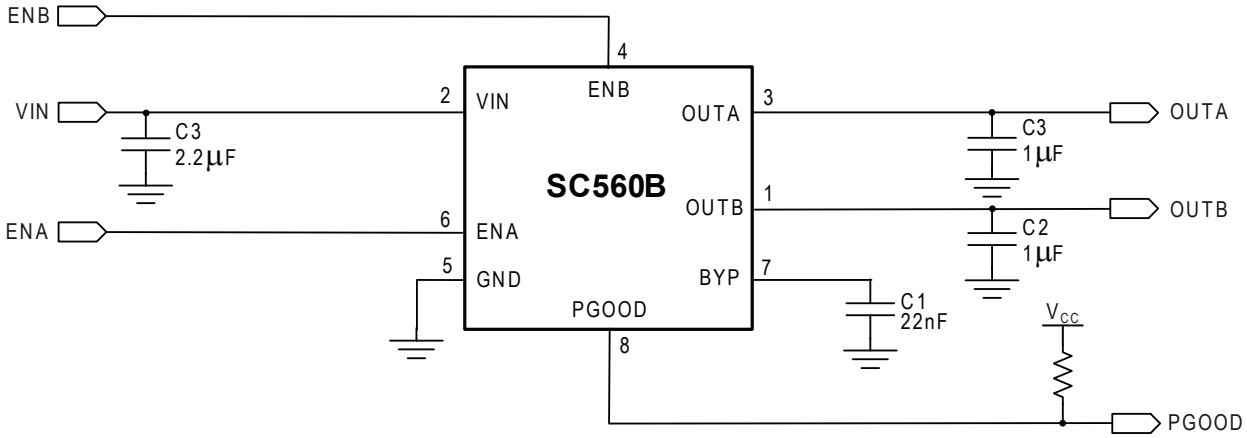
Block Diagrams (continued)



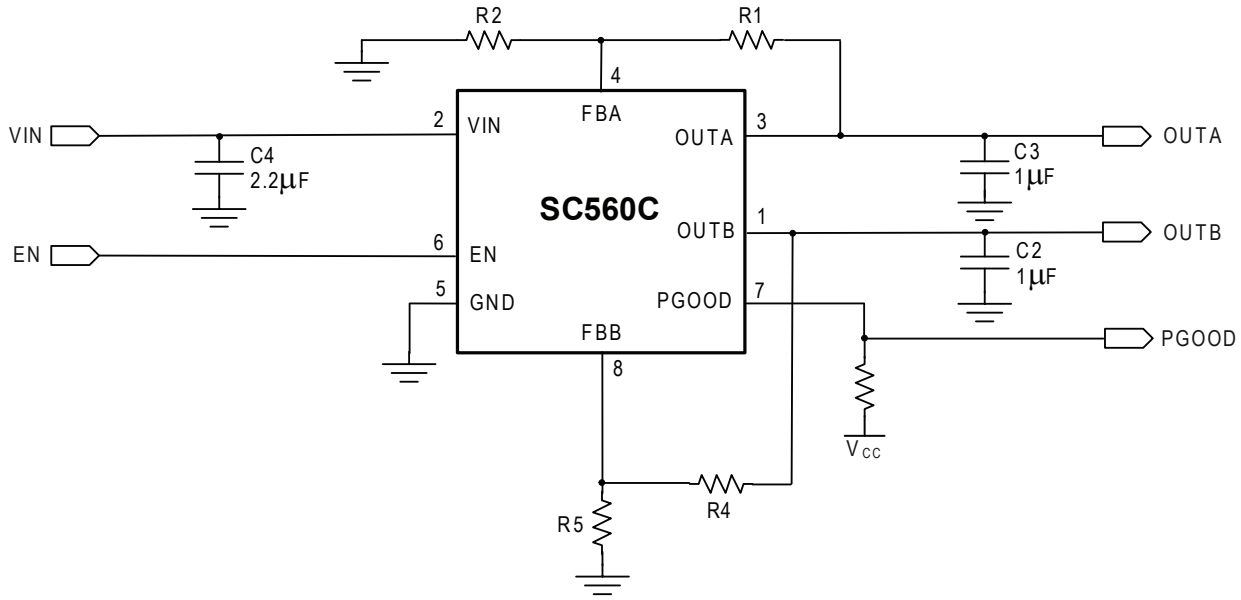


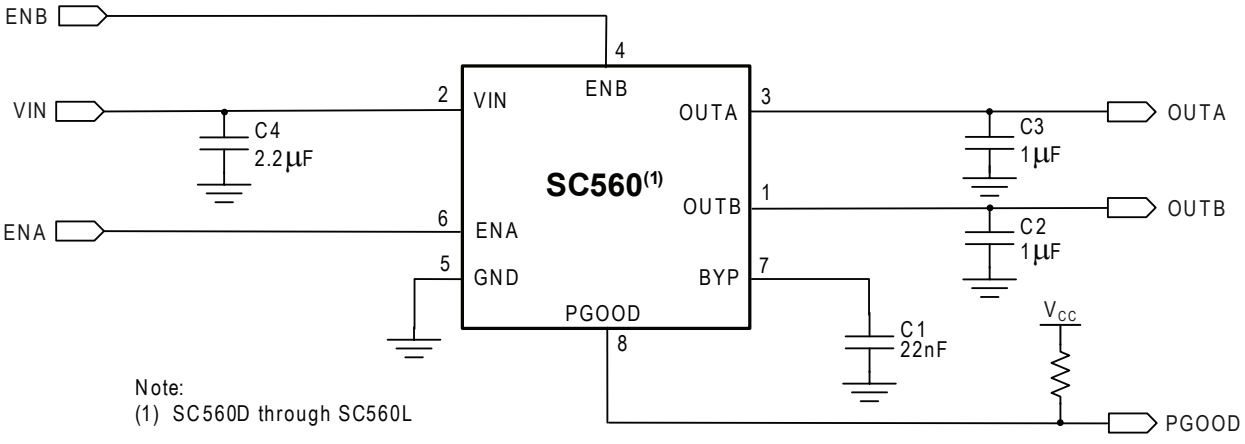
Detailed Application Circuits — SC560A and SC560B





Detailed Application Circuits — SC560C and SC560 Fixed Output Versions





Note:
(1) SC560D through SC560L

Applications Information

General Description

The SC560 is a family of dual output linear regulator devices intended for applications where low dropout voltage, low supply current, and low output noise are critical. Each device provides a very simple, low cost solution for two separate regulated outputs. Very little PCB area is required due to the miniature package size and the need for only four external capacitors.

The linear regulators LDOA and LDOB are powered from a single input supply rail, and each provides 300mA of output current. The SC560 can provide output voltages in the range 1.2V to 5.0V. The output voltages for the SC560A, SC560B and SC560C are set by connecting external resistor dividers to the feedback pins of each LDO. All other versions of the SC560 have fixed output voltage values shown in the Pinout and Voltage Options table on page 2. Refer to the previous two pages for detailed application circuits for each version.

Power On Control

The SC560A and SC560C devices have a single enable pin (EN) that controls both LDO outputs. Pulling this pin low causes the device to enter a low power shutdown mode where it typically draws 100nA from the input supply.

When EN transitions high, the output of LDOA is enabled. After a delay of 128µs, the output of LDOB is enabled. In the SC560C, when the output voltage of LDOA reaches 87% of its regulation point, the delay timer starts and the PGOOD signal transitions high after a delay of 200ms. The power up/down sequence is shown in the timing diagram in Figure 1.

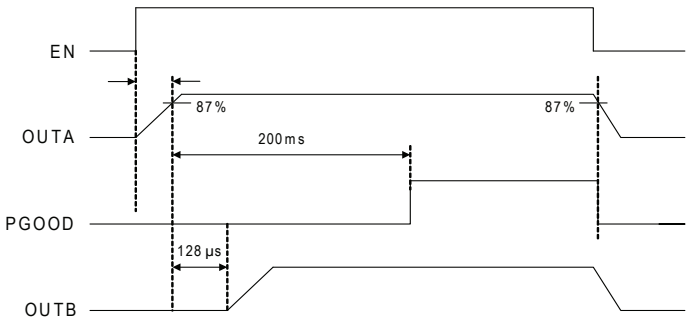


Figure 1 — Timing Diagram

The SC560B and the fixed output variants provide a separate enable pin for LDOB which allows LDOA and LDOB to be enabled independently. The EN pin controls the LDOA output and the ENB provides the same functionality relative to the LDOB output. The table shown below lists the effect of the polarity of the EN and ENB signals on the outputs of LDOA and LDOB. Note from the table that LDOB can only be enabled when LDOA is already active. Since LDOB can be enabled separately, there is no timing relationship between the two outputs at startup.

EN	ENB	LDOA	LDOB
Low	Low	Off	Off
Low	High	Off	Off
High	Low	On	Off
High	High	On	On

The SC560C and the fixed output variants have a PGOOD signal which monitors the output of LDOA and transitions high 200ms after LDOA has reached 87% of its regulation point. This can be used to hold a processor in reset when the output voltage is out of regulation. Note that when LDOA drops out of regulation and PGOOD is forced low, LDOB is also disabled until PGOOD is reset.

Output Voltage Selection

The output voltage of each LDO for the SC560A, SC560B, and SC560C version is set independently using external resistor dividers. Figure 2 illustrates the proper connection for LDOA.

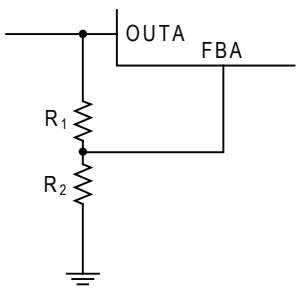


Figure 2 — Output Voltage Feedback Circuit

Applications Information (continued)

The values of the resistors in the voltage divider network can be calculated using the equation:

$$V_{OUT} = V_{REF} \frac{(R_1 + R_2)}{R_2}$$

where V_{REF} = 1V. The value of R2 should be 100kΩ or less to ensure noise performance and stability. Values significantly less than 100kΩ will impact the quiescent current.

Protection Features

The SC560 family provides the following protection features to ensure that no damage is incurred in the event of a fault condition:

- Under-Voltage Lockout
- Over-Temperature Protection
- Short-Circuit Protection

Under-Voltage Lockout

The Under-Voltage Lockout (UVLO) circuit protects the device from operating in an unknown state if the input voltage supply is too low.

When the V_{IN} drops below the UVLO threshold, the LDOs are disabled and PGOOD is held low (SC560C and fixed output variants only). When V_{IN} is increased above the hysteresis level, the LDOs are re-enabled into their previous states, provided EN has remained high. When powering up with V_{IN} below the UVLO threshold, the LDOs remain disabled and PGOOD is held low (SC560C and fixed output variants only).

Over-Temperature Protection

An internal Over-Temperature (OT) protection circuit is provided that monitors the internal junction temperature. When the temperature exceeds the OT threshold as defined in the Electrical Characteristics section, the OT protection disables both LDO outputs and holds the PGOOD signal low. When the junction temperature drops below the hysteresis level, the LDOs are re-enabled into their previous states and PGOOD transitions high after a 200ms delay, provided EN has remained high (SC560C and fixed output variants only).

Short-Circuit Protection

Each output has short-circuit protection. If the output current exceeds the current limit, the output voltage will drop and the output current will be limited until the load current returns to a specified level. If a short-circuit occurs on the output of LDOA, the output of LDOB will also be disabled until the fault is removed and the load current returns to a specified level.

Component Selection

A capacitance of 1µF or larger on each output is recommended to ensure stability. Ceramic capacitors of type X5R or X7R should be used because of their low ESR and stable temperature coefficients. It is also recommended that the input be bypassed with a 2.2µF, low ESR X5R or X7R capacitor to minimize noise and improve transient response. Note: Tantalum and Y5V capacitors are not recommended.

The BYP pin on the SC560D and the fixed output versions must have a minimum of 22nF connected to ground to meet all noise-sensitive requirements. Increasing the capacitance to 100nF will further improve PSRR and output noise.

Applications Information (continued)

Thermal Considerations

Although each of the two LDOs in the SC560 can provide 300mA of output current, the maximum power dissipation in the device is restricted by the miniature package size. The graphs in Figure 3 and Figure 4 can be used as a guideline to determine whether the input voltage, output voltages, output currents, and ambient temperature of the system result in power dissipation within the operating limits are met or if further thermal relief is required.

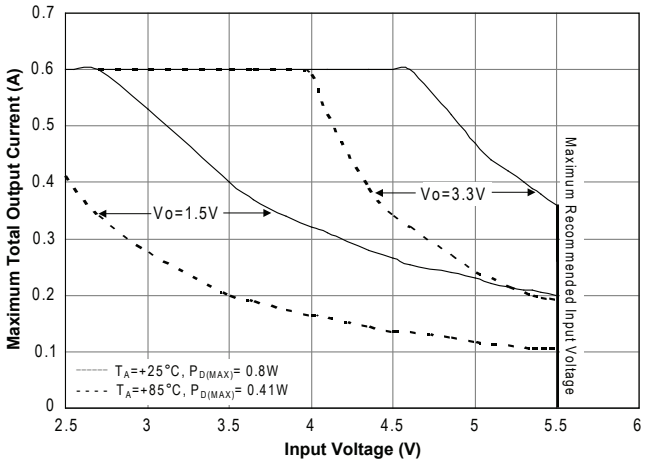


Figure 3 — Safe Operating Limit

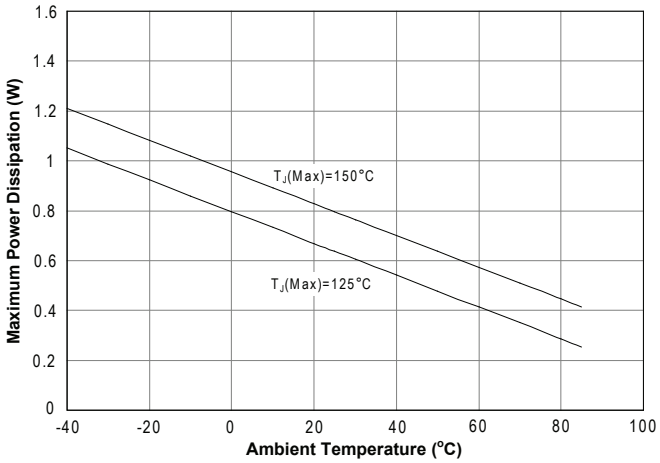


Figure 4 — Maximum P_D vs. T_A

The following procedure can be followed to determine if the thermal design of the system is adequate. The junction temperature of the SC560 can be determined in known operating conditions using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

where

T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
P_D = Power Dissipation (W)
θ_{JA} = Thermal Resistance Junction to Ambient (°C/W)

Example

An SC560D is used to provide outputs of 2.8V, 150mA from LDOA and 1.8V, 200mA from LDOB. The input voltage is 4.2V, and the ambient temperature of the system is 40°C.

$$P_D = 0.15(4.2 - 2.8) + 0.2(4.2 - 1.8)$$
$$= 0.69W$$

and

$$T_J = 40 + (0.69 \times 157) = 148.3°C$$

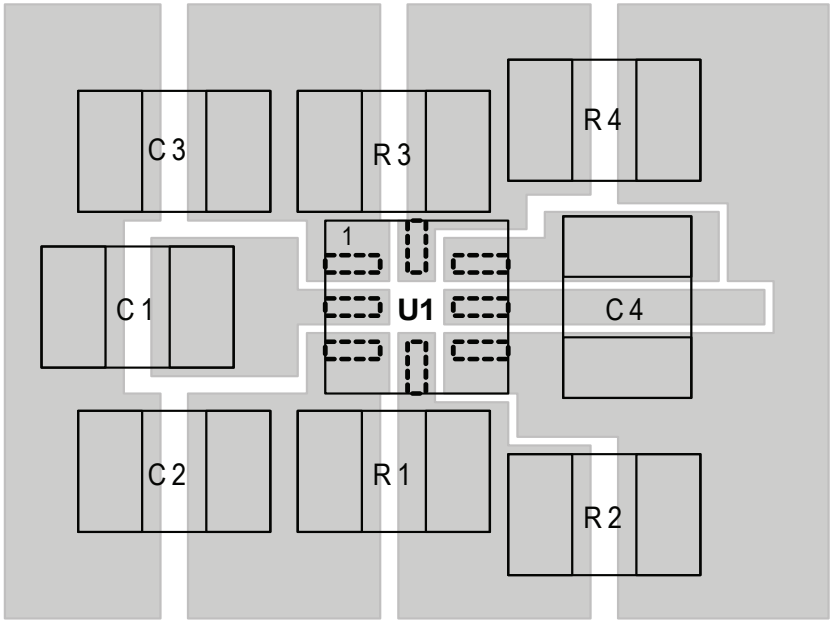
Figures 3 and 4 show that the junction temperature would be within the maximum specification of 150°C for this power dissipation. This means that operation of the SC560 under these conditions is within the specified limits and the device would not require further thermal relief measures.

Applications Information (continued)

Layout Considerations

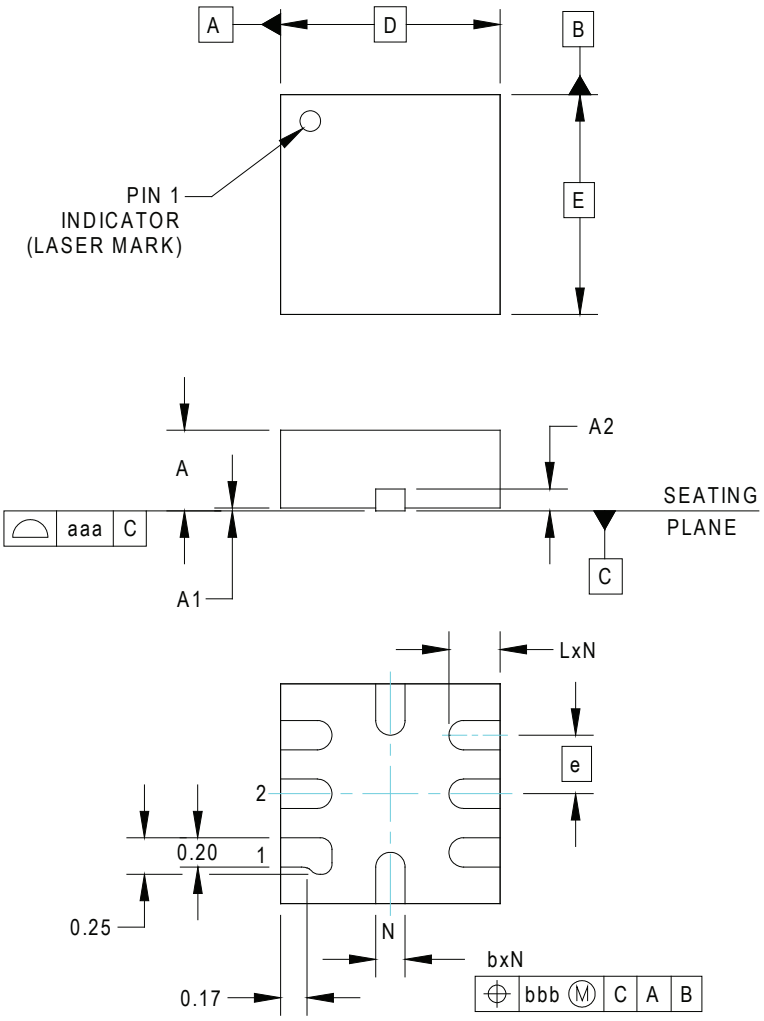
While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation. The diagram below illustrates proper layout of a circuit using the SC560A. For variants that don't require current setting resistors, these devices can be omitted from the layout.

- Attach the part to a large copper footprint, to enable better heat transfer from the device on PCBs where there are internal power and ground planes.
- Place the input, output, and bypass capacitors close to the device for optimal transient response and device behavior.
- Connect all ground connections directly to the ground plane whenever possible to minimize ground potential differences on the PCB.
- Ensure that the feedback resistors are placed as close as possible to the feedback pins.



U1 = SC560A

Outline Drawing — MLPQ-UT8

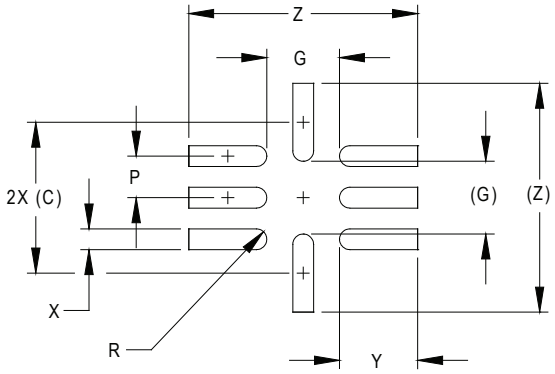


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.018	-	.024	0.45	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D		.059 BSC			1.50 BSC	
E		.059 BSC			1.50 BSC	
e		.016 BSC			0.40 BSC	
L	0.12	.014	0.16	0.30	0.35	0.40
N		8			8	
aaa		.004			0.10	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-UT8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.057)	(1.45)
G	.028	0.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.030	0.75
Z	.087	2.20

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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