Description

The DML22990LWG is a 3.9mΩ, single-channel load switch with controlled and adjustable turn-on and integrated PG indicator.

The DML22990LWG is an N-channel MOSFET operating over an input-voltage range of 0.6V to 5.5V. The switch supports a maximum continuous current of 10A. 3.9mΩ switches on resistance minimize both the voltage drop across the load switch and the power loss from the load switch.

Controlled rise time of the device switch reduces inrush currents caused by large bulk load capacitance, thereby reducing or eliminating power-supply drop. Adjustable slew rate through CT provides the design flexibility to trade off inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

The DML22990LWG has a 200Ω on-chip resistor for quick discharge of the output when switch is disabled. This avoids unknown state caused by floating supply to the downstream load.

Features and Benefits

- V_{BIAS} Voltage Range: 2.5V to 5.5V
- V_{IN} Voltage Range: 0.6V to V_{BIAS}
- Integrated N-Channel MOSFET with Ultra-Low R_{ON}
  - 3.9mΩ at V_{BIAS} = 5V, V_{IN} = 5V
  - 3.9mΩ at V_{BIAS} = 3.3V, V_{IN} = 3.3V
- 10A max Continuous Switch Current
- 80µA Low Quiescent Current
- Shutdown Current
  - I_{STBY_VBIAS} = 0.3µA at V_{BIAS} = 5V
  - I_{STBY_VIN} = 0.5µA at V_{BIAS} = 5V, V_{IN} = 5V
- Controlled and Adjustable Slew Rate via External Capacitor C_T
- Power-Good (PG) Indicator
- Integrated Quick Output Discharge Resistor
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

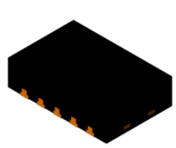
Applications

- Notebooks, tablet computers, desktop PCs and industrial PCs
- Telecoms, set−top boxes, servers, and gateways
- Solid states drives (SSDs)

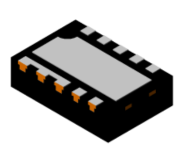
Mechanical Data

- Package: V-DFN3020-10
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.01523 grams (Approximate)

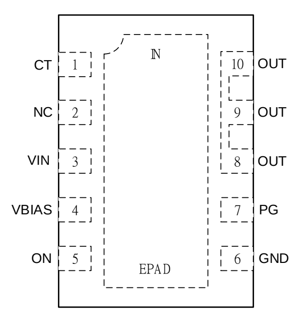
V-DFN3020-10 (Type C)



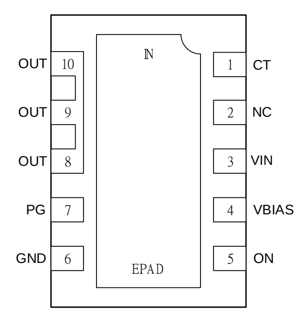
Top View



Bottom View



Top View



Bottom View

Ordering Information (Note 4)

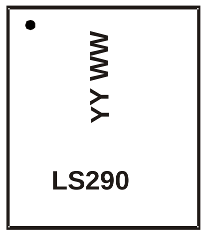
Part Number	Package	Packing	
		Qty.	Carrier
DML22990LWG-7	V-DFN3020-10 (Type C)	3000	Tape & Reel
DML22990LWG-13	V-DFN3020-10 (Type C)	10,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

Site 1:

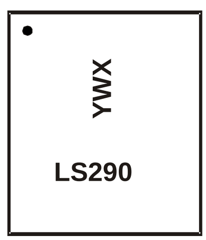
V-DFN3020-10 (Type C)



LS290 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 23 = 2023)
WW = Week Code (01 to 53)

Site 2:

V-DFN3020-10 (Type C)



LS290 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 3 = 2023)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

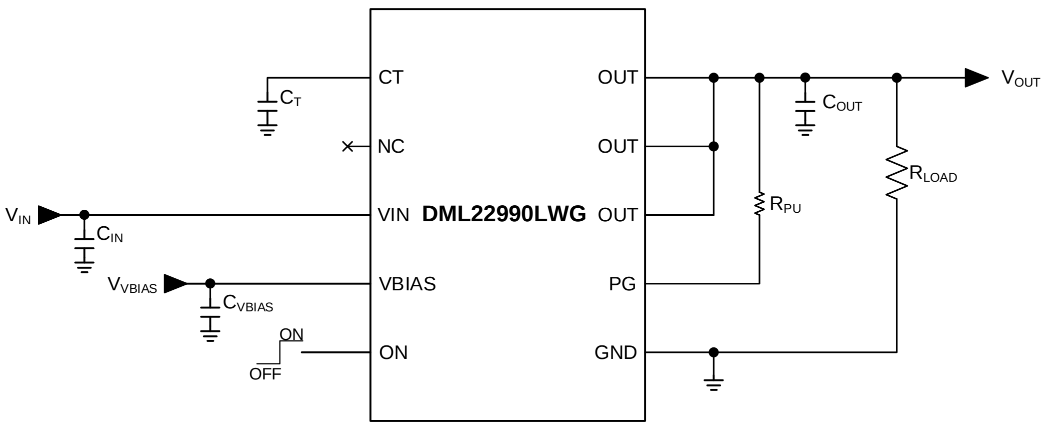
Date Code Key

Year	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	2	3	4	5	6	7	8	9	0	1	2	3

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

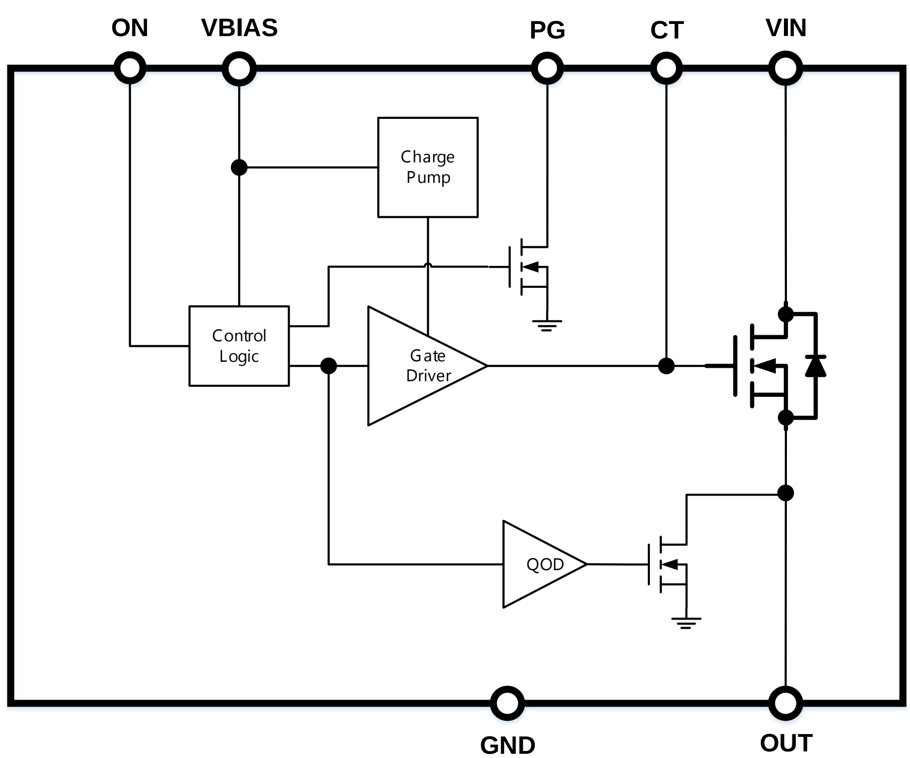
Typical Application Circuit



Pin Description

Pin Number	Pin Name	Pin Function
1	CT	VOUT slew rate control.
2	NC	Not internally connected.
3, EPAD	VIN	Load switch input. Bypass capacitor is recommended.
4	VBIAS	Bias voltage. Power-supply input for the device.
5	ON	Enable input. Load switch is on when ON is pulled high. Load switch is off when ON is pulled low. Do not leave floating.
6	GND	Ground.
7	PG	Power-good. Active High, open drain output. Tie to GND if not used.
8, 9, 10	OUT	Load switch output.

Function Block Diagram



Absolute Maximum Rating

Parameter	Rating
VIN, ON, VBIAS, PG, OUT to GND	-0.3V to 6V
CT	-0.3V to 15V
I_{MAX}	10A
Junction Temperature (T_J)	+125°C
Storage Temperature (T_S)	-65°C to +150°C

Recommended Operating Ranges

Parameter	Rating
Supply Voltage (V_{BIAS})	2.5V to 5.5V
Input Voltage (V_{IN})	0.6V to V_{BIAS}
Ambient Temperature (T_A)	-40°C to +105°C
Junction to Top Thermal Resistance ($R_{θJC\_top}$)	65°C/W
Junction to Bottom Thermal Resistance ($R_{θJC\_bot}$)	3.7°C/W
Junction to Ambient Thermal Resistance ($R_{θJA}$)	51°C/W

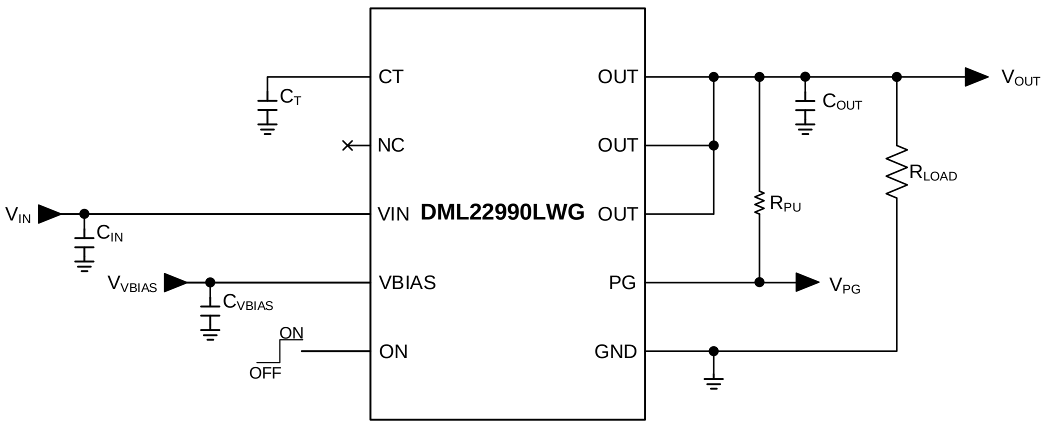
Electrical Characteristics (V_{BIAS} = 5V, V_{IN} = 1.05V, V_{ON} = 5V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	VIN Supply Voltage	V_{ON} = 5V	0.6	—	V_{BIAS}	V
V_{BIAS}	VBIAS Supply Voltage	—	2.5	3.3/5	5.5	V
I_{Q_VBIAS}	Quiescent Supply Current of VBIAS	V_{ON} = 5V, V_{OUT} = 0	—	65	85	µA
I_{STBY_VBIAS}	VBIAS Shutdown Supply Current	V_{ON} = 0, V_{OUT} = 0	—	0.1	1	µA
I_{STBY_VIN}	VIN Shutdown Supply Current	V_{IN} = V_{BIAS} = 3.3V, V_{ON} = V_{OUT} = 0	—	0.33	2	µA
		V_{IN} = V_{BIAS} = 5V, V_{ON} = V_{OUT} = 0	—	0.5	2	µA
V_{ONH}	ON High-Level Voltage	—	1.05	—	5.5	V
V_{ONL}	ON Low-Level Voltage	—	0	—	0.5	V
V_{ON_HYS}	Hysteresis Voltage of ON	—	—	60	—	mV
I_{ON}	ON Leakage Current	V_{ON} = 5V	—	—	0.1	µA
V_{PG_OL}	PG Output Low Voltage	V_{ON} = 0, I_{PG} = 1mA	—	—	0.2	V
I_{PG}	PG Output Leakage Current	V_{ON} = 5V, V_{PG} = 5V	—	—	0.5	µA
Switching ON Resistance						
R_{ON}	Switch ON-State Resistance V_{BIAS} = 5V	V_{IN} = 5V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 3.3V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 2.5V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 1.8V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 1.05V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 0.6V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
	Switch ON-State Resistance V_{BIAS} = 3.3V	V_{IN} = 3.3V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 2.5V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 1.8V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} =1.05V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
		V_{IN} = 0.6V, V_{ON} = 5V, I_{OUT} = -200mA	—	3.9	5	mΩ
R_{PD}	Output Pulldown Resistance	V_{IN} = V_{OUT} = 5V, V_{ON} = 0	—	200	280	Ω

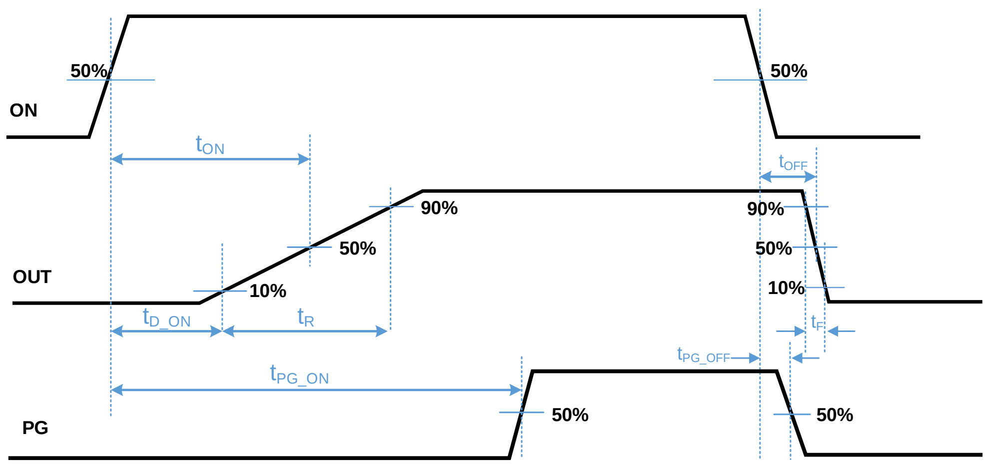
Switching Electrical Characteristics (C_{IN} = 1µF, C_{OUT} = 0.1µF, C_T = 0, R_{PU} = 10kΩ, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN} = 5V, V_{VBIAS} = V_{ON} = 5V					
t_{ON}	Output Turn-ON Time	—	28	—	µs
t_{OFF}	Output Turn-OFF Time	—	6	—	
t_R	Output Turn-ON Rise Time	—	38	—	
t_F	Output Turn-OFF Fall Time	—	1.5	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	13	—	
t_{PG_ON}	PG Turn-ON Time	—	188	—	
t_{PG_OFF}	PG Turn-OFF Time	—	2.8	—	
V_{IN} = 1.05V, V_{VBIAS} = V_{ON} = 5V					
t_{ON}	Output Turn-ON Time	—	23	—	µs
t_{OFF}	Output Turn-OFF Time	—	6.6	—	
t_R	Output Turn-ON Rise Time	—	15	—	
t_F	Output Turn-OFF Fall Time	—	1.3	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	15	—	
t_{PG_ON}	PG Turn-ON Time	—	166	—	
t_{PG_OFF}	PG Turn-OFF Time	—	2.8	—	
V_{IN} = 0.6V, V_{VBIAS} = V_{ON} = 5V					
t_{ON}	Output Turn-ON Time	—	20	—	µs
t_{OFF}	Output Turn-OFF Time	—	6.8	—	
t_R	Output Turn-ON Rise Time	—	10	—	
t_F	Output Turn-OFF Fall Time	—	1.3	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	15	—	
t_{PG_ON}	PG Turn-ON Time	—	162	—	
t_{PG_OFF}	PG Turn-OFF Time	—	2.8	—	
V_{IN} = 3.3V, V_{VBIAS} = V_{ON} = 3.3V					
t_{ON}	Output Turn-ON Time	—	42	—	µs
t_{OFF}	Output Turn-OFF Time	—	9.5	—	
t_R	Output Turn-ON Rise Time	—	33	—	
t_F	Output Turn-OFF Fall Time	—	1.5	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	27	—	
t_{PG_ON}	PG Turn-ON Time	—	170	—	
t_{PG_OFF}	PG Turn-OFF Time	—	4.5	—	
V_{IN} = 1.05V, V_{VBIAS} = V_{ON} = 3.3V					
t_{ON}	Output Turn-ON Time	—	41	—	µs
t_{OFF}	Output Turn-OFF Time	—	9.8	—	
t_R	Output Turn-ON Rise Time	—	16.5	—	
t_F	Output Turn-OFF Fall Time	—	1.3	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	32	—	
t_{PG_ON}	PG Turn-ON Time	—	158	—	
t_{PG_OFF}	PG Turn-OFF Time	—	4.5	—	
V_{IN} = 0.6V, V_{VBIAS} = V_{ON} = 3.3V					
t_{ON}	Output Turn-ON Time	—	39	—	µs
t_{OFF}	Output Turn-OFF Time	—	10	—	
t_R	Output Turn-ON Rise Time	—	13	—	
t_F	Output Turn-OFF Fall Time	—	1.2	—	
$t_{D\text{-}ON}$	Output Turn-ON Delay time	—	32	—	
t_{PG_ON}	PG Turn-ON Time	—	154	—	
t_{PG_OFF}	PG Turn-OFF Time	—	4.5	—	

Switching Electrical Characteristics (C_{IN} = 1µF, C_{OUT} = 0.1µF, C_T = 0, R_{PU} = 10kΩ, T_A = +25°C, unless otherwise specified.) (continued)



Timing Test Circuit

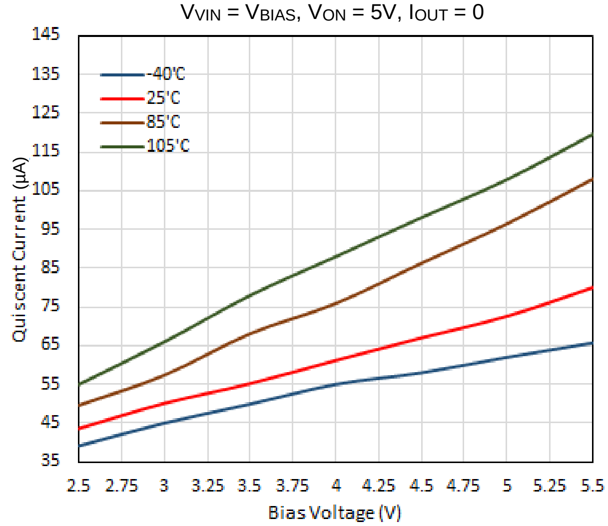


Timing Waveforms

Performance Characteristics (@T_A = +25°C, unless otherwise specified.)

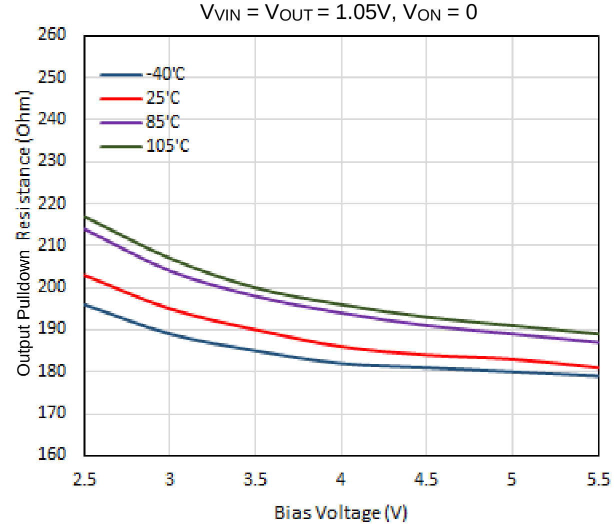
Quiescent Current vs. Bias Voltage

$V_{VIN} = V_{BIAS}$, V_{ON} = 5V, I_{OUT} = 0



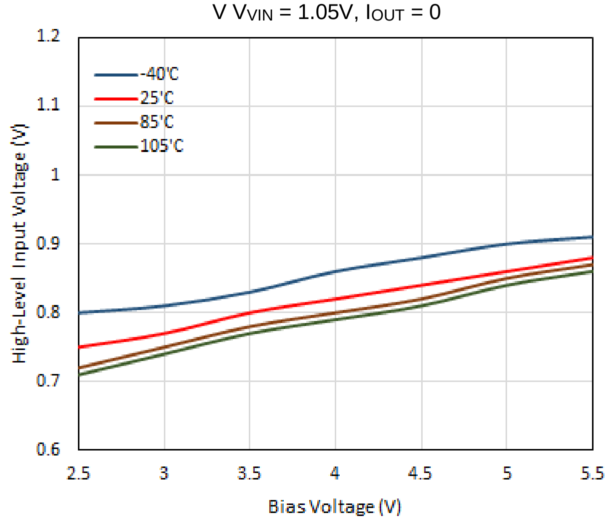
Output Pulldown Resistance vs. Bias Voltage

$V_{VIN} = V_{OUT}$ = 1.05V, V_{ON} = 0



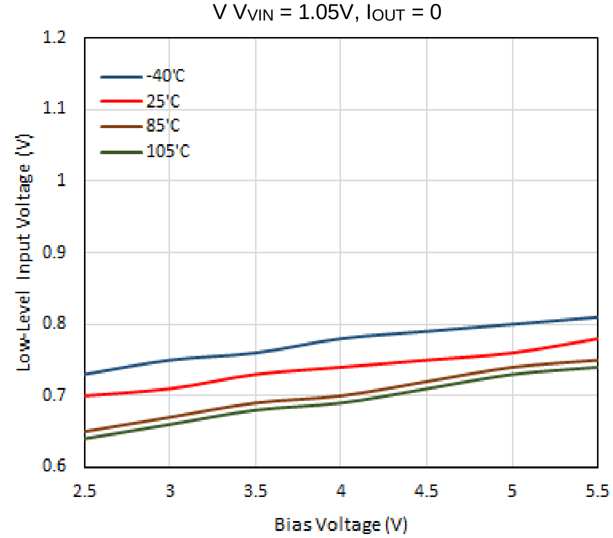
High-Level Input Voltage vs. Bias Voltage

V V_{VIN} = 1.05V, I_{OUT} = 0



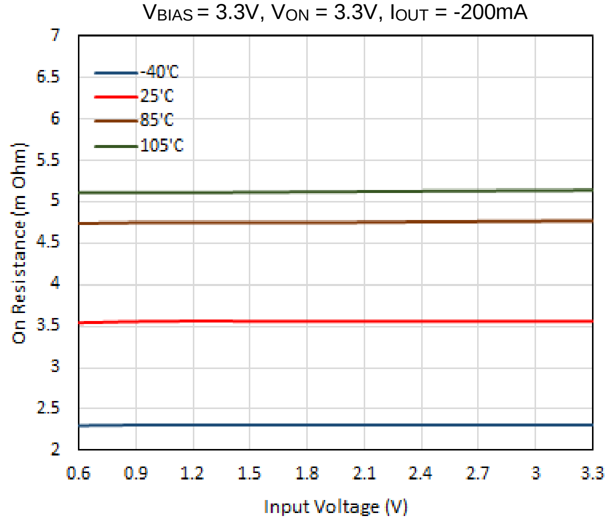
Low-Level Input Voltage vs. Bias Voltage

V V_{VIN} = 1.05V, I_{OUT} = 0



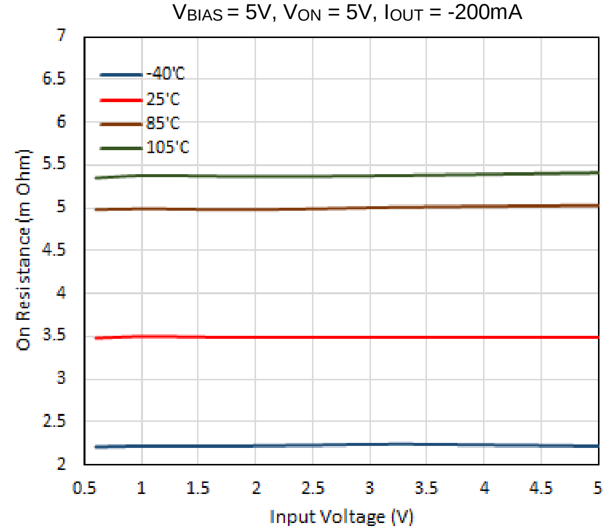
On-Resistance vs. Input Voltage

V_{BIAS} = 3.3V, V_{ON} = 3.3V, I_{OUT} = -200mA



On-Resistance vs. Input Voltage

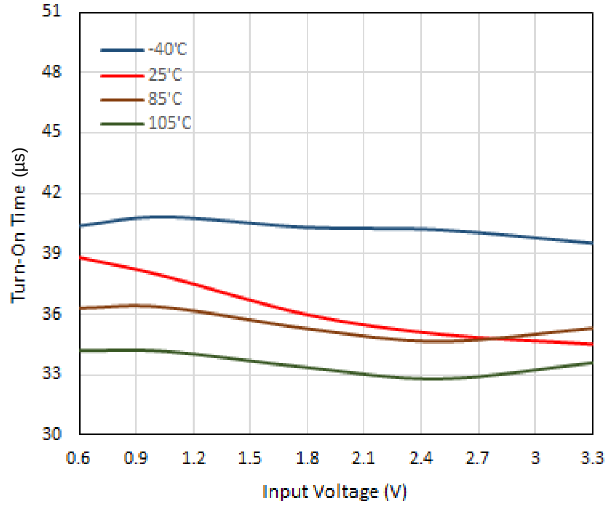
V_{BIAS} = 5V, V_{ON} = 5V, I_{OUT} = -200mA



Performance Characteristics (@T_A = +25°C, unless otherwise specified.) (continued)

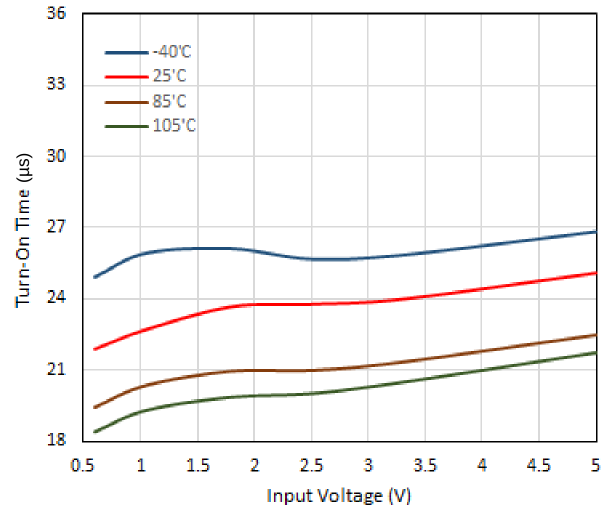
Turn-ON Time vs. Input Voltage

V_{BIAS} = 3.3V, V_{ON} = 3.3V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



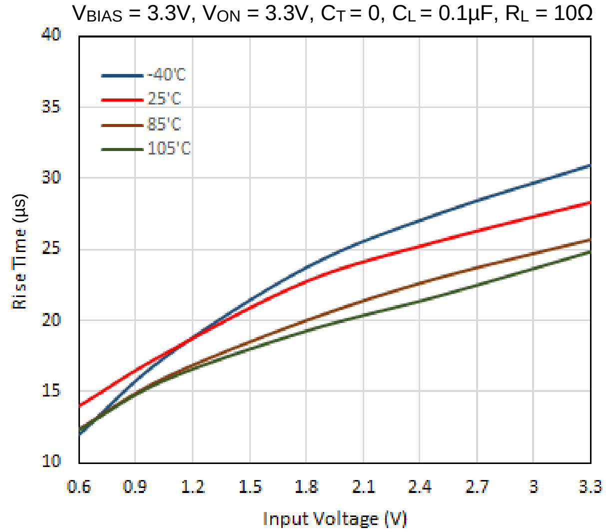
Turn-ON Time vs. Input Voltage

V_{BIAS} = 5V, V_{ON} = 5V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



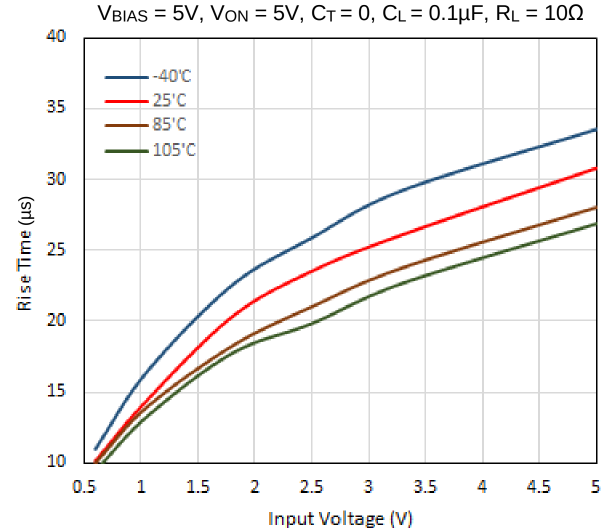
Rise Time vs. Input Voltage

V_{BIAS} = 3.3V, V_{ON} = 3.3V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



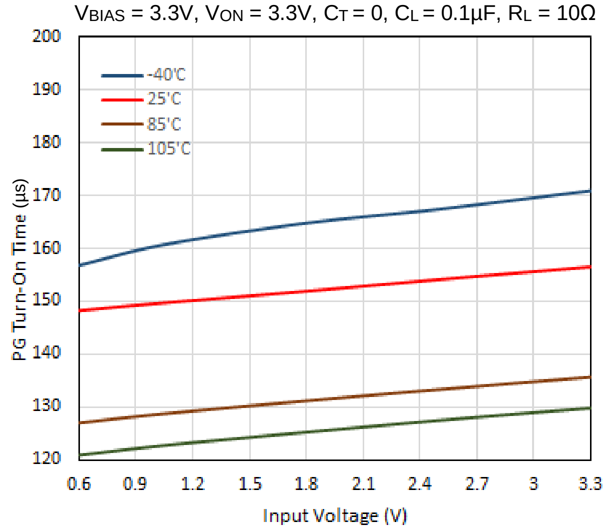
Rise Time vs. Input Voltage

V_{BIAS} = 5V, V_{ON} = 5V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



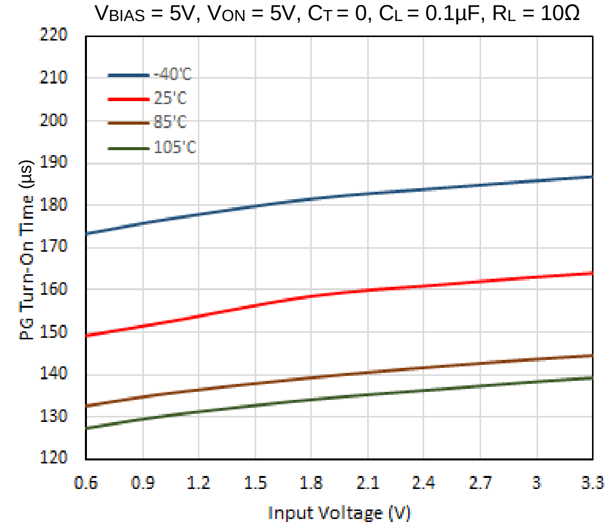
PG ON Time vs. Input Voltage

V_{BIAS} = 3.3V, V_{ON} = 3.3V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



PG ON Time vs. Input Voltage

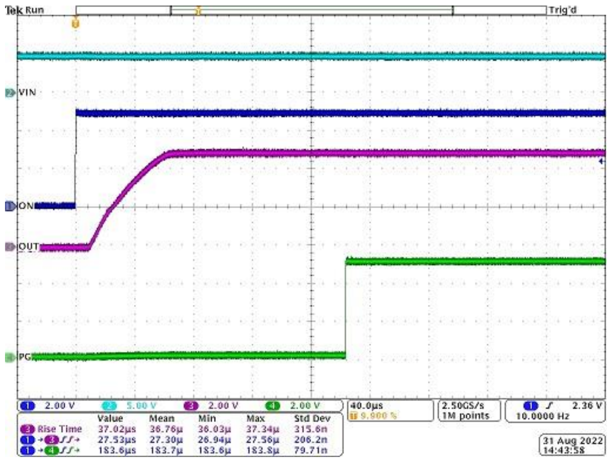
V_{BIAS} = 5V, V_{ON} = 5V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



Performance Characteristics (@T_A = +25°C, unless otherwise specified.) (continued)

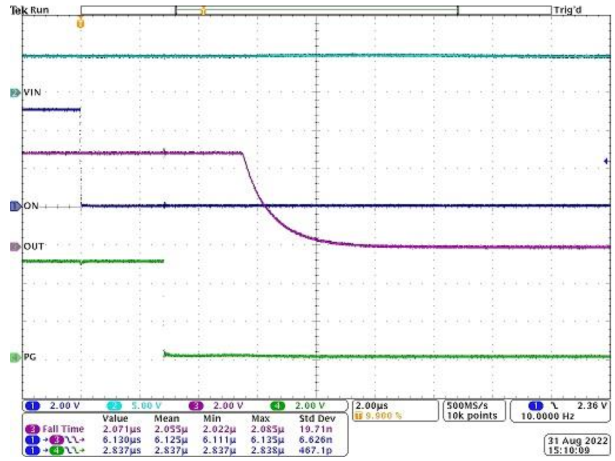
Turn-ON Response

V_{BIAS} = 5V, V_{VIN} = 5V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



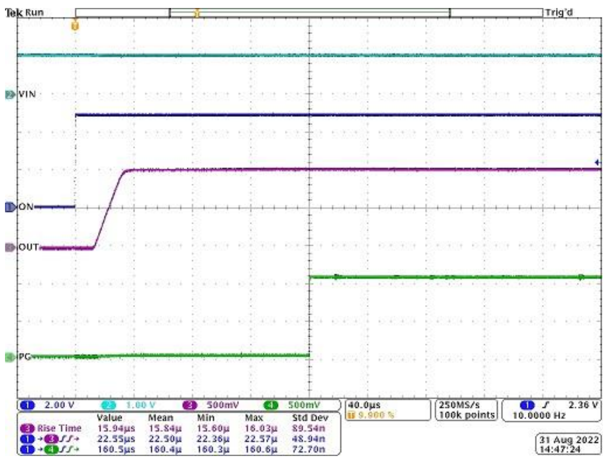
Turn-OFF Response

V_{BIAS} = 5V, V_{VIN} = 5V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



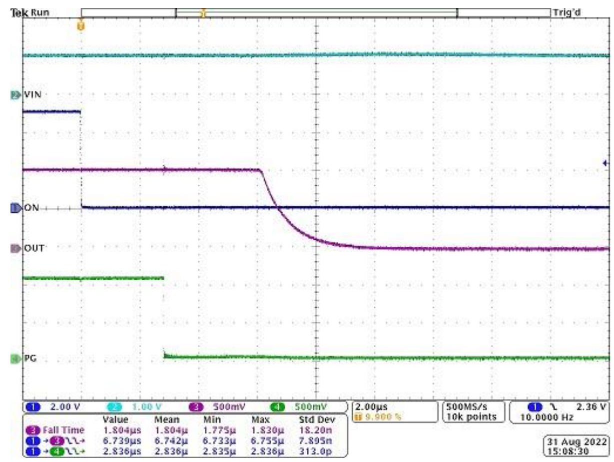
Turn-ON Response

V_{BIAS} = 5V, V_{VIN} = 1.05V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



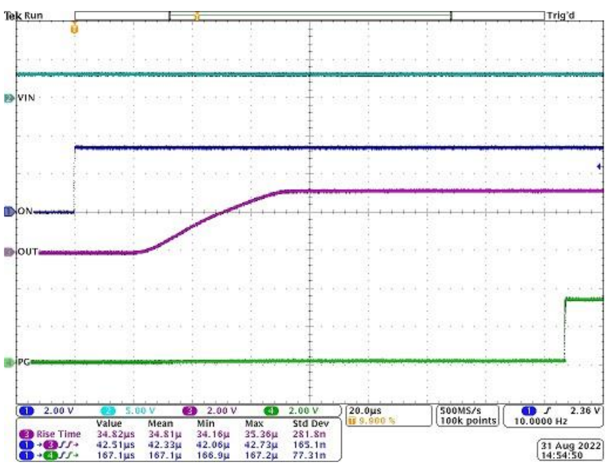
Turn-OFF Response

V_{BIAS} = 5V, V_{VIN} = 1.05V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



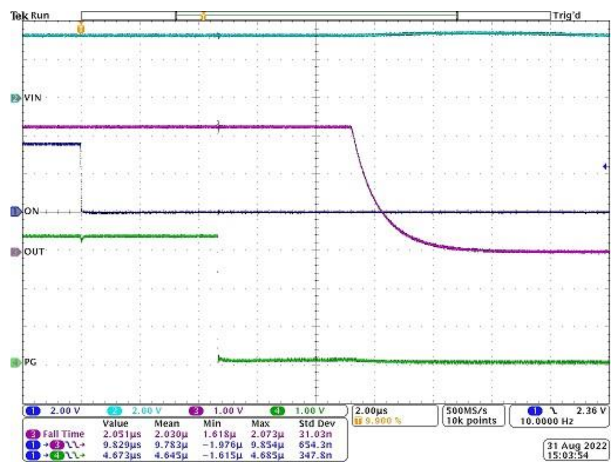
Turn-ON Response

V_{BIAS} = 3.3V, V_{VIN} = 3.3V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



Turn-OFF Response

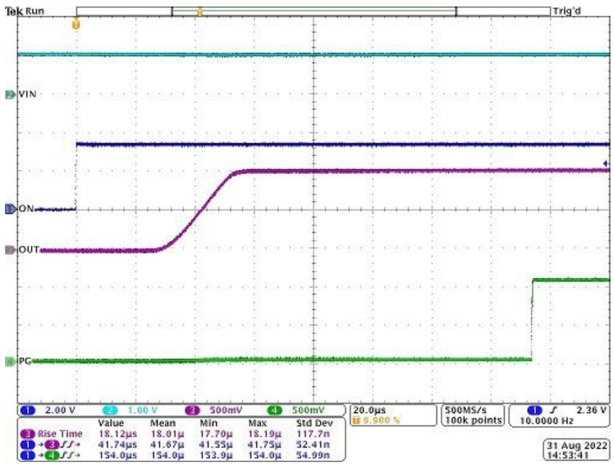
V_{BIAS} = 3.3V, V_{VIN} = 3.3V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



Performance Characteristics (@T_A = +25°C, unless otherwise specified.) (continued)

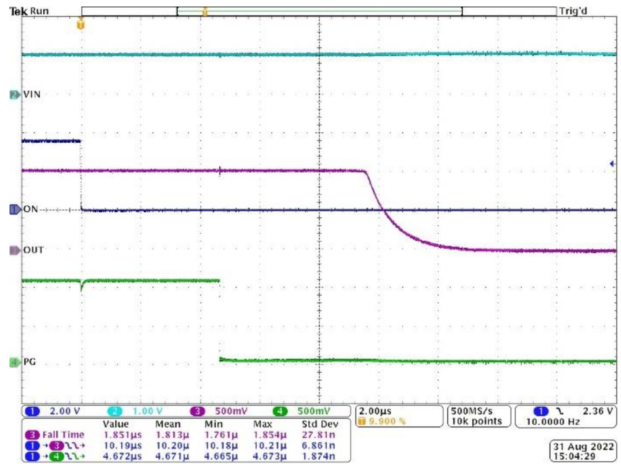
Turn-ON Response

V_{BIAS} = 3.3V, V_{VIN} = 1.05V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



Turn-OFF Response

V_{BIAS} = 3.3V, V_{VIN} = 1.05V, C_T = 0, C_L = 0.1µF, R_L = 10Ω



Application Information

General Description

The DML22990LWG is a single-channel load switch with a controlled adjustable turn-on and integrated PG indicator in a 10-pin V-DFN3020-10 (Type C) package. The device contains an N-channel MOSFET that can operate over an input-voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input-voltage range and high-current capability enable the device to be used across multiple designs and end equipment. 3.9mΩ on-resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current by large bulk load capacitances thereby reducing or eliminating power-supply drop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing. During shutdown, the device has very low leakage current thereby reducing unnecessary leakages for downstream modules during standby. The DML22990LWG also has an embedded 200Ω on-chip resistor for quick discharge of the output when switch is disabled.

Enable Control

The DML22990LWG device allows for enabling the MOSFET in an active-high configuration. When the VBIAS supply pin has an adequate voltage applied, and the EN pin is at logic-high level, the MOSFET is enabled. Similarly, when the EN pin is at logic-low level, the MOSFET is disabled. An internal pulldown resistor to ground on the EN pin ensures that the MOSFET disables when not being driven.

Power Sequencing

The DML22990LWG device functions with any power sequence, but the output turn-on delay performance can vary from what is specified. To archive the specified performance, there are two recommended power sequences:

1.) $V_{BIAS} \rightarrow V_{IN} \rightarrow V_{ON}$
2.) $V_{IN} \rightarrow V_{BIAS} \rightarrow V_{ON}$

Adjustable Rise Time (Slew Rate Control)

The DML22990LWG device has controlled rise time for inrush current control. The voltage on the CT pin can be as high as 15V. A capacitor to ground on the CT pin adjusts the rise time. Without a capacitor on CT, the rise time is at its minimum for fastest timing. Equation 1 approximately shows the relationship between C_T, V_{IN}, and rise time, t_R, when V_{BIAS} is set to 5V.

$$t_R = (K1 \cdot V_{IN} + K2) \cdot CT + K3 \cdot V_{IN} + K4 \quad \text{(Equation 1)}$$

Where: K1 = 5.8, K2 = 0.7, K3 = 6, and K4 = 6.5

t_R is the rise time in µs, and is the capacitance value on CT pin (in nF).

Table 1 contains rise time values measured on a typical device.

Table 1. Rise Times vs. CT Capacitor

C_T	Rise Time (µs) V_{BIAS} = 5V, C_L = 0.1µF, R_L = 10Ω, +25°C; Measure V_{OUT} Rising Time from 10% to 90% V_{IN}				
	V_{IN} = 5V	V_{IN} = 3.3V	V_{IN} = 2.5V	V_{IN} = 1.05V	V_{IN} = 0.6V
0 (floating)	37.5	31.9	26.5	14.5	10.1
0.22nF	43.5	33.7	28.9	16.1	11.2
0.47nF	50.2	39.3	32.5	17.6	11.9
1nF	66.4	50.3	40.3	21.5	14.3
2.2nF	100.3	73.5	58.7	29.5	19.3
4.7nF	175.8	124.5	95.6	45.9	30.8
10nF	325.3	226.9	175.4	81.7	54.1

Application Information (continued)

Power-Good

The DML22990LWG device has a power-good (PG) output that can be used to indicate when the gate of the MOSFET is driven high and the switch is on with the on-resistance close to its final value (full load ready). The PG pin is an active-high, open-drain output that requires an external pullup resistor, R_{PG}, greater than or equal to 1kΩ to an external voltage source, V_{TERM}, compatible with input levels of those devices connected to this pin. Equation 2 approximately shows the relationship between C_T, V_{IN}, and PG turn-on time, t_{PG_ON}.

$$t_R = (K1 \cdot V_{IN} + K2) \cdot CT + K3 \cdot V_{IN} + K4 \quad \text{(Equation 2)}$$

Where: K1 = 6.9, K2 = 4.7, K3 = 5.2, and K4 = 160

Table 2 contains PG turn-on time values measured on a typical device.

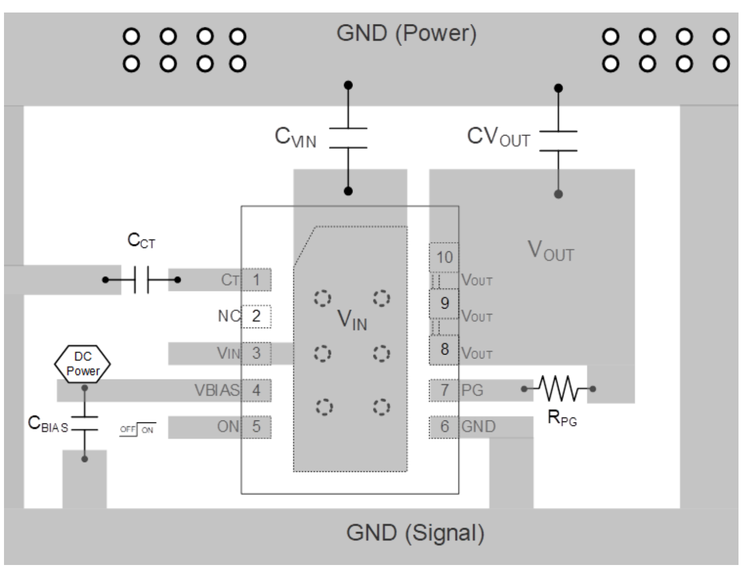
Table 2. PG Turn-On Times vs. CT Capacitor

C_T	PG Turn-On Time (μs) V_{BIAS} = 5V, C_L = 0.1μF, R_L = 10Ω, +25°C				
	V_{IN} = 5V	V_{IN} = 3.3V	V_{IN} = 2.5V	V_{IN} = 1.05V	V_{IN} = 0.6V
0 (floating)	187.6	181.9	176.8	166.1	161.6
0.22nF	195.7	187.9	181.4	168.8	163.6
0.47nF	204.4	192.3	185.9	170.5	164.3
1nF	223.8	206.2	197.4	177.5	170.1
2.2nF	269.5	239.6	223.9	192.1	180.6
4.7nF	367.5	308.8	279.2	222.4	203.4
10nF	568.6	450.6	393.6	286.3	249.1

The power-good output can be used as the enable signal for other active-high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals required from the system controller. If the power-good feature is not used in the application, the PG pin must be tied to GND.

PCB Layout Consideration

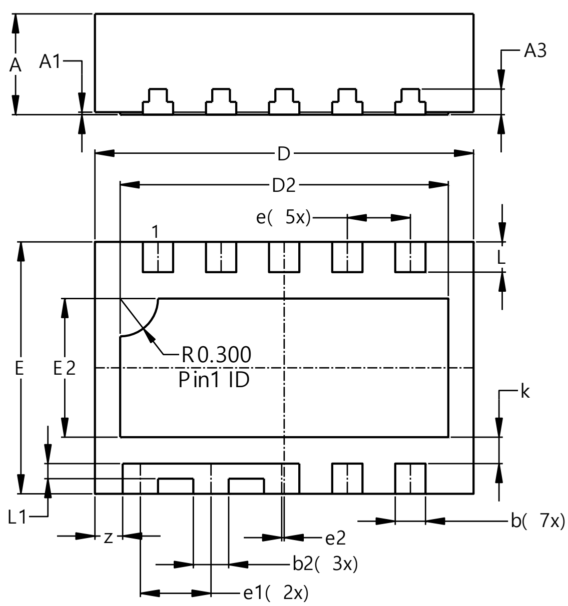
1. Place the input/output capacitors C_{VIN} and C_{VOUT} as close as possible to the V_{IN} and V_{OUT} pins.
2. The power traces, which are V_{IN} trace, V_{OUT} trace, and GND trace, should be short, wide, and direct for minimize parasitic inductance.
3. The CT trace must be as short as possible to reduce parasitic capacitance.
4. Place C_{BIAS} capacitor near the device pin.
5. Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input or output capacitors.
6. For better power dissipation, via holes are recommended to connect the exposed pad's landing area to a large copper polygon on the other side of the PCB. The copper polygons and exposed pad shall connect to V_{IN} pin on the printed circuit board.



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3020-10 (Type C)

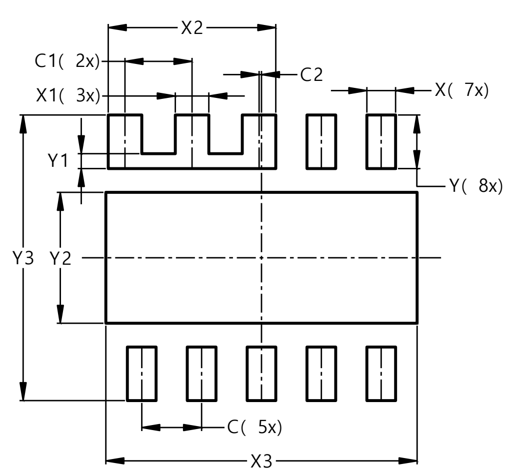


V-DFN3020-10 (Type C)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	--	--	0.203
b	0.19	0.29	0.24
b2	0.23	0.33	0.28
D	2.95	3.05	3.00
D2	2.50	2.70	2.60
E	1.95	2.05	2.00
E2	1.00	1.20	1.10
e	0.50 BSC		
e1	0.56 BSC		
e2	0.02 BSC		
k	--	--	0.21
L	0.19	0.29	0.24
L1	--	--	0.12
z	--	--	0.22
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3020-10 (Type C)



Dimensions	Value (in mm)
C	0.500
C1	0.560
C2	0.020
X	0.240
X1	0.280
X2	1.400
X3	2.600
Y	0.450
Y1	0.125
Y2	1.100
Y3	2.400

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