











CSD25480F3

SLPS578A - APRIL 2016 - REVISED AUGUST 2017

CSD25480F3 -20-V P-Channel FemtoFET™ MOSFET

Features

- Low On-Resistance
- Ultra-Low Q_q and Q_{qd}
- **Ultra-Small Footprint**
 - 0.73 mm × 0.64 mm
- Low Profile
 - 0.35-mm Max Height
- Integrated ESD Protection Diode
- Lead and Halogen Free
- **RoHS Compliant**

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching **Applications**
- **Battery Applications**
- Handheld and Mobile Applications

3 Description

This -20-V, $110\text{-m}\Omega$, P-Channel FemtoFETTM MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.

Product Summary

T _A = 25°	С	TYPICAL VA	UNIT		
V_{DS}	Drain-to-Source Voltage –20				
Q_g	Gate Charge Total (-4.5 V)	ıl (–4.5 V) 0.7		nC	
Q_{gd}	Gate Charge Gate-to-Drain	0.10	0.10		
		$V_{GS} = -1.8 \text{ V}$	420		
D	Drain-to-Source	$V_{GS} = -2.5 \text{ V}$	203	O	
R _{DS(on)}	On-Resistance	$V_{GS} = -4.5 \text{ V}$	132	mΩ	
		V _{GS} = -8.0 V	110		
$V_{GS(th)}$	Threshold Voltage	-0.95		V	

Device Information⁽¹⁾

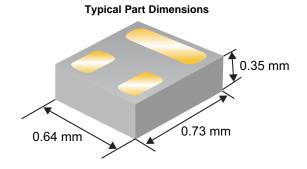
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25480F3	3000		Femto	Tape
CSD25480F3T	250	7-Inch Reel	0.73-mm × 0.64-mm Land Grid Array (LGA)	and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25$	°C (unless otherwise stated)	VALUE	UNIT					
V_{DS}	Drain-to-Source Voltage	-20	V					
V_{GS}	Gate-to-Source Voltage	-12	V					
I_D	Continuous Drain Current ⁽¹⁾	-1.7	Α					
I _{DM}	Pulsed Drain Current ⁽¹⁾⁽²⁾	-10.6	Α					
P _D	Power Dissipation ⁽¹⁾	500	mW					
	Human-Body Model (HBM)	4000						
$V_{(ESD)}$	Charged-Device Model (CDM)	2000	V					
T _J , T _{stg}	Operating Junction, Storage Temperature	-55 to 150	°C					

- (1) Typical $R_{\theta JA} = 255^{\circ}C/W$ mounted on FR4 material with minimum Cu mounting area.
- (2) Pulse duration ≤100 μs, duty cycle ≤1%.





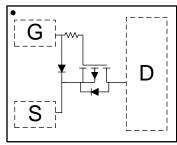




Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Specifications 3 5.1 Electrical Characteristics 3 5.2 Thermal Information 3 5.3 Typical MOSFET Characteristics 4 6 Device and Documentation Support 7	6.1 Receiving Notification of Documentation Updates 6.2 Community Resources
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4 Revision History

Cł	hanges from Original (April 2016) to Revision A	Page
•	Added the Receiving Notification of Documentation Updates section in Device and Documentation Support	7
•	Updated the Recommended Stencil Pattern	9

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5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^{\circ}C$ (unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC	CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_{DS} = -250 \mu\text{A}$	-20			V	
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = -16 V			-50	nA	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = -12 V			-25	nA	
V _{GS(th)}	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = -250 \mu A$	-0.70	-0.95	-1.20	V	
		$V_{GS} = -1.8 \text{ V}, I_{DS} = -0.1 \text{ A}$		420	840		
Ъ	B	$V_{GS} = -2.5 \text{ V}, I_{DS} = -0.4 \text{ A}$		203	260	0	
R _{DS(on)}	Drain-to-source on-resistance	$V_{GS} = -4.5 \text{ V}, I_{DS} = -0.4 \text{ A}$		132	159	mΩ	
		$V_{GS} = -8 \text{ V}, I_{DS} = -0.4 \text{ A}$		110	132		
9 _{fs}	Transconductance	$V_{DS} = -10 \text{ V}, I_{DS} = -0.4 \text{ A}$		8.0		S	
DYNAMI	C CHARACTERISTICS						
C _{iss}	Input capacitance		1		155	pF	
C _{oss}	Output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = -10 \text{ V},$ f = 1 MHz		48	62	pF	
C _{rss}	Reverse transfer capacitance	J = 1 WH12	3.6		4.7	pF	
R _G	Series gate resistance			16		Ω	
Q _g	Gate charge total (-4.5 V)			0.70	0.91	nC	
Q _{gd}	Gate charge gate-to-drain	V 40.V I 0.4.A		0.10		nC	
Q _{gs}	Gate charge gate-to-source	$V_{DS} = -10 \text{ V}, I_{DS} = -0.4 \text{ A}$		0.26		nC	
Q _{g(th)}	Gate charge at V _{th}			0.15		nC	
Q _{oss}	Output charge	V _{DS} = -10 V, V _{GS} = 0 V		1.3		nC	
t _{d(on)}	Turnon delay time			9		ns	
t _r	Rise time	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$		5		ns	
t _{d(off)}	Turnoff delay time	$I_{DS} = -0.4 \text{ A}, R_G = 10 \Omega$		13		ns	
t _f	Fall time			7		ns	
DIODE C	CHARACTERISTICS						
V _{SD}	Diode forward voltage	$I_{SD} = -0.4 \text{ A}, V_{GS} = 0 \text{ V}$		-0.78	-1.0	V	
Q _{rr}	Reverse recovery charge	V 40 V I 0 4 A di/d+ 400 A / -		1.2		nC	
t _{rr}	Reverse recovery time	$V_{DS} = -10 \text{ V}, I_F = -0.4 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		6.4		ns	

5.2 Thermal Information

 $T_{A} = 25^{\circ}C$ (unless otherwise stated)

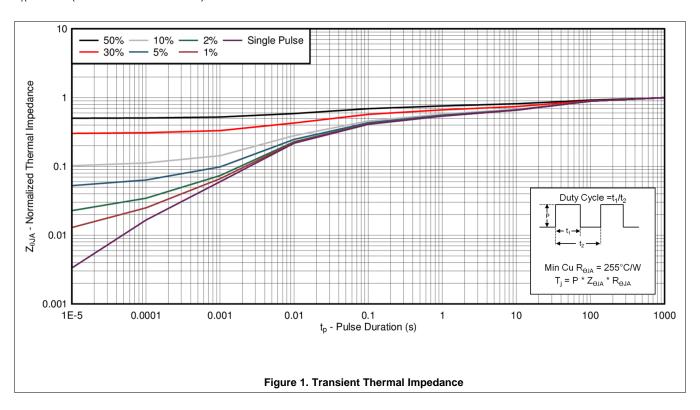
,,	THERMAL METRIC	TYPICAL VALUES	UNIT
Б	Junction-to-ambient thermal resistance ⁽¹⁾	90	9 0 AA7
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	255	°C/W

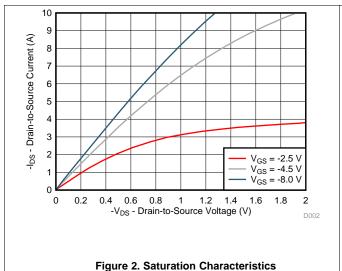
 ⁽¹⁾ Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz. (0.071-mm) thick Cu.
 (2) Device mounted on FR4 material with minimum Cu mounting area.

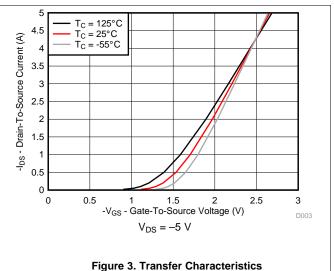


5.3 Typical MOSFET Characteristics

 $T_A = 25$ °C (unless otherwise stated)







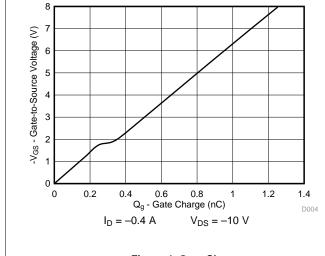
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Typical MOSFET Characteristics (continued)

 $T_A = 25$ °C (unless otherwise stated)



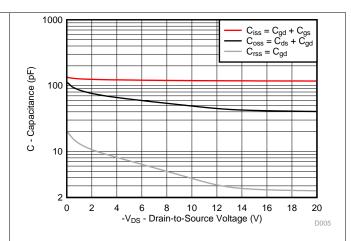


Figure 4. Gate Charge

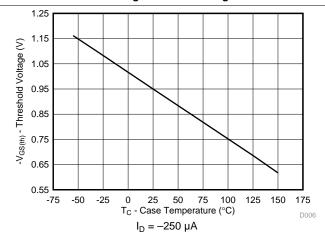


Figure 5. Capacitance

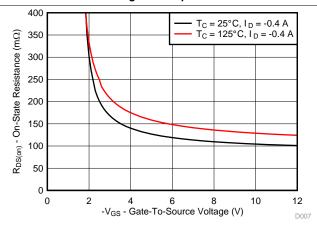


Figure 6. Threshold Voltage vs Temperature

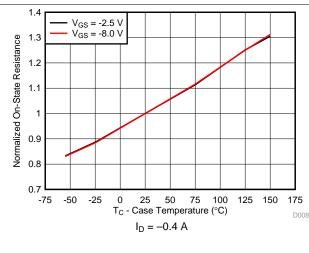


Figure 8. Normalized On-State Resistance vs Temperature

Figure 7. On-State Resistance vs Gate-to-Source Voltage

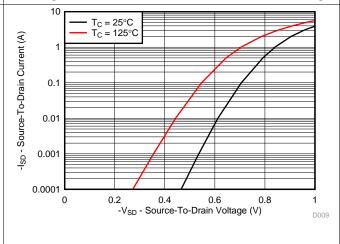
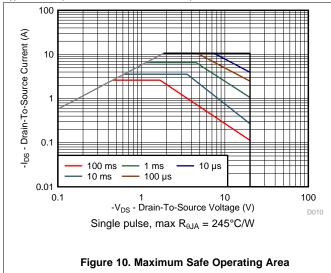


Figure 9. Typical Diode Forward Voltage



Typical MOSFET Characteristics (continued)

 $T_A = 25$ °C (unless otherwise stated)



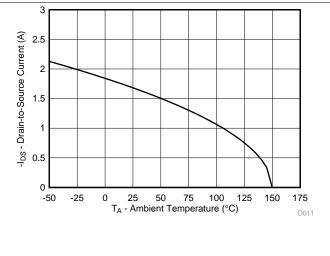


Figure 11. Maximum Drain Current vs Temperature



6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

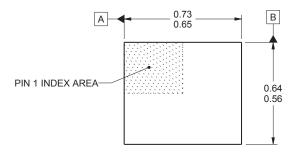
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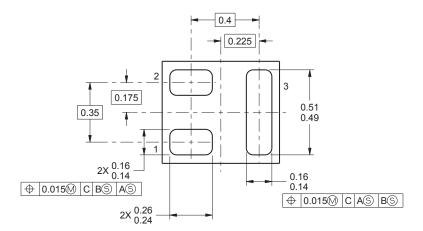
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions







- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a lead-free solder land design.

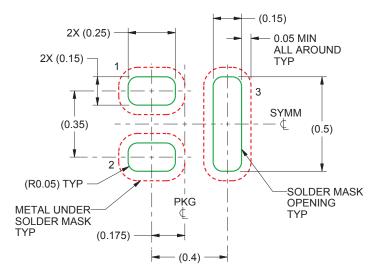
Table 1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

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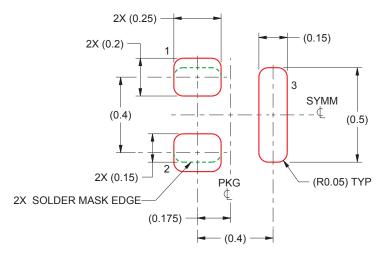


7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

ali difficisions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25480F3	PICOST AR	YJM	3	3000	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD25480F3	PICOST AR	YJM	3	3000	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOST AR	YJM	3	250	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOST AR	YJM	3	250	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2

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*All dimensions are nominal

7 till difficilities die Herminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25480F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD25480F3	PICOSTAR	YJM	3	3000	220.0	220.0	35.0
CSD25480F3T	PICOSTAR	YJM	3	250	220.0	220.0	35.0
CSD25480F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

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