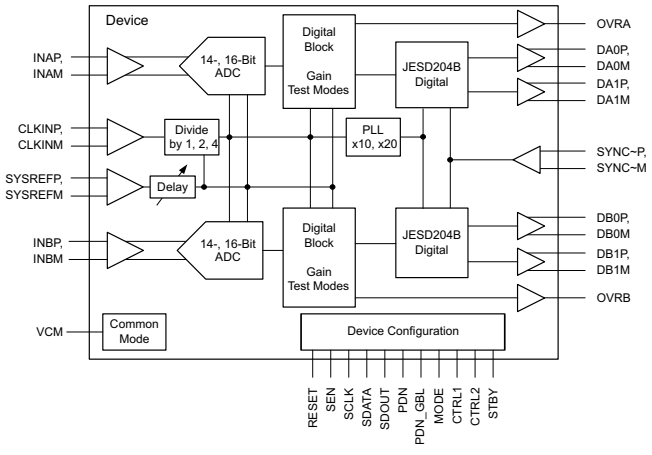
ADS42JB46 Dual-Channel, 14-Bit, 160-MSPS Analog-to-Digital Converter

1 Features

- Dual-Channel ADCs
- 14-Bit Resolution
- Maximum Clock Rate: 160 MSPS
- JESD204B Serial Interface
  - Subclass 0, 1, 2 Compliant
  - Up to 3.125 Gbps
  - Two- and Four-Lane Support
- Analog Input Buffer with High-Impedance Input
- Flexible Input Clock Buffer: Divide-by-1, -2, and -4
- Differential Full-Scale Input: 2 V_{PP} and 2.5 V_{PP} (Register Programmable)
- Package: 9-mm × 9-mm QFN-64
- Power Dissipation: 679 mW/Ch
- Aperture Jitter: 85 f_S rms
- Internal Dither
- Channel Isolation: 100 dB
- Performance:
  - f_{IN} = 170 MHz at 2 V_{PP}, –1 dBFS
    - SNR: 72.9 dBFS
    - SFDR: 90 dBc for HD2, HD3
    - SFDR: 100 dBc for Non HD2, HD3
  - f_{IN} = 170 MHz at 2.5 V_{PP}, –1 dBFS
    - SNR: 74.2 dBFS
    - SFDR: 84 dBc for HD2, HD3 and 95 dBc for Non HD2, HD3

Simplified Schematic



2 Applications

- Communication and Cable Infrastructure
- Multi-Carrier, Multimode Cellular Receivers
- Radar and Smart Antenna Arrays
- Broadband Wireless
- Test and Measurement Systems
- Software-Defined and Diversity Radios
- Microwave and Dual-Channel I/Q Receivers
- Repeaters
- Power Amplifier Linearization

3 Description

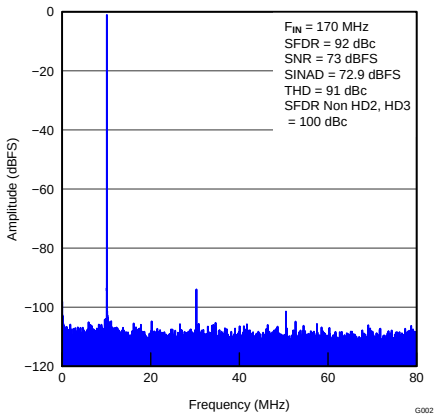
The ADS42JB46 is a high-linearity, dual-channel, 14-bit, 160-MSPS, analog-to-digital converter (ADC). This device supports the JESD204B serial interface with data rates up to 3.125 Gbps. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy, thus making driving analog inputs up to very high input frequencies easy. A sampling clock divider allows more flexibility for system clock architecture design. The device employs internal dither algorithms to provide excellent spurious-free dynamic range (SFDR) over a large input frequency range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS42JB46	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

FFT for 170-MHz Input Signal Sampled at 160 MSPS



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2013) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (July 2013) to Revision A — **Page**

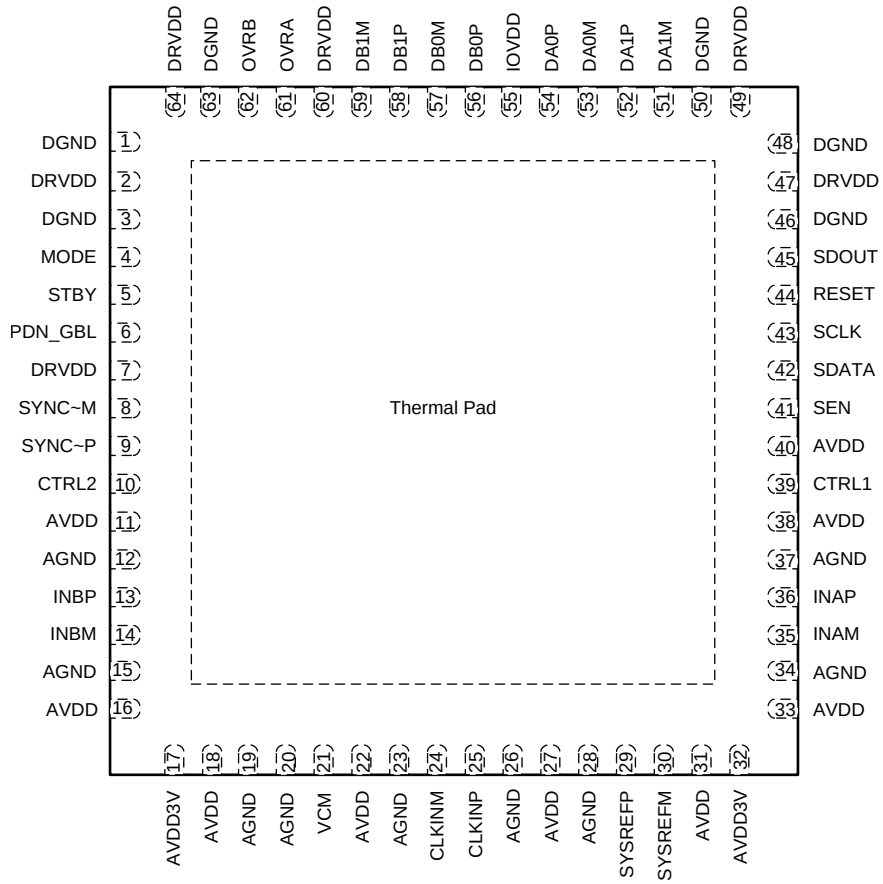
- Changed document status to Production Data; moved from 1-page Preview ... 1

5 Device Comparison Table

INTERFACE OPTION	14-BIT, 160 MSPS	14-BIT, 250 MSPS	16-BIT, 250 MSPS
DDR, QDR LVDS	—	ADS42LB49	ADS42LB69
JESD204B	ADS42JB46	ADS42JB46	ADS42JB69

6 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions: JESD204B Output Interface

PIN		I/O	FUNCTION	DESCRIPTION
NAME	NO.			
AGND	12, 15, 19, 20, 23, 26, 28, 34, 37	I	Supply	Analog ground
AVDD	11, 16, 18, 22, 27, 31, 33, 38, 40	I	Supply	1.8-V analog power supply
AVDD3V	17, 32	I	Supply	3.3-V analog supply for analog buffer
CLKINM	24	I	Clock	Differential ADC clock input (negative)
CLKINP	25	I	Clock	Differential ADC clock input (positive)
CTRL1	39	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
CTRL2	10	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
DA0M	53	O	Interface	JESD204B serial data output for channel A, lane 0 (negative)
DA0P	54	O	Interface	JESD204B serial data output for channel A, lane 0 (positive)
DA1M	51	O	Interface	JESD204B serial data output for channel A, lane 1 (negative)
DA1P	52	O	Interface	JESD204B serial data output for channel A, lane 1 (positive)
DB0M	57	O	Interface	JESD204B serial data output for channel B, lane 0 (negative)
DB0P	56	O	Interface	JESD204B serial data output for channel B, lane 0 (positive)
DB1M	59	O	Interface	JESD204B serial data output for channel B, lane 1 (negative)
DB1P	58	O	Interface	JESD204B serial data output for channel B, lane 1 (positive)
DGND	1, 3, 46, 48, 50, 63	I	Supply	Digital ground
DRVDD	2, 7, 47, 49, 60, 64	I	Supply	Digital 1.8-V power supply
INAM	35	I	Input	Differential analog input for channel A (negative)
INAP	36	I	Input	Differential analog input for channel A (positive)
INBM	14	I	Input	Differential analog input for channel B (negative)
INBP	13	I	Input	Differential analog input for channel B (positive)
IOVDD	55	I	Supply	Digital 1.8-V power supply for the JESD204B transmitter
MODE	4	I	Control	Connect to GND
OVRA	61	O	Interface	Overrange indication for channel A in CMOS output format
OVRB	62	O	Interface	Overrange indication for channel B in CMOS output format
PDN_GBL	6	I	Control	Global power-down. Active high with an internal 150-kΩ pull-down resistor.
RESET	44	I	Control	Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.
SCLK	43	I	Control	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	42	I	Control	Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	45	O	Control	Serial interface data output
SEN	41	I	Control	Serial interface enable. This pin has an internal 150-kΩ pull-up resistor.
STBY	5	I	Control	Standby. Active high with an internal 150-kΩ pull-down resistor.
SYNC~M	8	I	Interface	Synchronization input for JESD204B port (negative)
SYNC~P	9	I	Interface	Synchronization input for JESD204B port (positive)
SYSREFM	30	I	Clock	External SYSREF input, subclass 1 (negative)
SYSREFP	29	I	Clock	External SYSREF input, subclass 1 (positive)
VCM	21	O	Output	1.9-V common-mode output voltage for analog inputs
Thermal Pad	65	GND	Ground	Connect to ground plane

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	V
	DRVDD	–0.3	2.1	V
	IOVDD	–0.3	2.1	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	minimum (2.1, AVDD + 0.3)	V
	SYNC~P, SYNC~M	–0.3	minimum (2.1, AVDD + 0.3)	V
	SYSREFP, SYSREFM	–0.3	minimum (2.1, AVDD + 0.3)	V
	SCLK, SEN, SDATA, RESET, PDN_GBL, CTRL1, CTRL2, STBY, MODE	–0.3	3.9	V
Temperature	Operating free-air, T_A	–40	85	°C
	Operating junction, T_J		125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

Over operating free-air temperature range, unless otherwise noted.

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD3V	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
IOVDD	Output buffer supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default after reset		2		V_{PP}
		Register programmable(2)		2.5		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.025		V
	Maximum analog input frequency with 2.5-V_{PP} input amplitude			250		MHz
	Maximum analog input frequency with 2-V_{PP} input amplitude			400		MHz
CLOCK INPUT						
	Input clock sample rate	10x mode	60		160	MSPS
		20x mode	40		156.25	MSPS
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac-coupled	0.3(3)	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Single-ended load resistance			+50		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) To reset the device for the first time after power-up, only use the RESET pin. Refer to the *Register Initialization* section.
(2) For details, refer to the *Digital Gain* section.
(3) Refer to the *Performance vs Clock Amplitude* curves (Figure 32 and Figure 33).

7.4 Thermal Information

THERMAL METRIC(1)		ADS42JB46 RGC (QFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ADS42JB46

Typical values are at T_A = 25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling clock rate = 160 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.7			75.2		dBFS
		f_{IN} = 70 MHz		73.5			74.9		dBFS
		f_{IN} = 170 MHz	69.5	72.9			74.2		dBFS
		f_{IN} = 230 MHz		72.3			73.3		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.5			75.1		dBFS
		f_{IN} = 70 MHz		73.3			74.7		dBFS
		f_{IN} = 170 MHz	68.5	72.8			73.6		dBFS
		f_{IN} = 230 MHz		72			72.8		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		96			92		dBc
		f_{IN} = 70 MHz		94			90		dBc
		f_{IN} = 170 MHz	79	90			84		dBc
		f_{IN} = 230 MHz		86			83		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	76	87			82		dBc
		f_{IN} = 230 MHz		84			81		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		96			95		dBc
		f_{IN} = 70 MHz		94			90		dBc
		f_{IN} = 170 MHz	79	92			89		dBc
		f_{IN} = 230 MHz		88			86		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		97			92		dBc
		f_{IN} = 70 MHz		96			94		dBc
		f_{IN} = 170 MHz	79	90			84		dBc
		f_{IN} = 230 MHz		86			83		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			101		dBc
		f_{IN} = 70 MHz		102			100		dBc
		f_{IN} = 170 MHz	87	100			95		dBc
		f_{IN} = 230 MHz		98			92		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		90			89		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 90-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.8			12		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.4			±0.5		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.75	±3		±0.9		LSBs

7.6 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, , and sampling clock rate = 160 MSPS unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default (after reset)		2		V_{PP}
		Register programmed(1)		2.5		V_{PP}
		Differential input resistance (at 170 MHz)		1.2		kΩ
		Differential input capacitance (at 170 MHz)		4		pF
	Analog input bandwidth	With 50-Ω source impedance and 50-Ω termination		900		MHz
VCM	Common-mode output voltage			1.9		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20		20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.01		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			90	130	mA
IAVDD3V	Analog buffer supply current			234	330	mA
IDRVDD	Digital supply current			174	207	mA
IOVDD	Output buffer supply current	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz, 10x mode		61	100	mA
	Analog power			162		mW
	Analog buffer power			772		mW
	Digital power			313		mW
	Power consumption by output buffer	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz, 10x mode		109		mW
	Total power			1.36	1.64	W
	Global power-down				160	mW

(1) Refer to the *Serial Interface* section.

7.7 Timing Characteristics

Typical values are at 25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling clock rate = 160 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V. See Figure 3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLE TIMING CHARACTERISTICS						
	Aperture delay		0.4	0.7	1.1	ns
	Aperture delay matching	Between two channels on the same device		±70		ps
		Between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter			85		f_S rms
	Wake-up time	Time to valid data after exiting STANDBY mode		50	200	µs
		Time to valid data after exiting global power-down		250	1000	µs
$t_{SU\_SYNC\sim}$	Setup time for SYNC~	Referenced to input clock rising edge	400			ps
$t_{H\_SYNC\sim}$	Hold time for SYNC~	Referenced to input clock rising edge	100			ps
t_{SU_SYSREF}	Setup time for SYSREF	Referenced to input clock rising edge	400			ps
t_{H_SYSREF}	Hold time for SYSREF	Referenced to input clock rising edge	100			ps
CML OUTPUT TIMING CHARACTERISTICS						
	Unit interval		320		1667	ps
	Serial output data rate				3.125	Gbps
T_{Jitter}	Total jitter	1.6 Gbps (10x mode, f_S = 160 MSPS)		0.28		$_{P\text{-}P}$UI
		3.125 Gbps (20x mode, f_S = 156.25 MSPS)		0.3		$_{P\text{-}P}$UI
t_R, t_F	Data rise time, data fall time	Rise and fall times are measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps		105		ps

7.8 Digital Characteristics

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
V_{IL}	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		10		µA
I_{IL}	Low-level input current	SEN		10		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		0		µA
DIGITAL INPUTS (SYNC~P, SYNC~M, SYSREFP, SYSREFM)						
V_{IH}	High-level input voltage			1.3		V
V_{IL}	Low-level input voltage			0.5		V
V_{CM_DIG}	Input common-mode voltage			0.9		V
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB)						
V_{OH}	High-level output voltage		DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DA[0,1], DB[0,1])(2)						
V_{OH}	High-level output voltage			IOVDD		V
V_{OL}	Low-level output voltage			IOVDD – 0.4		V
$\lvert V_{OD} \rvert$	Output differential voltage			0.4		V
V_{OCM}	Output common-mode voltage			IOVDD – 0.2		V
	Transmitter short-circuit current	Transmitter terminals shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
	Single-ended output impedance			50		Ω
C_{OUT}	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, and MODE pins have a 150-kΩ (typical) internal pulldown resistor to ground. The SEN pin has a 150-kΩ (typical) pullup resistor to AVDD.
(2) 50-Ω, single-ended, external termination to IOVDD.

7.9 Reset Timing (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values are at 25°C and minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

7.10 Serial Interface Timing(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD3V = 3.3 V, and AVDD = DRVDD = IOVDD = 1.8 V, unless otherwise noted.

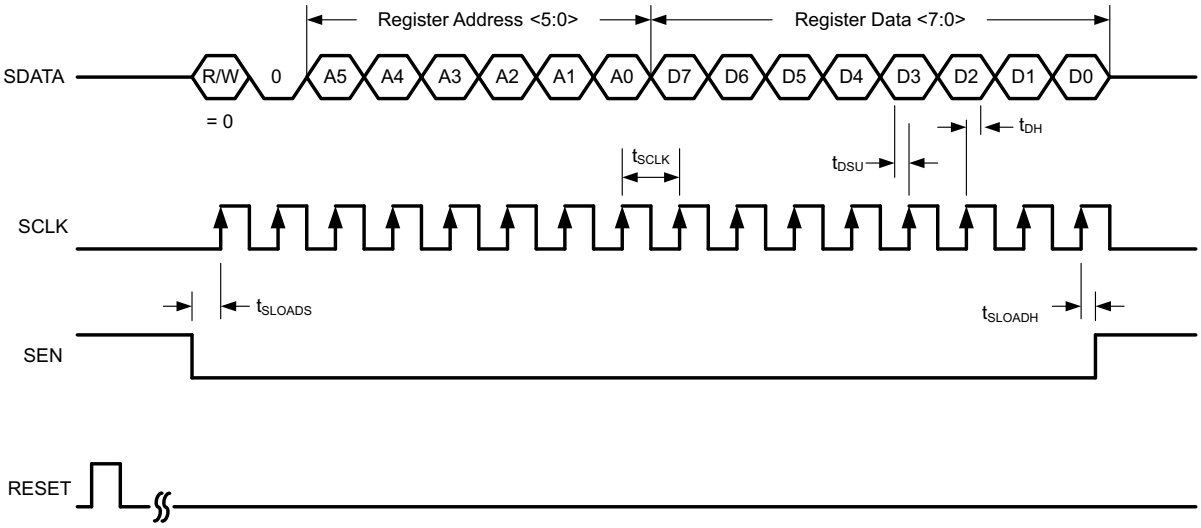
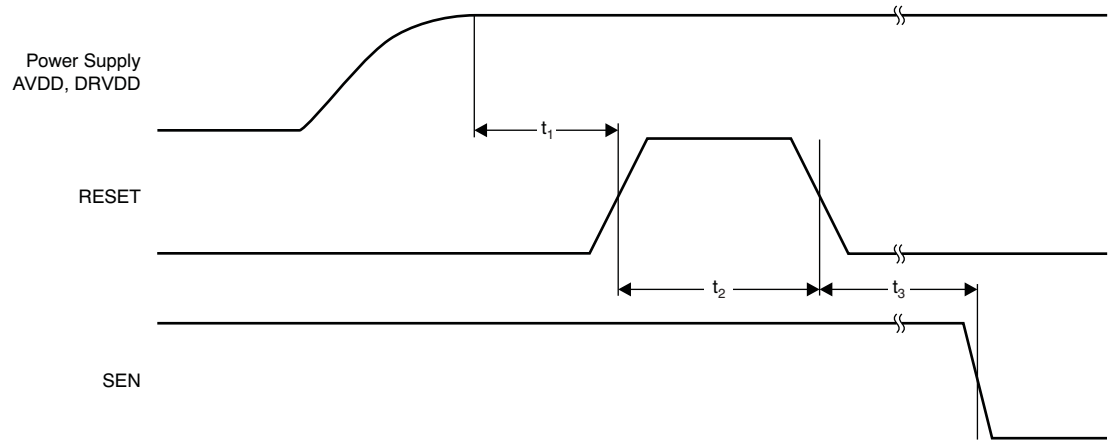
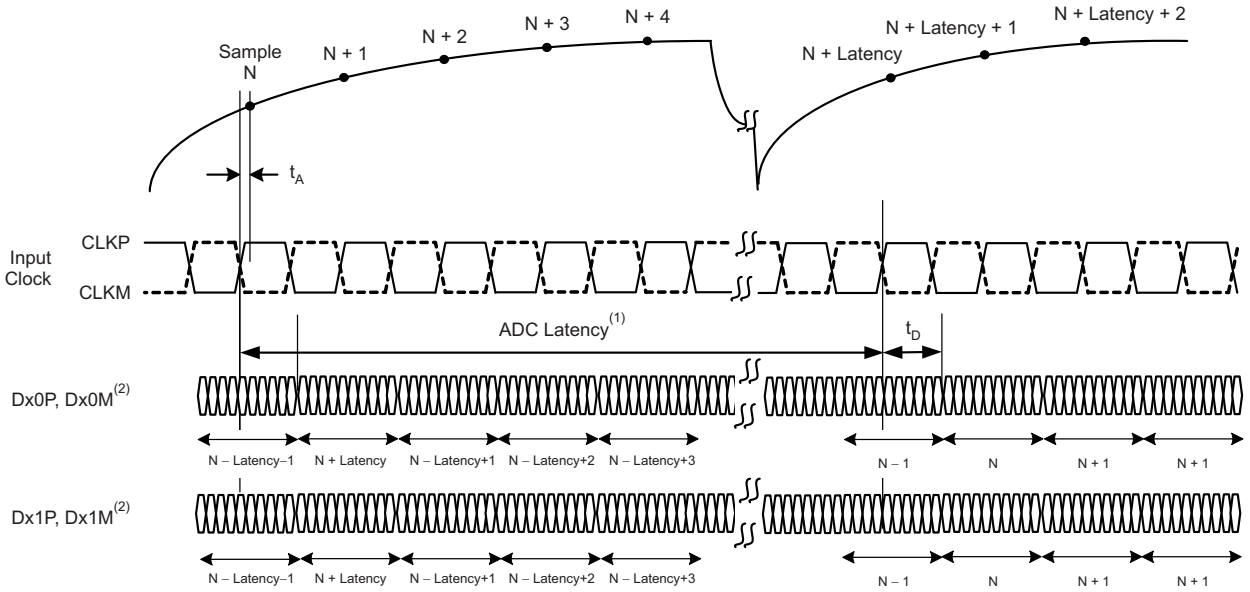


Figure 1. Serial Register Write Timing Diagram



NOTE: After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

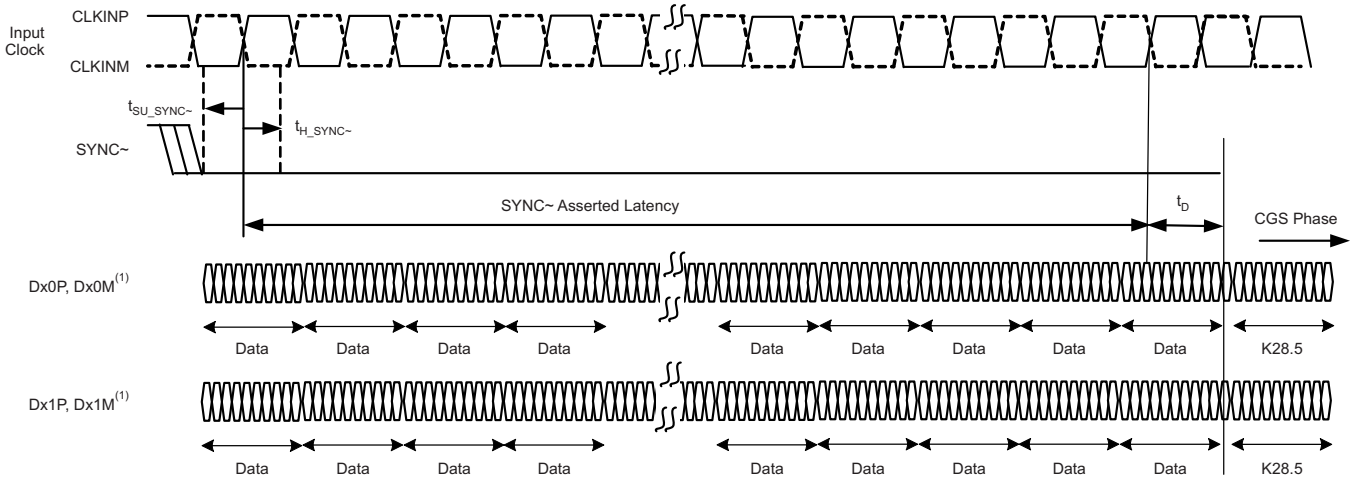
Figure 2. Reset Timing Diagram



(1) Overall latency = ADC latency + t_D.

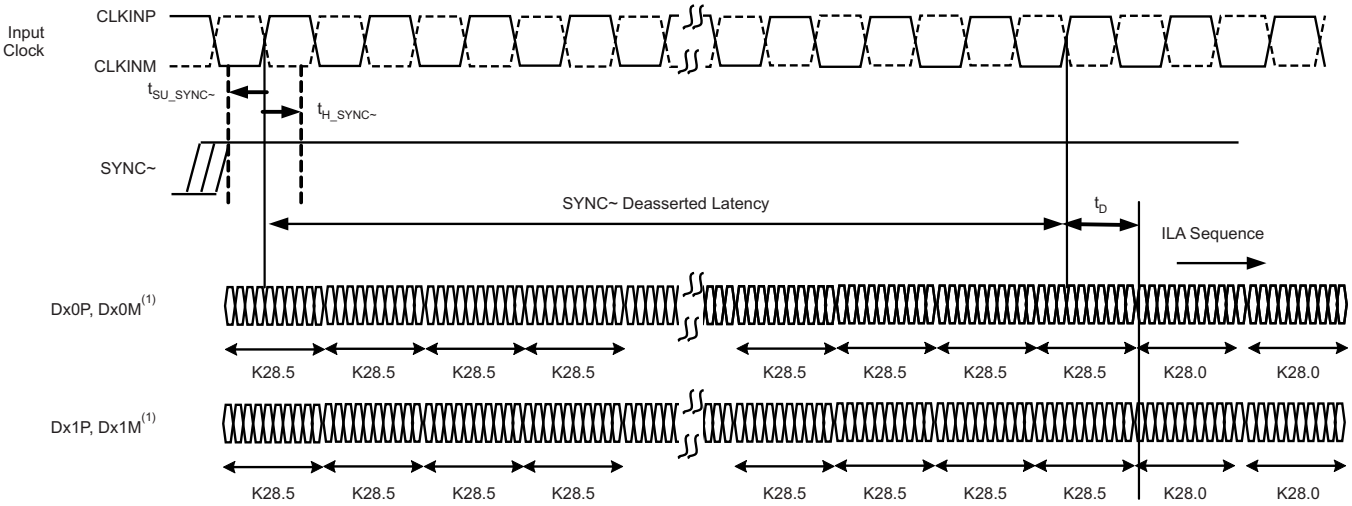
(2) x = A for channel A and B for channel B.

Figure 3. ADC Latency



(1) x = A for channel A and B for channel B.

Figure 4. SYNC~ Latency in CGS Phase (Two-Lane Mode)



(1) x = A for channel A and B for channel B.

Figure 5. SYNC~ Latency in ILAS Phase (Two-Lane Mode)

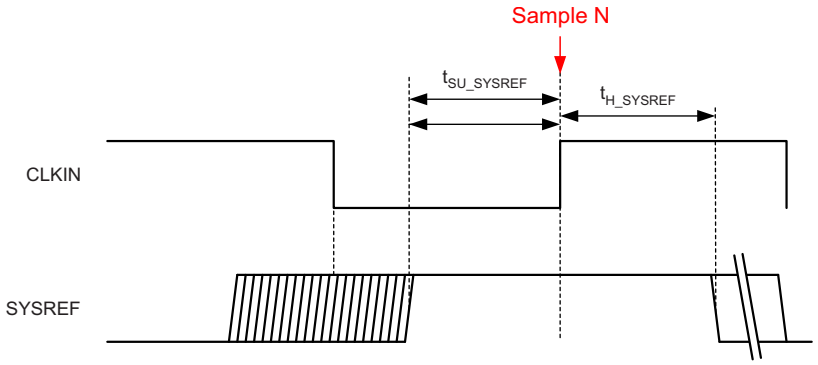


Figure 6. SYSREF Timing (Subclass 1)

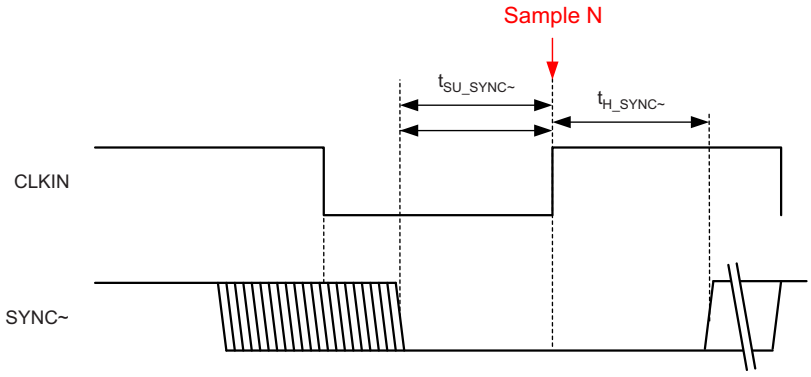


Figure 7. SYNC~ Timing (Subclass 2)

7.11 Typical Characteristics: ADS42JB46

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

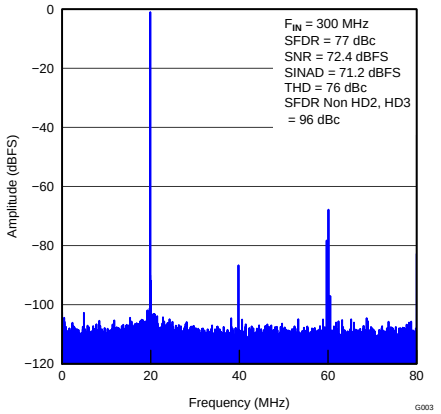


Figure 8. FFT for 300-MHz Input Signal

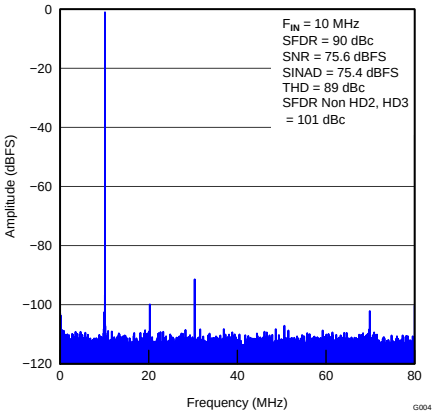


Figure 9. FFT for 10-MHz Input Signal (2.5-V_{PP} Full-Scale)

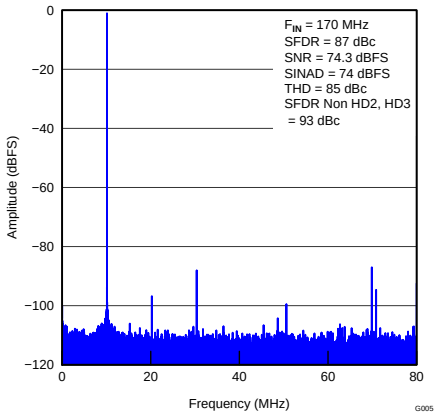


Figure 10. FFT for 170-MHz Input Signal (2.5-V_{PP} Full-Scale)

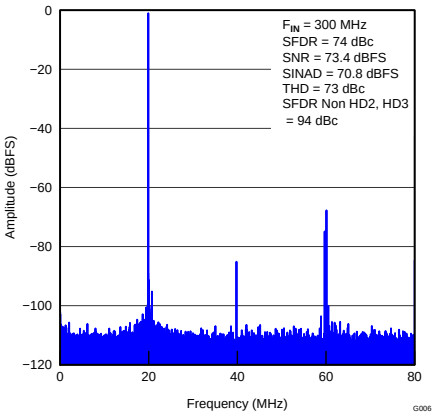


Figure 11. FFT for 300-MHz Input Signal (2.5-V_{PP} Full-Scale)

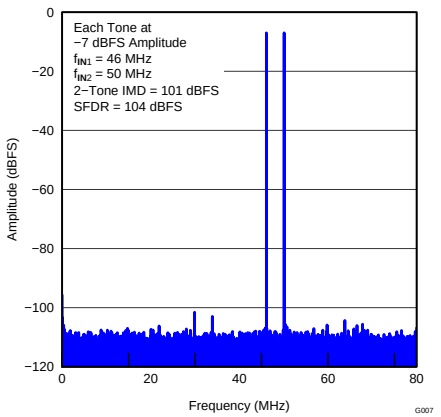


Figure 12. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

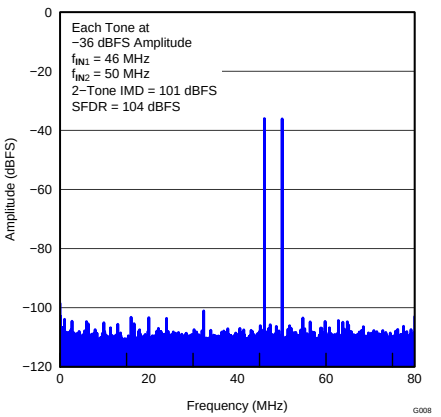


Figure 13. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

Typical Characteristics: ADS42JB46 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

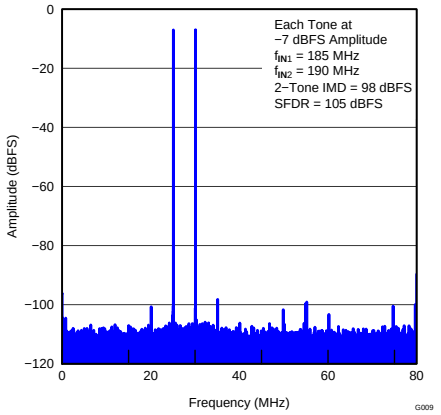


Figure 14. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)

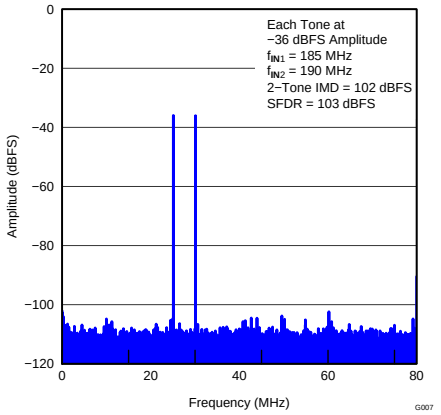


Figure 15. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

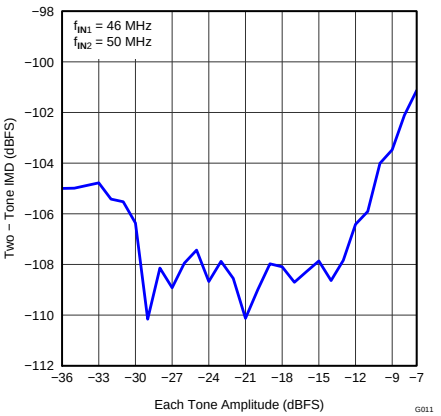


Figure 16. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

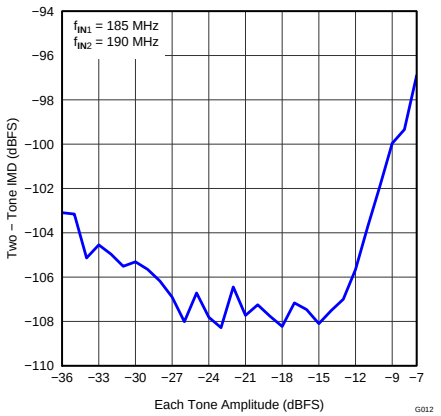


Figure 17. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

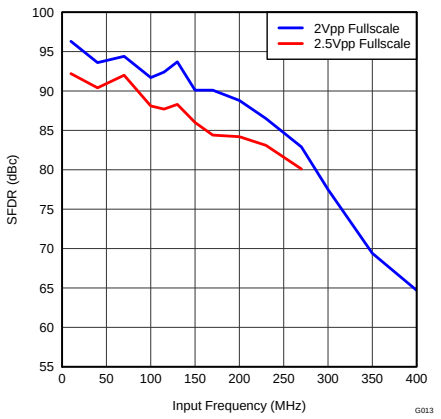


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

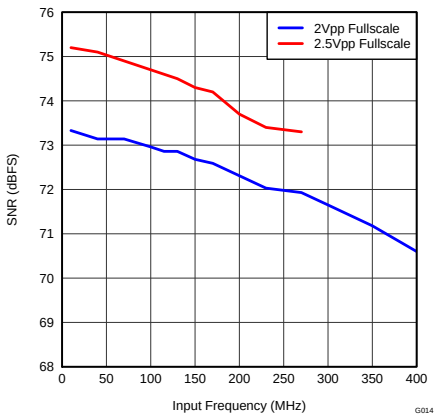


Figure 19. Signal-to-Noise Ratio vs Input Frequency

Typical Characteristics: ADS42JB46 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

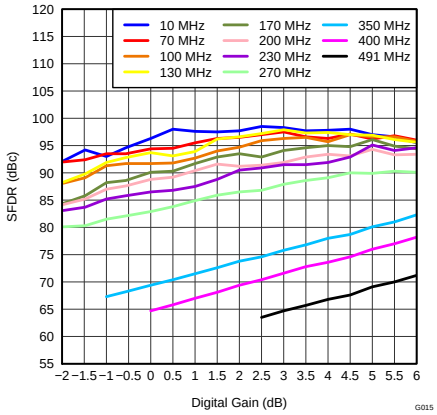


Figure 20. Spurious-Free Dynamic Range vs Digital Gain

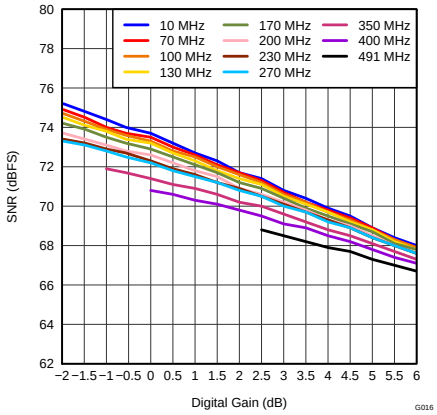


Figure 21. Signal-to-Noise Ratio vs Digital Gain

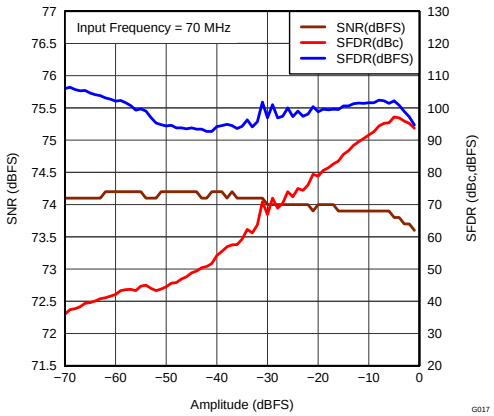


Figure 22. Performance vs Input Amplitude (70 MHz)

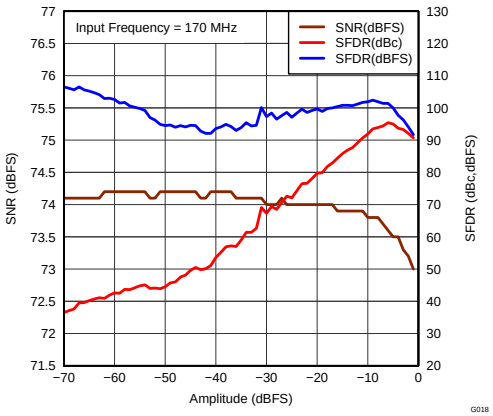


Figure 23. Performance vs Input Amplitude (170 MHz)

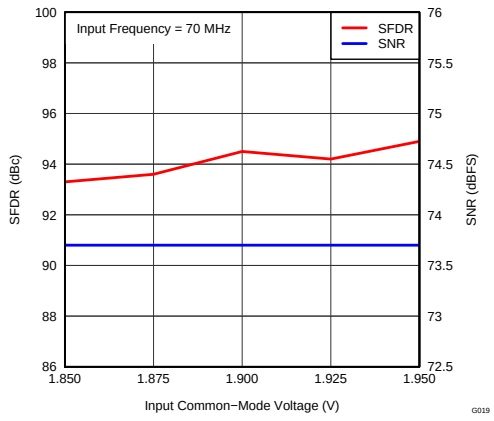


Figure 24. Performance vs Input Common-Mode Voltage (70 MHz)

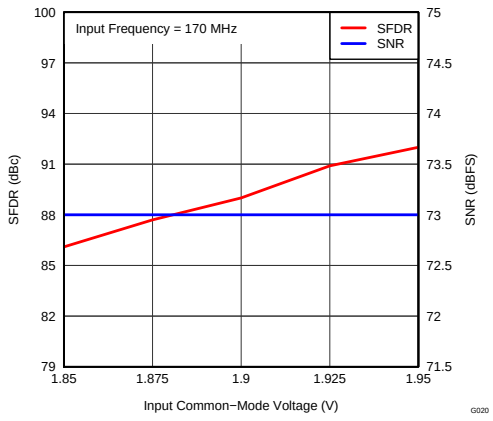


Figure 25. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADS42JB46 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

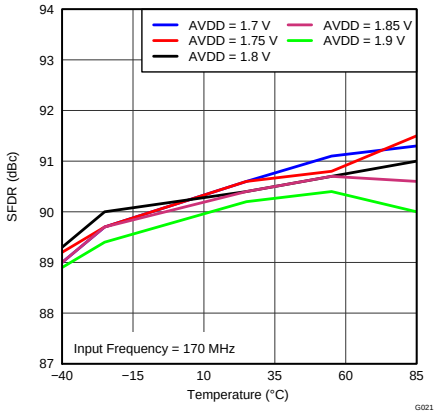


Figure 26. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

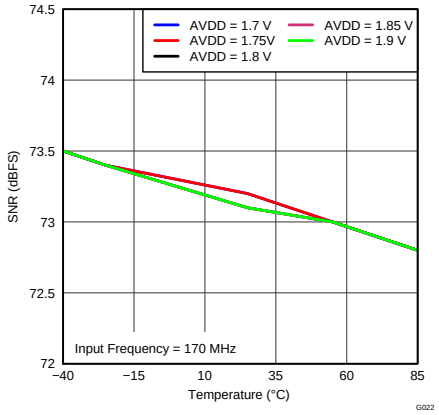


Figure 27. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

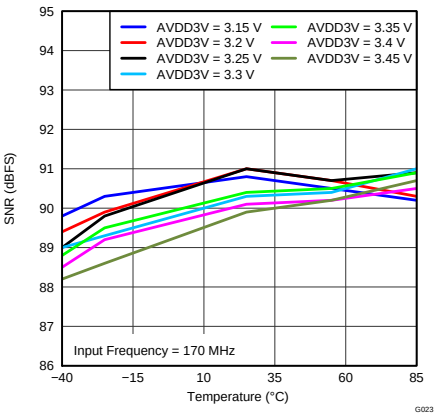


Figure 28. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature (170 Mhz)

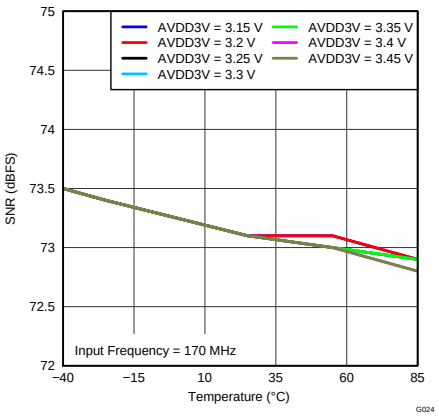


Figure 29. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature (170 MHz)

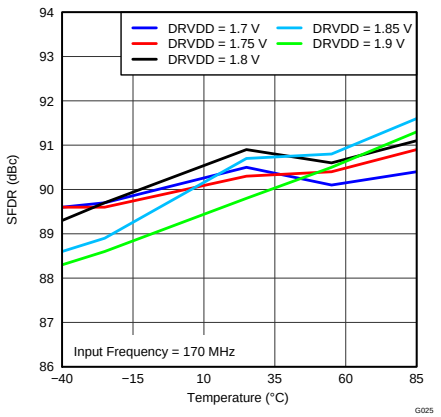


Figure 30. Spurious-Free Dynamic Range vs DRVDD Supply and Temperature (170 MHz)

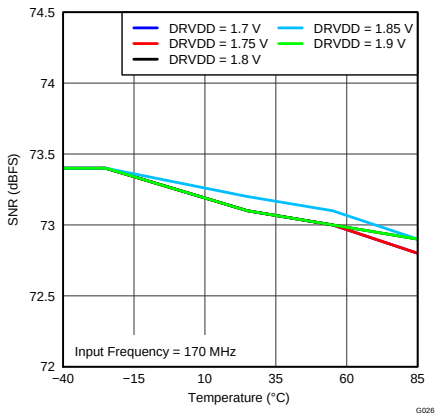


Figure 31. Signal-to-Noise Ratio vs DRVDD Supply and Temperature (170 MHz)

Typical Characteristics: ADS42JB46 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

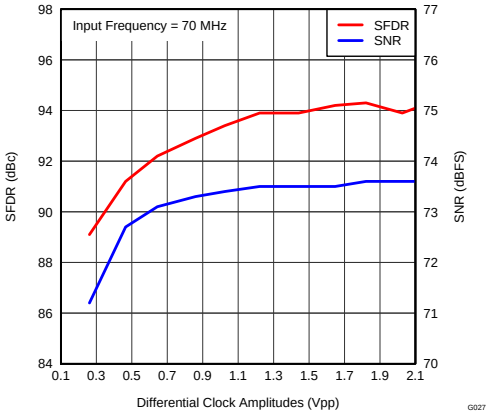


Figure 32. Performance vs Clock Amplitude (70 MHz)

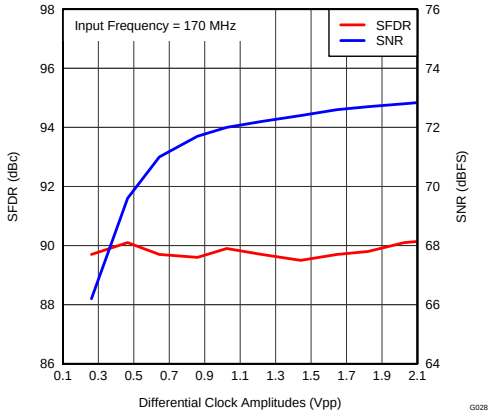


Figure 33. Performance vs Clock Amplitude (170 MHz)

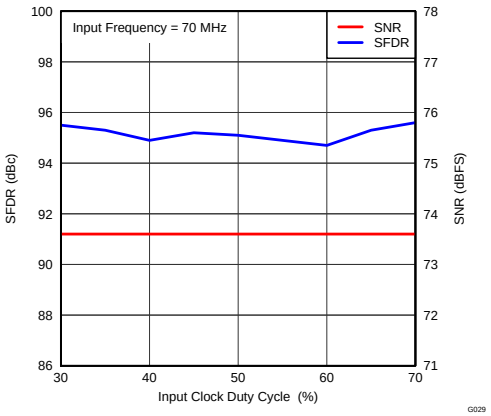


Figure 34. Performance vs Clock Duty Cycle (70 MHz)

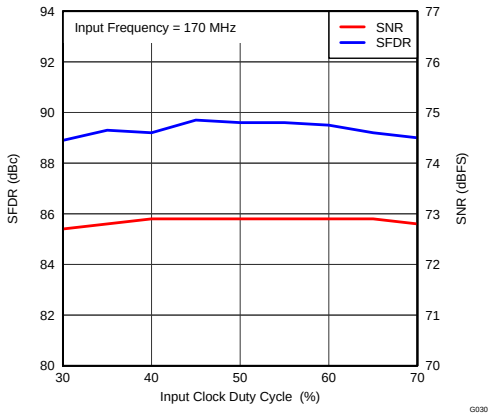


Figure 35. Performance vs Clock Duty Cycle (170 MHz)

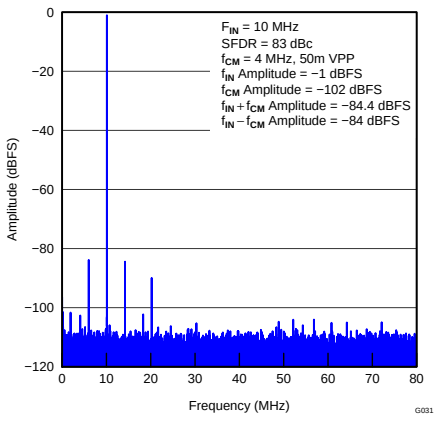


Figure 36. Common-Mode Rejection Ratio FFT

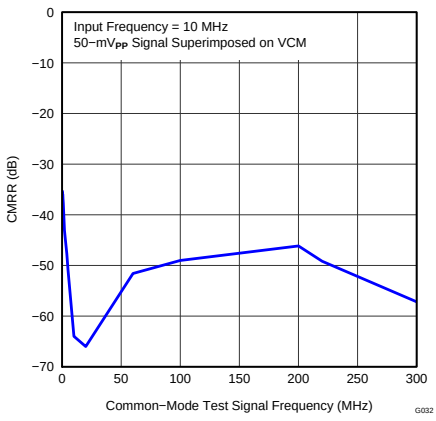


Figure 37. Common-Mode Rejection Ratio vs Test Signal Frequency

Typical Characteristics: ADS42JB46 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

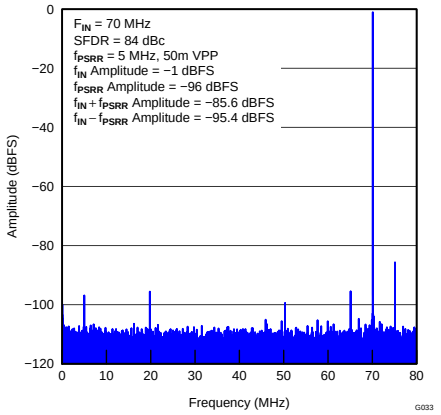


Figure 38. Power-Supply Rejection Ratio FFT for AVDD Supply

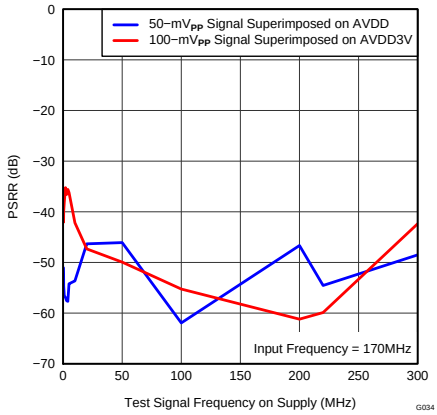


Figure 39. Power-Supply Rejection Ratio vs Test Signal Frequency

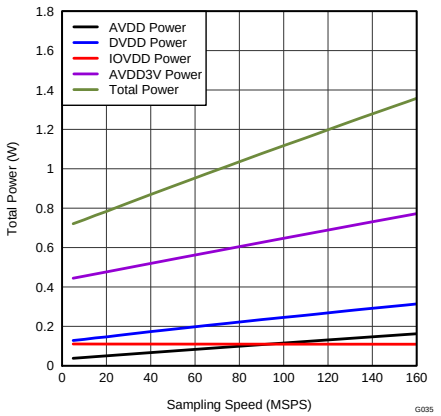


Figure 40. Total Power vs Sampling Frequency

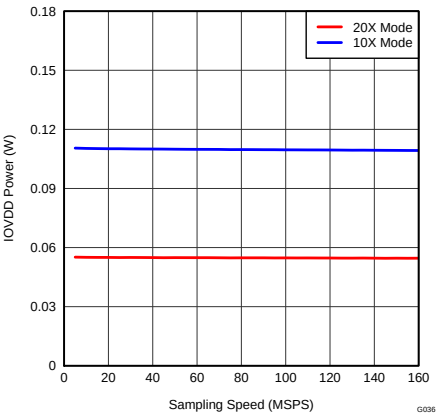


Figure 41. Analog Power vs Sampling Frequency

7.12 Typical Characteristics: Contour

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

7.12.1 Spurious-Free Dynamic Range (SFDR)

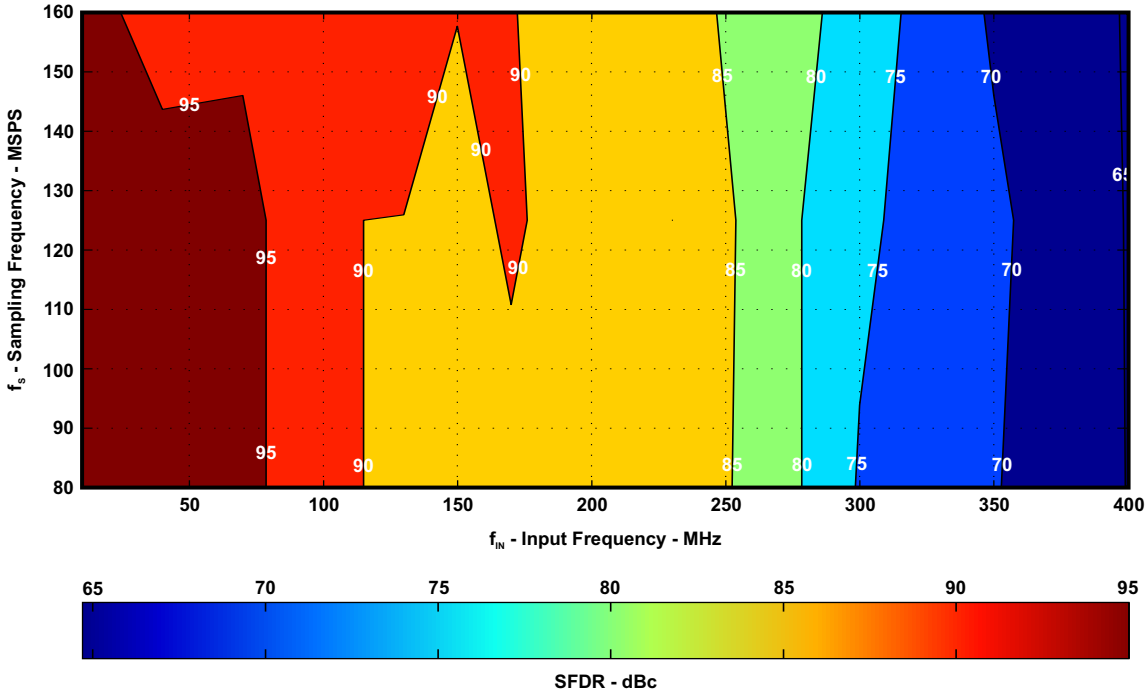


Figure 42. 0-dB Gain (SFDR)

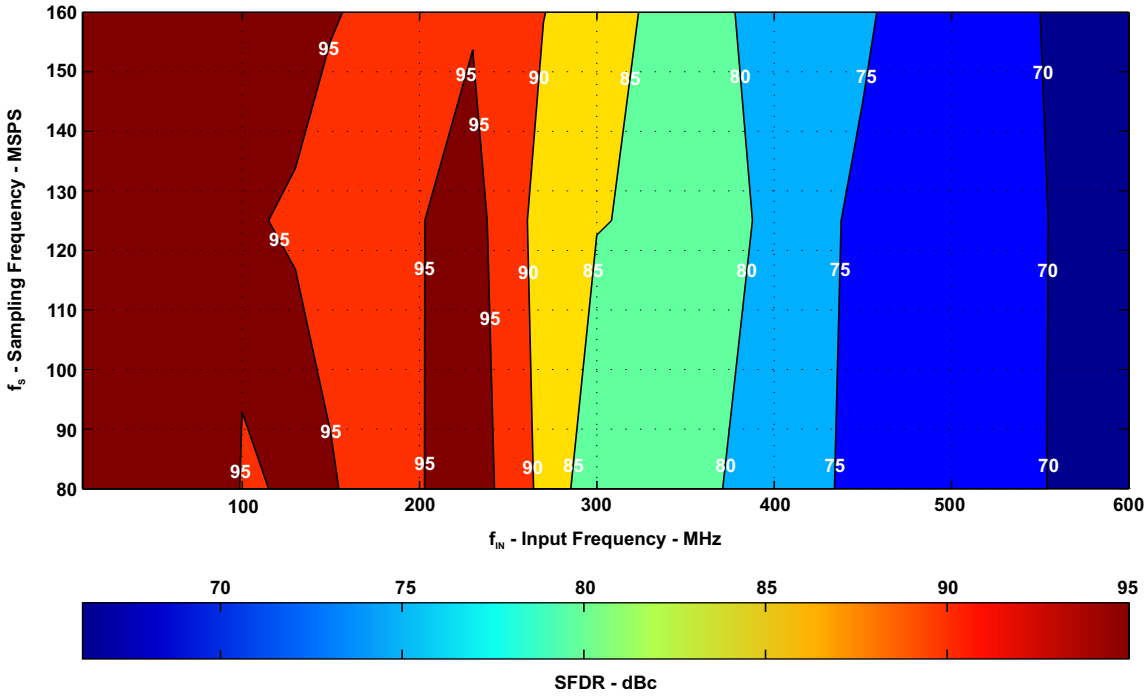


Figure 43. 6-dB Gain (SFDR)

7.12.2 Signal-to-Noise Ratio (SNR)

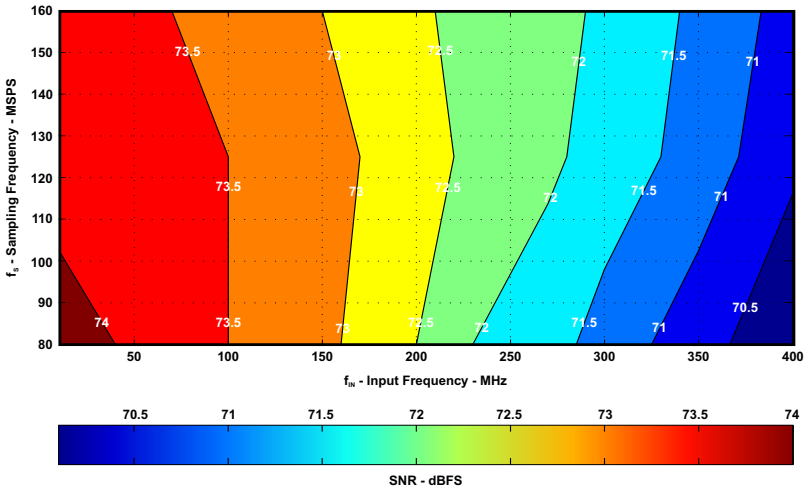


Figure 44. 0-dB Gain

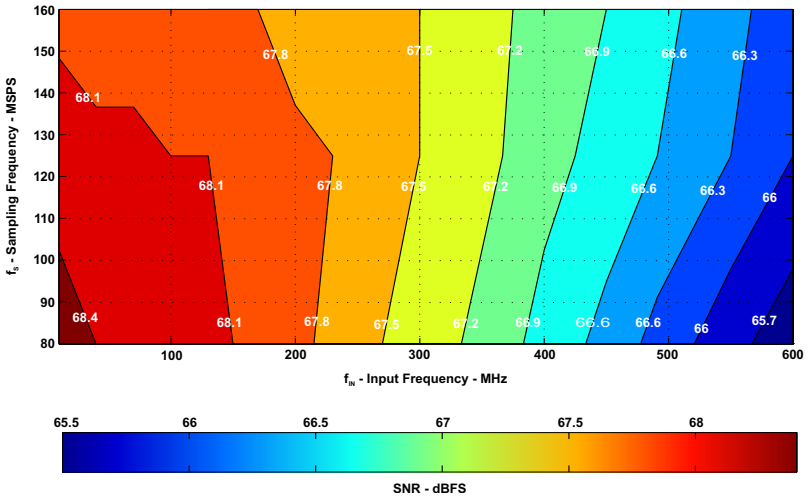


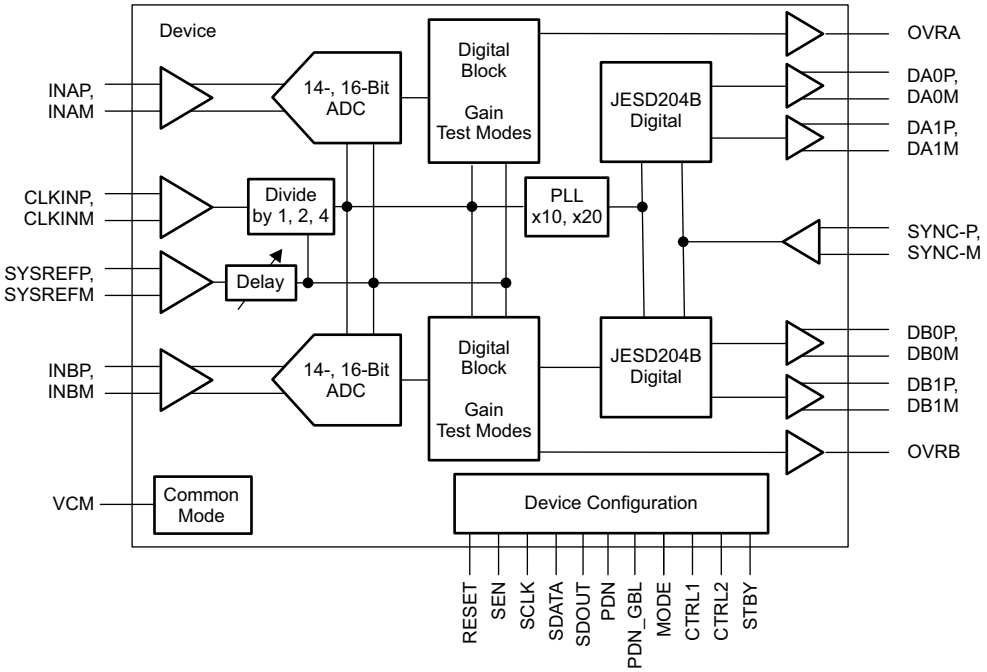
Figure 45. 6-dB Gain

8 Detailed Description

8.1 Overview

The ADS42JB46 is a highly linear, buffered analog input, dual-channel, analog-to-digital converter (ADC) with maximum sampling rate of 160 MSPS and JESD204B digital interface. The conversion process is initiated by a rising edge of the external input clock which samples the analog input signal. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline, resulting in a data latency of 23 clock cycles. The output is available in CML logic levels conforming to the JESD204B standard.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital Gain

The device includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from –2 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally. Table 1 shows how full-scale input voltage changes when digital gains are programmed in 1-dB steps. Refer to Table 13 to set digital gain with a serial interface register.

SFDR improvement is achieved at the expense of SNR; for a 1-dB increase in digital gain, SNR degrades approximately between 0.5 dB and 1 dB. Therefore, gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB with a 2.0-V_{PP} full-scale voltage.

Table 1. Full-Scale Range Across Gains

DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
–2 dB	2.5 V_{PP} (1)
–1 dB	2.2 V_{PP}
0 dB (default)	2.0 V_{PP}
1 dB	1.8 V_{PP}
2 dB	1.6 V_{PP}
3 dB	1.4 V_{PP}
4 dB	1.25 V_{PP}
5 dB	1.1 V_{PP}
6 dB	1.0 V_{PP}

(1) Shaded cells indicate performance settings used in the Electrical Characteristics and Typical Characteristics.

8.3.2 Overrange Indication

The device provides two different overrange indications. Normal OVR (default) is triggered if the final 16-bit data output exceeds the maximum code value. Fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRA and OVRB pins. Using the FAST OVR EN register bit, the fast OVR indication can be presented on the overrange pins instead.

The input voltage level at which the overload is detected is the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold voltage amplitude at which fast OVR is triggered is described in Equation 1:

$$1 \times [\text{the decimal value of the FAST OVR THRESH bits}] / 127 \quad (1)$$

When digital is programmed (for gain values > 0 dB), the threshold voltage amplitude is as given in Equation 2:

$$10^{-\text{Gain} / 20} \times [\text{the decimal value of the FAST OVR THRESH bits}] / 127 \quad (2)$$

8.3.3 Input Clock Divider

The device is equipped with an internal divider on the clock input. By default, the clock divider is set to divide-by-1 operation. The divide-by-2 option supports a maximum 500-MHz input clock and the divide-by-4 option supports a maximum 1-GHz input clock frequency. A 320-MHz input clock with the divide-by-2 option and a 640-MHz input clock with the divide-by-4 option can be accepted because the maximum conversion rate of the device is 160 MSPS.

8.3.4 Pin Controls

The device power-down functions can be controlled either through the parallel control pins (STBY, PDN_GBL, CTRL1, and CTRL2) or through an SPI register setting. Table 2, Table 3, and Table 4 describe the parallel control pin functionality.

STBY places the device in a standby power-down mode. PDN_GBL places the device in global power-down mode.

Table 2. CTRL1, CTRL2 Pin Functions

CTRL1	CTRL2	DESCRIPTION
Low	Low	Normal operation
High	Low	Channel A powered down
Low	High	Channel B powered down
High	High	Global power-down

Table 3. PDN_GBL Pin Function

PDN_GBL	DESCRIPTION
Low	Normal operation
High	Global power-down. Wake-up from this mode is slow.

Table 4. STBY Pin Function

STBY	DESCRIPTION
Low	Normal operation
High	The ADCs are powered down while the input clock buffer and output CML buffers are alive. Wake-up from this mode is fast.

8.4 Device Functional Modes

8.4.1 JESD204B Interface

The JESD interface of the device, as shown in Figure 46 , supports device subclasses 0, 1, and 2 with a maximum output data rate (per lane) of 3.125 Gbps. An external SYSREF (subclass 1) or SYNC~ (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

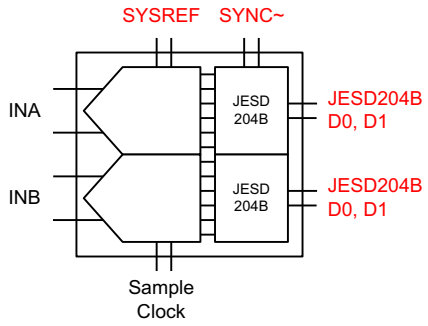


Figure 46. JESD204B Interface

Depending on the ADC sampling rate, the JESD204B output interface can be operated with either one or two lanes per ADC. The JESD204B interface can be configured with serial registers.

Device Functional Modes (continued)

The JESD204B transmitter block (as shown in Figure 47) consists of the transport layer, data scrambler, and link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and determines whether the ADC output data or test patterns are transmitted. The link layer performs the 8b and 10b data encoding as well as the synchronization and initial lane alignment using the SYNC~ input signal. Optionally, data from the transport layer can be scrambled.

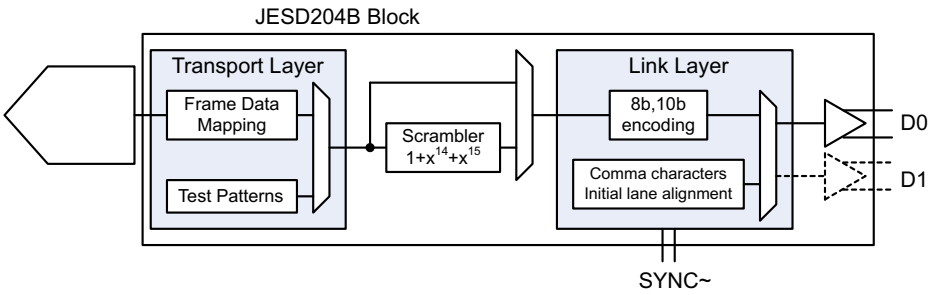


Figure 47. JESD204B Block

8.4.1.1 JESD204B Initial Lane Alignment (ILA)

When receiving, the device asserts the SYNC~ signal (that is, a logic low signal is applied on SYNC~P and SYNC~M). The device then begins transmitting comma (K28.5) characters to establish the code group synchronization (CGS). When synchronization completes, the receiving device de-asserts the SYNC~ signal and the device begins the initial lane alignment (ILA) sequence with the next local multiframe clock boundary. The device transmits four multiframes, each containing K frames (where K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

8.4.1.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The device supports a clock output pattern, an encoded pattern, and a PRBS (2^{15} – 1) pattern. These patterns can be enabled by a serial register write in register 26h, bits D[7:6].

8.4.1.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per lane.
- M is the number of converters per device.
- F is the number of octets per frame clock period.
- S is the number of samples per frame.

Table 5 lists the available JESD204B formats and valid device ranges. Ranges are limited by the maximum ADC sample frequency and the SERDES line rate.

Table 5. JESD240B Ranges

L	M	F	S	MAX ADC SAMPLING RATE (MSPS)	MAX f_{SERDES} (Gbps)
4	2	1	1	160	1.6
2	2	2	1	156.25	3.125

The detailed frame assembly in 10x and 20x modes for dual-channel operation is shown in Table 6. Note that unused lanes in 10x mode become 3-stated.

Table 6. Frame Assembly for Dual-Channel Mode(1)

LANE	LMF = 421				LMF = 222					
DA0	A_0[15:8]	A_1[15:8]	A_2[15:8]		A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_2[15:8]	A_2[7:0]
DA1	A_0[7:0]	A_1[7:0]	A_2[7:0]		—	—	—	—	—	—
DB0	B_0[15:8]	B_1[15:8]	B_2[15:8]		B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_2[15:8]	B_2[7:0]
DB1	B_0[7:0]	B_1[7:0]	B_2[7:0]		—	—	—	—	—	—

(1) Two LSBs of the 16-bit data are padded with '00' in the device.

Table 7. High-Frequency Modes Summary

REGISTER ADDRESS	VALUE	DESCRIPTION
Dh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.
Eh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.

8.4.1.4 JESD Link Configuration

During the lane alignment sequence, the device transmits JESD204B configuration parameters in the second multiframe of the ILA sequence. Configuration bits are mapped in octets, as per the JESD204B standard described in Figure 48 and Table 8.

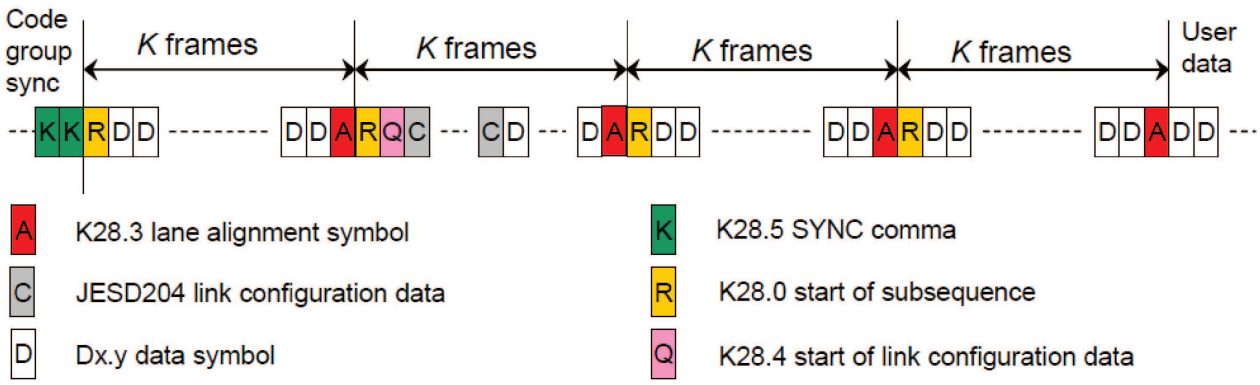


Figure 48. Initial Lane Alignment Sequence

Table 8. Mapping of Configuration Bits to Octets

OCTET NO	MSB	D6	D5	D4	D3	D2	D1	LSB
0	DID [7:0]							
1	ADJCNT[3:0]				BID[3:0]			
2	X	ADJDIR[0]	PHADJ[0]	LID[4:0]				
3	SCR[0]			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]		X	N[4:0]				
8	SUBCLASSV[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD[0]	X	X	CF[4:0]				
11	RES1[7:0]							
12	RES2[7:0]							
13	FCHK[7:0]							

8.4.1.4.1 Configuration for 2-Lane (20x) SERDES Mode

Table 9 lists the values of the JESD204B configuration bits applicable for the 2-lane SERDES mode. The default value of these bits after reset is also specified in Table 9.

Table 9. Configuration for 2-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust the DAC LMFC. Applies to subclass 2 operation only.	0:15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust the DAC LMFC. 0 = Advance 1 = Delay applies to subclass 2 operation only	0:1	ADJDIR[0]	Binary value	0
BID	Bank ID: extension to DID	0:15	BID[3:0]	Binary value	0
CF	Number of control words per frame clock period per link	0:32	CF[4:0]	Binary value	0
CS	Number of control bits per sample	0:3	CS[1:0]	Binary value	0
DID	Device (= link) identification number	0:255	DID[7:0]	Binary value	0
F	Number of octets per frame	1:256	F[7:0]	Binary value minus 1	1
HD	High-density format	0:1	HD[0]	Binary value	0
JESDV	JESD204 version 000 = JESD204A 001 = JESD204B	0:7	JESDV[2:0]	Binary value	1
K	Number of frames per multiframe	1:32	K[4:0]	Binary value minus 1	8
L	Number of lanes per converter device (link)	1:32	L[4:0]	Binary value minus 1	0
LID	Lane identification number (within link)	0:31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1
M	Number of converters per device	1:256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1:32	N[4:0]	Binary value minus 1	15
N’	Total number of bits per sample	1:32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only	0:1	PHADJ[0]	Binary value	0
S	Number of samples per converter per frame cycle	1:32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0:1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 = Subclass 0 001 = Subclass 1 010 = Subclass 2	0:7	SUBCLASSV[2:0]	Binary value	2
RES1	Device subclass version 000 = Subclass 0 001 = Subclass 1 010 = Subclass 2	0:255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0:255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ (all above fields) mod 256	0:255	FCHK[7:0]	Binary value	44, 45

8.4.1.4.2 Configuration for 4-Lane (10x) SERDES Mode

Table 10 lists the values of the JESD204 configuration bits applicable for the 4-lane SERDES mode. The default value of these bits after reset is also specified in Table 10.

Table 10. Configuration for 4-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust the DAC LMFC. Applies to subclass 2 operation only.	0:15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust the DAC LMFC. 0 = Advance 1 = Delay applies to subclass 2 operation only	0:1	ADJDIR[0]	Binary value	0
BID	Bank ID: extension to DID	0:15	BID[3:0]	Binary value	0
CF	Number of control words per frame clock period per link	0:32	CF[4:0]	Binary value	0
CS	Number of control bits per sample	0:3	CS[1:0]	Binary value	0
DID	Device (= link) identification number	0:255	DID[7:0]	Binary value	0
F	Number of octets per frame	1:256	F[7:0]	Binary value minus 1	0
HD	High-density format	0:1	HD[0]	Binary value	1
JESDV	JESD204 version 000 = JESD204A 001 = JESD204B	0:7	JESDV[2:0]	Binary value	1
K	Number of frames per multiframe	1:32	K[4:0]	Binary value minus 1	16
L	Number of lanes per converter device (link)	1:32	L[4:0]	Binary value minus 1	3
LID	Lane identification number (within link)	0:31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1, LID[2] = 2, LID[3] = 3
M	Number of converters per device	1:256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1:32	N[4:0]	Binary value minus 1	15
N’	Total number of bits per sample	1:32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only	0:1	PHADJ[0]	Binary value	0
S	Number of samples per converter per frame cycle	1:32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0:1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 = Subclass 0 001 = Subclass 1 010 = Subclass 2	0:7	SUBCLASSV[2:0]	Binary value	2
RES1	Device subclass version 000 = Subclass 0 001 = Subclass 1 010 = Subclass 2	0:255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0:255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ (all above fields) mod 256	0:255	FCHK[7:0]	Binary value	54, 55, 56, 57

Table 11. Latency in Different Modes(1)(2)

MODE	PARAMETER	LATENCY (N Cycles)	TYPICAL DATA DELAY (t_D, ns)
10x	ADC latency	23	0.65 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	From SYNC~ falling edge to CGS phase(3)	16	0.65 × t_S + 3
	From SYNC~ rising edge to ILA sequence(4)	25	0.65 × t_S + 3
20x	ADC latency	22	0.85 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	From SYNC~ falling edge to CGS phase(3)	15	0.85 × t_S + 3
	From SYNC~ rising edge to ILA sequence(4)	16	0.85 × t_S + 3

(1) Overall latency = latency + t_D.
(2) t_S is the time period of the ADC conversion clock.
(3) Latency is specified for subclass 2. In subclass 0, the SYNC~ falling edge to CGS phase latency is 16 clock cycles in 10x mode and 15 clock cycles in 20x mode.
(4) Latency is specified for subclass 2. In subclass 0, the SYNC~ rising edge to ILA sequence latency is 11 clock cycles in 10x mode and 11 clock cycles in 20x mode.

8.4.1.5 CML Outputs

The device JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using register settings.

The output driver includes an internal 50-Ω termination to the IOVDD supply. External 50-Ω termination resistors connected to the receiver common-mode voltage should be placed close to the receiver pins. AC-coupling can be used to avoid the common-mode mismatch between the transmitter and receiver, as shown in Figure 49.

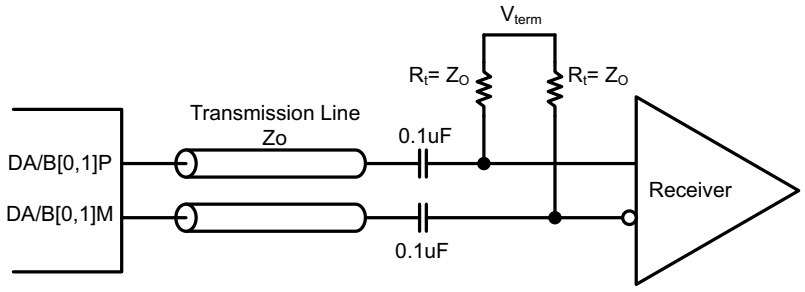


Figure 49. CML Output Connections

Figure 50 shows the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 3.125 Gbps (20x mode).

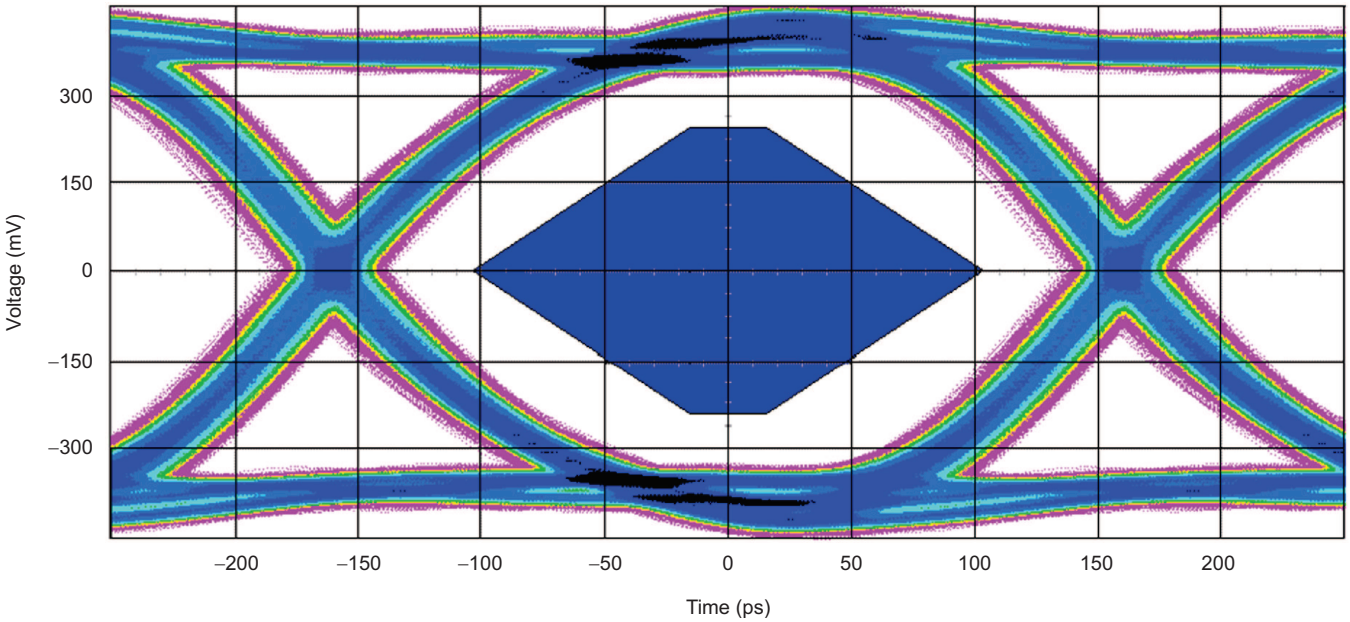


Figure 50. Eye Diagram: 3.125 Gbps

8.5 Programming

The ADS42JB46 can be configured using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has four dedicated parallel pins (PDN_GBL, STBY, CTRL1, and CTRL2) for controlling the power-down modes.

8.5.1 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK rising edge when SEN is active (low). Serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface functions with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

8.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a **hardware reset** by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 2. During operation, the serial interface registers can be cleared (if required) either by:

1. A hardware reset or
2. By applying a software reset. When using the serial interface, set the RESET bit (register 08h, bit D0) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin remains low.

Programming (continued)

8.5.1.2 Serial Register Write

The internal device register can be programmed following these steps:

1. Drive the SEN pin low.
2. Set the R/W bit to ‘0’ (bit A7 of the 8-bit address).
3. Set bit A6 in the address field to ‘0’.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content must be written (as shown in Figure 1 and).
5. Write the 8-bit data that are latched on the SCLK rising edge.

Programming (continued)

8.5.1.3 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set the MSB of the 8-bit address A7 to '1'.
2. Write the register address on bits A5 through A0 whose contents must be read. See Figure 51.
3. The device outputs the contents (D[7:0]) of the selected register on the SDOUT pin (pin 45).
4. The external controller can latch the contents at the SCLK rising edge.

When serial registers are enabled for writing (when bit A7 of the 8-bit address bus is '0'), the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 51 shows a timing diagram of this readout mode. SDOUT comes out at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 52.

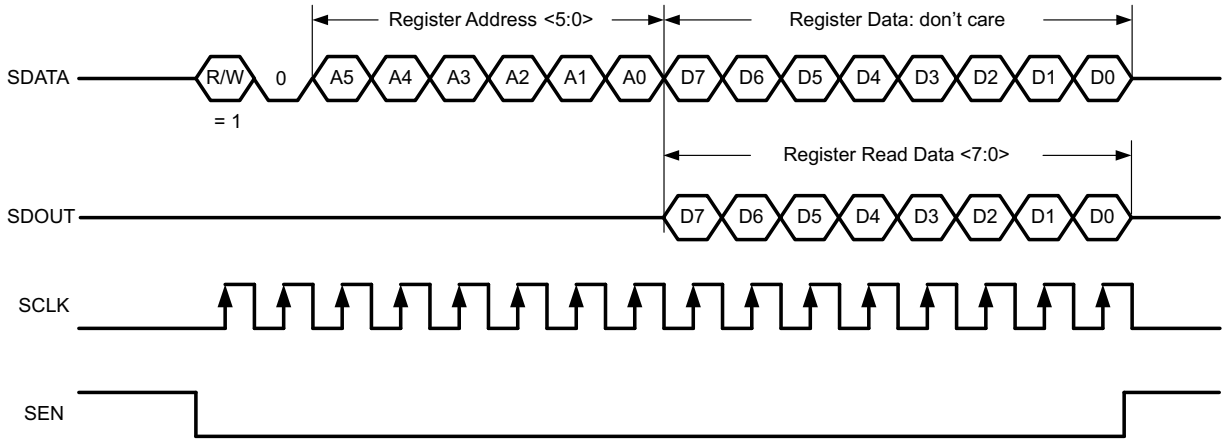


Figure 51. Serial Register Readout Timing Diagram

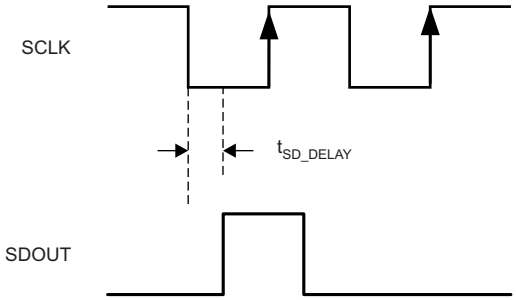


Figure 52. SDOUT Timing Diagram

8.6 Register Maps

8.6.1 Summary of Serial Interface Registers

Table 12 lists the device registers.

Table 12. Register Map

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
06	0	0	0	0	0	0	CLK DIV	
07	0	0	0	0	0	SYSREF DELAY		
08	PDN CHA	PDN CHB	STDBY	DATA FORMAT	Always write 1	0	0	RESET
0B	CHA GAIN					CHA GAIN EN	0	0
0C	CHBGAIN					CHB GAIN EN	0	0
0D	HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN
0E	HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0
0F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN[15:8]							
11	CUSTOM PATTERN[15:8]							
12	CUSTOM PATTERN[15:8]							
13	CUSTOM PATTERN[15:8]							
1F	Always write 0	FAST OVR THRESHOLD						
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LAN ALIGN	FRAME ALIGN	TX LINK CONFIG DATA0
27	0	0	0	0	0	0	CTRLK	CTRLF
2B	SCRAMBLE EN	0	0	0	0	0	0	0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME
2D	0	0	0	FRAMES PER MULTIFRAME				
30	SUBCLASS			0	0	0	0	0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

8.6.2 Description of Serial Interface Registers

8.6.2.1 Register Address 06

Figure 53. Register Address 06

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
06	0	0	0	0	0	0	CLK DIV	

Default: 00h

D[1:0] **CLK DIV** Internal clock divider for input sample clock

00 Divide-by-1 (clock divider bypassed)

01 Divide-by-2

10 Divide-by-1

11 Divide-by-4

8.6.2.2 Register Address 07

Figure 54. Register Address 07

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
07	0	0	0	0	0	0	SYSREF DELAY	

Default: 00h

D[2:0] **SYSREF DELAY** Controls the delay of the SYSREF input with respect to the input clock. Typical values for the expected delay of different settings are:

000 0-ps delay

001 60-ps delay

010 120-ps delay

011 180-ps delay

100 240-ps delay

101 300-ps delay

110 360-ps delay

111 420-ps delay

8.6.2.3 Register Address 08

Figure 55. Register Address 08

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
08	PDN CHA	PDN CHB	STDBY	DATA FORMAT	Always write 1	0	0	RESET

Default: 00h

D7 **PDN CHA** Power-down channel A

0 Normal operation

1 Channel A power down

D6 **PDN CHB** Power-down channel B

0 Normal operation

1 Channel B power down

D5 **STBY** Dual ADC is placed into standby mode

0 Normal operation

1 Both ADCs are powered down (input clock buffer and CML output buffers are alive)

D4 **DATA FORMAT** Digital output data format

0 Twos complement

1 Offset binary

D3 **Always write 1**

Default value of this bit is '0'. This bit must always be set to '1'.

D0 **RESET** Software reset applied

This bit resets all internal registers to the default values and self-clears to ‘0’.

8.6.2.4 Register Address 0B

Figure 56. Register Address 0B

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0B	CHA GAIN					CHA GAIN EN	0	0

Default: 00h

D[7:3] **CHA GAIN** Digital gain for channel A (must set the CHA GAIN EN bit first, bit D2)

Table 13. Digital Gain for Channel A

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	**2.0 V_{PP}**		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	**2.5 V_{PP}**		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	**2.0 V_{PP}**		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

D2 **CHA GAIN EN** Digital gain enable bit for channel A

0 Digital gain disabled

1 Digital gain enabled

8.6.2.5 Register Address 0C

Figure 57. Register Address 0C

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0C	CHB GAIN					CHB GAIN EN	0	0

Default: 00h

D[7:3] **CHB GAIN** Digital gain for channel B (must set the CHA GAIN EN bit first, bit D2)

Table 14. Digital Gain for Channel B

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	**2.0 V_{PP}**		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	**2.5 V_{PP}**		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	**2.0 V_{PP}**		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

D2 **CHB GAIN EN** Digital gain enable bit for channel B

0 Digital gain disabled

1 Digital gain enabled

8.6.2.6 Register Address 0D

Figure 58. Register Address 0D

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0D	HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN

D7, D4 **HIGH FREQ 1** High-frequency mode 1

00 Default

11 Use for input frequencies > 250 MHz along with HIGH FREQ 2

D0 **FAST OVR EN** Selects if normal or fast OVR signal is presented on OVRA, OVRB pins

0 Normal OVR on OVRA, OVRB pins

1 Fast OVR on OVRA, OVRB pins

8.6.2.7 Register Address 0E

Figure 59. Register Address 0E

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0E	HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0

D7, D4 **HIGH FREQ 2** High-frequency mode 2
00 Default
11 Use for input frequencies > 250 MHz along with HIGH FREQ 1

8.6.2.8 Register Address 0F

Figure 60. Register Address 0F

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0F	CHA TEST PATTERNS				CHB TEST PATTERNS			

Default: 00h

D[7:4] **CHA TEST PATTERNS** Channel A test pattern programmability
The 16-bit test pattern data are selected as the input to the JESD block (the last two LSBs of the 16-bit data are replaced by '00').

0000	Normal operation	
0001	All '0's	
0010	All '1's	
0011	Toggle pattern:	Data alternate between *10101010101010* and *01010101010101*.
0100	Digital ramp:	Data increment by 1 LSB every fourth clock cycle from code 0 to 16383.
0101	Do not use	
0110	Single pattern:	Data are the same as that programmed by the CUSTOM PATTERN 1[15:2] register bits.
0111	Double pattern:	Data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	Data are AAA8h.
1001	Do not use	
1010	PRBS pattern:	Data are a sequence of pseudo random numbers.
1011	8-point sine wave:	Data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.

D3-D0 **CHB TEST PATTERNS** Channel B test pattern programmability
The 16-bit test pattern data are selected as the input to the JESD block (the last two LSBs of the 16-bit data are replaced by '00').

0000	Normal operation	
0001	All '0's	
0010	All '1's	
0011	Toggle pattern:	Data alternate between *10101010101010* and *01010101010101*.
0100	Digital ramp:	Data increment by 1 LSB every fourth clock cycle from code 0 to 16383.
0101	Do not use	
0110	Single pattern:	Data are the same as that programmed by the CUSTOM PATTERN 1[15:2] register bits.
0111	Double pattern:	Data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	Data are AAA8h.
1001	Do not use	
1010	PRBS pattern:	Data are a sequence of pseudo random numbers.
1011	8-point sine wave:	Data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.

8.6.2.9 Register Address 10

Figure 61. Register Address 10

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	CUSTOM PATTERN 1[15:8]							

Default: 00h

D[7:0] **CUSTOM PATTERN 1[15:8]** These bits set the custom pattern 1[15:8] for both channels.

8.6.2.10 Register Address 11

Figure 62. Register Address 11

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	CUSTOM PATTERN 1[7:0]							

Default: 00h

D[7:0] **CUSTOM PATTERN 1[7:0]** These bits set the custom pattern 1[7:0] for both channels.

8.6.2.11 Register Address 12

Figure 63. Register Address 12

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
12	CUSTOM PATTERN 2[15:8]							

Default: 00h

D[7:0] **CUSTOM PATTERN 2[15:8]** These bits set the custom pattern 2[15:8] for both channels.

8.6.2.12 Register Address 13

Figure 64. Register Address 13

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
13	CUSTOM PATTERN 2[7:0]							

Default: 00h

D[7:0] **CUSTOM PATTERN 2[7:0]** These bits set the custom pattern 2[7:0] for both channels.

8.6.2.13 Register Address 1F

Figure 65. Register Address 1F

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
1F	Always write 0	FAST OVR THRESHOLD						

Default: FFh

D7 **Always write 0**

Default value of this bit is '1'. Always write this bit to '0' when the fast OVR thresholds are programmed.

D[6:0] **FAST OVR THRESHOLD**

The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the *threshold* and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127). See the *Overrange Indication* section for details.

8.6.2.14 Register Address 26

Figure 66. Register Address 26

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRANE ALIGN	TX LINK CONFIG DATA

Default: 00h

D[7:6]	**SERDES TEST PATTERN**	Sets test patterns in the transport layer of the JESD204B interface.
00	Normal operation	
01	Outputs clock pattern:	Output is in a *10101010* pattern
10	Encoded pattern:	Output is *1111111100000000*
11	PRBS sequence:	Output is $2^{15} – 1$
D5	**IDLE SYNC**	Sets the output pattern when SYNC~ is asserted.
0	Sync code is k28.5 (0xBCBC)	
1	Sync code is 0xBC50	
D4	**TESTMODE EN**	Generates a long transport layer test pattern mode according to clause 5.1.63 of the JESD204B specification.
0	Test mode disabled	
1	Test mode enabled	
D3	**FLIP ADC DATA**	
0	Normal operation	
1	Output data order is reversed:	MSB – LSB
D2	**LANE ALIGN**	Inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification.
0	Lane alignment characters are not inserted.	
1	Inserts lane alignment characters	
D1	**FRAME ALIGN**	Inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary, as per section 5.3.3.4 of the JESD204B specification.
0	Frame alignment characters are not inserted.	
1	Inserts frame alignment characters	
D0	**TX LINK CONFIG DATA**	Disables sending the initial link alignment (ILA) sequence when SYNC~ is de-asserted, '0'.
0	ILA enabled	
1	ILA disabled	

8.6.2.15 Register Address 27

Figure 67. Register Address 27

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
27	0	0	0	0	0	0	CTRL K	CTRL F

Default: 00h

D1 **CTRL K** Enables bit for number of frames per multiframe.

0 Default

1 Frames per multiframe can be set in register 2Dh

D0 **CTRL F** Enables bit for number of octets per frame.

0 Default

1 Octets per frame can be specified in register 2Ch

8.6.2.16 Register Address 2B

Figure 68. Register Address 2B

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2B	SCRAMBLE EN	0	0	0	0	0	0	0

Default: 00h

D7 **SCRAMBLE EN** Scramble enable bit in the JESD204B interface

0 Scrambling disabled

1 Scrambling enabled

8.6.2.17 Register Address 2C

Figure 69. Register Address 2C

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME

Default: 00h

D[7:0] **OCTETS PER FRAME** Sets number of octets per frame (F).

0 10x mode using two lanes per ADC

1 20x mode using one lane per ADC

8.6.2.18 Register Address 2D

Figure 70. Register Address 2D

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2D	0	0	0	FRAMES PER MULTIFRAME				

Default: 00h

D[4:0] **FRAMES PER MULTIFRAME** Sets number of frames per multiframe.

After reset, the default settings for frames per multiframe are:

10x K = 16

20x K = 8

For each mode, K should not be set to a lower value.

8.6.2.19 Register Address 30

Figure 71. Register Address 30

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
30	SUBCLASS			0	0	0	0	0

Default: 40h

D[7:5] **SUBCLASS** Sets JESD204B subclass. Note that the default value of these bits after reset is '010', which makes subclass 2 the default class.

000 Subclass 0 Backward compatibility with JESD204A

001 Subclass 1 Deterministic latency using the SYSREF signal

010 Subclass 2 Deterministic latency using SYNC~ detection (default subclass after reset)

8.6.2.20 Register Address 36

Figure 72. Register Address 36

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			

Default: 00h

D7	**SYNC REQ**	Generates a synchronization request.	
0	Normal operation		
1	Generates sync request		
D6	**LMFC RESET MASK**	Mask the LMFC reset coming to digital.	
0	LMFC reset is not masked		
1	Ignores LMFC reset		
D3-D0	**OUTPUT CURRENT SEL**	Changes the JESD output buffer current.	
0000	16 mA	1000	8 mA
0001	15 mA	1001	7 mA
0010	14 mA	1010	6 mA
0011	13 mA	1011	5 mA
0100	20 mA	1100	12 mA
0101	19 mA	1101	11 mA
0110	18 mA	1110	10 mA
0111	17 mA	1111	9 mA

8.6.2.21 Register Address 37

Figure 73. Register Address 37

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

Default: 00h

D[7:5] **LINK LAYER TESTMODE** Generates a pattern according to clause 5.3.3.8.2 of the JESD204B document.

000 Normal ADC data

001 D21.5 (high-frequency jitter pattern)

010 K28.5 (mixed-frequency jitter pattern)

011 Repeats initial lane alignment (generates a K28.5 character and continuously repeats the lane alignment sequences)

100 12-octet RPAT jitter pattern

D4 **LINK LAYER RPAT** Changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100).

0 Normal operation

1 Changes disparity

D[2:0] **PULSE DET MODES** Selects different detection modes for SYSREF (subclass 1) and SYNC (subclass 2).

D2	D1	D0	FUNCTIONALITY
0	Don't care	0	Allows all pulses to reset input clock dividers
1	Don't care	0	Do not allow reset of analog clock dividers
Don't care	0 -> 1 transition	1	Allows one pulse immediately after the 0 -> 1 transition to reset the divider

8.6.2.22 Register Address 38

Figure 74. Register Address 38

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

Default: 00h

D7 **FORCE LMFC COUNT** Forces an LMFC count.

0 Normal operation

1 Enables using a different starting value for the LMFC counter

D[6:2] **LMFC COUNT INIT** SYSREF receives the digital block and resets the LMFC count to '0'.

K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx gets the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.

D[1:0] **RELEASE ILANE SEQ** Delays the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization.

00 0

01 1

10 2

11 3

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A device clock and sysref signal must be provided to the ADC and it is recommended that these are source synchronous (generated from a common source with match trace lengths) if synchronizing multiple ADCs. An example of a device that can be used to generate source synchronous device clock and sysref is the LMK04828. The device clock frequency must be the same frequency as the desired sampling rate. The sysref period is required to be an integer multiple of the period of the multi-frame clock. Consequently, the frequency of sysref must be restricted to (Device Clock Frequency) / (2×n×K),n = 1,2,3… K is set by the value in spi register 0x2D and it ranges from 1 to 32. A large enough K is recommended (greater than 16) to absorb the lane skews and avoid data transmission errors across the JESD204B interface. The sync~ signal is used by the FPGA or ASIC to acknowledge the correct reception of comma characters from the ADC during the JESD204B link initialization process. During normal operation this signal should be logic 1 if there are no errors in the data transmission from the ADC to the FPGA or ASIC.

9.2 Typical Application

In a typical application, such as a dual channel digitizer, the ADS42JB46 is connected to an FPGA or ASIC as shown in Figure 75.

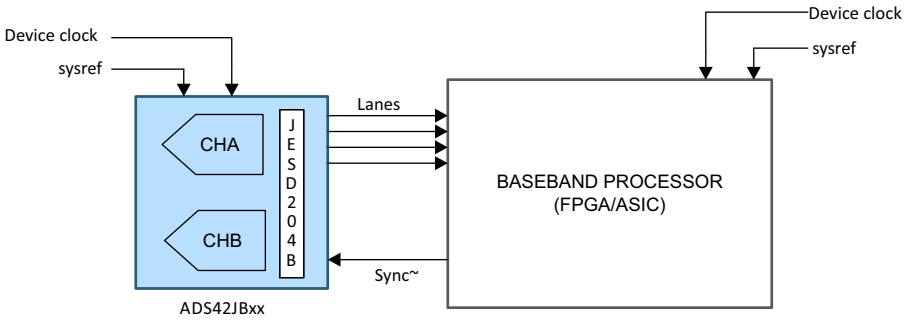


Figure 75. ADS42JBxx in a Dual-Channel Digitizer

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 15 as the input parameters.

Table 15. Design Parameters

PARAMETER	EXAMPLE VALUE
Fsampling	160 MSPS
IF	10 MHz,170 MHz
SNR	>72 dBc
SFDR	>80 dBc
HD2	>90 dBc

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input

The analog input pins have analog buffers (running from the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 4-pF input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

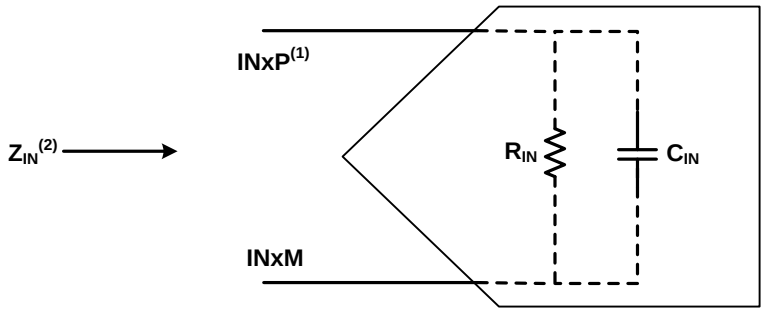
The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V $_{PP}$ differential input swing. When programmed for a 2.5-V $_{PP}$ full-scale, each input pin must swing symmetrically between (VCM + 0.625 V) and (VCM – 0.625 V).

The input sampling circuit has a high 3-dB bandwidth that extends up to 900 MHz (measured with a 50-Ω source driving a 50-Ω termination between INP and INM). The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 250 MHz (with a 2.5-V_{PP} full-scale amplitude) and to approximately 400 MHz (with a 2-V_{PP} full-scale amplitude). This 3-dB bandwidth is different than the analog bandwidth of 900 MHz, which is only an indicator of signal amplitude versus frequency.

9.2.2.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 76, Figure 77, and Figure 78 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} \parallel (1 / j\omega C_{IN})$.

Figure 76. ADC Equivalent Input Impedance

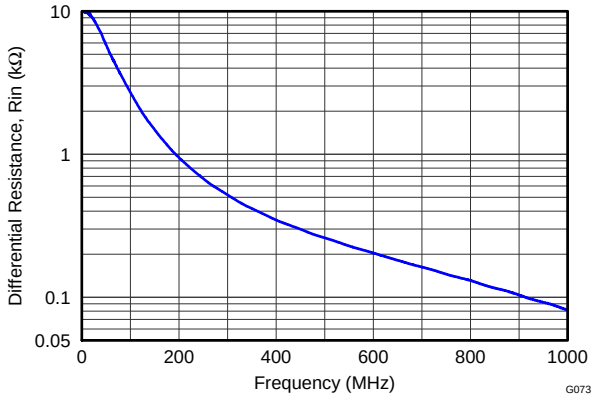


Figure 77. ADC Analog Input Resistance (R_{IN}) Across Frequency

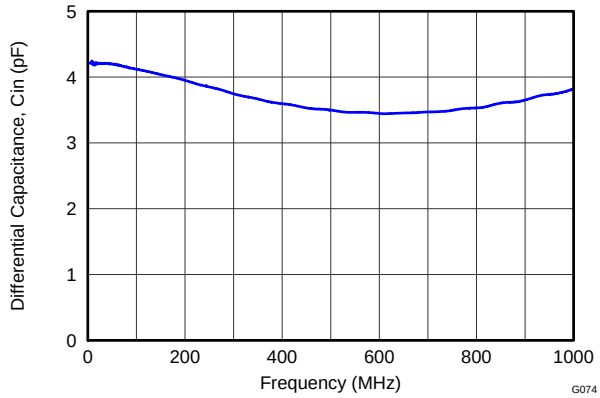


Figure 78. ADC Analog Input Capacitance (C_{IN}) Across Frequency

9.2.2.1.2 Driving Circuit

An example driving circuit configuration is shown in Figure 79. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 79. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage. An additional R-C-R (39 Ω – 6.8 pF – 39 Ω) circuit placed near the device pins helps further improve HD3.

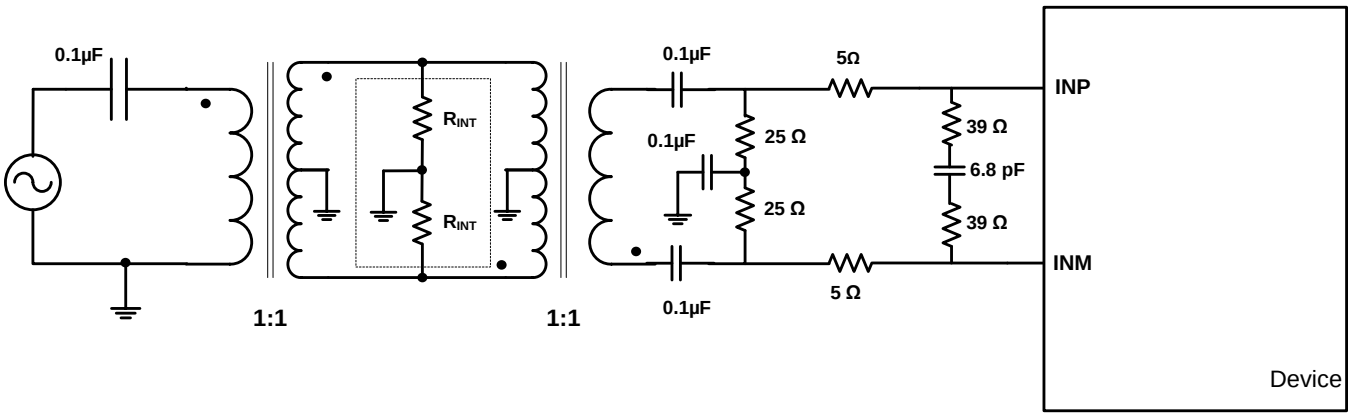


Figure 79. Drive Circuit for Input Frequencies up to 250 MHz

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 79. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance). For high input frequencies (> 250 MHz), the R-C-R circuit can be removed, as indicated in Figure 80.

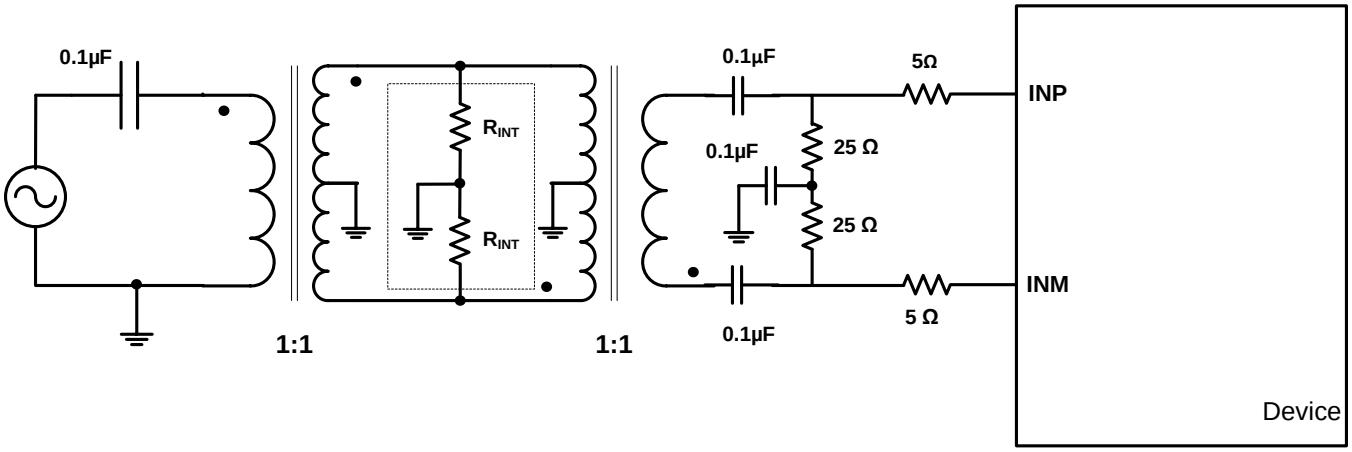
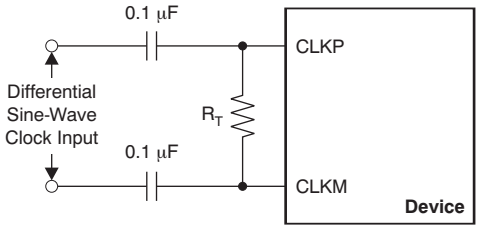


Figure 80. Drive Circuit for Input Frequencies > 250 MHz

9.2.2.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the device can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 81, Figure 82, and Figure 83. Figure 84 details the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 81. Differential Sine-Wave Clock Driving Circuit

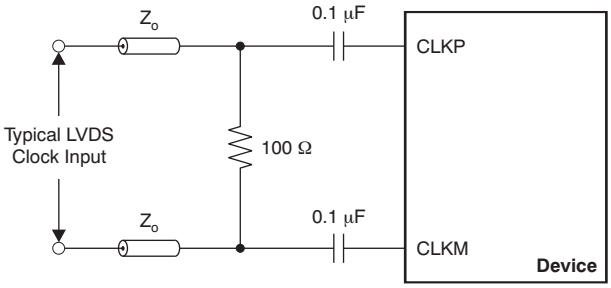


Figure 82. LVDS Clock Driving Circuit

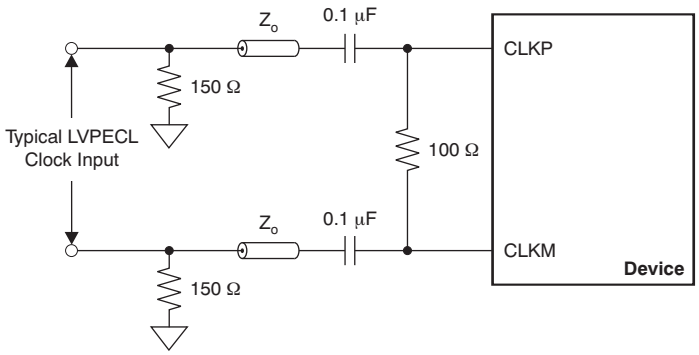
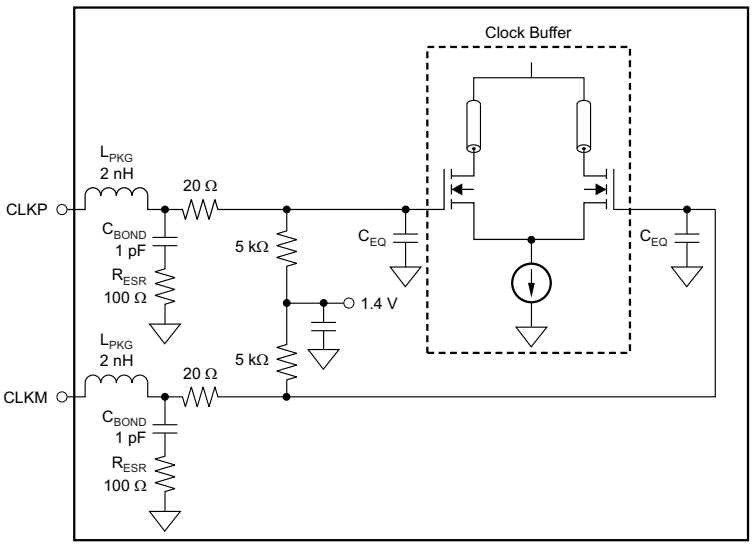


Figure 83. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 84. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 85. However, for best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

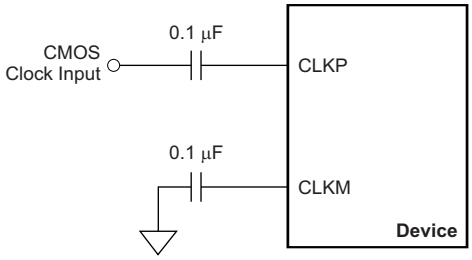


Figure 85. Single-Ended Clock Driving Circuit

9.2.2.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 3. Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (3)$$

SNR limitation is a result of sample clock jitter and can be calculated by Equation 4:

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (4)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter (85 f_S for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by Equation 5:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (5)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an 85-f_S internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure 86.

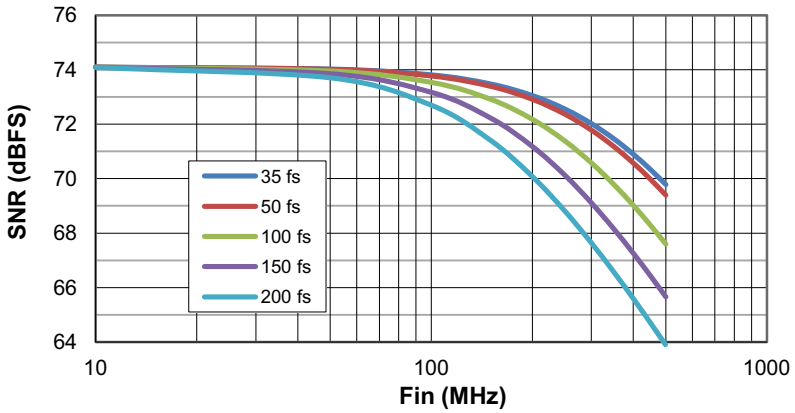


Figure 86. SNR versus Input Frequency and External Clock Jitter

9.2.3 Application Curves

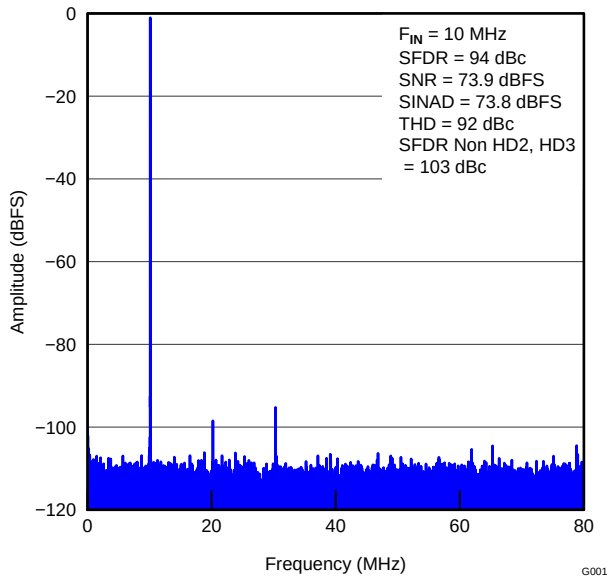


Figure 87. FFT for 10-MHz Input Signal

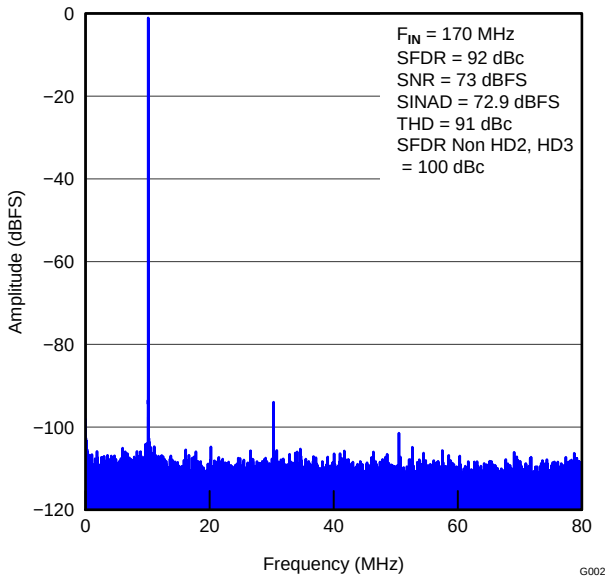


Figure 88. FFT for 170-MHz Input Signal

10 Power Supply Recommendations

Four different power supply rails are required for ADS42JBxx device family:

- 3.3-V AVDD3V is used to supply power to the analog buffers.
- 1.8-V AVDD is used to supply power to the analog core of the ADC.
- 1.8-V DRVDD is used to supply power to the digital core of the ADC.
- 1.8-V IOVDD is used to supply power to the output buffers.

Because of the switching activities on the digital rail, it is recommended to provide the 1.8-V digital and analog supplies from separate sources. Both IOVDD and DRVDD may be supplied from a common source and a ferrite bead is recommended to separate these two supply rails. An example power supply scheme suitable for the ADS42JB46 is shown in Figure 89. In this example supply scheme, AVDD3V, AVDD, DRVDD and IOVDD are supplied from LDOs. To improve on the efficiency of the power supply scheme and to minimize heat dissipation, it is recommended that a DC-DC converter (or switcher) is used before the LDOs if the input voltage is greater than 4.5 V.

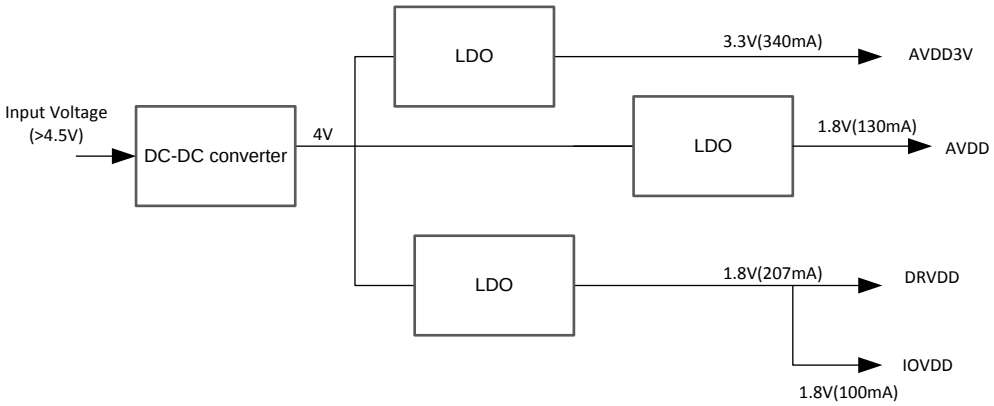


Figure 89. Example Power Supply Scheme

11 Layout

11.1 Layout Guidelines

- The length of the positive and negative traces of a differential pair should be matched to within 2 mils (0.051mm) of each other.
- Each differential pair length should be matched within 10 mils (0.254 mm) of each other.
- When the ADC is used on the same PCB with a digital intensive component such as FPGA or ASIC, separate digital and analog ground planes should be used. These separate ground planes should not overlap to minimize undesired coupling.
- Connect decoupling caps directly to ground and place close to the ADC power pins and the power supply pins to filter high-frequency current transients directly to the ground plane. This is illustrated in Figure 90.
- Ground and power planes should be wide enough to keep the impedance very low. In a multi-layer PCB, one layer each should be dedicated to ground and power planes.
- All high speed serdes traces should be routed straight with minimum curves and bends. Where a bend is necessary, avoid making very sharp right angle bends in the trace.
- FR4 material may be used for the PCB core dielectric up to the maximum 3.125-Gbps bit rate supported by ADS42JBxx device family. Path loss can be compensated for by adjusting the drive strength from the ADS42JBxx using SPI register 0x36.

Layout Guidelines (continued)

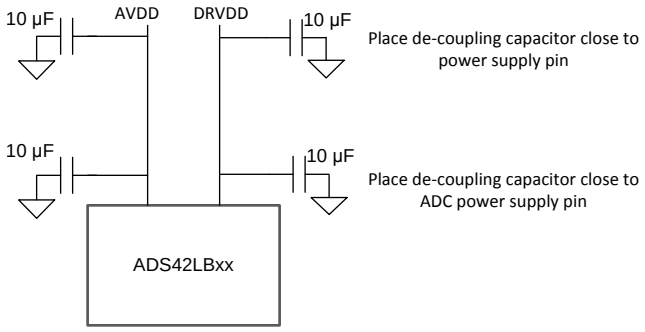


Figure 90. Recommended Placement of Power Supply De-coupling Capacitors

11.2 Layout Example

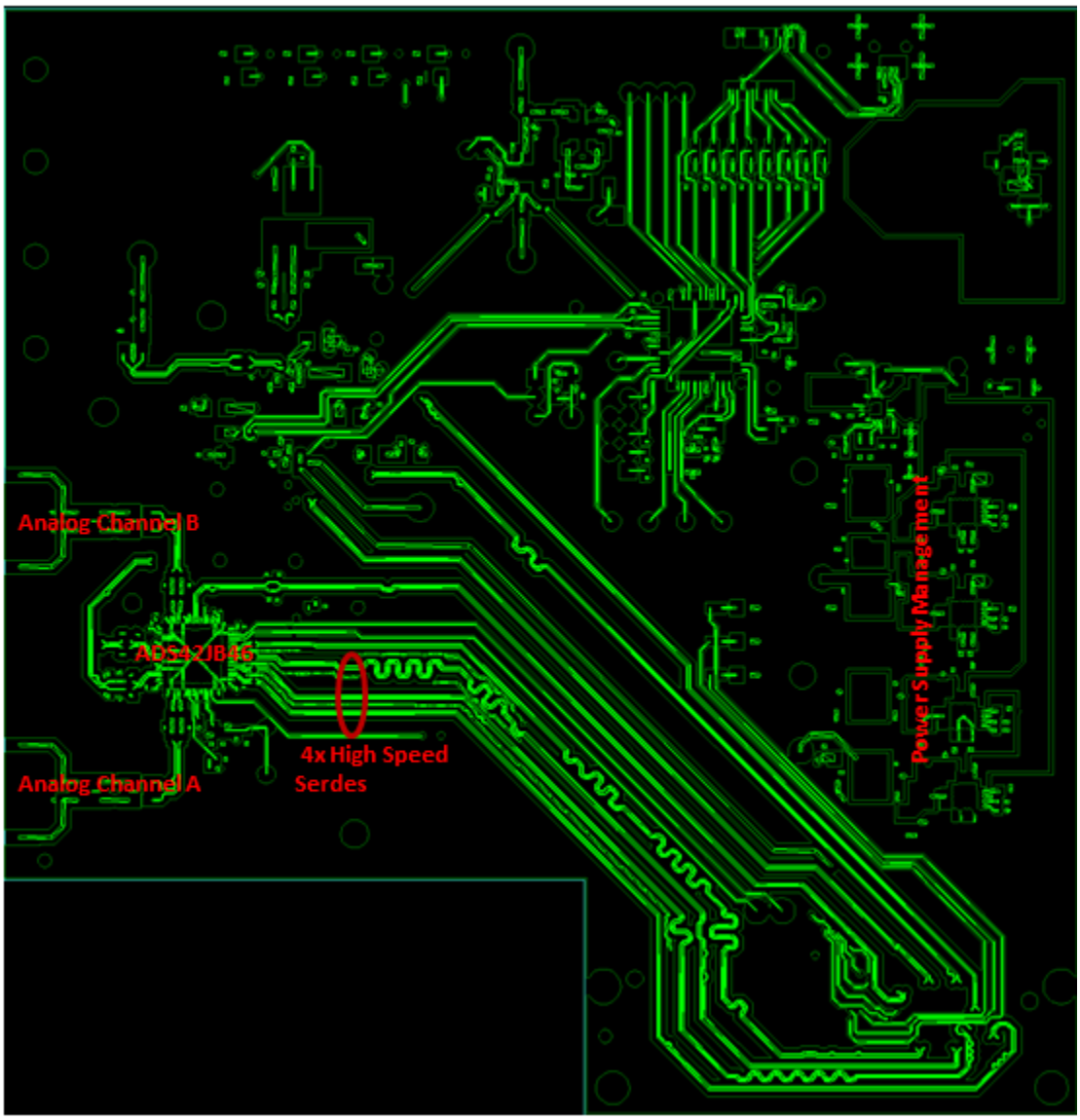


Figure 91. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS42JB46IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB46	Samples
ADS42JB46IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB46	Samples
ADS42JB46IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB46	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

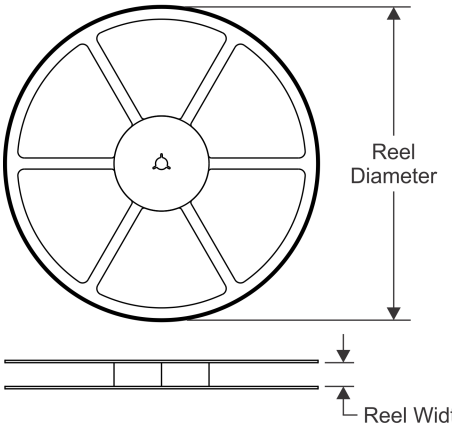
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

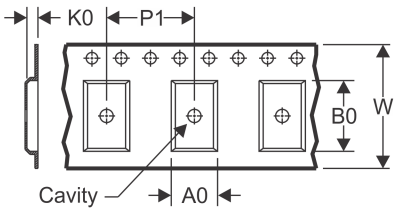
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

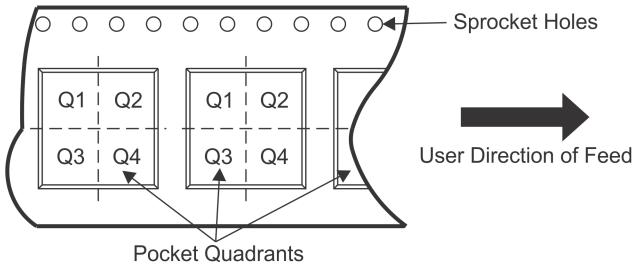


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

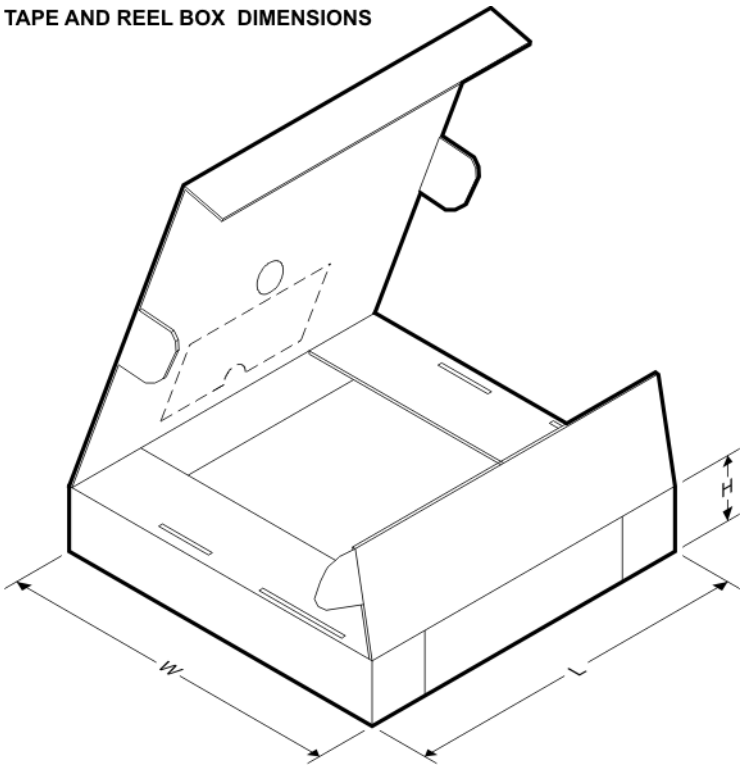
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS42JB46IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42JB46IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

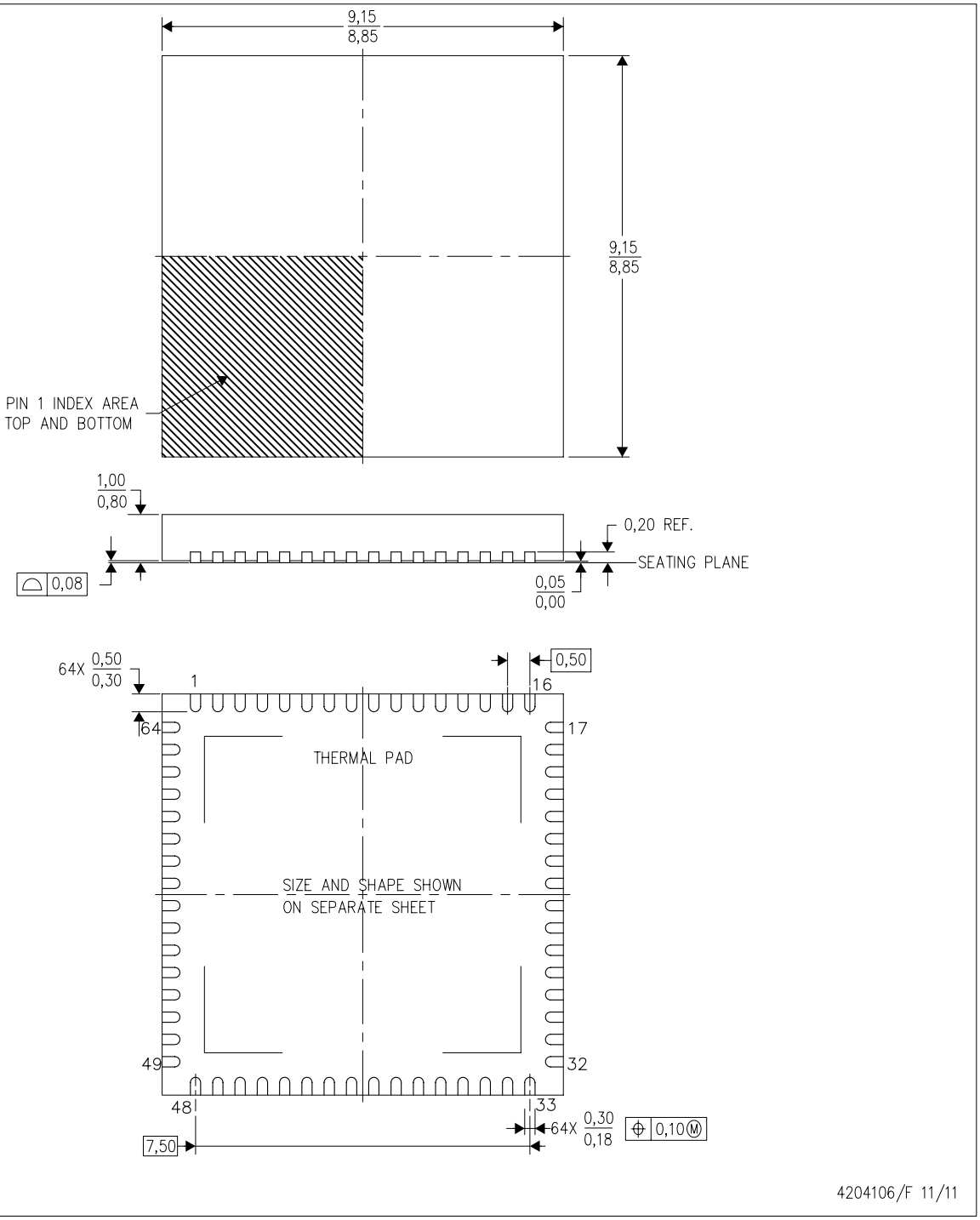
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS42JB46IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42JB46IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

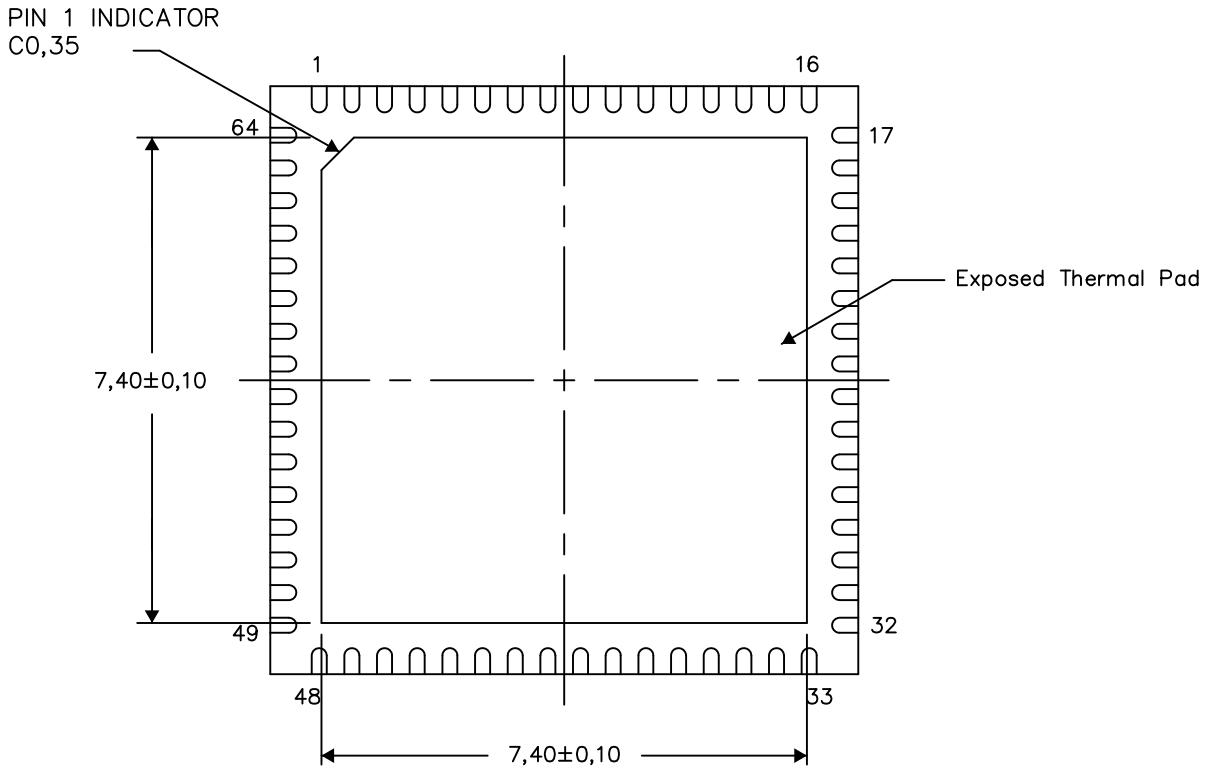
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



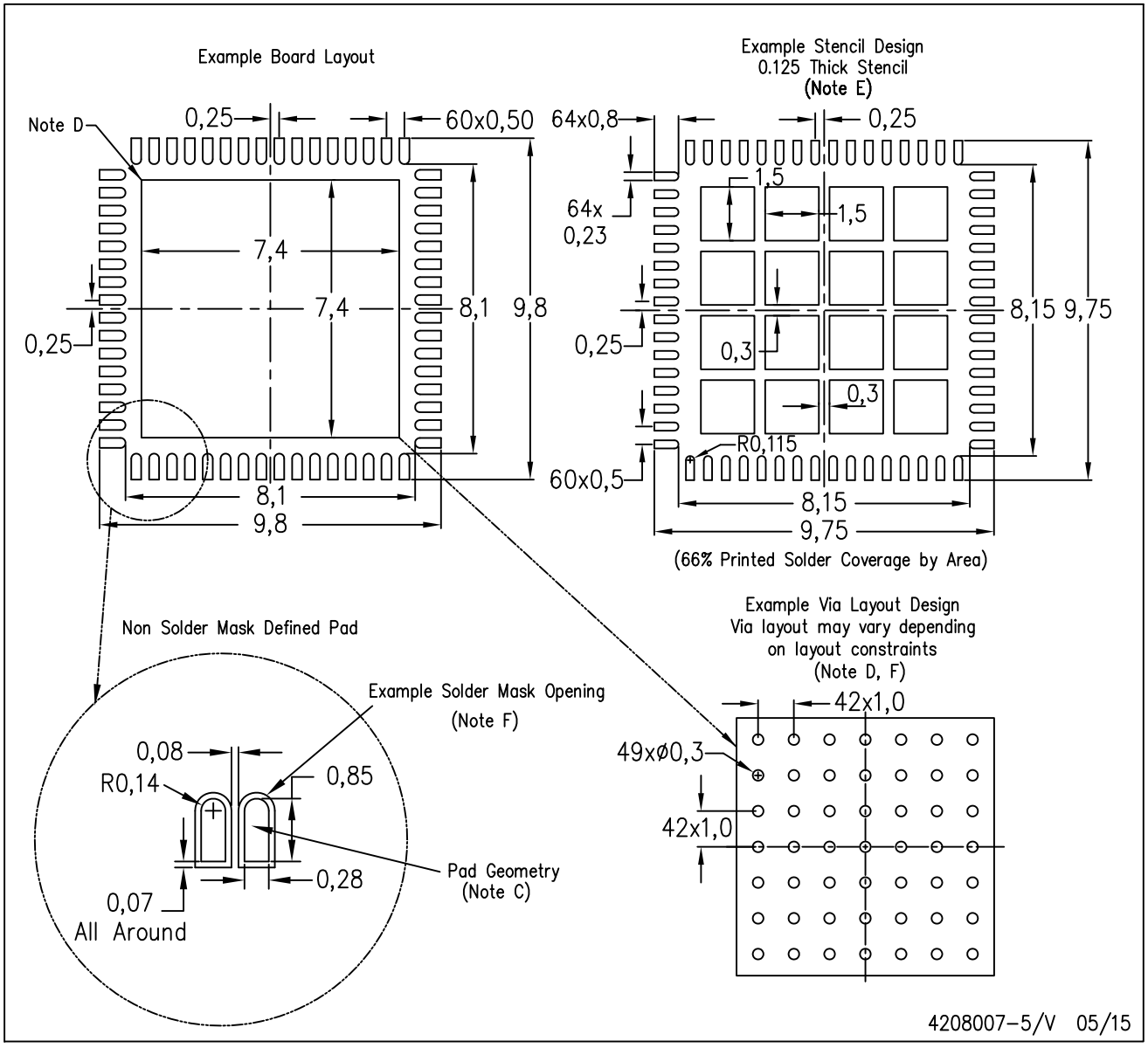
Bottom View

Exposed Thermal Pad Dimensions

4206192–4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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