

# CSD95372BQ5M Synchronous Buck NexFET™ Smart Power Stage

## 1 Features

- 60 A Continuous Operating Current Capability
- 93.4% System Efficiency at 30 A
- Low Power Loss of 2.8 W at 30 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Mode With FCCM
- Temperature Compensated Bi-Directional Current Sense
- Analog Temperature Output (600 mV at 0°C)
- Fault Monitoring
  - High-Side Short, Overcurrent, and Overtemperature Protection
- 3.3 and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Diode
- Optimized Deadtime for Shoot Through Protection
- High-Density SON 5 × 6 mm Footprint
- Ultra-Low Inductance Package
- System Optimized PCB Footprint
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

## 2 Applications

- Multiphase Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low-Duty Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR11.x / VR12.x V-Core and Memory Synchronous Converters

## 3 Description

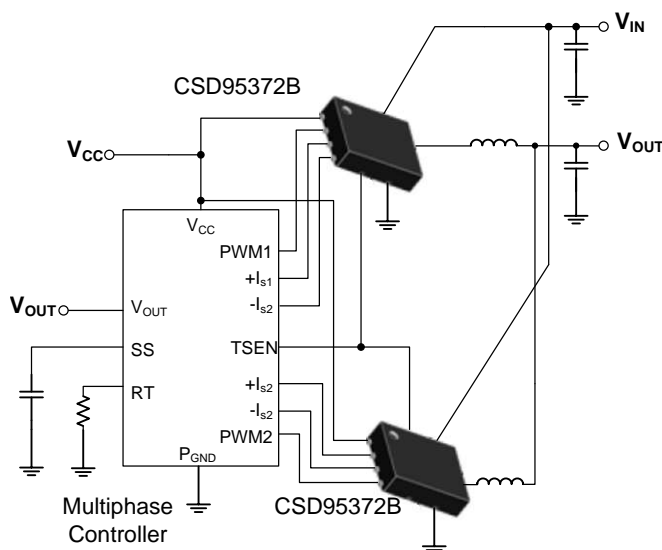
The CSD95372BQ5M NexFET™ smart power stage is a highly optimized design for use in a high-power, high-density Synchronous Buck converter. This product integrates the Driver IC and Power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing system and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

### Device Information<sup>(1)</sup>

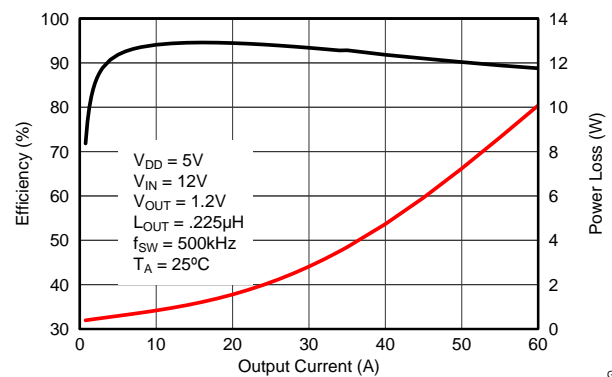
Device	Media	Qty	Package	Ship
CSD95372BQ5M	13-Inch Reel	2500	SON 5 mm × 6 mm Package	Tape and Reel
CSD95372BQ5MT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss



G001



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 4 6.1 Absolute Maximum Ratings ..... 4 6.2 Handling Ratings..... 4 6.3 Recommended Operating Conditions..... 4 6.4 Thermal Information ..... 4	<b>7 Application Schematic</b> ..... 5 <b>8 Device and Documentation Support</b> ..... 6 8.1 Trademarks ..... 6 8.2 Electrostatic Discharge Caution ..... 6 8.3 Glossary ..... 6 <b>9 Mechanical, Packaging, and Orderable Information</b> ..... 7 9.1 Mechanical Drawing..... 7 9.2 Recommended PCB Land Pattern..... 8 9.3 Recommended Stencil Opening ..... 8
---	--

## 4 Revision History

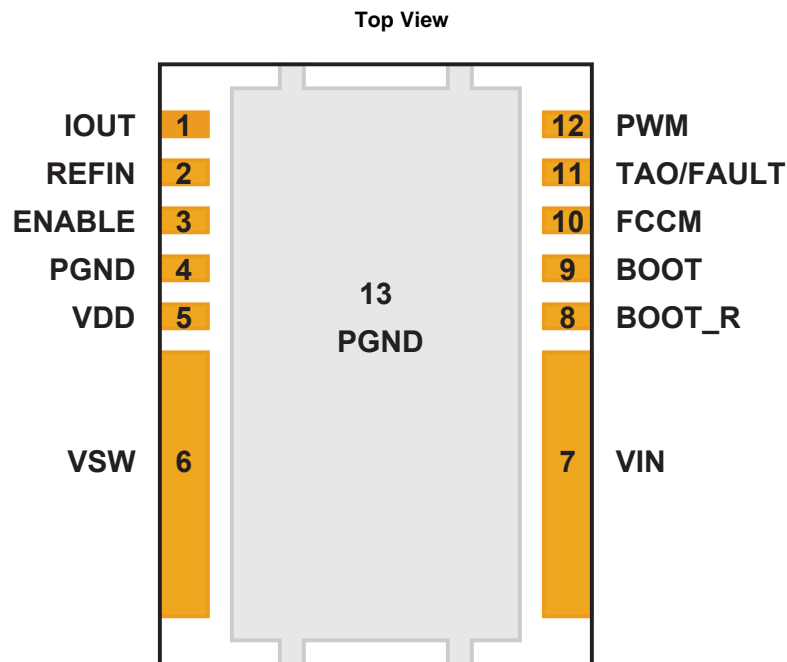
### Changes from Revision A (June 2014) to Revision B Page

- Changed application schematic to show  $I_{OUT}$  (not  $I_{MON}$ ) for each CSD95372B device. .... 5

### Changes from Original (March 2014) to Revision A Page

- Removed "input voltage up to 14.5 V" and "DualCool™ package" bullets from the Features ..... 1
- Fixed TAO/FAULT pin function to state that TAO will be pulled up to 3.3 V in the event of thermal shutdown ..... 3
- Added minimum ESD Ratings ..... 4
- Increased maximum input voltage to 16 V ..... 4
- Added table note for max input voltage ..... 4

## 5 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
BOOT	9	Bootstrap capacitor connection. Connect a minimum of 0.1 $\mu$ F 16 V X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
BOOT_R	8	Return path for HS gate driver, connected to $V_{SW}$ internally.
ENABLE	3	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100-k $\Omega$ pulldown resistor will pull the ENABLE pin LOW if left floating.
FCCM	10	This pin enables the Diode Emulation function. When this pin is held LOW, Diode Emulation Mode is enabled for sync FET. When FCCM is HIGH, the device is operated in Forced Continuous Conduction Mode. An internal 5 $\mu$ A current source will pull the FCCM pin to 3.3 V if left floating.
IOUT	1	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
P <sub>GND</sub>	4	Power ground, connected directly to pin 13.
P <sub>GND</sub>	13	Power ground
PWM	12	Pulse width modulated 3-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the 3-state shutdown hold-off time ( $t_{3HT}$ ).
REFIN	2	External reference voltage input for current sensing amplifier
TAO/ FAULT	11	Temperature Analog Output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the IC's. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P <sub>GND</sub> with a 1-nF 16-V X7R ceramic capacitor.
V <sub>DD</sub>	5	Supply voltage to gate driver and internal circuitry
V <sub>IN</sub>	7	Input voltage pin. Connect input capacitors close to this pin.
V <sub>SW</sub>	6	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
$V_{IN}$ to $P_{GND}$	-0.3	25	V
$V_{IN}$ to $V_{SW}$	-0.3	25	V
$V_{IN}$ to $V_{SW}$ (10 ns)	-7	27	V
$V_{SW}$ to $P_{GND}$	-0.3	20	V
$V_{SW}$ to $P_{GND}$ (10 ns)	-7	23	V
$V_{DD}$ to $P_{GND}$	-0.3	7	V
ENABLE, PWM, FCCM, TAO, IOOUT, REFIN to $P_{GND}$	-0.3	$V_{DD} + 0.3\text{ V}$	V
BOOT to BOOT_R <sup>(2)</sup>	-0.3	$V_{DD} + 0.3\text{ V}$	V
$P_D$ , power dissipation		12	W
$T_J$ , operating junction	-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Should not exceed 7 V

### 6.2 Handling Ratings

	MIN	MAX	UNIT	
$T_{stg}$ Storage temperature range	-55	150	$^\circ\text{C}$	
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM)	-2000	2000	V
	Charged device model (CDM)	-500	500	V

### 6.3 Recommended Operating Conditions

 $T_A = 25^\circ$  (unless otherwise noted)

	MIN	MAX	UNIT
$V_{DD}$ Gate drive voltage	4.5	5.5	V
$V_{IN}$ Input supply voltage <sup>(1)</sup>		16	V
$V_{OUT}$ Output voltage		5.5	V
$I_{OUT}$ Continuous output current	$V_{IN} = 12\text{ V}, V_{DD} = 5\text{ V}, V_{OUT} = 1.2\text{ V},$ $f_{SW} = 500\text{ kHz}, L_{OUT} = 0.225\text{ }\mu\text{H}$ <sup>(2)</sup>	60	
$I_{OUT-PK}$ Peak output current <sup>(3)</sup>		90	A
$f_{SW}$ Switching frequency	$C_{BST} = 0.1\text{ }\mu\text{F}$ (min)	1250	kHz
On-time duty cycle	$f_{SW} = 1\text{ MHz}$	85	%
Minimum PWM on-time		40	ns
Operating temperature	-40	125	$^\circ\text{C}$

- (1) Operating at high  $V_{IN}$  can create excessive AC voltage overshoots on the switch node ( $V_{SW}$ ) during MOSFET switching transients. For reliable operation, the switch node ( $V_{SW}$ ) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
- (2) Measurement made with six 10  $\mu\text{F}$  (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across  $V_{IN}$  to  $P_{GND}$  pins.
- (3) System conditions as defined in Note 1. Peak output current is applied for  $t_p = 50\text{ }\mu\text{s}$ .

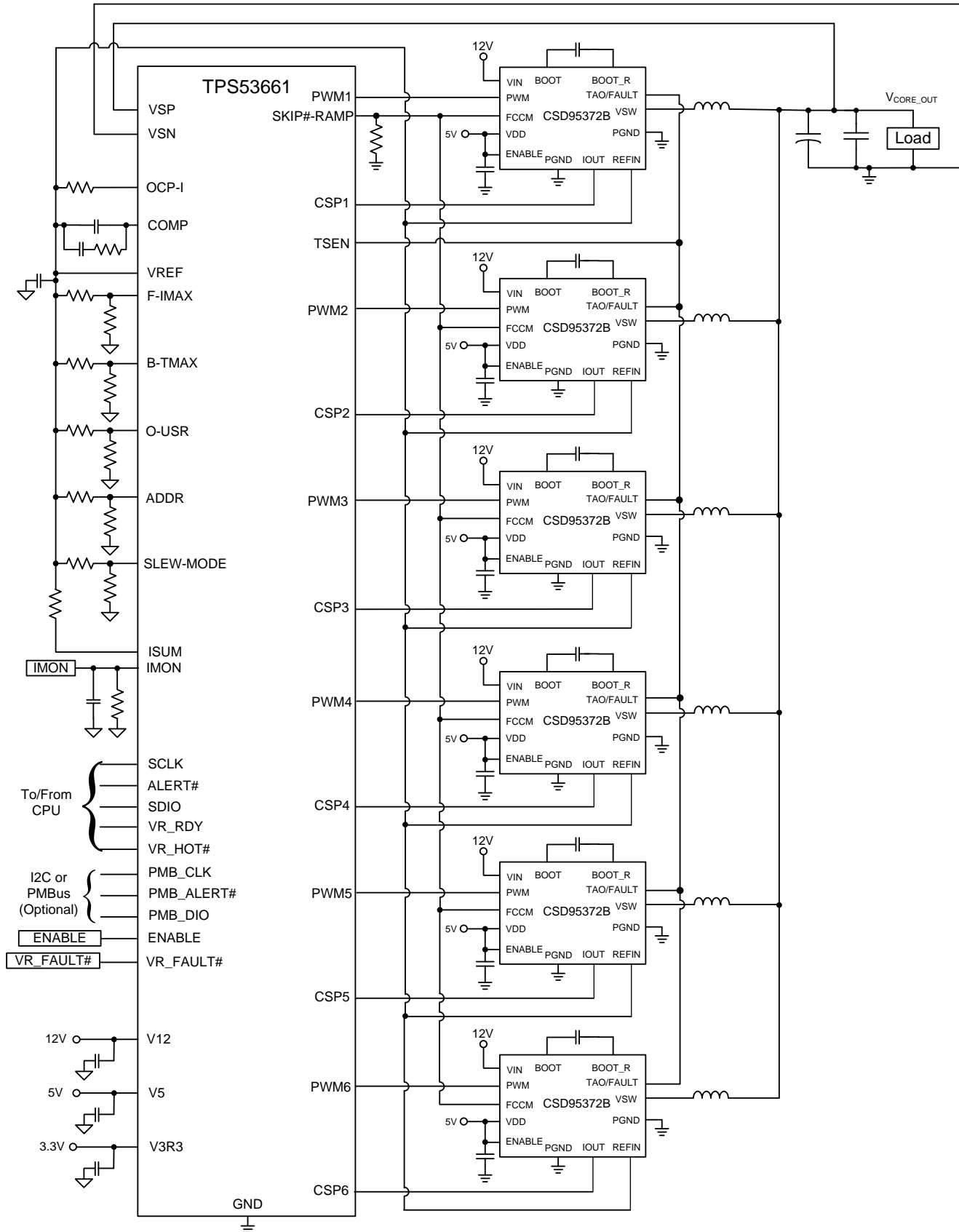
### 6.4 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) <sup>(1)</sup>			15	$^\circ\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance <sup>(2)</sup>			1.5	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz (0.071 mm thick) Cu pad on a 1.5 inches x 1.5 inches, 0.06 inch (1.52 mm) thick FR4 board.
- (2)  $R_{\theta JB}$  value based on hottest board temperature within 1 mm of the package.

## 7 Application Schematic



## 8 Device and Documentation Support

### 8.1 Trademarks

NexFET, DualCool are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 8.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.3 Glossary

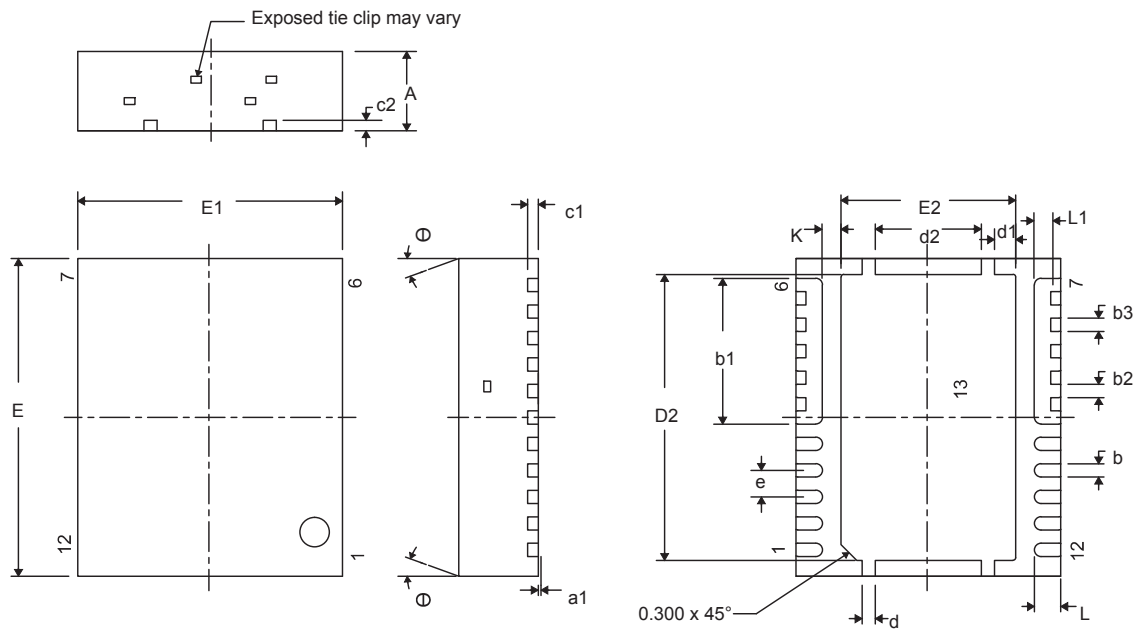
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

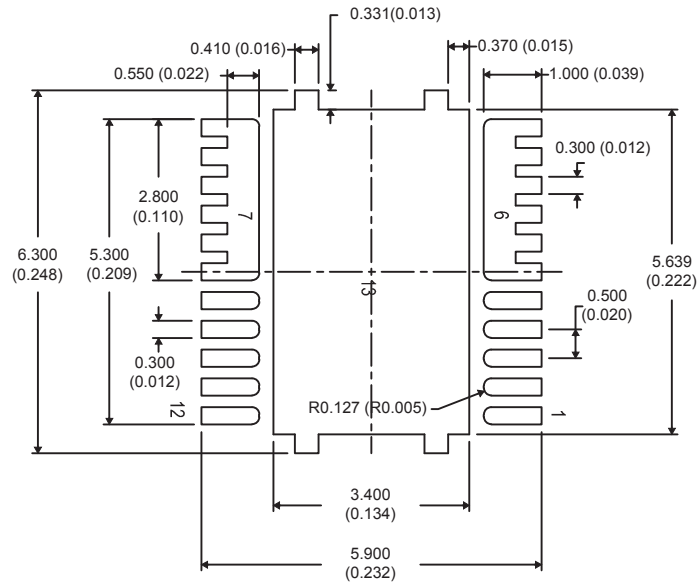
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 9.1 Mechanical Drawing



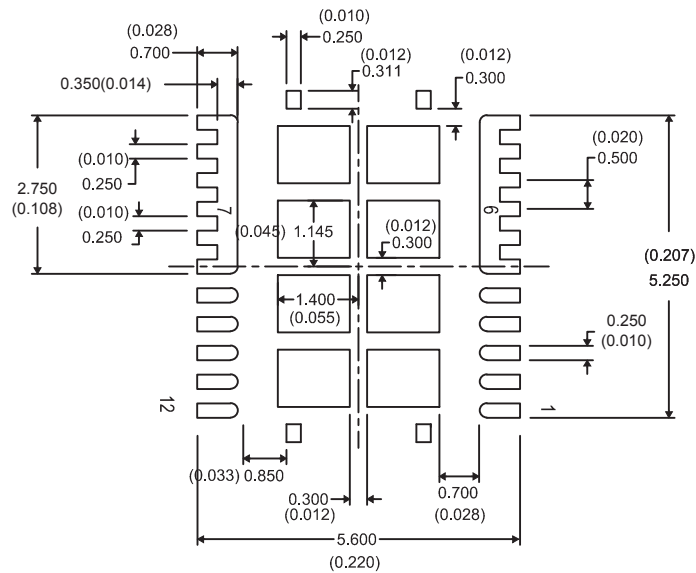
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.400	1.450	1.500	0.057	0.059	0.061
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1	2.750 TYP			0.108 TYP		
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3	0.250 TYP			0.010 TYP		
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e	0.500 TYP			0.020 TYP		
K	0.350 TYP			0.014 TYP		
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

## 9.2 Recommended PCB Land Pattern



1. Dimensions are in mm (inches).

## 9.3 Recommended Stencil Opening



1. Dimensions are in mm (inches).
2. Stencil thickness is 100  $\mu\text{m}$ .



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95372BQ5M	ACTIVE	LSON-CLIP	DQP	12	2500	Pb-Free (RoHS Exempt)	CU NIPDAU   CU SN	Level-2-260C-1 YEAR	-55 to 150	95372BM	<a href="#">Samples</a>
CSD95372BQ5MT	ACTIVE	LSON-CLIP	DQP	12	250	Pb-Free (RoHS Exempt)	CU NIPDAU   CU SN	Level-2-260C-1 YEAR	-55 to 150	95372BM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95372BQ5M	LSON-CLIP	DQP	12	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
CSD95372BQ5M	LSON-CLIP	DQP	12	2500	330.0	15.4	5.3	6.3	1.8	8.0	12.0	Q1
CSD95372BQ5MT	LSON-CLIP	DQP	12	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95372BQ5M	LSON-CLIP	DQP	12	2500	367.0	367.0	35.0
CSD95372BQ5M	LSON-CLIP	DQP	12	2500	336.6	336.6	41.3
CSD95372BQ5MT	LSON-CLIP	DQP	12	250	210.0	185.0	35.0

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.