TEXAS INSTRUMENTS

DRV8805

SLVSAW3D – JULY 2011 – REVISED JANUARY 2016

DRV8805 Unipolar Stepper Motor Driver IC

1 Features

- 4-Channel Protected Low-Side Driver
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes
- Indexer/Translator for Unipolar Stepper Motors
  - Simple Step/Direction Interface
  - Three Step Modes (2-Phase Full-Step, 1-2-Phase Half-Step, 1-Phase Wave Drive)
- DW Package: 1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)
- PWP Package: 2-A (Single Channel On) / 1-A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- 8.2-V to 60-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package

2 Applications

- Gaming Machines
- General Unipolar Stepper Motor Drivers

3 Description

The DRV8805 provides an integrated solution for driving unipolar stepper motors. It includes four low-side drivers with overcurrent protection and provides built-in diodes to clamp turnoff transients generated by the motor windings.

Indexer logic to control a unipolar stepper motor using a simple step/direction interface is also integrated. Three stepping modes are supported: 2 phase (full-step), 1-2 phase (half-step), and 1-phase (wave drive).

In the SOIC (DW) package, the DRV8805 can supply up to 1.5-A (one channel on) or 800-mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, it can supply up to 2-A (one channel on) or 1-A (four channels on) continuous output current per channel, at 25°C with proper PCB heatsinking.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, under voltage lockout, and overtemperature, and faults are indicated by a fault output pin.

The DRV8805 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8805	SOIC (20)	12.80 mm x 7.50 mm
	HTSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
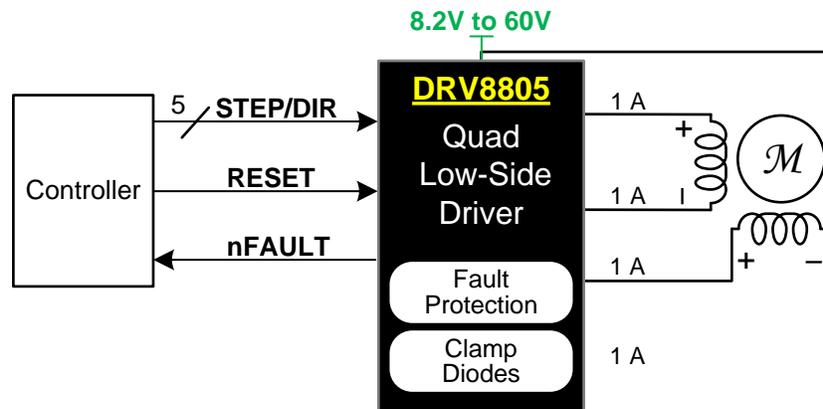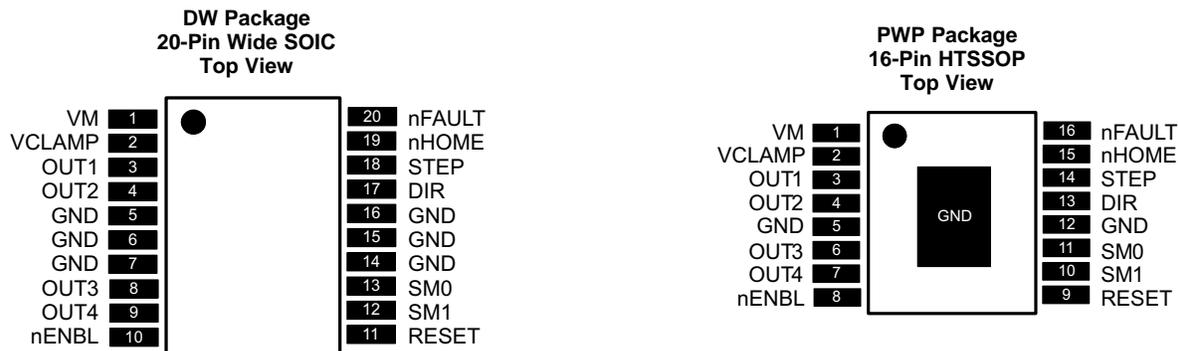
Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2012) to Revision D   **Page**

- Changed Catch Diodes to Clamp Diodes in *Features* 1

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

- Updated the text in the EXTERNAL COMPONENTS OR CONNECTIONS column for nHOME row 3

- Updated PARAMETERS, TEST CONDTIONS, MIN, TYP, and MAX values in the nHOME OUTPUT section in the *Electrical Characteristics* table 5

5 Pin Configuration and Functions

DW Package
20-Pin Wide SOIC
Top View

```
           VM    1        20   nFAULT
        VCLAMP   2        19   nHOME
          OUT1   3        18   STEP
          OUT2   4        17   DIR
           GND   5        16   GND
           GND   6        15   GND
           GND   7        14   GND
          OUT3   8        13   SM0
          OUT4   9        12   SM1
         nENBL  10        11   RESET
```

PWP Package
16-Pin HTSSOP
Top View

```
           VM    1        16   nFAULT
        VCLAMP   2        15   nHOME
          OUT1   3        14   STEP
          OUT2   4    GND  13   DIR
           GND   5        12   GND
          OUT3   6        11   SM0
          OUT4   7        10   SM1
         nENBL   8         9   RESET
```

Pin Functions

PIN			I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC	HTSSOP			
POWER AND GROUND					
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	—	Device ground	All pins must be connected to GND.
VM	1	1	—	Device power supply	Connect to motor supply (8.2 V to 60 V).
CONTROL					
DIR	17	13	I	Direction input	Level controls direction of rotation – internal pulldown
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
SM0	13	11	I	Step mode	Sets step mode – see step modes section for details – internal pulldowns
SM1	12	10			
STEP	18	14	I	Step input	Rising edge advances motor to next step – internal pulldown
STATUS					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
nHOME	19	15	OD	Home	Logic low when indexer is at home position – push-pull structure
OUTPUT					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	—	Output clamp voltage	Connect to VM supply, or Zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
VM	Power supply voltage	−0.3	65	V
VOUTx	Output voltage	−0.3	65	V
VCLAMP	Clamp voltage	−0.3	65	V
	Digital input pin voltage	−0.5	7	V
nHOME, nFAULT	Digital output pin voltage	−0.5	−0.5 to 7	V
nHOME, nFAULT	Output current		20	mA
	Peak clamp diode current		2	A
	DC or RMS clamp diode current		1	A
	Peak motor drive output current, t < 1 µS	Internally limited		A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_M	Power supply voltage	8.2		60	V
V_{CLAMP}	Output clamp voltage [1]	0		60	V
I_{OUT}	Continuous output current, single channel on, T_A = 25°C, SOIC package[2]			1.5	A
	Continuous output current, four channels on, T_A = 25°C, SOIC package[2]			0.8	
	Continuous output current, single channel on, T_A = 25°C, HTSSOP package[2]			2	
	Continuous output current, four channels on, T_A = 25°C, HTSSOP package[2]			1	

(1) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC[1]		DRV8805		UNIT
		DW (SOIC)	PWP (HTSSOP)	
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	39.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	20.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS(SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	−20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
nHOME OUTPUT (OPEN-DRAIN OUTPUT WITH WEAK INTERNAL PULLUP)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output high voltage	I_O = 100 µA, V_M = 11 V – 60 V, peak			6.5	V
		I_O = 100 µA, V_M = 11 V – 60 V, steady state	3.3	4.5	5.6	
		I_O = 100 µA, V_M = 8.2 V – 11 V, steady state	2.5			
I_{SRC}	Output source current	V_M = 24 V			1	mA
I_{SNK}	Output sink current	V_M = 24 V			5	mA
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
I_{OFF}	Off-state leakage current		−50		50	µA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	−50		50	µA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns

Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		µs
t_{RETRY}	Overcurrent protection retry time			1.2		ms
t_{TSD}	Thermal shutdown temperature	Die temperature[1]	150	160	180	°C

(1) Not production tested.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
1	f_{STEP}	Step frequency			250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9			µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9			µs
4	$t_{SU(STEP)}$	Setup time, DIR, SMx to STEP rising	1			µs
5	$t_{H(STEP)}$	Hold time, DIR, SMx to STEP rising	1			µs
6	$t_{OE(ENABLE)}$	Enable time, nENBL to output low			50	ns
7	$t_{PD(L-H)}$	Propagation delay time, STEP to OUTx, low to high			500	ns
8	$t_{PD(H-L)}$	Propagation delay time, STEP to OUTx, high to low			500	ns
—	t_{RESET}	RESET pulse width	20			µs

(1) Not production tested.
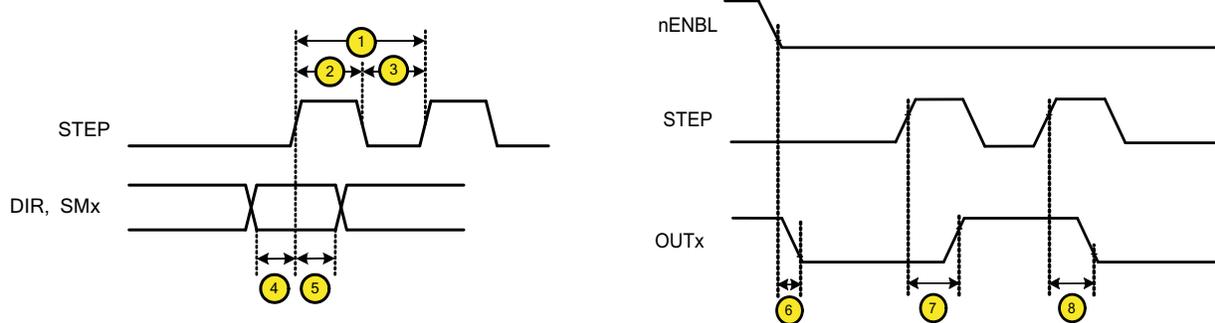

Figure 1. DRV8805 Timing Requirements

Product Folder Links: *DRV8805*

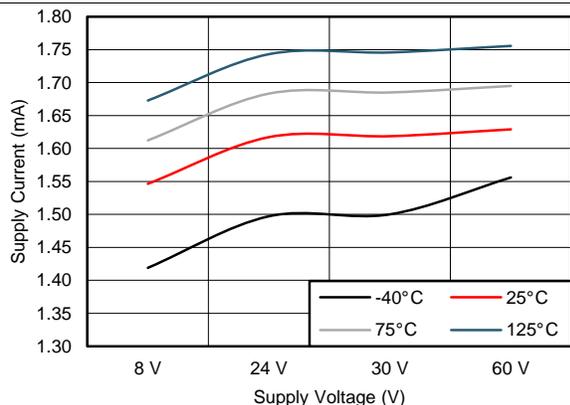## 6.7 Typical Characteristics

Figure 2. Supply Current Over V$_M$
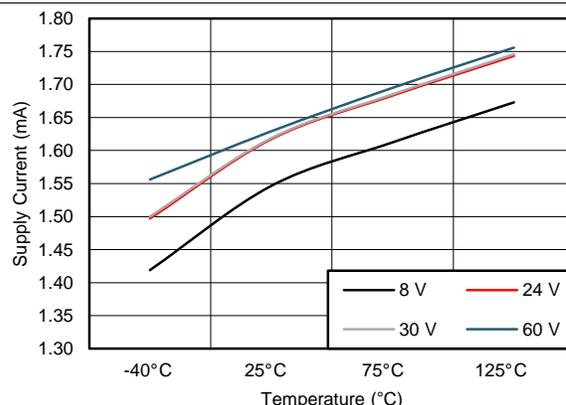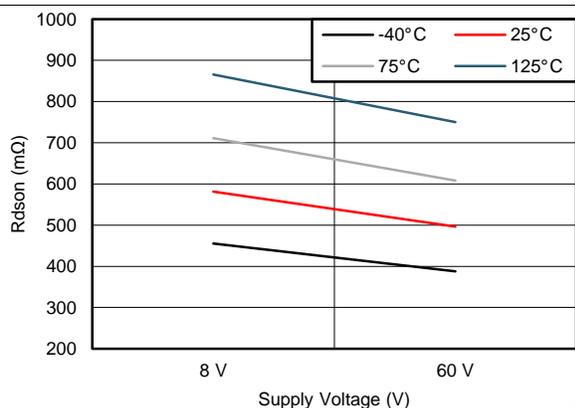

Figure 3. Supply Current Over Temperature
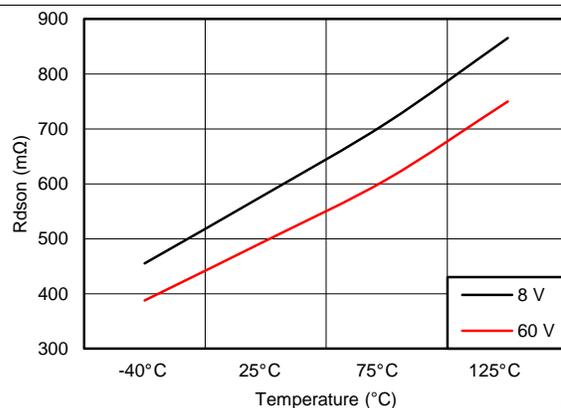

Figure 4. R$_{DS(ON)}$ Over V$_M$

Figure 5. R$_{DS(ON)}$ Over Temperature

7 Detailed Description

7.1 Overview

The DRV8805 is an integrated 4-channel unipolar stepper motor driver with a step / direction interface that controls the low-side driver outputs and allows for simple control schemes. The four low-side driver outputs consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500 mΩ. A single motor supply input VM serves as device power and is internally regulated to power the low-side gate drive. The device outputs can be disabled by bringing the nENBL pin logic high. This device has several safety features including integrated overcurrent protection that limits the motor current to a fixed maximum above which the device will shut down. Thermal shutdown protection enables the device to automatically shut down if the die temperature exceeds a TTSD limit and will restart once the die reaches a safe temperature. UVLO protection will disable all circuitry in the device if VM drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram

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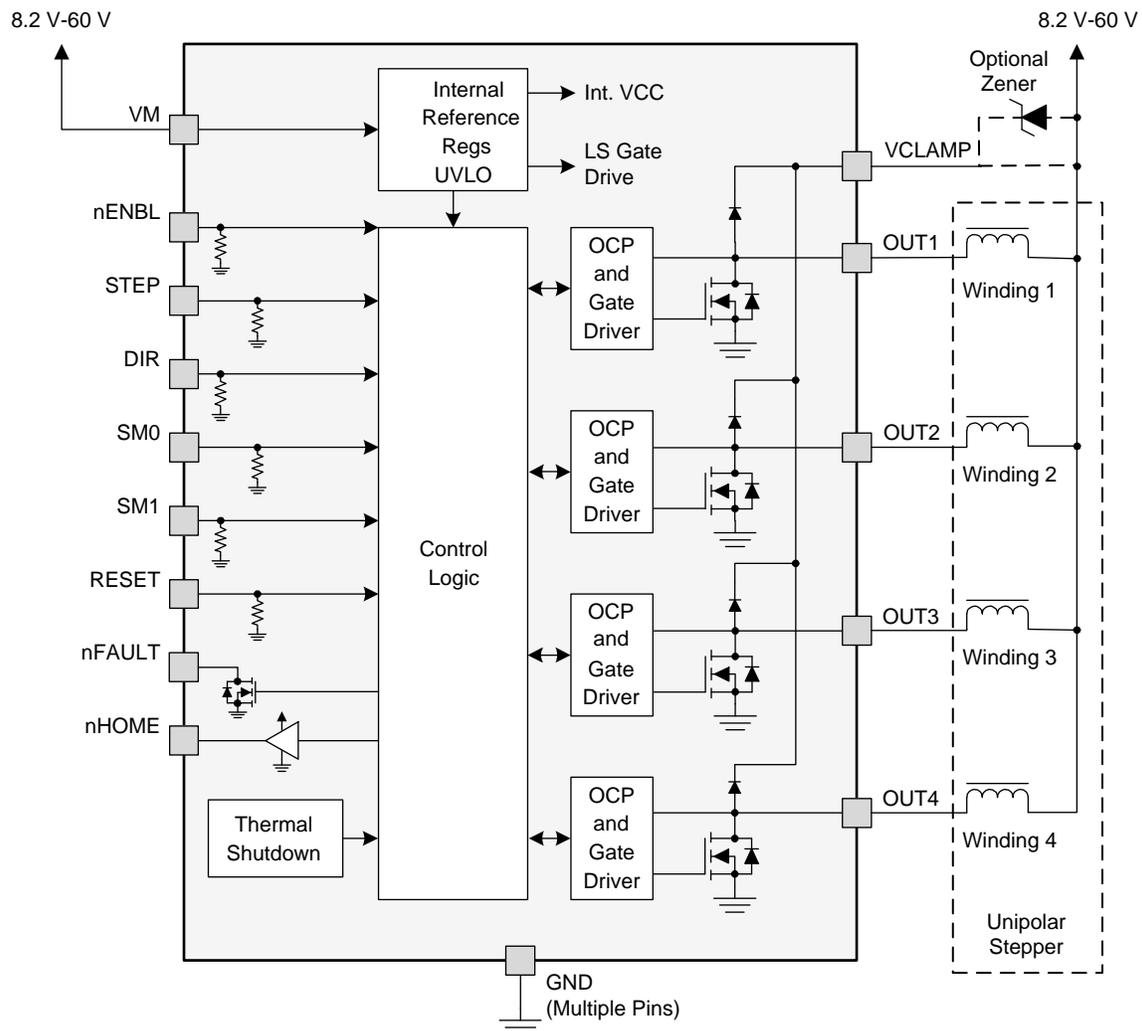
7.3 Feature Description

7.3.1 Output Drivers

The DRV8805 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a Zener or TVS diode to V_M, allowing the switch voltage to exceed the main supply voltage V_M. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Indexer Operation

The DRV8805 integrates an indexer to allow motor control with a simple step-and-direction interface. Logically, the indexer is shown in Figure 6.
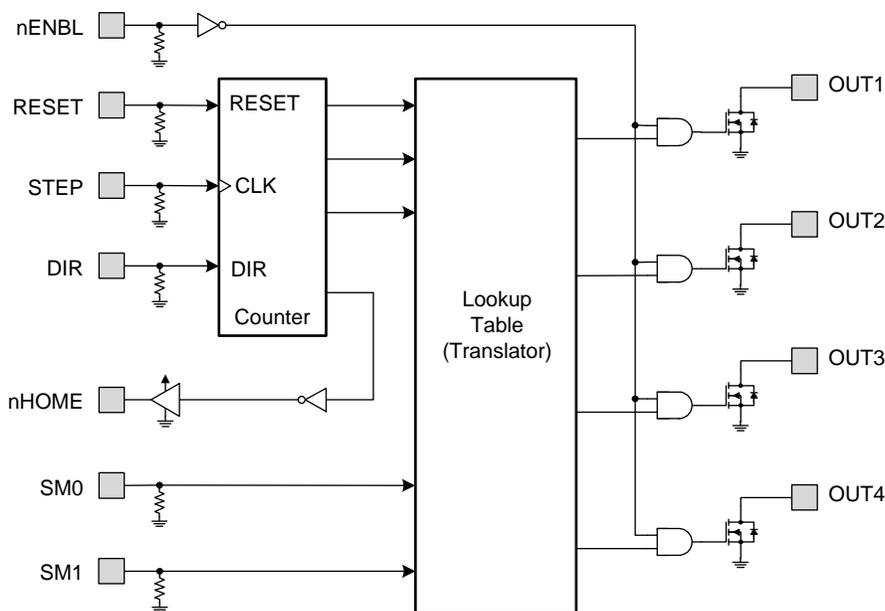

Figure 6. Indexer Operation

7.3.3 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets the internal logic. The indexer is reset to the home state. All inputs are ignored while RESET is active. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power up.

7.3.4 Protection Circuits

The DRV8805 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 μs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or V_M is removed and re-applied.

Feature Description (continued)

7.3.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. The STEP input will be ignored. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the V_M pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Step Modes

The SM0 and SM1 pins select the stepping mode of the translator as shown in Table 1.

Table 1. Step Modes

SM1	SM0	MODE
0	0	2-phase drive (full step)
0	1	1-2 phase drive (half step)
1	0	1-phase excitation (wave drive)
1	1	Reserved

In all modes, during a fault condition, the STEP input will be ignored. See *Protection Circuits* for more information.

The sequence of the outputs is shown in Table 2, Table 3, and Table 4.

Table 2. 2-Phase Excitation (Full-Step)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	ON
CW	2	0	1	↑	1	ON	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	ON	ON	OFF
CW	4	0	1	↑	1	OFF	OFF	ON	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	ON
CCW	4	0	0	↑	1	OFF	OFF	ON	ON
CCW	3	0	0	↑	1	OFF	ON	ON	OFF
CCW	2	0	0	↑	1	ON	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	ON
Hold	X	0	X	‾↑	no chg	no chg	no chg	no chg	no chg

Product Folder Links: *DRV8805*

Table 3. 1-2-Phase Excitation (Half-Step)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	OFF
CW	2	0	1	↑	1	ON	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	ON	OFF	OFF
CW	4	0	1	↑	1	OFF	ON	ON	OFF
CW	5	0	1	↑	1	OFF	OFF	ON	OFF
CW	6	0	1	↑	1	OFF	OFF	ON	ON
CW	7	0	1	↑	1	OFF	OFF	OFF	ON
CW	8	0	1	↑	1	ON	OFF	OFF	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	OFF
CCW	8	0	0	↑	1	ON	OFF	OFF	ON
CCW	7	0	0	↑	1	OFF	OFF	OFF	ON
CCW	6	0	0	↑	1	OFF	OFF	ON	ON
CCW	5	0	0	↑	1	OFF	OFF	ON	OFF
CCW	4	0	0	↑	1	OFF	ON	ON	OFF
CCW	3	0	0	↑	1	OFF	ON	OFF	OFF
CCW	2	0	0	↑	1	ON	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	OFF
Hold	X	0	X	$\overline{\uparrow}$	no chg	no chg	no chg	no chg	no chg

Table 4. 1-Phase Excitation (Wave Drive)

Function	Step	RESET	DIR	STEP	nHOME	OUT1	OUT2	OUT3	OUT4
Reset	1	1	X	X	0	ON	OFF	OFF	OFF
CW	2	0	1	↑	1	OFF	ON	OFF	OFF
CW	3	0	1	↑	1	OFF	OFF	ON	OFF
CW	4	0	1	↑	1	OFF	OFF	OFF	ON
CW to home	1	0	1	↑	0	ON	OFF	OFF	OFF
CCW	4	0	0	↑	1	OFF	OFF	OFF	ON
CCW	3	0	0	↑	1	OFF	OFF	ON	OFF
CCW	2	0	0	↑	1	OFF	ON	OFF	OFF
CCW to home	1	0	0	↑	0	ON	OFF	OFF	OFF
Hold	X	0	X	$\overline{\uparrow}$	no chg	no chg	no chg	no chg	no chg

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8805 can be used to drive one unipolar stepper motor.

8.2 Typical Application
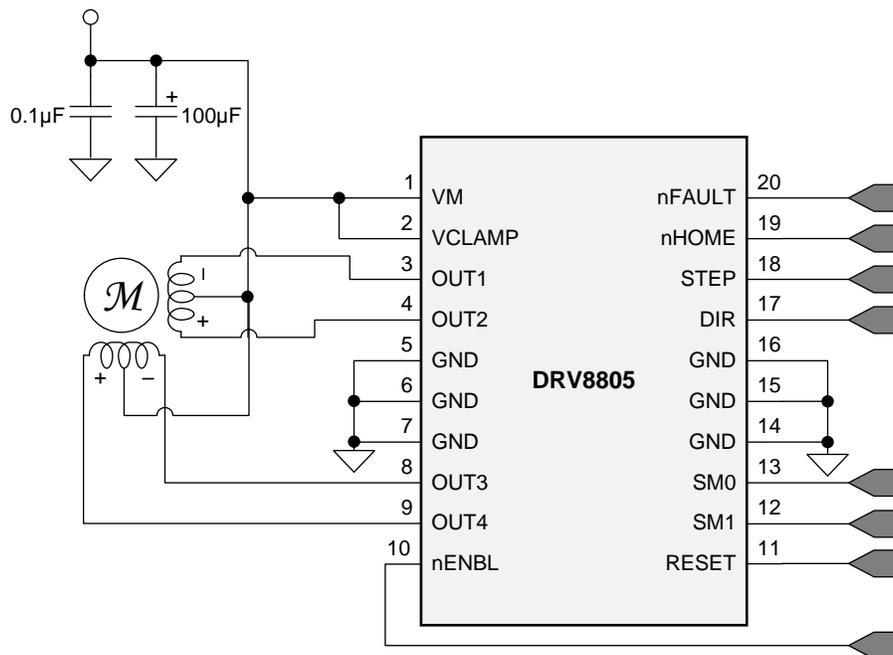
Figure 7. Typical Application Schematic

8.2.1 Design Requirements

Table 5 lists the design parameters for this design example.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24 V
Motor Winding Resistance	R_L	7.4 Ω/phase
Motor Full Step Angle	θstep	1.8°/step
Motor Rated Current	I_{RATED}	0.75 A
PWM frequency	f_{PWM}	31.25 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

Product Folder Links: *DRV8805*

8.2.2.2 Drive Current

The current path is starts from the supply V_M, moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in the following equation.

$$P = I^2 \times R_{DS(on)} \tag{1}$$

The DRV8805 has been measured to be capable of 1.5-A Single Channel or 800-mA Four Channels with the DW package and 2-A Single Channel or 1-A Four Channels with the PWP package at 25°C on standard FR-4 PCBs. The maximum RMS current will vary based on PCB design and the ambient temperature.

8.2.3 Application Curves
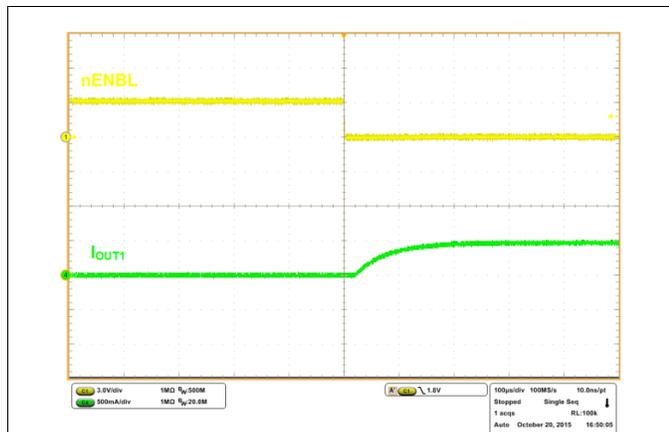
Figure 8. Current Ramp With a 16-Ω, 1-mH, R_L Load and V_M = 8.2 V
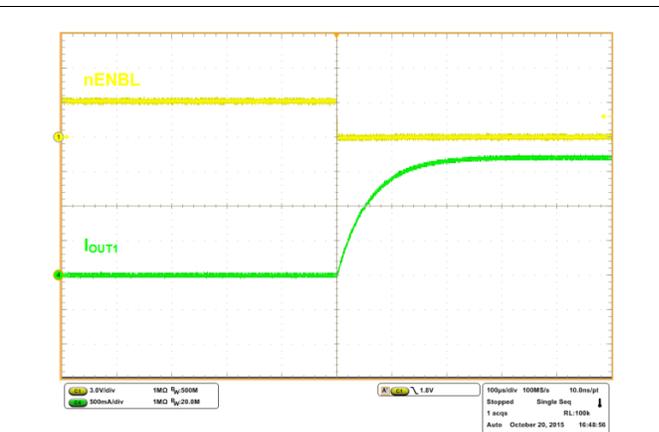
Figure 9. Current Ramp With a 16-Ω, 1-mH R_L Load and V_M = 30 V
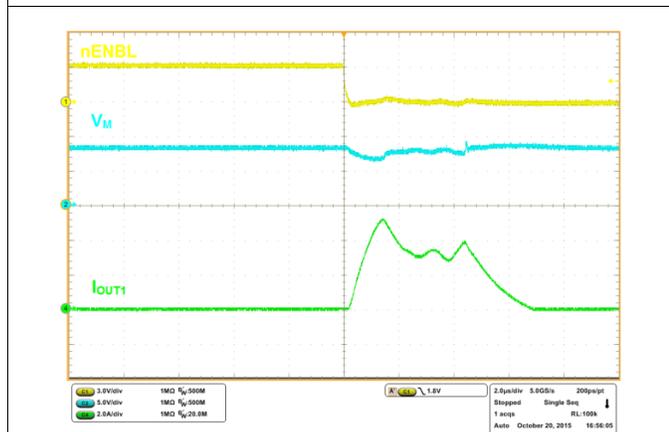
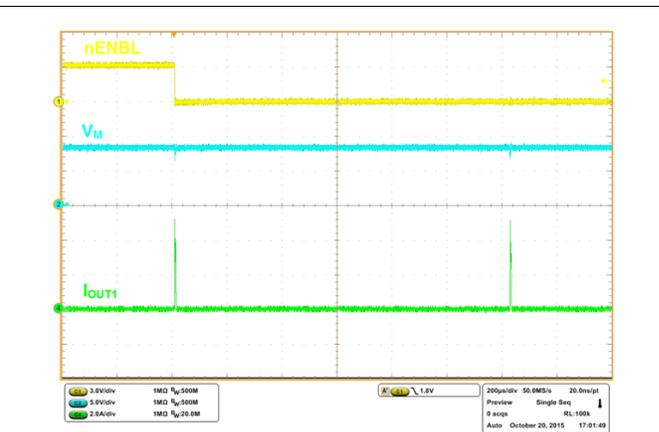**Figure 10. OCP With 8.2 V and OUT1 Shorted to V_M**

Figure 11. OCP Separated by t_{RETRY} With V_M = 8.2 V and OUT1 Shorted to V_M

Product Folder Links: *DRV8805*

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:
- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.
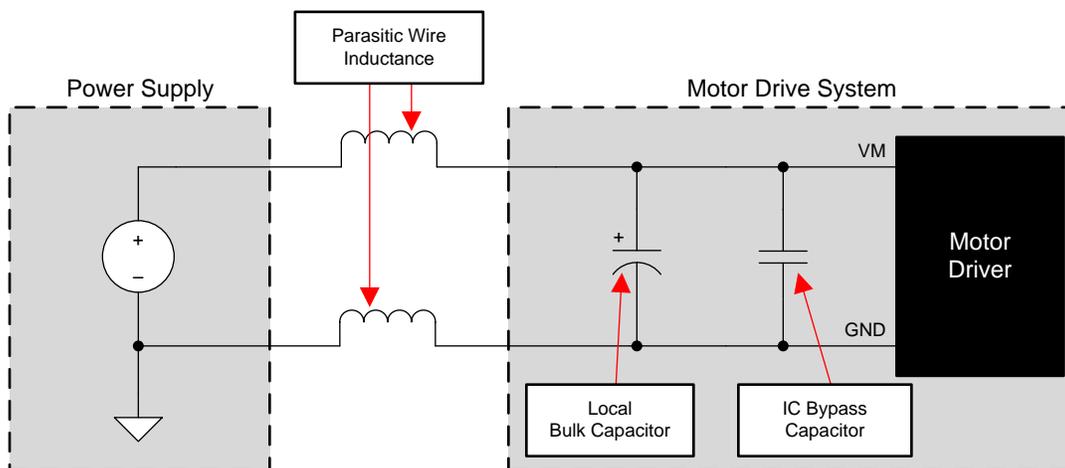

Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

- Small-value capacitors should be ceramic, and placed closely to device pins.
- The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.
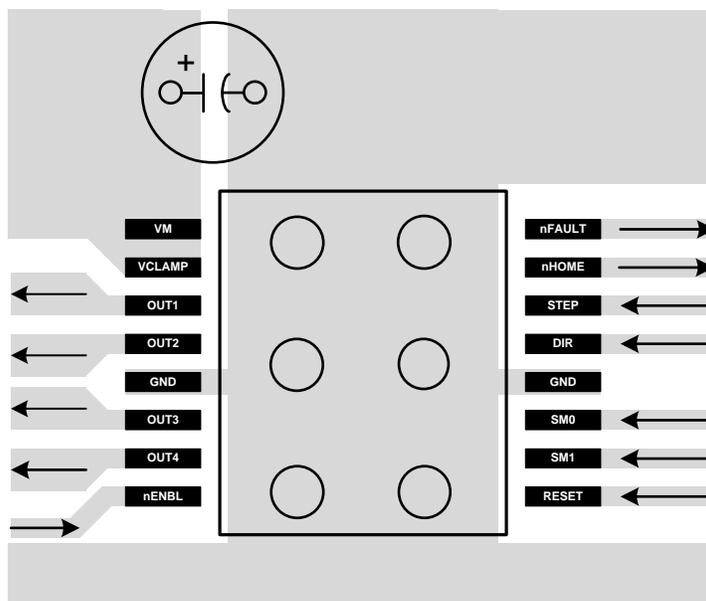
10.2 Layout Example

Figure 13. Example Layout Drawing

10.3 Thermal Considerations

The DRV8805 has thermal shutdown (TSD) as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Thermal Considerations (continued)

10.3.1 Power Dissipation

Power dissipation in the DRV8805 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 2.

$$P = R_{DS(ON)} \bullet (I_{OUT})^2$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load   (2)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The DRV8805DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8805PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI Application Report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:
- *PowerPAD™ Thermally Enhanced Package*, SLMA002.
- *PowerPAD Made Easy*, SLMA004.

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8805DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8805DW	Samples
DRV8805DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8805DW	Samples
DRV8805PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8805	Samples
DRV8805PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8805	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
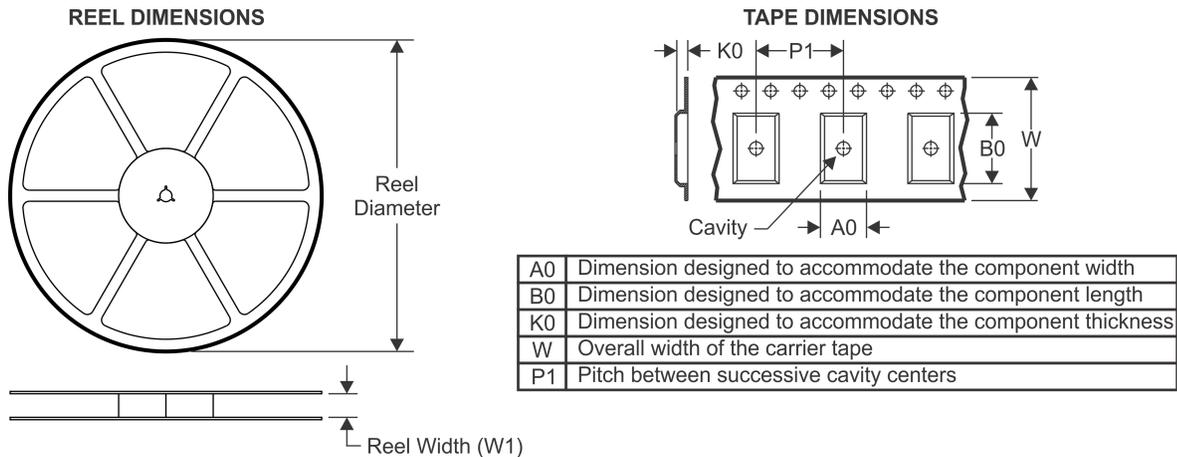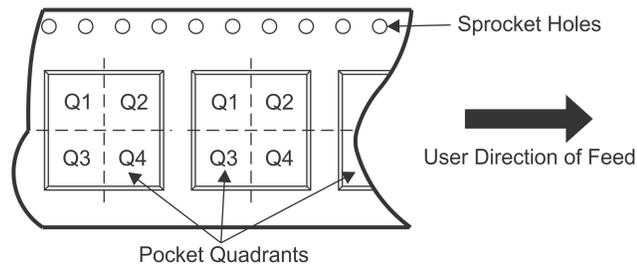
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8805DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV8805PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
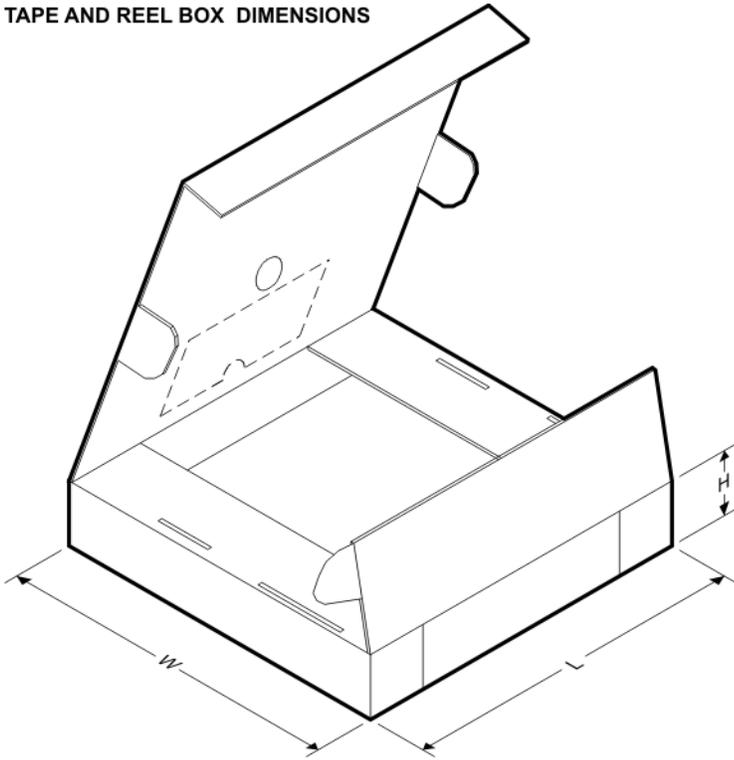
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8805DWR	SOIC	DW	20	2000	367.0	367.0	45.0
DRV8805PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
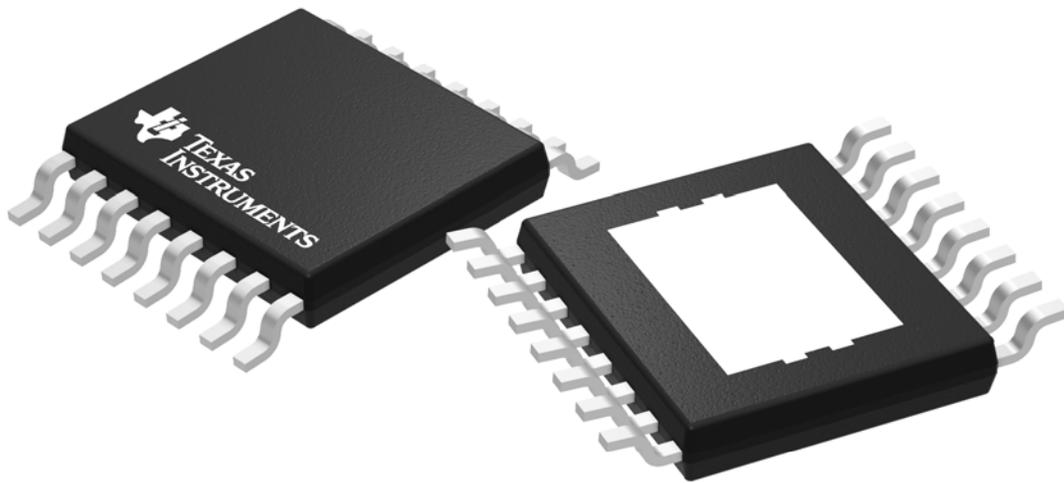
Images above are just a representation of the package family, actual package may vary.
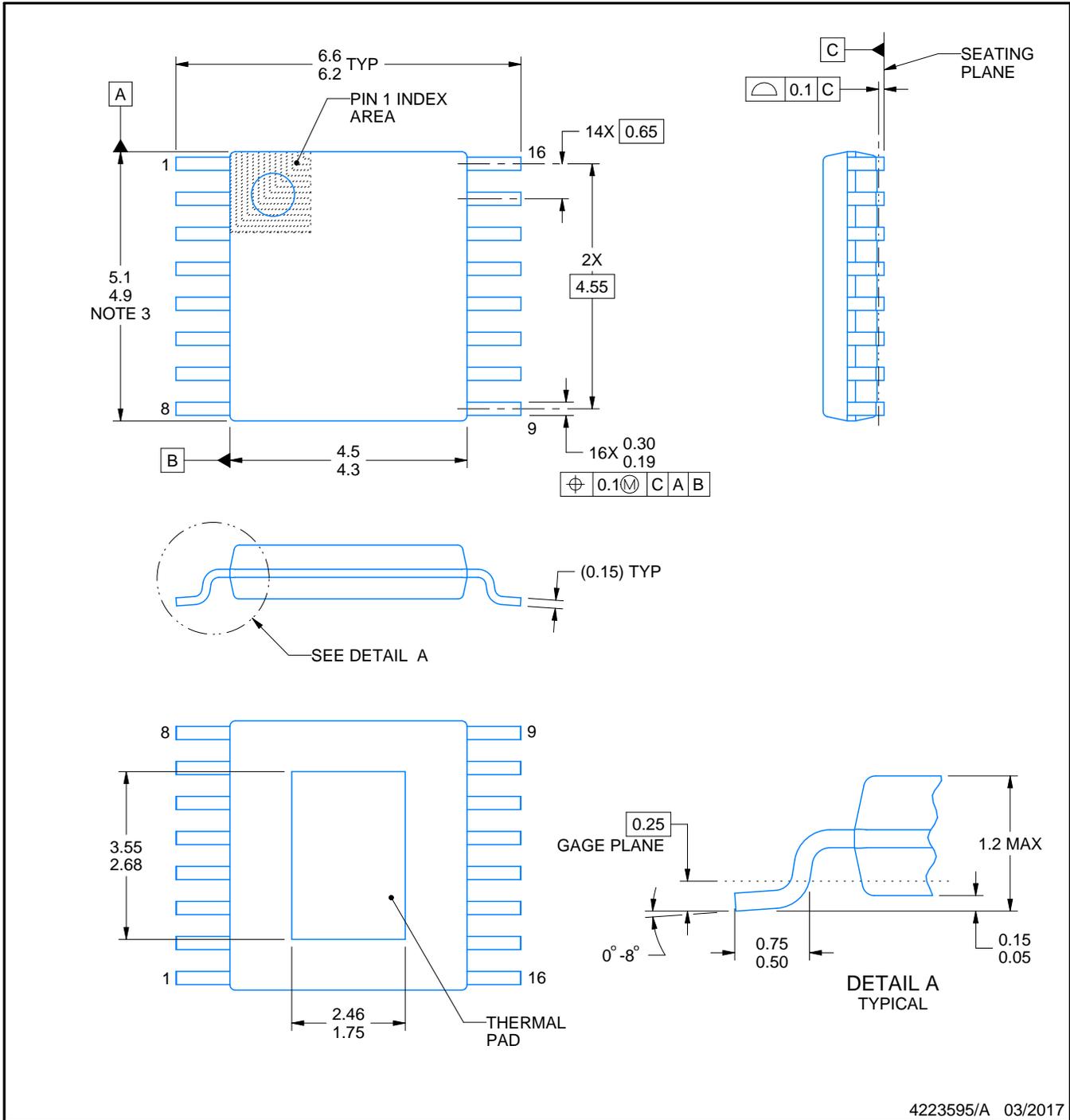Refer to the product data sheet for package details.
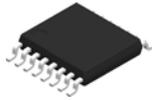
4073225-3/J

6.6
6.2 TYP

A

PIN 1 INDEX
AREA

14X 0.65

1

16

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C

SEATING
PLANE

⌒ 0.1 C

SEE DETAIL A

(0.15) TYP

8

9

3.55
2.68

1

16

2.46
1.75

THERMAL
PAD

0.25

GAGE PLANE

0°-8°

0.75
0.50

1.2 MAX

0.15
0.05

DETAIL A
TYPICAL

4223595/A   03/2017

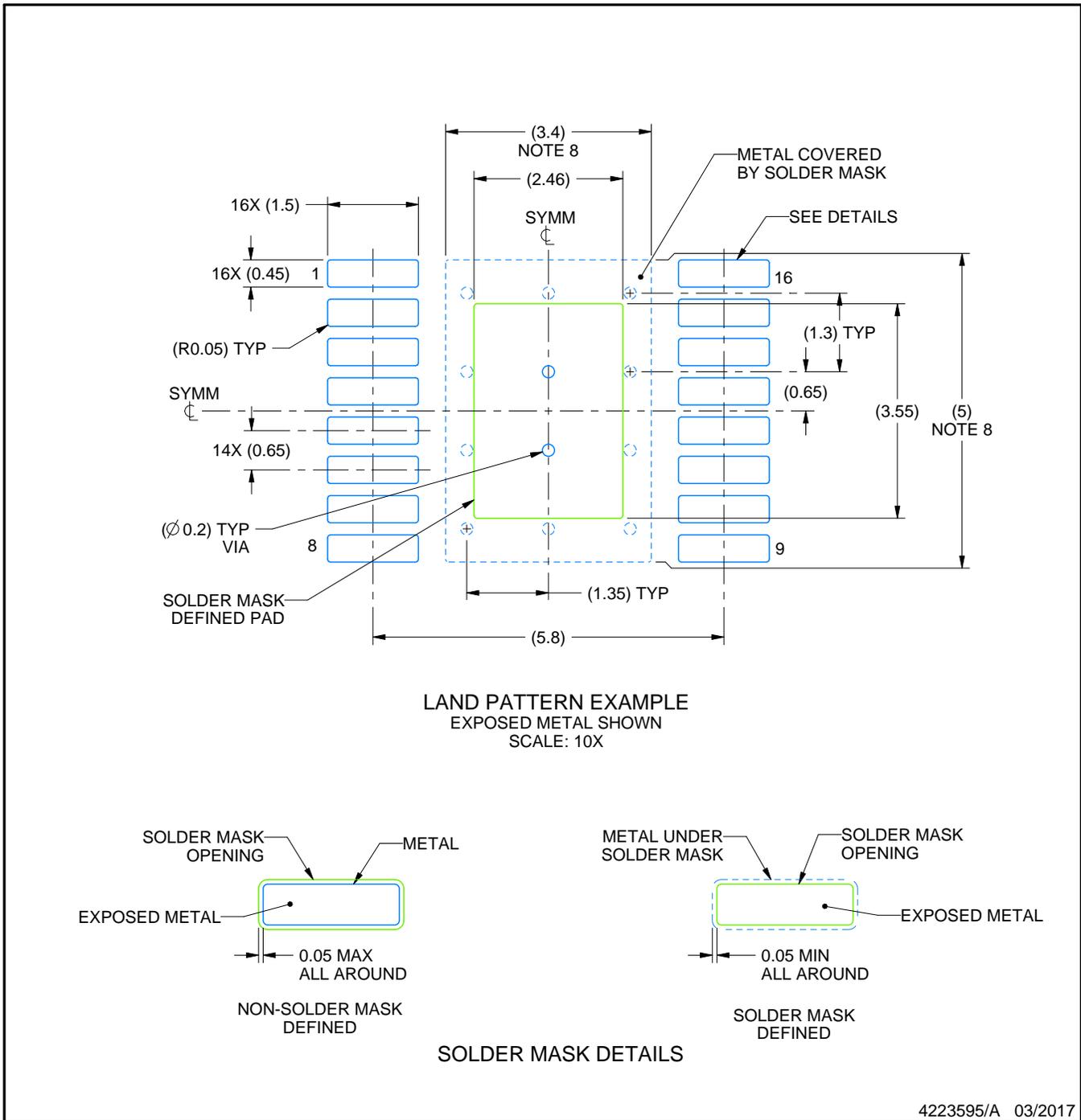PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

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PWP0016J

(3.4)
NOTE 8

METAL COVERED
BY SOLDER MASK

(2.46)

SYMM
℄

SEE DETAILS

16X (1.5)

16X (0.45)   1

16

(1.3) TYP

(R0.05) TYP

(0.65)

SYMM
℄

(3.55)

(5)
NOTE 8

14X (0.65)

(⌀ 0.2) TYP
VIA

8

9

SOLDER MASK
DEFINED PAD

(1.35) TYP

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

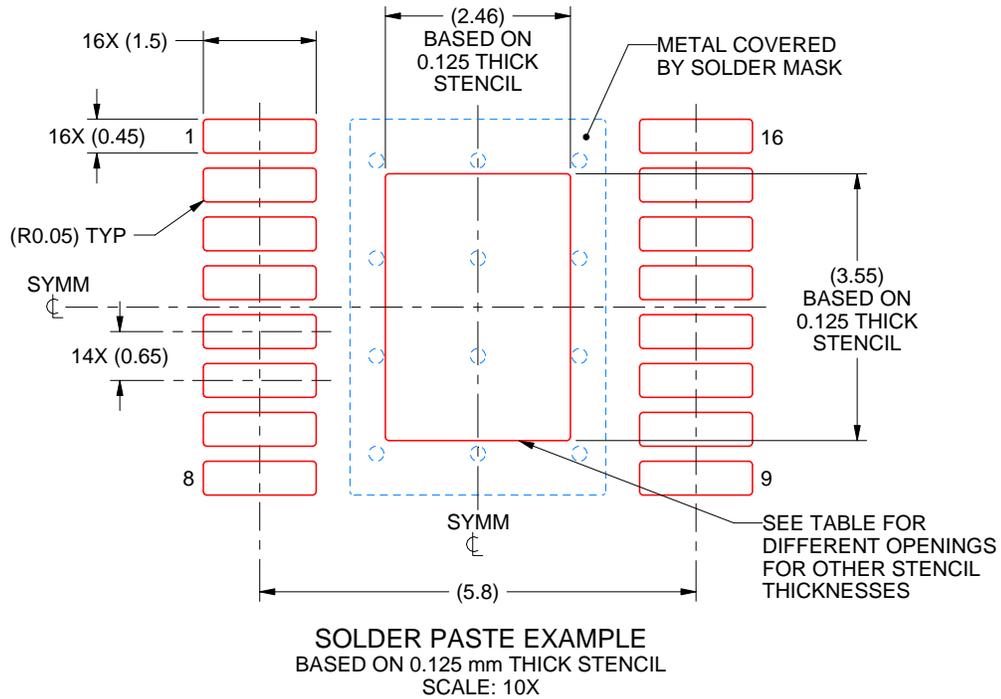4223595/A   03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

PWP0016J

16X (1.5)

16X (0.45) 1

(R0.05) TYP

SYMM

14X (0.65)

8

(2.46)
BASED ON
0.125 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

16

(3.55)
BASED ON
0.125 THICK
STENCIL

9

SYMM

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A   03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
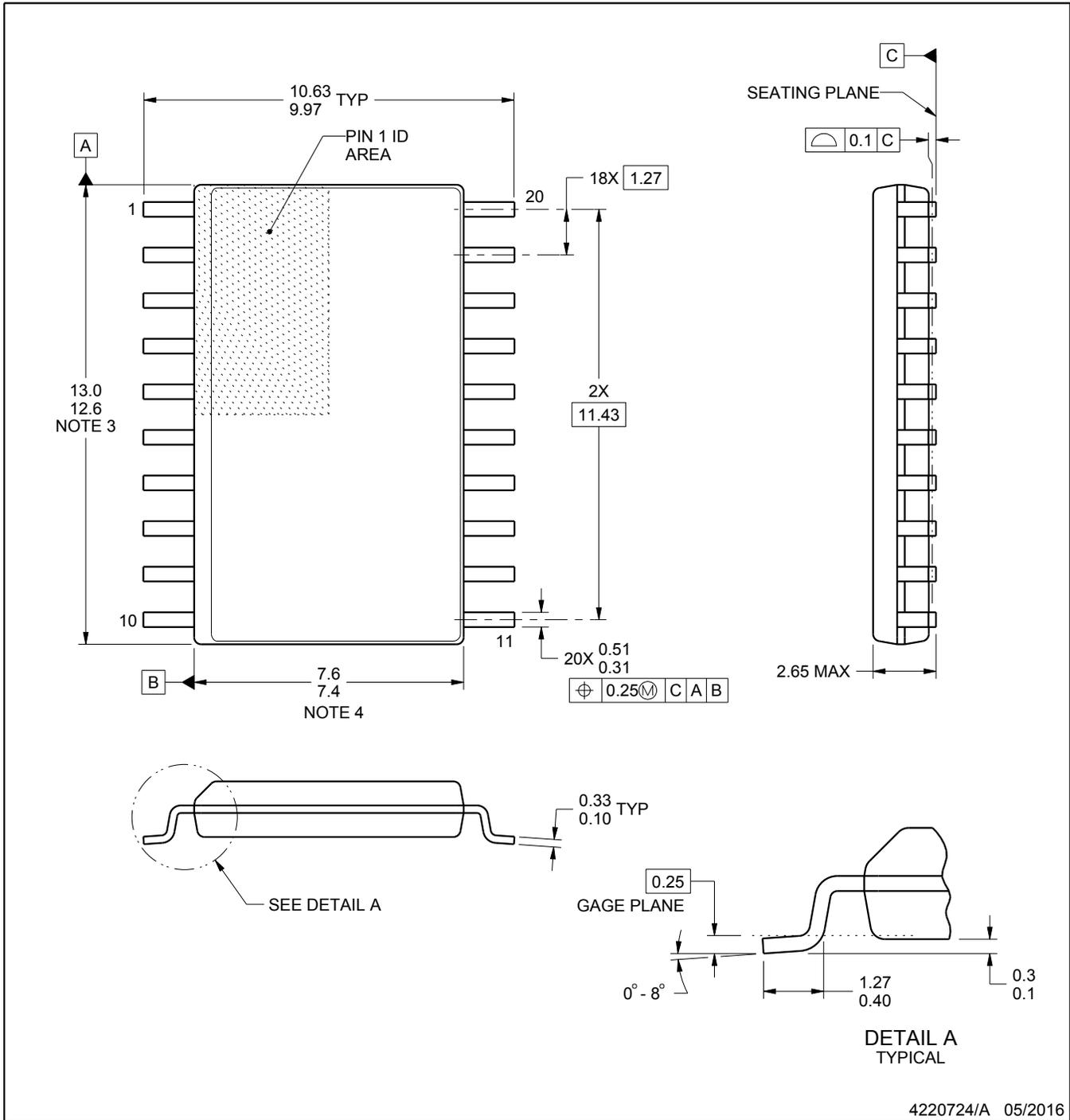11. Board assembly site may have different recommendations for stencil design.

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

20

18X 1.27

13.0 / 12.6
NOTE 3

2X
11.43

10

11

B

7.6 / 7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

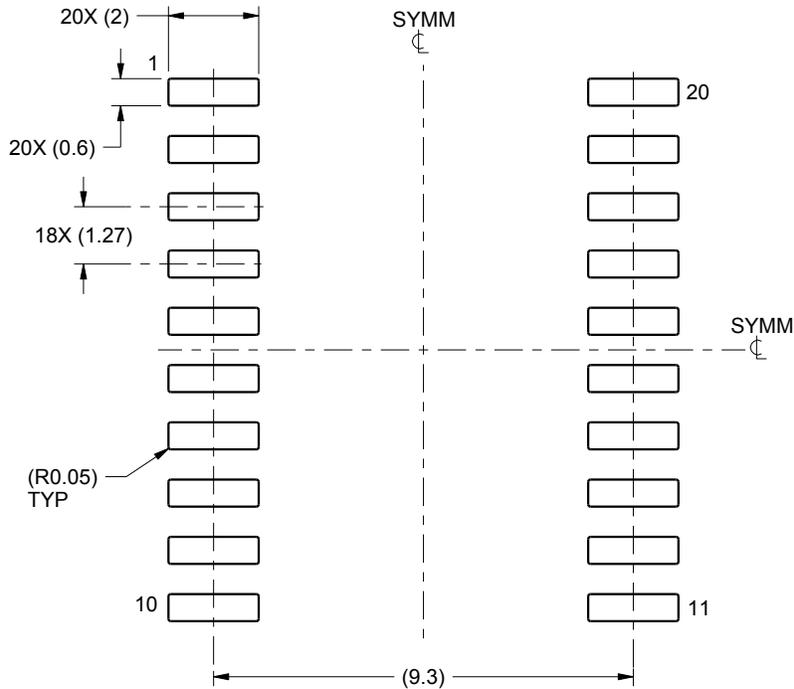0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
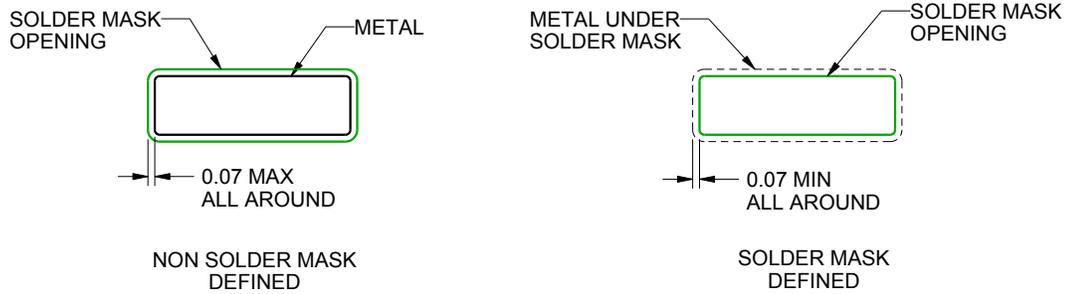5. Reference JEDEC registration MS-013.

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20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
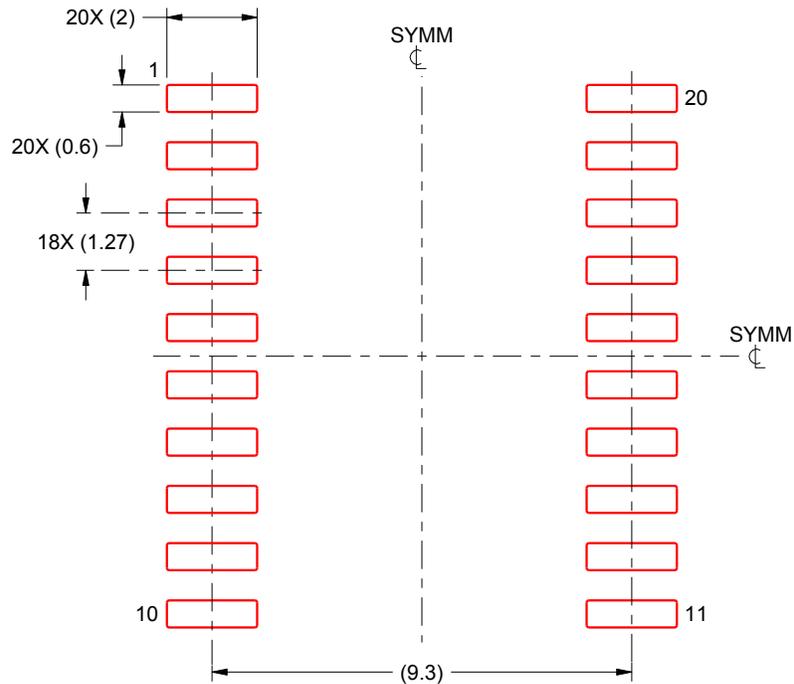DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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