

## FEATURES

- Four 10-bit ADCs
- 10-bit high dynamic range processing
- 12-channel analog input mux
- 10-bit deep color processing
- Analog monitor output
- NTSC/PAL/SECAM color standards support
- NTSC/PAL 3D comb filter
- 3D digital noise reduction (DNR)
- Advanced time base correction (TBC) with frame synchronization
- Interlaced-to-progressive conversion for 525i and 625i
- Advanced VBI data slicer, including Teletext, CC, and V-chip
- IF compensation filter
- SCART fast blank support including slow switch detect
- Programmable internal antialias filters
- Weak, poor time base, and nonstandard signal support
- Vertical peaking, horizontal peaking, CTI, LTI
- Simultaneous interlaced and progressive parallel output for 525i/525p and 625i/625p
- 525p/625p component progressive scan support
- 720p/1080i/1080p component HDTV support
- Digitizes RGB graphics with maximum pixel clock rate of 150 MHz (150 MHz speed grade only)
- 24-bit digital input port supports data from DVI/HDMI Rx IC
- Any-to-any, advanced 3 × 3 color space conversion matrix
- Flexible output pixel interface supporting 8-/10-/16-/20-/24-/30-bit SDR/DDR 4:2:2/4:4:4 data formats
- Programmable interrupt request output pin

## APPLICATIONS

- AV receivers
- LCD HDTVs
- PDP HDTVs
- CRT HDTVs
- HDTV STBs with PVR
- DVD recorders with progressive scan input support
- Projectors

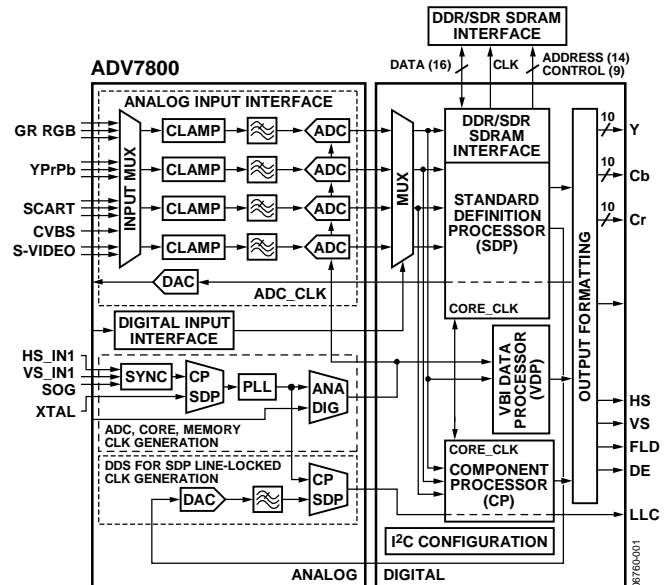


Figure 1. Simplified Functional Block Diagram

## GENERAL DESCRIPTION

The ADV7800<sup>1</sup> is a high quality, single-chip, multiformat 3D comb filter, video decoder, and graphics digitizer. This multiformat 3D comb filter decoder supports the conversion of PAL, NTSC, and SECAM standards in the form of a composite or an S-Video into a digital ITU-R BT.656 format. The ADV7800 also supports the decoding of a component RGB/YPrPb video signal into a digital YCrCb or RGB pixel output stream.

The support for component video includes standards such as 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HD and SMPTE standards. Graphics digitization is supported by the ADV7800; it is capable of digitizing RGB graphics signals from VGA to SXGA rates and converting them into a digital RGB or YCrCb pixel output stream. SCART and overlay functionality are enabled by the ability of the ADV7800 to simultaneously process CVBS and standard definition RGB signals.

The ADV7800 contains two main processing sections. The first section is the standard definition processor (SDP), which processes all PAL, NTSC, SECAM, and component (up to 525p/625p) signal types. The second section is the component processor (CP), which processes YPrPb and RGB component formats, including RGB graphics.

<sup>1</sup> Protected by U.S. Patent Number 4,907,093 and other intellectual property rights.

### Rev. C

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**REVISION HISTORY**

8/11—Revision C: Initial Version

FUNCTIONAL BLOCK DIAGRAM

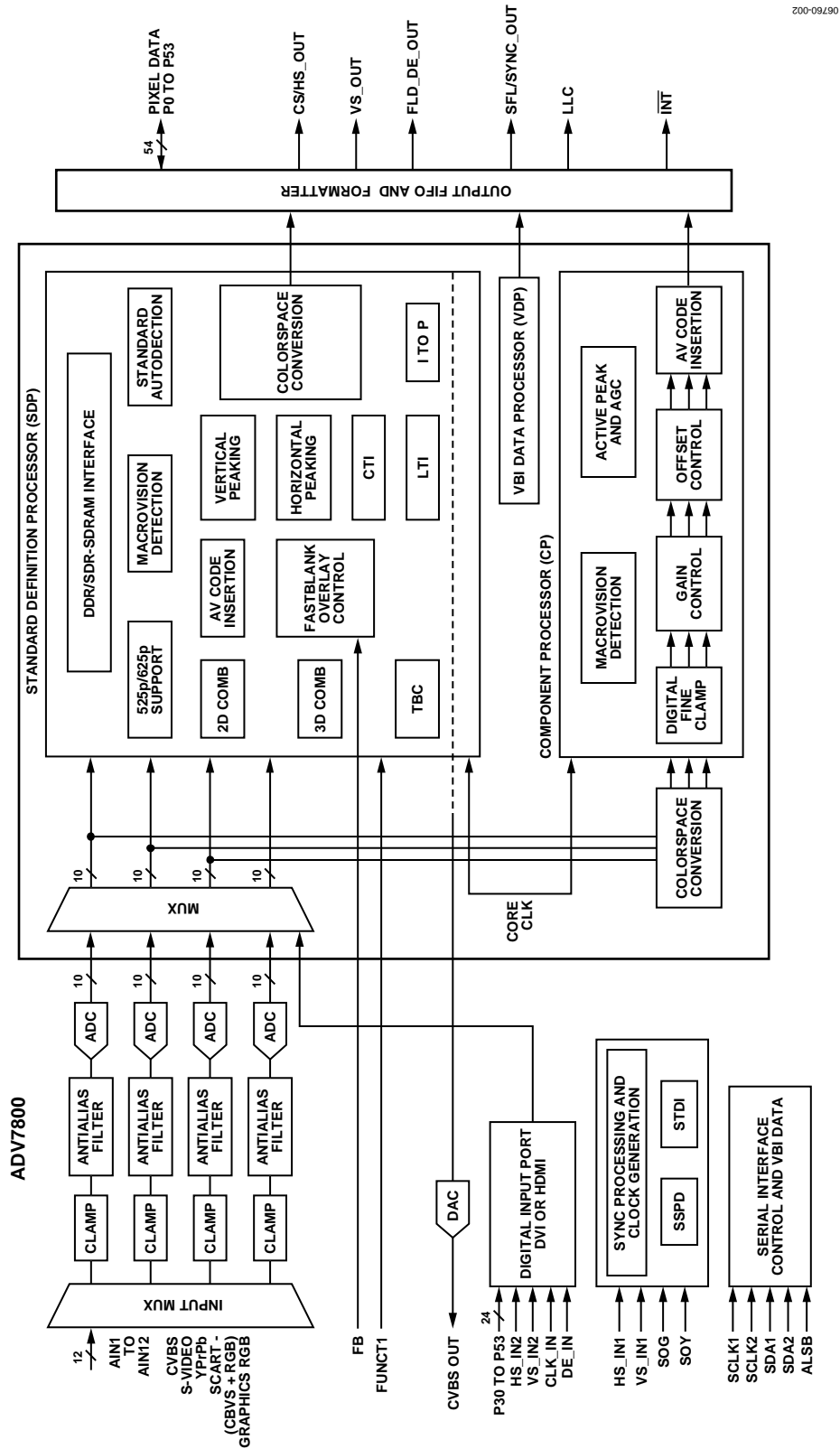


Figure 2.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.75 V to 1.85 V, DVDDIO = 3.0 V to 3.6 V, DVDDIO\_SDRAM = 2.35 V to 2.65 V (DDR), DVDDIO\_SDRAM = 3.2 V to 3.4 V (SDR), PVDD = 1.71 V to 1.89 V, nominal input range 1.6 V. T<sub>A</sub> = 0°C to 85°C, unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE <sup>2, 3</sup>						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity <sup>4</sup>	INL	BSL at 27 MHz (at a 10-bit level)		-0.3/+0.4		LSB
		BSL at 54 MHz (at a 10-bit level)		-0.4/+0.5		LSB
		BSL at 74 MHz (at a 10-bit level)		-0.3/+0.2		LSB
		BSL at 110 MHz (at a 10-bit level)		-0.3/+0.6		LSB
		BSL at 150 MHz (at an 8-bit level)		-0.6/+0.6		LSB
Differential Nonlinearity <sup>4</sup>	DNL	At 27 MHz (at a 10-bit level)		-0.2/+0.3		LSB
		At 54 MHz (at a 10-bit level)		-0.2/+0.3		LSB
		At 74 MHz (at a 10-bit level)		-0.5/+0.4		LSB
		At 110 MHz (at a 10-bit level)		-0.2/+0.3		LSB
		At 150 MHz (at an 8-bit level)		-0.2/+0.4		LSB
POWER REQUIREMENTS <sup>5</sup>						
Digital Core Power Supply	DVDD		1.75	1.8	1.85	V
Digital I/O Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Memory Interface Power Supply	DVDDIO_SDRAM	DDR	2.35	2.5	2.65	V
		SDR	3.2	3.3	3.4	V
Digital Core Supply Current	IDVDD	CVBS input sampling at 54 MHz		236		mA
		Graphics RGB sampling at 78 MHz		103		mA
		SCART RGB FB sampling at 54 MHz		236		mA
		525p input sampling at 54 MHz		319		mA
		CVBS input sampling at 54 MHz		6		mA
Digital I/O Supply Current	IDVDDIO	Graphics RGB sampling at 78 MHz		15		mA
		CVBS input sampling at 54 MHz		13		mA
PLL Supply Current	IPVDD	Graphics RGB sampling at 78 MHz		10		mA
		CVBS input sampling at 54 MHz		99		mA
Analog Supply Current	IAVDD	Graphics RGB sampling at 78 MHz		263		mA
		CVBS input sampling at 54 MHz		269		mA
		SCART RGB FB sampling at 54 MHz		17		mA
Memory Interface Supply Current	IVDDRAM	CVBS input sampling at 54 MHz		17		mA
Power-Down Current	IPWRDN			8		mA
Power-Up Time	TPWRUP			20		ms
DIGITAL INPUTS						
Input High Voltage	V <sub>IH</sub>			2		V
Input Low Voltage	V <sub>IL</sub>			0.8		V
Input Current	I <sub>IN</sub>			±10		μA
Input Capacitance	C <sub>IN</sub>			15		pF
DIGITAL OUTPUTS						
Output High Voltage <sup>6</sup>	V <sub>OH</sub>	ISOURCE = 0.4 mA		2.4		V
Output Low Voltage <sup>6</sup>	V <sub>OL</sub>	ISINK = 3.2 mA		0.4		V
High Impedance Leakage Current	I <sub>LEAK</sub>			10		μA
Output Capacitance	C <sub>OUT</sub>			20		pF

<sup>1</sup> Temperature range T<sub>MIN</sub> to T<sub>MAX</sub>.

<sup>2</sup> All ADC linearity tests performed with part configured for component video input.

<sup>3</sup> All ADC linearity tests performed at input range of full scale – 12.5% and at zero scale + 12.5%.

<sup>4</sup> Maximum INL and DNL specifications obtained with part configured for component video input.

<sup>5</sup> Guaranteed by characterization.

<sup>6</sup> V<sub>OH</sub> and V<sub>OL</sub> levels obtained using default drive strength.

**VIDEO SPECIFICATIONS**

AVDD = 3.15 V to 3.45 V, DVDD = 1.75 V to 1.85 V, DVDDIO = 3.0 V to 3.6 V, DVDDIO\_SDRAM = 2.35 V to 2.65 V (DDR), DVDDIO\_SDRAM = 3.2 V to 3.4 V (SDR), PVDD = 1.71 V to 1.89 V. T<sub>A</sub> = 0°C to 85°C, unless otherwise noted.

**Table 2.**

Parameter <sup>1</sup>	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>NONLINEAR SPECIFICATIONS</b>						
Differential Phase	DP	CVBS input (modulated 5-step)		0.47		Degrees
Differential Gain	DG	CVBS input (modulated 5-step)		0.47		%
Luma Nonlinearity	LNL	CVBS input (modulated 5-step)		0.8		%
<b>NOISE SPECIFICATIONS</b>						
SNR Unweighted		Luma ramp		61		dB
		Luma flat field		62		dB
Analog Front-End Crosstalk				60		dB
<b>LOCK TIME SPECIFICATIONS (SDP)</b>						
Horizontal Lock Range				±5		%
Vertical Lock Range			40		70	Hz
Subcarrier Lock Range, f <sub>sc</sub>				±0.8		kHz
Color Lock-In Time				60		Lines
Sync Depth Range <sup>2</sup>			20		200	%
Color Burst Range			1		200	%
Vertical Lock Time				300		ms
Horizontal Lock Time				100		Lines
<b>CHROMA SPECIFICATIONS (SDP)</b>						
Chroma Amplitude Error				0.4		%
Chroma Phase Error				0.3		Degrees
Chroma Luma Intermodulation				0.2		%

<sup>1</sup> Guaranteed by characterization.

<sup>2</sup> Nominal sync depth is 300 mV at 100% sync depth range.

**TIMING CHARACTERISTICS**

AVDD = 3.15 V to 3.45 V, DVDD = 1.75 V to 1.85 V, DVDDIO = 3.0 V to 3.6 V, DVDDIO\_SDRAM = 2.35 V to 2.65 V (DDR), DVDDIO\_SDRAM = 3.2 V to 3.4 V (SDR), PVDD = 1.71 V to 1.89 V. T<sub>A</sub> = 0°C to 85°C, unless otherwise noted.

**Table 3.**

Parameter <sup>1</sup>	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SYSTEM CLOCK AND CRYSTAL</b>						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		90	kHz
LLC Frequency Range			12.825		150	MHz
<b>I<sup>2</sup>C PORT</b>						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t <sub>1</sub>		0.6			µs
SCLK Minimum Pulse Width Low	t <sub>2</sub>		1.3			µs
Hold Time (Start Condition)	t <sub>3</sub>		0.6			µs
Setup Time (Start Condition)	t <sub>4</sub>		0.6			µs
SDA Setup Time	t <sub>5</sub>		100			ns
SCLK and SDA Rise Time	t <sub>6</sub>				300	ns
SCLK and SDA Fall Time	t <sub>7</sub>				300	ns
Setup Time (Stop Condition)	t <sub>8</sub>			0.6		µs
<b>FAST I<sup>2</sup>C PORT<sup>2</sup></b>						
SCLK Frequency					3.4	MHz
SCLK Minimum Pulse Width High	t <sub>1</sub>		60			ns
SCLK Minimum Pulse Width Low	t <sub>2</sub>		160			ns
Hold Time (Start Condition)	t <sub>3</sub>		160			ns
Setup Time (Start Condition)	t <sub>4</sub>		160			ns
SDA Setup Time	t <sub>5</sub>		10			ns
SCLK and SDA Rise Time	t <sub>6</sub>		10		80	ns
SCLK and SDA Fall Time	t <sub>7</sub>		10		80	ns
Setup Time (Stop Condition)	t <sub>8</sub>		160			ns
<b>RESET FEATURE</b>						
Reset Pulse Width			5			ms
<b>CLOCK OUTPUTS</b>						
LLC Mark Space Ratio	t <sub>9</sub> , t <sub>10</sub>		45:55		55:45	% duty cycle
<b>DATA AND CONTROL OUTPUTS<sup>3</sup></b>						
Data Output Transition Time, SDR (SD Core)	t <sub>11</sub>	Negative clock edge to start of valid data			4.5	ns
Data Output Transition Time, SDR (SD Core)	t <sub>12</sub>	End of valid data to negative clock edge			0	ns
Data Output Transition Time, SDR (CP Core)	t <sub>13</sub>	Negative clock edge to start of valid data			2.5	ns
Data Output Transition Time, SDR (CP Core)	t <sub>14</sub>	End of valid data to negative clock edge			0.2	ns
<b>DATA AND CONTROL INPUTS<sup>4</sup></b>						
Input Setup Time (Digital Input Port)	t <sub>17</sub>	HS_IN1, VS_IN1 HS_IN2, VS_IN2	9.5			ns
Input Hold Time (Digital Input Port)	t <sub>18</sub>	DE_IN, data inputs	2			ns
		HS_IN1, VS_IN1 HS_IN2, VS_IN2 DE_IN, data inputs	-4			ns
			0.8			ns

<sup>1</sup> Guaranteed by characterization.<sup>2</sup> With a bus line load less than 100 pF.<sup>3</sup> Timing figures obtained using default drive strength value.<sup>4</sup> TTL input values are 0 V to 3 V, with rise/fall times ≥ 3 ns, measured between the 10% and 90% points.

TIMING DIAGRAMS

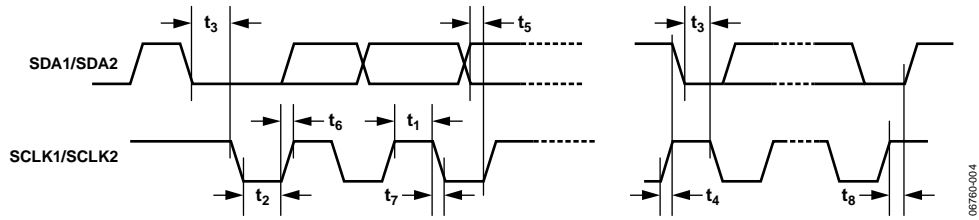


Figure 3. I<sup>2</sup>C Timing

06760-004

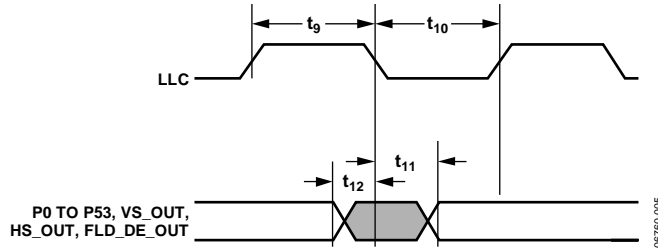


Figure 4. Pixel Port and Control SDR Output Timing (SD Core)

06760-005

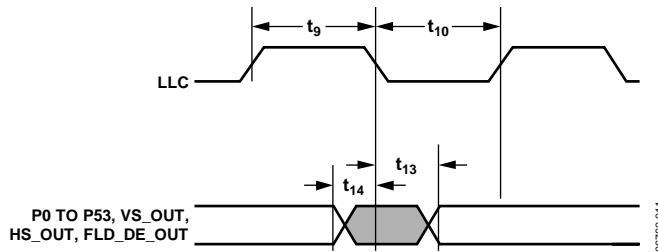


Figure 5. Pixel Port and Control SDR Output Timing (CP Core)

06760-011

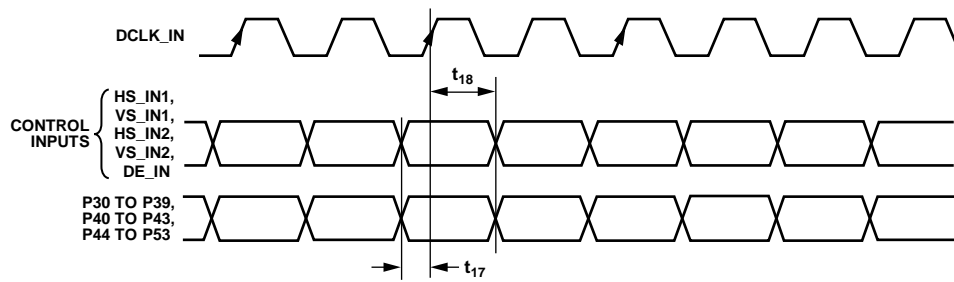


Figure 6. Digital Input Port and Control Input Timing

06760-007

**ANALOG SPECIFICATIONS**

AVDD = 3.15 V to 3.45 V, DVDD = 1.75 V to 1.85 V, DVDDIO = 3.0 V to 3.6 V, DVDDIO\_SDRAM = 2.35 V to 2.65 V (DDR), DVDDIO\_SDRAM = 3.2 V to 3.4 V (SDR), PVDD = 1.71 V to 1.89 V.  $T_A = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise noted. Recommended analog input video signal range is 0.5 V to 1.6 V, typically 1 V p-p. Recommended external clamp capacitor value is 0.1  $\mu\text{F}$ .

**Table 4.**

Parameter <sup>1, 2</sup>	Test Conditions	Min	Typ	Max	Unit
<b>CLAMP CIRCUITRY</b>					
Input Impedance <sup>3</sup>	Clamps switched off		10		M $\Omega$
Input Impedance of Pin 90 (FB)			20		k $\Omega$
CML			2.0		V
ADC Full-Scale Level			CML + 0.8		V
ADC Zero-Scale Level			CML – 0.8		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML – 0.292		V
	SCART RGB input (R, G, B signals)		CML – 0.3		V
	S-Video input (Y signal)		CML – 0.292		V
	S-Video input (C signal)		CML – 0		V
	Component input (Y signal)		CML – 0.3		V
	Component input (Pr, Pb signals)		CML – 0		V
	PC RGB input (R, G, B signals)		CML – 0.3		V
Large Clamp Source Current	SDP only		0.75		mA
Large Clamp Sink Current	SDP only		0.9		mA
Fine Clamp Source Current	SDP only		17		$\mu\text{A}$
Fine Clamp Sink Current	SDP only		17		$\mu\text{A}$

<sup>1</sup> The minimum/maximum specifications are guaranteed over  $0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

<sup>2</sup> Guaranteed by characterization.

<sup>3</sup> Except Pin 90 (FB).



## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	4.0 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4.0 V
DVDDIO_SDRAM to DGND_SDRAM (DDR)	2.7 V
DVDDIO_SDRAM to DGND_SDRAM (SDR)	4.0 V
DVDDIO to AVDD	-0.3 V to +0.3 V
DVDDIO to DVDD	-0.3 V to +2 V
DVDDIO_SDRAM to DVDD (DDR)	-0.3 V to +2.5 V
DVDDIO_SDRAM to DVDD (SDR)	-0.3 V to +3.3 V
AVDD to PVDD	-0.3 V to +2 V
AVDD to DVDD	-0.3 V to +2 V
DVDDIO to DVDDIO_SDRAM (DDR)	-0.3 V to +2 V
DVDDIO to DVDDIO_SDRAM (SDR)	-0.3 V to +3.3 V
AVDD to DVDDIO_SDRAM (DDR)	-0.3 V to +2.5 V
AVDD to DVDDIO_SDRAM (SDR)	-0.3 V to +1.8 V
Digital Inputs Voltage to DGND	DGND - 0.3 V to DVDDIO + 0.3 V
DVDDIO_SDRAM Inputs to DGND_SDRAM	DGND_SDRAM - 0.3 V to DVDDIO_SDRAM + 0.3 V
Analog Inputs to AGND	AGND - 0.3 V to AVDD + 0.3 V
SCLK/SDA Data Pins to DVDDIO	DVDDIO - 0.3 V to DVDDIO + 3.6 V
Maximum Junction Temperature (T <sub>J MAX</sub> )	125°C
Storage Temperature Range	-65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the part, the user is advised to turn off any unused ADCs.

The junction temperature must always stay below the maximum junction temperature (T<sub>J MAX</sub>) of 125°C. This equation shows how to calculate the junction temperature:

$$T_J = T_{A MAX} + (\theta_{JA} \times W_{MAX})$$

where:

$$T_{A MAX} = 85^\circ\text{C}$$

$$\theta_{JA} = 21.0330^\circ\text{C/W}$$

$$W_{MAX} = ((AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (PVDD \times I_{PVDD}) + (DVDD\_SDRAM \times I_{DVDD\_SDRAM})).$$

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$ <sup>1</sup>	$\theta_{JC}$ <sup>2</sup>	Unit
176-Lead LQFP	21	7	°C/W

<sup>1</sup> 4-layer PCB with solid ground plane.

<sup>2</sup> 4-layer PCB with solid ground plane (still air).

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

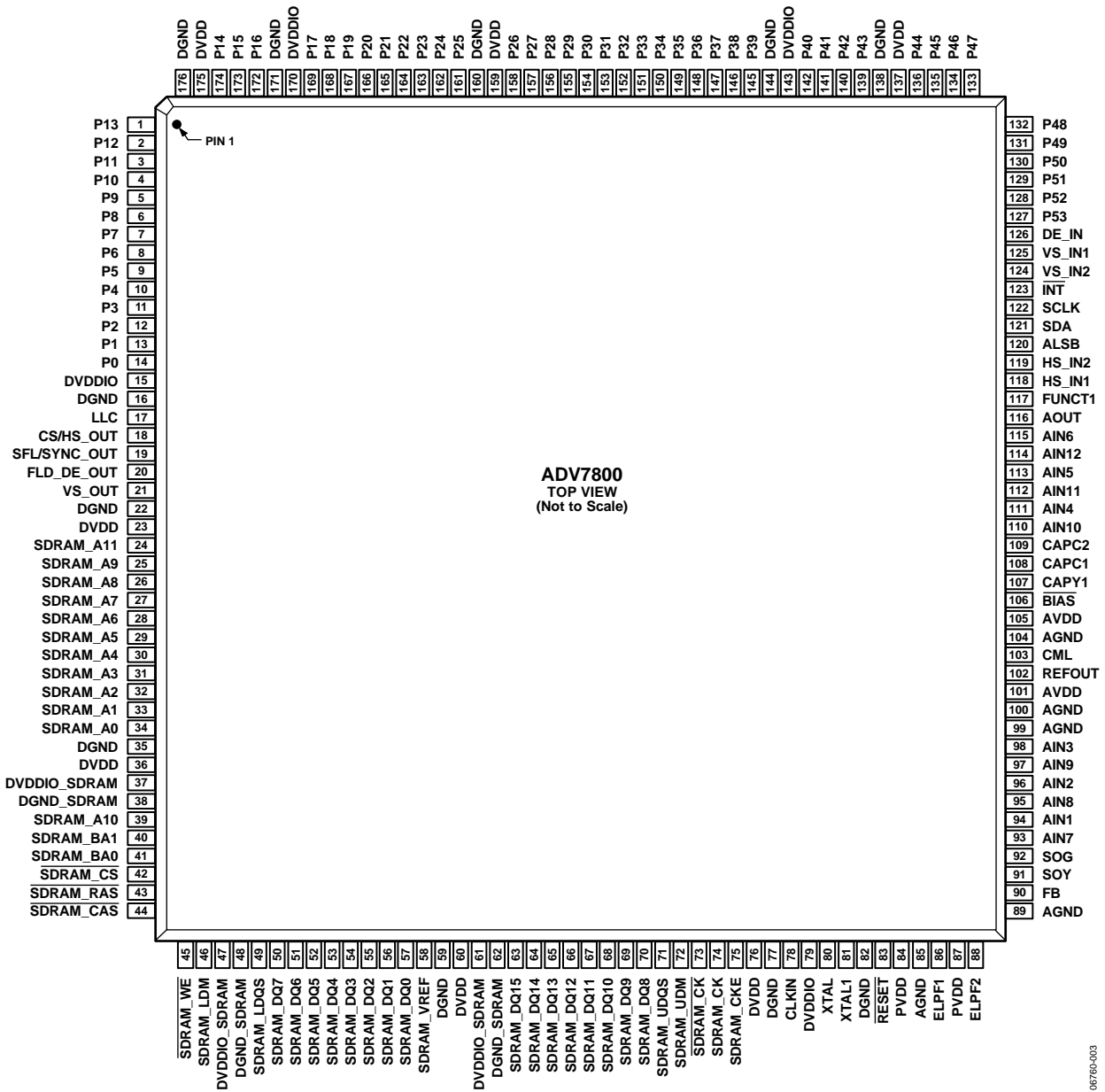


Figure 7. Pin Configuration

06760-003

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1 to 14, 155 to 158, 161 to 169, 172 to 174	P0 to P29	O	Video Pixel Output Port. See Figure 7 for details on pin mapping.
15, 79, 143, 170	DVDDIO	P	Digital Input/Output Supply Voltage (3.3 V).
16, 22, 35, 59, 77, 82, 138, 144, 160, 171, 176	DGND	GND	Digital Ground.
17	LLC	O	Line-Locked Output Clock for the Pixel Data.
18	CS/HS_OUT	O	Horizontal Synchronization or Composite Synchronization Signal. This signal can be selected while in SDP mode.
19	SFL/SYNC_OUT	O	Subcarrier Frequency Lock. This pin contains a serial output stream, which can be used to lock the subcarrier frequency when this decoder is connected to any digital video encoder from Analog Devices, Inc. SYNC_OUT is the sliced synchronization output signal available only in CP mode.
20	FLD_DE_OUT	O	Field Synchronization Output Signal (All Interlaced Video Modes). This pin can also be enabled as a data enable signal (DE) to allow direct connection to a HDMI™/DVI Tx IC.
21	VS_OUT	O	Vertical Synchronization Output Signal (SDP and CP modes).
23, 36, 60, 76, 137, 159, 175	DVDD	P	Digital Core Supply Voltage (1.8 V).
24 to 34, 39	SDRAM_A0 to SDRAM_A11	O	Address Outputs. Interface to external RAM address lines. See Figure 7 for details on pin mapping.
37, 47, 61	DVDDIO_SDRAM	P	External Memory Interface Digital Input/Output Supply (2.5 V for DDR, or 3.3 V for SDR).
38, 48, 62	DGND_SDRAM	GND	External Memory Interface Digital GND.
40, 41	SDRAM_BA1, SDRAM_BA0	O	Bank Address Outputs. Interface to external RAM bank address lines.
42	SDRAM_CS	O	<u>SDRAM_CS</u> is a chip select function that enables and disables the command decoder on the RAM.
43	SDRAM_RAS	O	<u>Row Address Select Command Signal</u> . <u>SDRAM_RAS</u> , <u>SDRAM_CAS</u> , <u>SDRAM_WE</u> , and <u>SDRAM_CS</u> define the command to the RAM.
44	SDRAM_CAS	O	<u>Column Address Select Command Signal</u> . <u>SDRAM_RAS</u> , <u>SDRAM_CAS</u> , <u>SDRAM_WE</u> , and <u>SDRAM_CS</u> define the command to the RAM.
45	SDRAM_WE	O	<u>Write Enable Output Command Signal</u> . <u>SDRAM_RAS</u> , <u>SDRAM_CAS</u> , <u>SDRAM_WE</u> , and <u>SDRAM_CS</u> define the command to the RAM.
46, 72	SDRAM_LDM, SDRAM_UDM	O	Data Mask Output. Data is masked when DM is high, for write data to the external RAM. LDM corresponds to the data on SDRAM_DQ0 to SDRAM_DQ7, and UDM corresponds to the data on SDRAM_DQ8 to SDRAM_DQ15.
49	SDRAM_LDQS	I/O	Lower Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an output with read data and an input with write data. It is edge aligned with write data and centered in read data. SDRAM_LDQS corresponds to the data on SDRAM_DQ0 to SDRAM_DQ7.
50 to 57, 63 to 70	SDRAM_DQ0 to SDRAM_DQ15	I/O	Data Bus. Interface to external RAM 16-bit data bus. See Figure 7 for details on pin mapping.
58	SDRAM_VREF	P	1.25 V reference for DDR SDRAM interface or 1.65 V for SDR SDRAM interface.
71	SDRAM_UDQS	I/O	Upper Data Strobe Pin. Data strobe pins for the RAM interface. This is an output with read data and an input with write data. It is edge aligned with write data and centered in read data. SDRAM_UDQS corresponds to the data on SDRAM_DQ8 to SDRAM_DQ16.
73, 74	SDRAM_CK, SDRAM_CK	O	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of <u>SDRAM_CK</u> .
75	SDRAM_CKE	O	Clock Enable. This pin is used to enable the clock signals of the external RAM.
78	CLKIN	I	Clock Input Signal. Used in 24-bit digital input mode (for example, processing 24-bit RGB data from a DVI/HDMI Rx IC) and also in digital CVBS input mode.

Pin No.	Mnemonic	Type <sup>1</sup>	Description
80	XTAL	I	Crystal Input. Input pin for 28.63636 MHz crystal.
81	XTAL1	O	Crystal Output. This pin should be connected to the 28.63636 MHz crystal.
83	$\overline{\text{RESET}}$	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7800 circuitry.
84, 87	PVDD	P	PLL Supply Voltage (1.8 V).
85, 89, 99, 100, 104	AGND	GND	Analog Ground.
86, 88	ELPF1, ELPF2	I	External Loop Filter. The recommend external loop filter must be connected to each ELPF pin (see Figure 8).
90	FB	I	SCART Fast Blank Input.
91	SOY	I	Sync On Luma Input. Used in embedded synchronization mode.
92	SOG	I	Sync On Green Input. Used in embedded synchronization mode.
93 to 98, 110 to 115	AIN1 to AIN12	I	Analog Video Input Channels. See Figure 7 for details on pin mapping.
101, 105	AVDD	P	Analog Supply Voltage (3.3 V).
102	REFOUT	O	Internal Voltage Reference Output.
103	CML	O	Common-Mode Level Pin Used for the Internal ADCs.
106	$\overline{\text{BIAS}}$	O	External Bias Setting Pin. Connect the recommended resistor (1.35 k $\Omega$ ) between the pin and ground.
107	CAPY1	I	ADC Capacitor Network.
108, 109	CAPC1, CAPC2	I	ADC Capacitor Network.
116	AOUT	O	Analog Monitor Output.
117	FUNCT1	I	SCART Function Select Input.
118	HS_IN1	I	Horizontal Synchronization Input Signal. Used in CP mode for 5-wire timing mode.
119	HS_IN2	I/O	Horizontal Synchronization Input Signal. Used in 24-bit digital input mode port mode (for example, processing 24-bit RGB data from an HDMI Rx IC). HS_IN2 in conjunction with VS_IN2 can be configured as a fast I <sup>2</sup> C interface for teletext data extraction. HS_IN2 is used as the I <sup>2</sup> C port serial clock input.
120	ALSB	I	ALSB selects the I <sup>2</sup> C address for the ADV7800 control. ALSB set to Logic 0 configures the address for a write to the input/output port of 0x40. ALSB set to Logic 1 configures the address for a write to the input/output port of 0x42.
121	SDA	I/O	I <sup>2</sup> C Port Serial Data Input/Output Pin.
122	SCLK	I	I <sup>2</sup> C Port Serial Clock Input (Maximum Clock Rate of 400 kHz).
123	$\overline{\text{INT}}$	O	Interrupt Output. This pin can be active low or active high. When SDP/CP status bits change, this pin triggers. The set of events that triggers an interrupt is under user control.
124	VS_IN2	I/O	Vertical Synchronization Input Signal. Used in 24-bit digital input mode (for example, processing 24-bit RGB data from an DVI/HDMI Rx IC). VS_IN2 in conjunction with HS_IN2 can be configured as a fast I <sup>2</sup> C interface for teletext data extraction. VS_IN2 is used as the I <sup>2</sup> C port serial data input/output pins.
125	VS_IN1	I	Vertical Synchronization Input Signal.
126	DE_IN	I	Data Enable Input Signal. Used in 24-bit digital input port mode (for example, processing 24-bit RGB data from an DVI/HDMI Rx IC).
127 to 136, 139 to 142, 145 to 154	P30 to P53	I/O	Video Pixel Input/Output Port. See Figure 7 for details on pin mapping.

<sup>1</sup> GND = ground, I = input, I/O = input/output, O = output, P = power.

## THEORY OF OPERATION

### KEY FEATURES

The ADV7800 is a high quality, single-chip, multiformat 3D comb filter video decoder, and graphics digitizer. Key features of the device include

- Four 10-bit ADCs
- NTSC/PAL/SECAM video decoder
- Adaptive 3D comb filtering
- 3D digital noise reduction
- Advanced frame time-base correction (TBC)
- Composite, S-Video, YPrPb/RGB SCART support
- YPrPb component HD and RGB graphics input support
- 30-bit digital YPrPb/RGB output supporting 10-bit deep color

### ANALOG FRONT END

The ADV7800 analog front end comprises four 10-bit ADCs that digitize the analog video signal before applying it to the SDP or CP.

The front end includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7800 without the requirement of an external mux. Current and voltage clamps are positioned in front of each ADC to ensure the video signal remains within the range of the converter.

The ADCs are configured to run up to 4× oversampling mode when decoding composite and S-Video inputs or components up to 525i and 625i. 2× oversampling is available for 525p and 625p. All other video standards are 1× oversampled. In oversampling the video signals, a reduction in the cost and complexity of external antialiasing filters can be obtained with the benefit of an increased signal-to-noise ratio (SNR).

Optional internal antialiasing filters with programmable bandwidth are positioned in front of each ADC. These filters can be used to band-limit standard definition video signals, removing spurious, out-of-band noise.

The ADV7800 can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed and can be output under the control of I<sup>2</sup>C registers and the fast blank pin.

Analog front-end features include

- Four 150 MHz, 10-bit ADCs that enable true 10-bit video decoding
- 12-channel analog input mux that enables multiple source connections without the requirement of an external mux
- Four current and voltage clamp control loops that ensure any dc offsets are removed from the video signal
- SCART functionality and SD RGB overlay on CVBS controlled by fast blank input
- SCART source switching detection through FUNCT1 input
- Four programmable antialias filters on standard definition video signals and enhance definition
- CVBS monitor output

### STANDARD DEFINITION PROCESSOR

The standard definition processor (SDP) is capable of decoding a large selection of baseband video signals in composite, S-Video, and YUV formats. The video standards supported by the SDP include PAL, PAL 60, PAL M, PAL N, PAL NC, NTSC M/J, NTSC 4.43, and SECAM. The ADV7800 can automatically detect the video standard and process it accordingly. The ADV7800 can process video up to 525p/625p formats.

The SDP has a 3D temporal comb filter and a 5-line adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency chroma spectrum due to a tuner SAW filter. The SDP has specific luminance and chrominance parameter controls for brightness, contrast, saturation, and hue.

The ADV7800 implements a patented adaptive digital line length tracking (ADLLT) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7800 to track and decode poor quality video sources (such as VCRs) and noisy sources (such as tuner outputs, VCRs, and camcorders). Frame TBC ensures stable clock synchronization between the decoder and the downstream devices to prevent disruptions.

The SDP also contains both a luma transient improvement (LTI) and a chroma transient improvement (CTI) processor. This processor increases the edge rate on the luma and chroma transitions, resulting in a sharper video image.

The SDP has a Macrovision® detection circuit, which allows Type I, Type II, and Type III Macrovision protection levels. The decoder is also fully robust to all Macrovision signal inputs.

SDP features include

- Full automatic detection and autoswitching of all worldwide standards (PAL, NTSC, and SECAM)
- Advanced adaptive 3D comb with concurrent 3D noise reduction (using either external DDR or SDR memory)
- Adaptive 2D 5-line comb filters for NTSC and PAL that give superior chrominance and luminance separation for composite video
- Automatic gain control with white peak mode that ensures the video is always processed without loss of the video processing range
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block that compensates for high frequency luma attenuation due to a tuner SAW filter
- LTI and CTI
- Vertical and horizontal programmable luma peaking filters
- 10-bit deep color processing path from front to back end in RGB/YCrCb formats
- Macrovision copy protection detection on composite and S-Video for all worldwide formats (PAL, NTSC, and SECAM)
- 4× oversampling (54 MHz) for CVBS, S-Video, and YUV modes
- 2× oversampling (54 MHz) for 525p and 625p modes
- Line-locked clock output (LLC)
- Free run output mode that provides stable timing when no video input is present
- Internal color bar test pattern
- Advanced TBC with frame synchronization, which ensures nominal clock and data for nonstandard input
- Interlace-to-progressive conversion for 525i and 625i formats, enabling direct drive of HDMI Tx devices
- Color controls that include hue, brightness, saturation, and contrast
- Differential gain (DG), typically 0.45%
- Differential phase (DP), typically 0.45°
- Video SNR, typically 61 dB

## VBI DATA PROCESSOR

The VBI data processor (VDP) of the ADV7800 is capable of slicing multiple vertical blanking interval data standards on SD video and component video. The VDP decodes the VBI data on the incoming CVBS/YC or YUV data processed by the SDP core. It can also decode VBI data on the luma channel of YUV data processed through the CP core.

The VDP can process a variety of VBI data services, such as

- Teletext
- Video programming system (VPS)
- Vertical interval time codes (VITC)
- Closed captioning (CC) and extended data service (EDS)
- Wide screen signaling (WSS)
- Copy generation management system (CGMS, CGMS Type B)
- Gemstar® 1×/2× electronic program guide compatible
- Extended data service (SDS); the data extracted can be read back over a fast I<sup>2</sup>C interface

## COMPONENT PROCESSOR

The component processor (CP) is capable of decoding and digitizing a wide range of component video formats in any color space. The CP can accept video data from the analog front end or from the HDMI receiver. Component video standards supported by the CP include 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and VGA (up to SXGA at 75 Hz), and many other standards.

A fully programmable any-to-any, 3 × 3 color space conversion (CSC) matrix is placed before the CP. This enables YPrPb-to-RGB and RGB-to-YCrCb conversions of video data coming from the analog front end or from the HDMI receiver. Many other standards of color space can be implemented using the color space converter.

The CP of the ADV7800 contains an automatic gain control (AGC) block. The AGC is followed by a clamp circuit that ensures the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness). Manual adjustment controls are also supported. In cases where no embedded synchronization is preset, the video gain can be set manually.

The CP contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust to these types of signals.

CP features include

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats supported
- Automatic adjustments including gain (contrast) and offset (brightness); manual adjustment controls also supported
- Support for analog component YPrPb and RGB video formats with embedded synchronization or with separate HS, VS, or CS
- Any-to-any,  $3 \times 3$  color space conversion matrix that supports YCrCb-to-RGB and RGB-to-YCrCb, fully programmable or preprogrammable configurations
- Synchronization source polarity detector (SSPD) that determines the source and polarity of the synchronization signals that accompany the input video
- Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free run output mode that provides stable timing when no video input is present
- Arbitrary pixel sampling support for nonstandard video sources
- 150 MHz conversion rate, which supports RGB input resolutions up to  $1280 \times 1024$  at 75 Hz
- Automatic or manual clamp-and-gain controls for graphics modes
- Contrast, brightness, hue, and saturation controls
- 32-phase DLL that allows optimum pixel clock sampling
- Automatic detection of synchronization source and polarity by SSPD block
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for videocentric back-end IC interfacing
- DE output signal that is supplied for direct connection to HDMI/DVI Tx IC
- Arbitrary pixel sampling support for nonstandard video sources

### ADDITIONAL FEATURES

The ADV7800 also includes

- HS, VS, FIELD, and DE output signals with programmable position, polarity, and width
- Programmable interrupt request output pin ( $\overline{\text{INT}}$ ) that signals SDP/CP status changes
- Two I<sup>2</sup>C host port interface (control and VBI) support
- Integrated programmable antialiasing filters
- 176-lead, 26 mm  $\times$  26 mm, RoHS-compliant LQFP

For more detailed product information about the ADV7800, email [video.products@analog.com](mailto:video.products@analog.com) or contact a local Analog Devices sales representative.

## EXTERNAL MEMORY REQUIREMENTS

### SINGLE DATA RATE (SDR)

The ADV7800 uses SDR external memory for 3D comb, frame synchronizer operation, or 3D-DNR nonconcurrent operation.

- 64 Mb SDR SDRAM minimum memory requirement
- The memory architecture required is four banks of 1 Mb × 16 (4M16)
- Speed grade of 133 MHz at CAS latency (CL) 3 is required
- 22 Ω series termination resistors are recommended for this configuration
- Recommended memory that is compatible with the ADV7800 includes the MT48LC4M16A2 from Micron

### DOUBLE DATA RATE (DDR)

The ADV7800 uses DDR external memory for simultaneous 3D comb, frame synchronizer, and 3D-DNR operation.

- 128 Mb DDR SDRAM minimum memory requirement
- The memory architecture required is four banks of 2 Mb × 16 (8M16)
- Speed grade of 133 MHz at CAS latency (CL) 2.5 is required
- Termination resistors not recommended for this configuration
- Recommended memory that is compatible with the ADV7800 includes K4H281638B-TCB0 from Samsung, the MT46V8M16-TGP-75 from Micron, and the HYB25D128160CE-6 from Infineon



## RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

The external loop filter components for the ELPF pins should be placed as close as possible to the respective pins. Figure 8 shows the recommended component values.

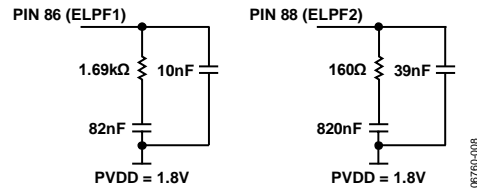


Figure 8. ELPF Components

TYPICAL CONNECTION DIAGRAMS

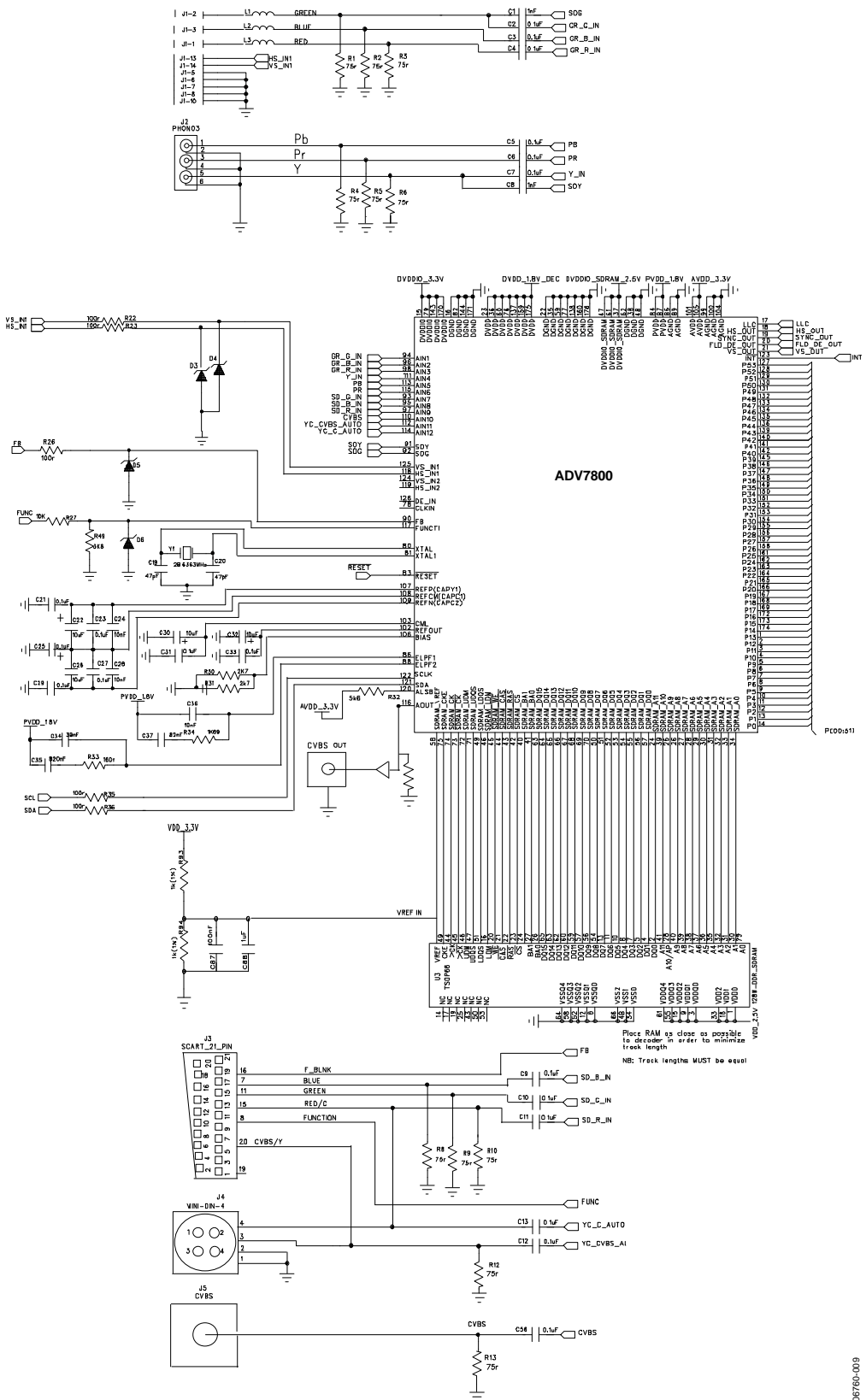


Figure 9. Typical Connection Diagram (External DDR Memory)

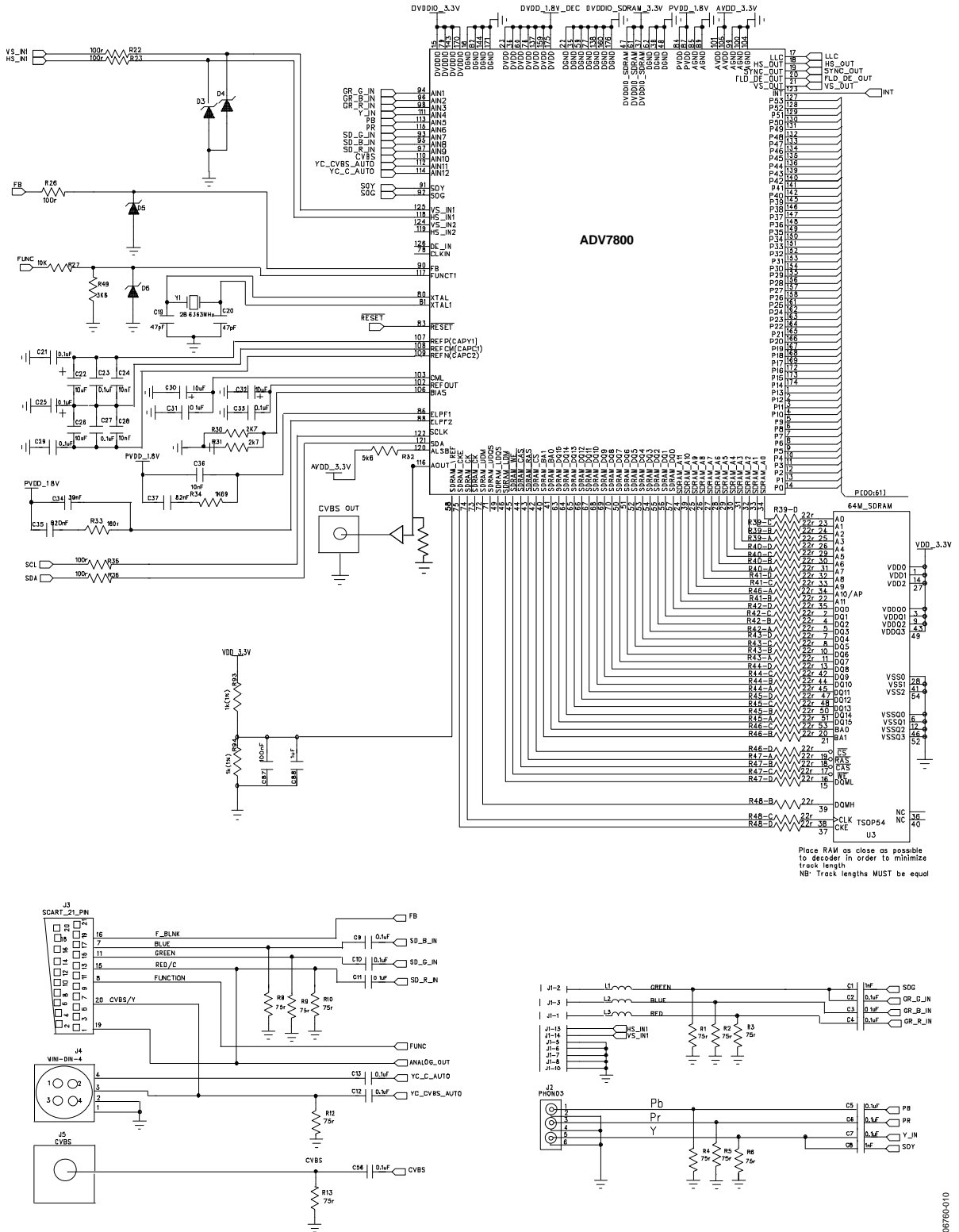


Figure 10. Typical Connection Diagram (External SDR Memory)

087800-010

## PIXEL INPUT/OUTPUT FORMATTING

There are several modes in which the ADV7800 pixel port can be configured. These modes are under the I<sup>2</sup>C control of OP\_FORMAT\_SEL[5:0].

### PIXEL DATA OUTPUT MODES HIGHLIGHTS

The ADV7800 has a flexible pixel port, which can be configured in a variety of formats to accommodate downstream ICs. See Table 8 and Table 9 for more information on each mode. The output pixel port features include

- 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS\_OUT, VS\_OUT, and FLD\_DE\_OUT pin timing
- 16-/20-/24-bit YCrCb with embedded time codes and/or HS\_OUT, VS\_OUT, and FLD\_DE\_OUT pin timing
- 24-/30-bit YCrCb/RGB with embedded time codes and/or HS\_OUT, VS\_OUT, and FLD\_DE\_OUT pin timing

- DDR 8-/10-bit 4:2:2 YCrCb for all standards
- DDR 24-/30-bit 4:4:4 RGB for all standards
- Simultaneous output modes 16-/20-bit YCrCb and 8-/10-bit 4:2:2 YCrCb up to 525i/525p and 625i/625p

### DIGITAL VIDEO INPUT PORT HIGHLIGHTS

The ADV7800 contains a 24-bit digital input port. Main features are as follows:

- Support for 24-bit RGB input data from the DVI/HDMI Rx IC, pass-through, or output converted to 4:2:2 YCrCb
- Support for 24-bit 4:4:4, 16-/20-bit 4:2:2 525i, 625i, 525p, 625p, 1080i, 720p, 1080p, and VGA to SXGA at 75 Hz input data from the DVI/HDMI Rx IC chip, pass-through, or output converted to 4:2:2 YCrCb
- Dedicated synchronization and pixel port inputs

Table 8. SDR Pixel Port Output Modes<sup>1</sup>

OP_FORMAT_SEL [5:0]	0x00	0x01	0x05	0x06	0x0A	0x2C
Pixel Output	8-Bit SDR ITU-656 Mode 1	10-Bit SDR ITU-656 Mode 1	16-Bit SDR ITU-656 4:2:2 Mode 1	20-Bit SDR ITU-656 4:2:2 Mode 1	24-Bit SDR 4:4:4 Mode 1	24-Bit SDR 4:4:4 Mode 2
P29	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y7	Y9	G7	G7
P28	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y6	Y8	G6	G6
P27	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y5	Y7	G5	G5
P26	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y4	Y6	G4	G4
P25	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y3	Y5	G3	G3
P24	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y2	Y4	G2	G2
P23	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y1	Y3	G1	G1
P22	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y0	Y2	G0	G0
P21	Z	Y1, Cb1, Cr1	Z	Y1	Z	B7
P20	Z	Y0, Cb0, Cr0	Z	Y0	Z	B6
P19	Z	Z	Cb7, Cr7	Cb9, Cr9	B7	B5
P18	Z	Z	Cb6, Cr6	Cb8, Cr8	B6	B4
P17	Z	Z	Cb5, Cr5	Cb7, Cr7	B5	B3
P16	Z	Z	Cb4, Cr4	Cb6, Cr6	B4	B2
P15	Z	Z	Cb3, Cr3	Cb5, Cr5	B3	B1
P14	Z	Z	Cb2, Cr2	Cb4, Cr4	B2	B0
P13	Z	Z	Cb1, Cr1	Cb3, Cr3	B1	R7
P12	Z	Z	Cb0, Cr0	Cb2, Cr2	B0	R6
P11	Z	Z	Z	Cb1, Cr1	Z	R5
P10	Z	Z	Z	Cb0, Cr0	Z	R4
P9	Z	Z	Z	Z	R7	R3
P8	Z	Z	Z	Z	R6	R2
P7	Z	Z	Z	Z	R5	R1
P6	Z	Z	Z	Z	R4	R0
P5	Z	Z	Z	Z	R3	Z
P4	Z	Z	Z	Z	R2	Z
P3	Z	Z	Z	Z	R1	Z
P2	Z	Z	Z	Z	R0	Z
P1	Z	Z	Z	Z	Z	Z
P0	Z	Z	Z	Z	Z	Z

<sup>1</sup> It is recommended to print this table (located on this page and the following page) and read as one horizontal expanded table.

OP_FORMAT_SEL [5:0]	0x2D	0x2E	0x0B	0x28	0x29
Pixel Output	24-Bit SDR 4:4:4 Mode 1	24-Bit SDR 4:4:4 Mode 1	30-Bit SDR 4:4:4 Mode 1	16-Bit and 8-Bit SDR 4:2:2 Mode 1 Parallel Output	20-Bit and 10-Bit SDR 4:2:2 Mode 1 Parallel Output
P29	R7	B7	G9	Main Y7	Main Y9
P28	R6	B6	G8	Main Y6	Main Y8
P27	R5	B5	G7	Main Y5	Main Y7
P26	R4	B4	G6	Main Y4	Main Y6
P25	R3	B3	G5	Main Y3	Main Y5
P24	R2	B2	G4	Main Y2	Main Y4
P23	R1	B1	G3	Main Y1	Main Y3
P22	R0	B0	G2	Main Y0	Main Y2
P21	G7	R7	G1	Z	Main Y1
P20	G6	R6	G0	Z	Main Y0
P19	G5	R5	B9	Main Cb7, Cr7	Main Cb9, Cr9
P18	G4	R4	B8	Main Cb6, Cr6	Main Cb8, Cr8
P17	G3	R3	B7	Main Cb5, Cr5	Main Cb7, Cr7
P16	G2	R2	B6	Main Cb4, Cr4	Main Cb6, Cr6
P15	G1	R1	B5	Main Cb3, Cr3	Main Cb5, Cr5
P14	G0	R0	B4	Main Cb2, Cr2	Main Cb4, Cr4
P13	B7	G7	B3	Main Cb1, Cr1	Main Cb3, Cr3
P12	B6	G6	B2	Main Cb0, Cr0	Main Cb2, Cr2
P11	B5	G5	B1	Z	Main Cb1, Cr1
P10	B4	G4	B0	Z	Main Cb0, Cr0
P9	B3	G3	R9	Aux Y7, Cb7, Cr7	Aux Y9, Cb9, Cr9
P8	B2	G2	R8	Aux Y6, Cb6, Cr6	Aux Y8, Cb8, Cr8
P7	B1	G1	R7	Aux Y5, Cb5, Cr5	Aux Y7, Cb7, Cr7
P6	B0	G0	R6	Aux Y4, Cb4, Cr4	Aux Y6, Cb6, Cr6
P5	Z	Z	R5	Aux Y3, Cb3, Cr3	Aux Y5, Cb5, Cr5
P4	Z	Z	R4	Aux Y2, Cb2, Cr2	Aux Y4, Cb4, Cr4
P3	Z	Z	R3	Aux Y1, Cb1, Cr1	Aux Y3, Cb3, Cr3
P2	Z	Z	R2	Aux Y0, Cb0, Cr0	Aux Y2, Cb2, Cr2
P1	Z	Z	R1	Z	Aux Y1, Cb1, Cr1
P0	Z	Z	R0	Z	Aux Y0, Cb0, Cr0

Table 9. DDR Pixel Port Output Modes<sup>1</sup>

OP_FORMAT_SEL [5:0]	0x10		0x11		0x3D		0x3E	
Pixel Output	8-Bit DDR ITU-656		10-Bit DDR ITU-656		24-Bit DDR 4:2:2 RGB (CLK/2) Mode 1		24-Bit DDR 4:2:2 RGB (CLK/2) mode 2	
	Clock Rise	Clock Fall	Clock Rise	Clock Fall	Clock Rise	Clock Fall	Clock Rise	Clock Fall
P29	Cb7, Cr7	Y7	Cb9, Cr9	Y9	B7-0	B7-1	R7-0	R7-1
P28	Cb6, Cr6	Y6	Cb8, Cr8	Y8	B6-0	B6-1	R6-0	R6-1
P27	Cb5, Cr5	Y5	Cb7, Cr7	Y7	B5-0	B5-1	R5-0	R5-1
P26	Cb4, Cr4	Y4	Cb6, Cr6	Y6	B4-0	B4-1	R4-0	R4-1
P25	Cb3, Cr3	Y3	Cb5, Cr5	Y5	B3-0	B3-1	R3-0	R3-1
P24	Cb2, Cr2	Y2	Cb4, Cr4	Y4	B2-0	B2-1	R2-0	R2-1
P23	Cb1, Cr1	Y1	Cb3, Cr3	Y3	B1-0	B1-1	R1-0	R1-1
P22	Cb0, Cr0	Y0	Cb2, Cr2	Y2	B0-0	B0-1	R0-0	R0-1
P21	Z	Z	Cb1, Cr1	Y1	R7-0	R7-1	G7-0	G7-1
P20	Z	Z	Cb0, Cr0	Y0	R6-0	R6-1	G6-0	G6-1
P19	Z	Z	Z	Z	R5-0	R5-1	G5-0	G5-1
P18	Z	Z	Z	Z	R4-0	R4-1	G4-0	G4-1
P17	Z	Z	Z	Z	R3-0	R3-1	G3-0	G3-1
P16	Z	Z	Z	Z	R2-0	R2-1	G2-0	G2-1
P15	Z	Z	Z	Z	R1-0	R1-1	G1-0	G1-1
P14	Z	Z	Z	Z	R7-0	R7-1	G0-0	G0-1
P13	Z	Z	Z	Z	G7-0	G7-1	B7-0	B7-1
P12	Z	Z	Z	Z	G6-0	G6-1	B6-0	B6-1
P11	Z	Z	Z	Z	G5-0	G5-1	B5-0	B5-1
P10	Z	Z	Z	Z	G4-0	G4-1	B4-0	B4-1
P9	Z	Z	Z	Z	G3-0	G3-1	B3-0	B3-1
P8	Z	Z	Z	Z	G2-0	G2-1	B2-0	B2-1
P7	Z	Z	Z	Z	G1-0	G1-1	B1-0	B1-1
P6	Z	Z	Z	Z	G0-0	G0-1	B0-0	B0-1
P5	Z	Z	Z	Z	Z	Z	Z	Z
P4	Z	Z	Z	Z	Z	Z	Z	Z
P3	Z	Z	Z	Z	Z	Z	Z	Z
P2	Z	Z	Z	Z	Z	Z	Z	Z
P1	Z	Z	Z	Z	Z	Z	Z	Z
P0	Z	Z	Z	Z	Z	Z	Z	Z

<sup>1</sup> It is recommended to print this table (located on this page and the following page) and read as one horizontal expanded table.

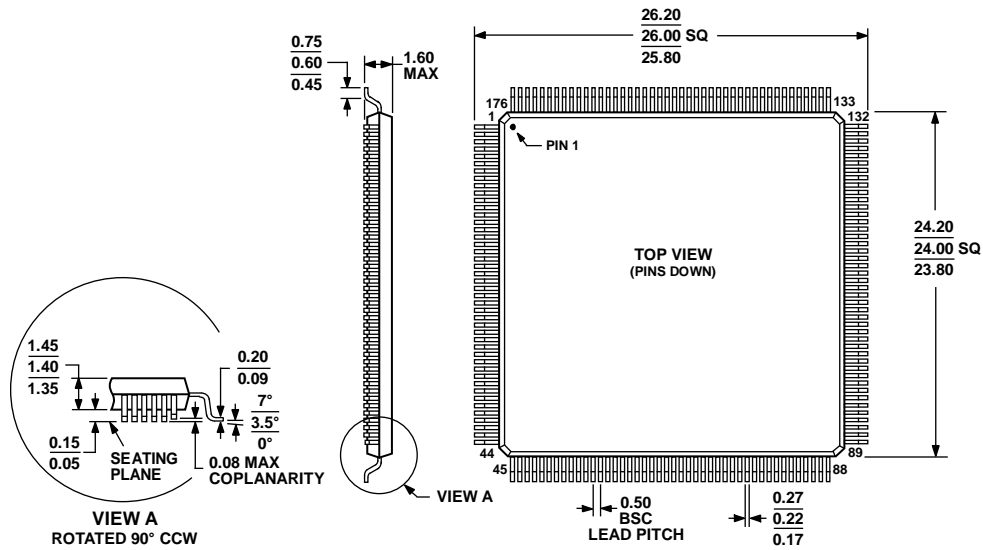
OP_FORMAT_SEL [5:0]	0x38		0x39		0x3C	
Pixel Output	16-Bit and 8-Bit DDR 4:2:2 Mode 1 Parallel Output (CLK/2)		20-Bit and 10-Bit DDR 4:2:2 Mode 1 Parallel Output (CLK/2)		24-Bit DDR 4:2:2RGB (CLK/2)	
	Clock Rise	Clock Fall	Clock Rise	Clock Fall	Clock Rise	Clock Fall
P29	Main Y7	Main Y7	Main Y9	Main Y9	G7-0	G7-1
P28	Main Y6	Main Y6	Main Y8	Main Y8	G6-0	G6-1
P27	Main Y5	Main Y5	Main Y7	Main Y7	G5-0	G5-1
P26	Main Y4	Main Y4	Main Y6	Main Y6	G4-0	G4-1
P25	Main Y3	Main Y3	Main Y5	Main Y5	G3-0	G3-1
P24	Main Y2	Main Y2	Main Y4	Main Y4	G2-0	G2-1
P23	Main Y1	Main Y1	Main Y3	Main Y3	G1-0	G1-1
P22	Main Y0	Main Y0	Main Y2	Main Y2	G0-0	G0-1
P21	Z	Z	Main Y1	Main Y1	B7-0	B7-1
P20	Z	Z	Main Y0	Main Y0	B6-0	B6-1
P19	Main Cb7	Main Cr7	Main Cb9	Main Cr9	B5-0	B5-1
P18	Main Cb6	Main Cr6	Main Cb8	Main Cr8	B4-0	B4-1
P17	Main Cb5	Main Cr5	Main Cb7	Main Cr7	B3-0	B3-1
P16	Main Cb4	Main Cr4	Main Cb6	Main Cr6	B2-0	B2-1
P15	Main Cb3	Main Cr3	Main Cb5	Main Cr5	B1-0	B1-1
P14	Main Cb2	Main Cr2	Main Cb4	Main Cr4	B0-0	B0-1
P13	Main Cb1	Main Cr1	Main Cb3	Main Cr3	R7-0	R7-1
P12	Main Cb0	Main Cr0	Main Cb2	Main Cr2	R6-0	R6-1
P11	Z	Z	Main Cb1	Main Cr1	R5-0	R5-1
P10	Z	Z	Main Cb0	Main Cr0	R4-0	R4-1
P9	Aux Cb7, Cr7	Aux Y7	Aux Cb9, Cr9	Aux Y9	R3-0	R3-1
P8	Aux Cb6, Cr6	Aux Y6	Aux Cb8, Cr8	Aux Y8	R2-0	R2-1
P7	Aux Cb5, Cr5	Aux Y5	Aux Cb7, Cr7	Aux Y7	R1-0	R1-1
P6	Aux Cb4, Cr4	Aux Y4	Aux Cb6, Cr6	Aux Y6	R0-0	R0-1
P5	Aux Cb3, Cr3	Aux Y3	Aux Cb5, Cr5	Aux Y5	Z	Z
P4	Aux Cb2, Cr2	Aux Y2	Aux Cb4, Cr4	Aux Y4	Z	Z
P3	Aux Cb1, Cr1	Aux Y1	Aux Cb3, Cr3	Aux Y3	Z	Z
P2	Aux Cb0, Cr0	Aux Y0	Aux Cb2, Cr2	Aux Y2	Z	Z
P1	Z	Z	Aux Cb1, Cr1	Aux Y1	Z	Z
P0	Z	Z	Aux Cb0, Cr0	Aux Y0	Z	Z



Table 10. Pixel Port Input Modes

IP_DATA_SEL[5:0]	0x00	0x01	0x04	0x06	0x07
Pixel Input	24-Bit 4:4:4 Input	20-Bit 4:2:2 Input	16-Bit 4:2:2 Input	10-Bit 4:2:2 Input	8-Bit 4:2:2 Input
P53	G7	Y9	Y7	Y9, Cb9, Cr9	Y7, Cb7, Cr7
P52	G6	Y8	Y6	Y8, Cb8, Cr8	Y6, Cb6, Cr6
P51	G5	Y7	Y5	Y7, Cb7, Cr7	Y5, Cb5, Cr5
P50	G4	Y6	Y4	Y6, Cb6, Cr6	Y4, Cb4, Cr4
P49	G3	Y5	Y3	Y5, Cb5, Cr5	Y3, Cb3, Cr3
P48	G2	Y4	Y2	Y4, Cb4, Cr4	Y2, Cb2, Cr2
P47	G1	Y3	Y1	Y3, Cb3, Cr3	Y1, Cb1, Cr1
P46	G0	Y2	Y0	Y2, Cb2, Cr2	Y0, Cb0, Cr0
P45	B7	Cb9, Cr9	Cb7, Cr7	Y1, Cb1, Cr1	Z
P44	B6	Cb8, Cr8	Cb6, Cr6	Y0, Cb0, Cr0	Z
P43	B5	Cb7, Cr7	Cb5, Cr5	Z	Z
P42	B4	Cb6, Cr6	Cb4, Cr4	Z	Z
P41	B3	Cb5, Cr5	Cb3, Cr3	Z	Z
P40	B2	Cb4, Cr4	Cb2, Cr2	Z	Z
P39	B1	Cb3, Cr3	Cb1, Cr1	Z	Z
P38	B0	Cb2, Cr2	Cb0, Cr0	Z	Z
P37	R7	Y1	Z	Z	Z
P36	R6	Y0	Z	Z	Z
P35	R5	Z	Z	Z	Z
P34	R4	Z	Z	Z	Z
P33	R3	Cb1, Cr1	Z	Z	Z
P32	R2	Cb0, Cr0	Z	Z	Z
P31	R1	Z	Z	Z	Z
P30	R0	Z	Z	Z	Z

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BG A

Figure 11. 176-Lead Low Profile Quad Flat Package [LQFP] (ST-176)

Dimensions shown in millimeters

051706-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADV7800BSTZ-80	0°C to +85°C	176-Lead Low Profile Quad Flat Package (LQFP)	ST-176
ADV7800BSTZ-150	0°C to +85°C	176-Lead Low Profile Quad Flat Package (LQFP)	ST-176
EVAL-ADV7800EB1Z		Evaluation Board (External DDR SD Memory)	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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