# SGM7229
# High-Speed USB 2.0 (480Mbps) DPDT Analog Switch

## GENERAL DESCRIPTION

The SGM7229 is a DPDT (double-pole/double-throw) analog switch. It operates from a 1.8V to 5.5V single power supply. Each switch of the SGM7229 is bidirectional, which can ensure that the high speed signals have little or no attenuation at the outputs.

The SGM7229 features high speed, low bit-to-bit skew and wide bandwidth. These high performances make it very suitable for multiple applications, such as cellular phones and computer peripherals, etc.

The SGM7229 has power-off and power-on protections. Because of the special circuitry on the D+/D- pins, the device will not be damaged even if $V_{BUS}$ short-circuit occurs during data transmission. In addition, it can prevent accidental from leaking and ensure system reliability under power-down and over-voltage conditions.

The SGM7229 is available in Green MSOP-10 and UTQFN-1.8×1.4-10L packages. It operates over an ambient temperature range of -40℃ to +85℃.

## FEATURES

- **Single Supply Voltage Range: 1.8V to 5.5V**
- **On-Resistance: 6Ω (TYP) at 3V**
- **High Off-Isolation: -26dB ($R_L$ = 50Ω, f = 250MHz)**
- **Low Crosstalk: -20dB ($R_L$ = 50Ω, f = 250MHz)**
- **-3dB Bandwidth: 850MHz**
- **Fast Switching Times at $V_{CC}$ = 3.3V:**
  - **$t_{ON}$ = 30ns**
  - **$t_{OFF}$ = 18ns**
- **Break-Before-Make Switching**
- **Rail-to-Rail Input and Output Operation**
- **Power-Off and Power-On Protections**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green UTQFN-1.8×1.4-10L and MSOP-10 Packages**

## APPLICATIONS

Cellular Phones
Digital Cameras
Portable Equipment
Computer Peripherals
Battery-Powered Systems
Routes Signals for USB 2.0 Full-Speed

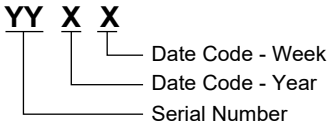
# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM7229 | UTQFN-1.8×1.4-10L | -40℃ to +85℃ | SGM7229YUWQ10G/TR | NDXX | Tape and Reel, 3000 |
| | MSOP-10 | -40℃ to +85℃ | SGM7229YMS10G/TR | SGM7229<br>YMS10<br>XXXXX | Tape and Reel, 4000 |

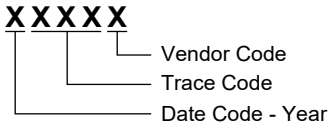
## MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

**UTQFN-1.8×1.4-10L**




**MSOP-10**




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND ..... 0V to 6V
Analog, Digital Voltage Range ..... -0.3V to $V_{CC}$ + 0.3V
Continuous Current HSDn or Dn ..... ±50mA
Peak Current HSDn or Dn ..... ±100mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 2500V
MM ..... 400V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

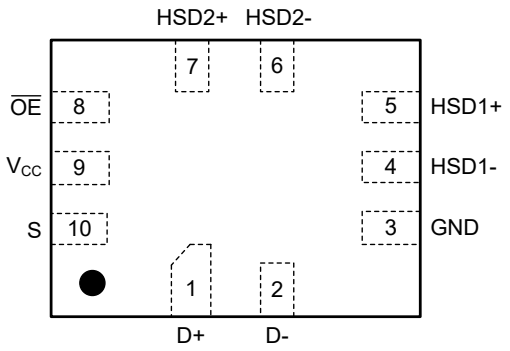
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

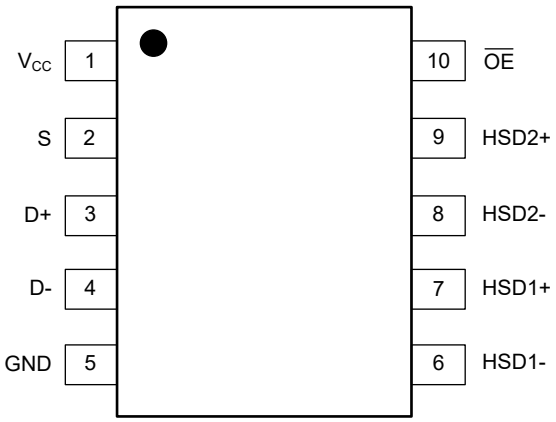
## PIN CONFIGURATIONS

(TOP VIEW)




UTQFN-1.8×1.4-10L

(TOP VIEW)

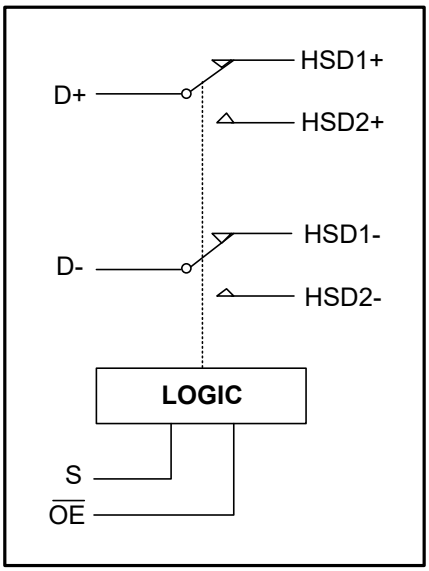



MSOP-10

## PIN DESCRIPTION

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| UTQFN-1.8×1.4-10L | MSOP-10 | | |
| 1 | 3 | D+ | USB Data Bus. |
| 2 | 4 | D- | USB Data Bus. |
| 3 | 5 | GND | Ground. |
| 4 | 6 | HSD1- | Multiplexed Source Input. |
| 5 | 7 | HSD1+ | Multiplexed Source Input. |
| 6 | 8 | HSD2- | Multiplexed Source Input. |
| 7 | 9 | HSD2+ | Multiplexed Source Input. |
| 8 | 10 | $\overline{OE}$ | Output Enable Control Pin. |
| 9 | 1 | $V_{CC}$ | Positive Power Supply Pin. |
| 10 | 2 | S | Select Input Pin. |

## BLOCK DIAGRAM




## FUNCTION TABLE

| $\overline{OE}$ | S | HSD1+, HSD1- | HSD2+, HSD2- |
|---|---|---|---|
| 0 | 0 | ON | OFF |
| 0 | 1 | OFF | ON |
| 1 | × | OFF | OFF |

NOTE: Switches shown for logic "0" input.

# ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.3V, Full = -40℃ to +85℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog I/O Voltage (HSD1+, HSD1-, HSD2+, HSD2-) | $V_{IS}$ | | Full | 0 | | $V_{CC}$ | V |
| On-Resistance | $R_{ON}$ | $V_{CC}$ = 3V, $V_{IS}$ = 0V to 0.4V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 6 | 7 | Ω |
| | | | Full | | | 8 | |
| On-Resistance Match between Channels | $\Delta R_{ON}$ | $V_{CC}$ = 3V, $V_{IS}$ = 0V to 0.4V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 0.2 | 0.8 | Ω |
| | | | Full | | | 0.9 | |
| On-Resistance Flatness | $R_{FLAT(ON)}$ | $V_{CC}$ = 3V, $V_{IS}$ = 0V to 1V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 2 | 3 | Ω |
| | | | Full | | | 3.5 | |
| Increase in $I_{CC}$ per Control Voltage | $I_{CCT}$ | $V_{CC}$ = 3.6V, $V_S$ or $V_{\overline{OE}}$ = 1.8V | +25℃ | | 2 | 3 | μA |
| | | | Full | | | 3.5 | |
| Power Off Leakage Current (D+, D-) | $I_{OFF}$ | $V_{CC}$ = 0V, $V_D$ = 0V to 3.6V, $V_S$, $V_{\overline{OE}}$ = 0V or 3.6V | Full | | | 0.5 | μA |
| Source Off Leakage Current | $I_{HSD2(OFF)}$, $I_{HSD1(OFF)}$ | $V_{CC}$ = 3.6V, $V_{IS}$ = 3.3V/0.3V, $V_D$ = 0.3V/3.3V | Full | | | 0.5 | μA |
| Channel On Leakage Current | $I_{HSD2(ON)}$, $I_{HSD1(ON)}$ | $V_{CC}$ = 3.6V, $V_{IS}$ = 3.3V/0.3V, $V_D$ = 3.3V/0.3V or floating | Full | | | 0.5 | μA |
| **DIGITAL INPUTS** | | | | | | | |
| Input High Voltage | $V_{IH}$ | | Full | 1.5 | | | V |
| Input Low Voltage | $V_{IL}$ | | Full | | | 0.4 | V |
| Input Leakage Current | $I_{IN}$ | $V_S$, $V_{\overline{OE}}$ = 0V or $V_{CC}$ | Full | | | 0.5 | μA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{IS}$ = 0.8V, $R_L$ = 50Ω, $C_L$ = 10pF, Test Circuit 2 | +25℃ | | 30 | | ns |
| Turn-Off Time | $t_{OFF}$ | | +25℃ | | 18 | | ns |
| Break-Before-Make Time Delay | $t_D$ | $V_{IS}$ = 0.8V, $R_L$ = 50Ω, $C_L$ = 10pF, Test Circuit 3 | +25℃ | | 14 | | ns |
| Propagation Delay | $t_{PD}$ | $R_L$ = 50Ω, $C_L$ = 10pF | +25℃ | | 0.5 | | ns |
| Off Isolation | $O_{ISO}$ | Signal = 0dBm, $R_L$ = 50Ω, f = 250MHz, Test Circuit 4 | +25℃ | | -26 | | dB |
| Channel-to-Channel Crosstalk | $X_{TALK}$ | Signal = 0dBm, $R_L$ = 50Ω, f = 250MHz, Test Circuit 5 | +25℃ | | -20 | | dB |
| -3dB Bandwidth | BW | Signal = 0dBm, $R_L$ = 50Ω, $C_L$ = 5pF, Test Circuit 6 | +25℃ | | 850 | | MHz |
| Channel-to-Channel Skew | $t_{SKEW}$ | $R_L$ = 50Ω, $C_L$ = 10pF | +25℃ | | 0.5 | | ns |
| Charge Injection Select Input to Common I/O | Q | $V_G$ = GND, $C_L$ = 1nF, $R_G$ = 0Ω, Q = $C_L$ × $V_{OUT}$, Test Circuit 7 | +25℃ | | 2.5 | | pC |
| HSD+, HSD-, D+, D- On-Capacitance | $C_{ON}$ | f = 1MHz | +25℃ | | 8 | | pF |

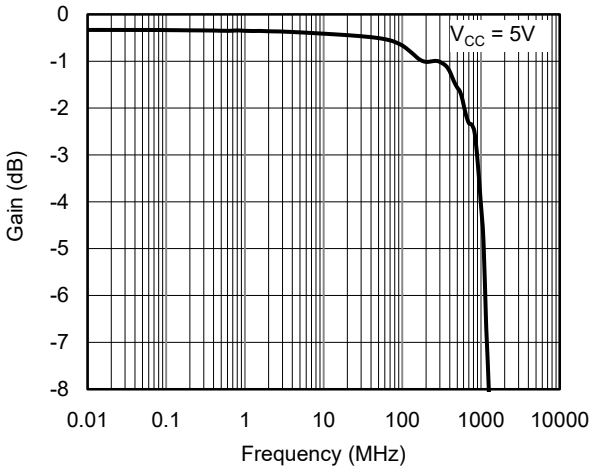
## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 5V, Full = -40℃ to +85℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

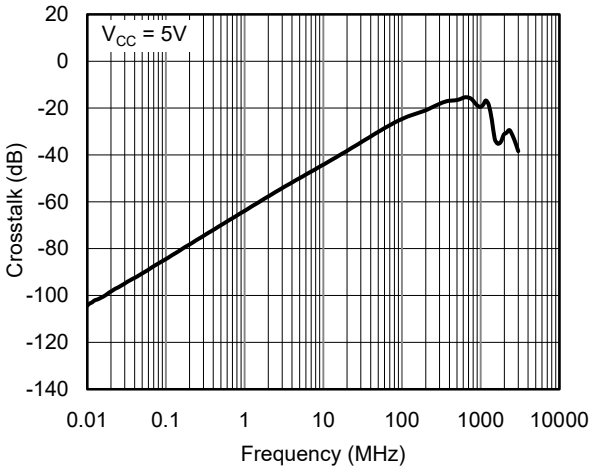
| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog I/O Voltage (HSD1+, HSD1-, HSD2+, HSD2-) | $V_{IS}$ | | Full | 0 | | $V_{CC}$ | V |
| On-Resistance | $R_{ON}$ | $V_{IS}$ = 0V to 0.4V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 4.5 | 5.5 | Ω |
| | | | Full | | | 6.5 | |
| On-Resistance Match between Channels | $\Delta R_{ON}$ | $V_{IS}$ = 0V to 0.4V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 0.2 | 0.8 | Ω |
| | | | Full | | | 0.9 | |
| On-Resistance Flatness | $R_{FLAT(ON)}$ | $V_{IS}$ = 0V to 1V, $I_D$ = 8mA, Test Circuit 1 | +25℃ | | 0.5 | 0.75 | Ω |
| | | | Full | | | 0.9 | |
| Increase in $I_{CC}$ per Control Voltage | $I_{CCT}$ | $V_{CC}$ = 5.5V, $V_S$ or $V_{\overline{OE}}$ = 1.8V | +25℃ | | 14 | 18 | μA |
| | | | Full | | | 22 | |
| Power Off Leakage Current (D+, D-) | $I_{OFF}$ | $V_{CC}$ = 0V, $V_D$ = 0V to 5.5V, $V_S$, $V_{\overline{OE}}$ = 0V or 5.5V | Full | | | 0.5 | μA |
| Source Off Leakage Current | $I_{HSD2(OFF)}$, $I_{HSD1(OFF)}$ | $V_{CC}$ = 5.5V, $V_{IS}$ = 4.5V/1V, $V_D$ = 1V/4.5V | Full | | | 0.5 | μA |
| Channel On Leakage Current | $I_{HSD2(ON)}$, $I_{HSD1(ON)}$ | $V_{CC}$ = 5.5V, $V_{IS}$ = 4.5V/1V, $V_D$ = 4.5V/1V or floating | Full | | | 0.5 | μA |
| **DIGITAL INPUTS** | | | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{CC}$ = 5.5V | Full | 1.8 | | | V |
| Input Low Voltage | $V_{IL}$ | $V_{CC}$ = 5.5V | Full | | | 0.6 | V |
| Input Leakage Current | $I_{IN}$ | $V_{CC}$ = 5.5V, $V_S$, $V_{\overline{OE}}$ = 0V or $V_{CC}$ | Full | | | 0.5 | μA |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{IS}$ = 0.8V, $R_L$ = 50Ω, $C_L$ = 10pF, Test Circuit 2 | +25℃ | | 22 | | ns |
| Turn-Off Time | $t_{OFF}$ | | +25℃ | | 14 | | ns |
| Break-Before-Make Time Delay | $t_D$ | $V_{IS}$ = 0.8V, $R_L$ = 50Ω, $C_L$ = 10pF, Test Circuit 3 | +25℃ | | 9 | | ns |
| Propagation Delay | $t_{PD}$ | $R_L$ = 50Ω, $C_L$ = 10pF | +25℃ | | 0.5 | | ns |
| Off Isolation | $O_{ISO}$ | Signal = 0dBm, $R_L$ = 50Ω, f = 250MHz, Test Circuit 4 | +25℃ | | -26 | | dB |
| Channel-to-Channel Crosstalk | $X_{TALK}$ | Signal = 0dBm, $R_L$ = 50Ω, f = 250MHz, Test Circuit 5 | +25℃ | | -20 | | dB |
| -3dB Bandwidth | BW | Signal = 0dBm, $R_L$ = 50Ω, $C_L$ = 5pF, Test Circuit 6 | +25℃ | | 850 | | MHz |
| Channel-to-Channel Skew | $t_{SKEW}$ | $R_L$ = 50Ω, $C_L$ = 10pF | +25℃ | | 0.5 | | ns |
| Charge Injection Select Input to Common I/O | Q | $V_G$ = GND, $C_L$ = 1nF, $R_G$ = 0Ω, Q = $C_L$ × $V_{OUT}$, Test Circuit 7 | +25℃ | | 3.5 | | pC |
| HSD+, HSD-, D+, D- On-Capacitance | $C_{ON}$ | f = 1MHz | +25℃ | | 8 | | pF |
| **POWER REQUIREMENTS** | | | | | | | |
| Power Supply Range | $V_{CC}$ | | Full | 1.8 | | 5.5 | V |
| Power Supply Current | $I_{CC}$ | $V_{CC}$ = 5.5V, $V_S$, $V_{\overline{OE}}$ = 0V or $V_{CC}$ | Full | | | 0.5 | μA |

## TYPICAL PERFORMANCE CHARACTERISTICS

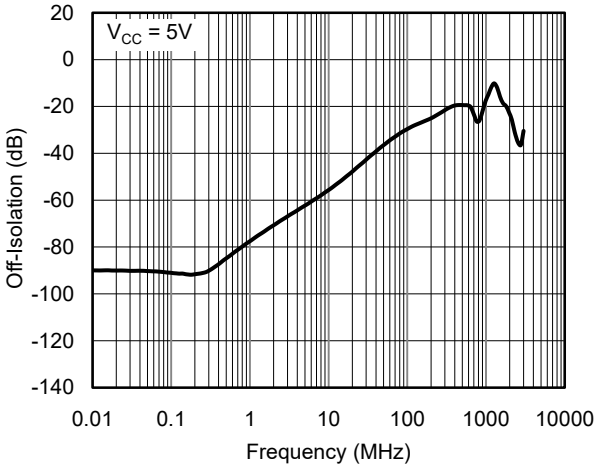
Gain vs. Frequency



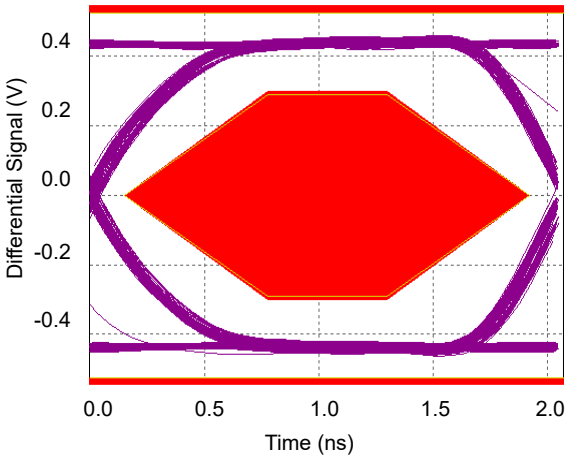

Crosstalk vs. Frequency



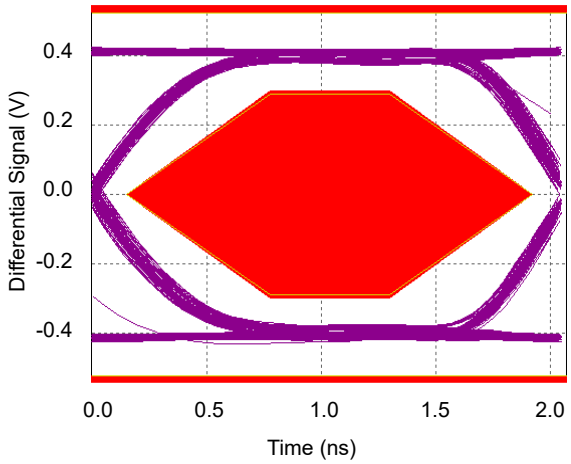

Off-Isolation vs. Frequency



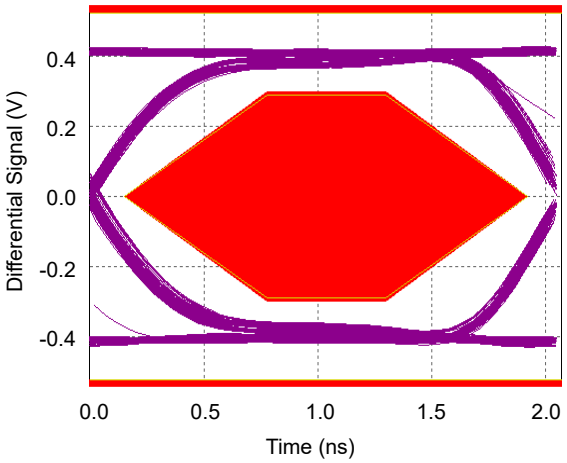

Eye Pattern: 480Mbps USB 2.0 Signal with No Switch (Through Path)



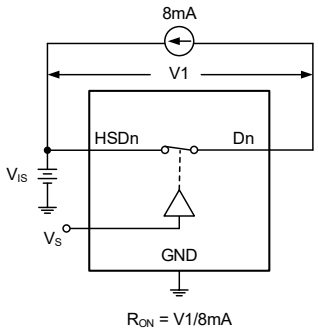

Eye Pattern: 480Mbps USB 2.0 Signal with Switch NO Path



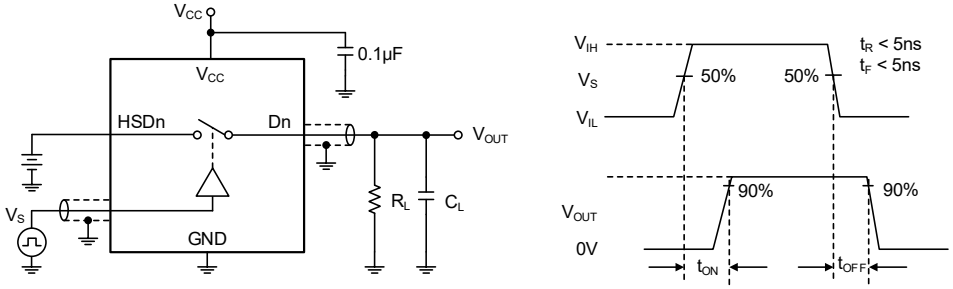

Eye Pattern: 480Mbps USB 2.0 Signal with Switch NC Path



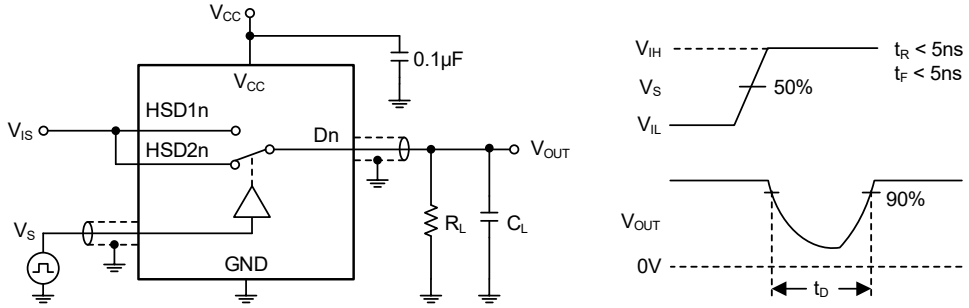
## TEST CIRCUITS



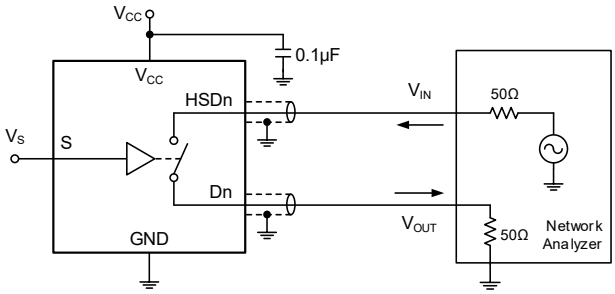

**Test Circuit 1. On-Resistance**




**Test Circuit 2. Switching Times ($t_{ON}$, $t_{OFF}$)**

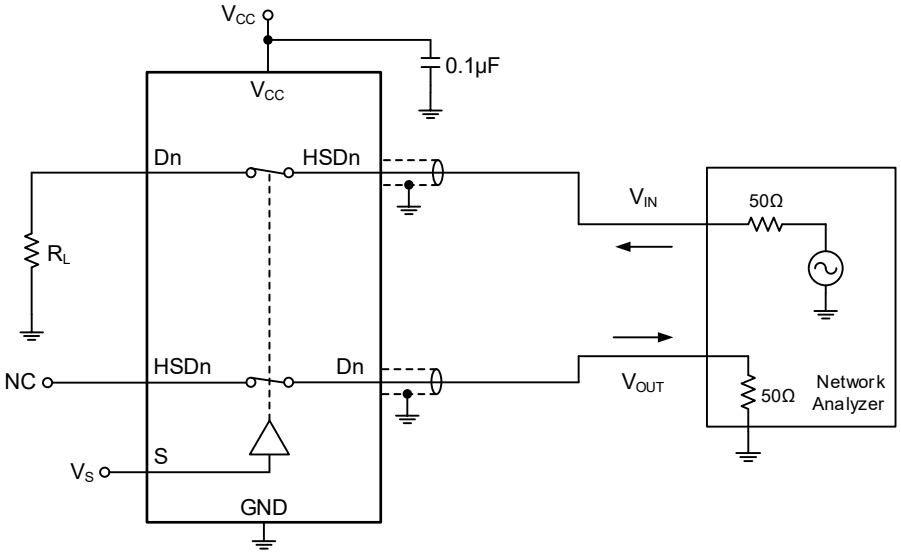



**Test Circuit 3. Break-Before-Make Time Delay ($t_D$)**



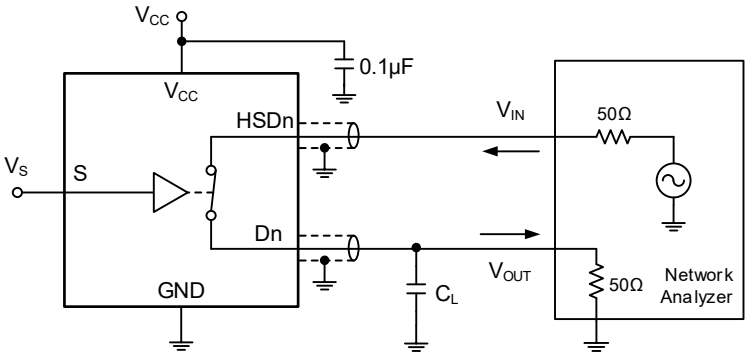

**Test Circuit 4. Off Isolation**

## TEST CIRCUITS (continued)

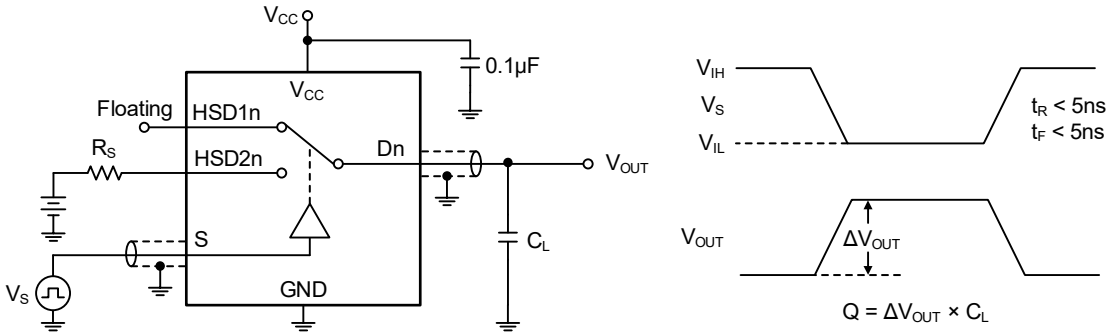



Channel-to-Channel Crosstalk = -20 log ($V_{HSDn}$/$V_{OUT}$)

**Test Circuit 5. Channel-to-Channel Crosstalk**




**Test Circuit 6. -3dB Bandwidth**




**Test Circuit 7. Charge Injection (Q)**

# APPLICATION NOTES

## Meeting USB 2.0 $V_{BUS}$ Short Requirements

### Power-Off Protection

When D+ or D- is shorted to $V_{BUS}$, there is a special protection circuit inside the SGM7229, so that the device will not be damaged within 24 hours. In case of power-down or over-voltage event, the protection circuit can prevent the leakage signal on D+/D- pins to ensure the reliability of the system.

### Power-On Protection

The USB 2.0 specification requires USB device to ensure that the device will not be damaged even if $V_{BUS}$ short-circuit occurs during data transmission. Therefore, under over-voltage conditions, the SGM7229 will limit the current flowing back to the $V_{CC}$ track, and the current will not exceed the safe operating range.

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| December 2021 – REV.A to REV.B | Page |
|---|---|
| Updated Electrical Characteristics section | 5, 6 |

| Changes from Original (DECEMBER 2018) to REV.A | |
|---|---|
| Changed from product preview to production data | All |