TI380C30A
INTEGRATED TOKEN-RING COMMPROCESSOR AND PHYSICAL-LAYER INTERFACE

SPWS034 – MARCH 1998

- **Single-Chip Token-Ring Solution**
- **IBM™ Token-Ring Network™ Compatible**
- **Compatible With ISO/IEC IEEE Std 802.5:1992 Token-Ring Access-Method and Physical-Layer Specifications**
- **Compatible With TI380FPA PacketBlaster™**
- **Glueless Memory Interface**
- **Digital Phase-Locked Loop (PLL)**
  - **Precise Control of Bandwidths**
  - **Improved Jitter Tolerance**
  - **Minimizes Accumulated Phase Slope**
- **Phantom Drive for Physical Insertion Onto Ring**
- **Differential Line Receiver With Level-Dependent Frequency Equalization**
- **Low-Impedance Differential Line Driver to Ease Transmit-Filter Design**
- **On-Chip Watchdog Timer**
- **Internal Crystal Oscillator for Reference-Clock Generation**
- **Expandable LAN-Subsystem Memory up to 2M Bytes**
- **32-Bit Host Address Bus**
- **80x8x or 68xxx-Type Bus and Memory Organization**
- **Dual-Port Direct Memory Access (DMA) and Direct Input/Output Transfers to Host Bus**
- **Supports 8- or 16-Bit Pseudo-Direct Memory Access (PDMA) Operation**
- **Electrostatic Discharge (ESD) Protection Exceeds 2 kV (All Pins)**
- **0.8-μm CMOS Technology**
- **Token-Ring Features**
  - **16- or 4-Megabit-Per-Second (Mbit/s) Data Rates**
  - **Supports up to 18K-Byte Frame Size (16 Mbit/s Only)**
  - **Supports Universal and Local Addressing**
  - **Early Token-Release Option (16 Mbit/s Only)**
  - **Built-In Real-Time Error Detection**
  - **Automatic Frame-Buffer Management**
  - **2-MHz to 33-MHz System-Bus Clock**
  - **Slow-Clock Low-Power Mode**
- **176-Pin Thin Quad Flat Package**

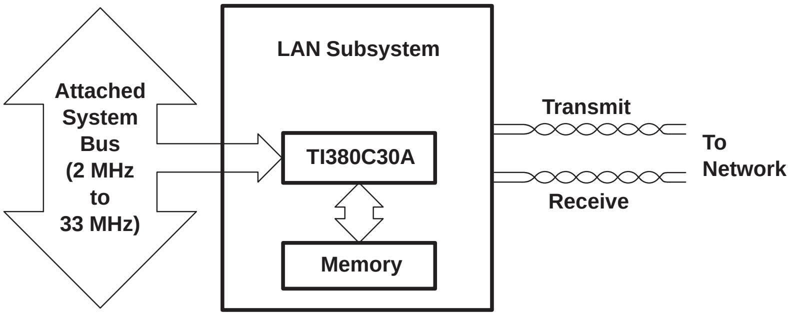

Figure 1. Network-Commprocessor Applications Diagram

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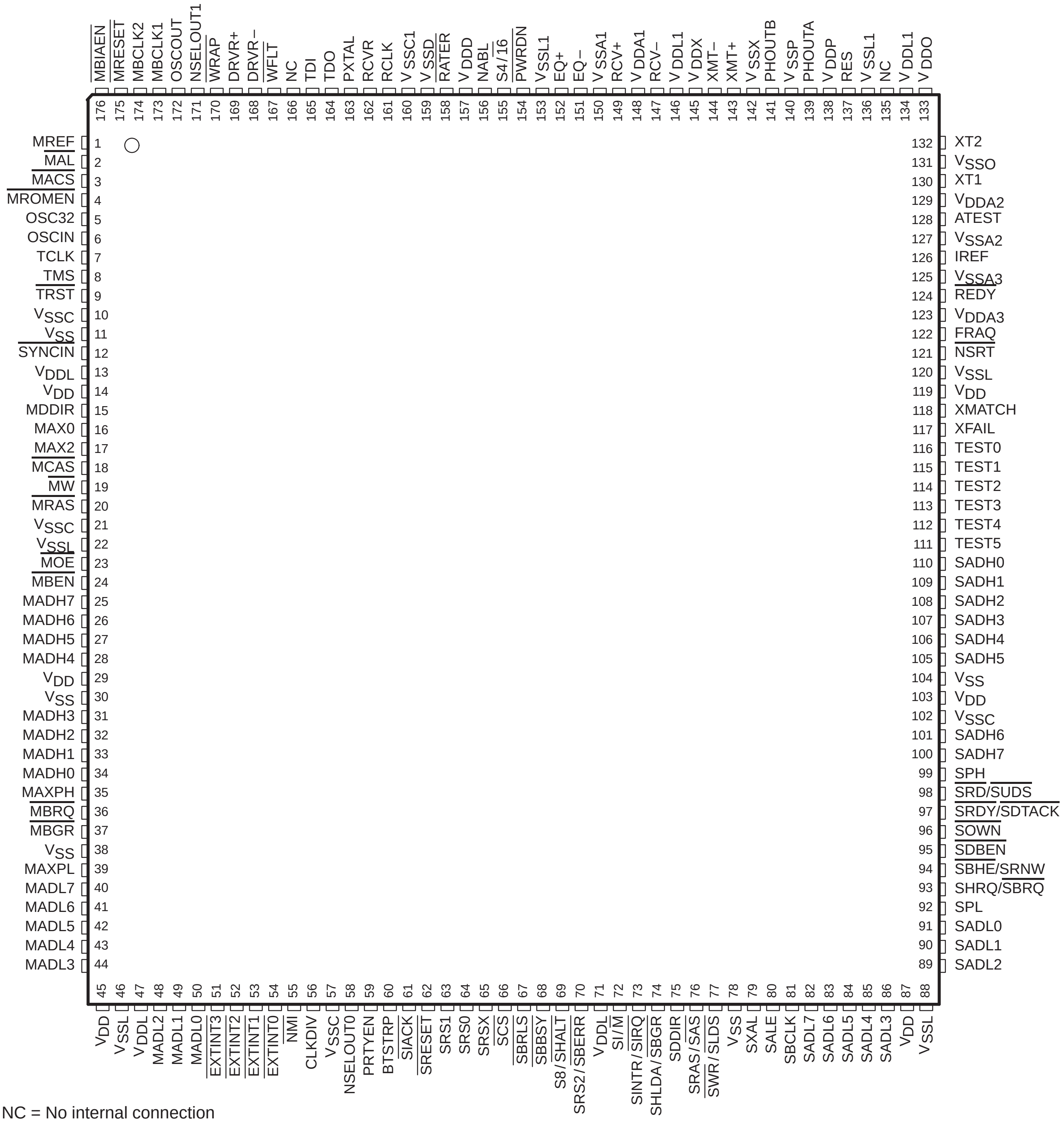
Table 1. Abbreviations and Acronyms

APS	Accumulated Phase Slope
ASF	Adapter-Support Function
ARI/FCI	Address-Recognize Indicator/Frame-Copied Indicator
BIA	Burn-In Address
CAF	Copy All Frames
CG	Clock Generator
CP	Communications Processor
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DIO	Direct Input/Output
DMA	Direct Memory Access
ESD	Electrostatic Discharge
EACO	Enhanced-Address-Copy Option
LLC	Logical Link Control
LSB	Least Significant Bit
MAC	Media-Access Control
Mbit/s	Megabits Per Second
Mbit/s	Megabytes Per Second
MIF	Memory Interface
MIPS	Million Instructions Per Second
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
PDMA	Pseudo-Direct Memory Access
PH	Protocol Handler
PHY	Physical-Layer Interface
PLL	Phase-Locked Loop
SIF	System Interface
SIFACL	SIF Adapter Control Register
S/W	Software
TCU	Trunk-Coupling Unit
UNA	Upstream Neighbor Address

PGF PACKAGE
(TOP VIEW)



NC = No internal connection

description

The TI380C30A is a single-chip token-ring solution, combining the commprocessor and the physical-layer (PHY) interface onto a single device. The TI380C30A supports 16 Mbit/s and 4 Mbit/s of operation, conforms to ISO 8802–5/IEEE Std 802.5–1992 standards, and has been verified to be completely IBM Token-Ring Network compatible.

The TI380C30A provides a high degree of integration as it combines the functions of the TI380C25 and the TI380C60A onto a single chip. Additional information on the PHY section can be found in the TI380C60A data sheet, literature number SPWS033. With the TI380C30A, only local memory and minimal additional components such as PAL® devices and crystal oscillators need to be added to complete the LAN-subsystem design.

The TI380C30A provides a 32-bit system-memory address reach with a high-speed bus-master direct memory access (DMA) interface that supports rapid communications with the host system. In addition, the TI380C30A supports direct I/O and a low-cost 8-bit or 16-bit pseudo-DMA interface that requires only a chip-select to work directly on an 80x8x 8-bit slave I/O interface. Selectable 80x8x or 68xxx-type host-system bus and memory organization add to design flexibility.

The TI380C30A supports addressing for up to 2M bytes of local memory. This expanded memory capacity can improve LAN-subsystem performance by minimizing the frequency of host LAN-subsystem communications by allowing larger blocks of information to be transferred at one time. The support of large local memory is important in applications that require large data transfers (such as graphics or database transfers) and in heavily loaded networks where the extra memory can provide data buffers to store data until it can be processed by the host.

The proprietary central processing unit (CPU) used in the TI380C30A allows protocol software to be downloaded into RAM or stored in ROM in the local-memory space. By moving protocols [such as logical link control (LLC)] to the LAN-subsystem, overall system performance is increased. This is accomplished by offloading processing from the host-system to the TI380C30A, which also can reduce LAN-subsystem-to-host communications. As other protocol software is developed, greater differentiation of end products with enhanced system performance is possible.

The TI380C30A includes hardware counters that provide real-time error detection and automatic frame-buffer management. These counters control system-bus retries and burst size, and track host- and LAN-subsystem-buffer status. Previously, these counters were maintained in software. By integrating them into hardware, software overhead is reduced and LAN-subsystem performance is improved.

The TI380C30A implements a Texas Instruments (TI™)-patented enhanced-address-copy-option (EACO) interface. This interface supports external address-checking devices, such as the TMS380SRA source-routing accelerator. The TI380C30A has a 128-word external I/O space in its memory to support external address-checker devices and other hardware extensions to the TMS380 architecture.

At the PHY, the Manchester-encoded data stream is received and phase-aligned using an on-chip dual-digital phase-locked loop (PLL). Both the recovered clock and data are passed to the protocol-handling circuits on the TI380C30A for serial-to-parallel conversion and data processing. On transmit, the TI380C30A buffers the output from the protocol-handling circuit and drives the media by way of suitable isolation and waveform-shaping components.

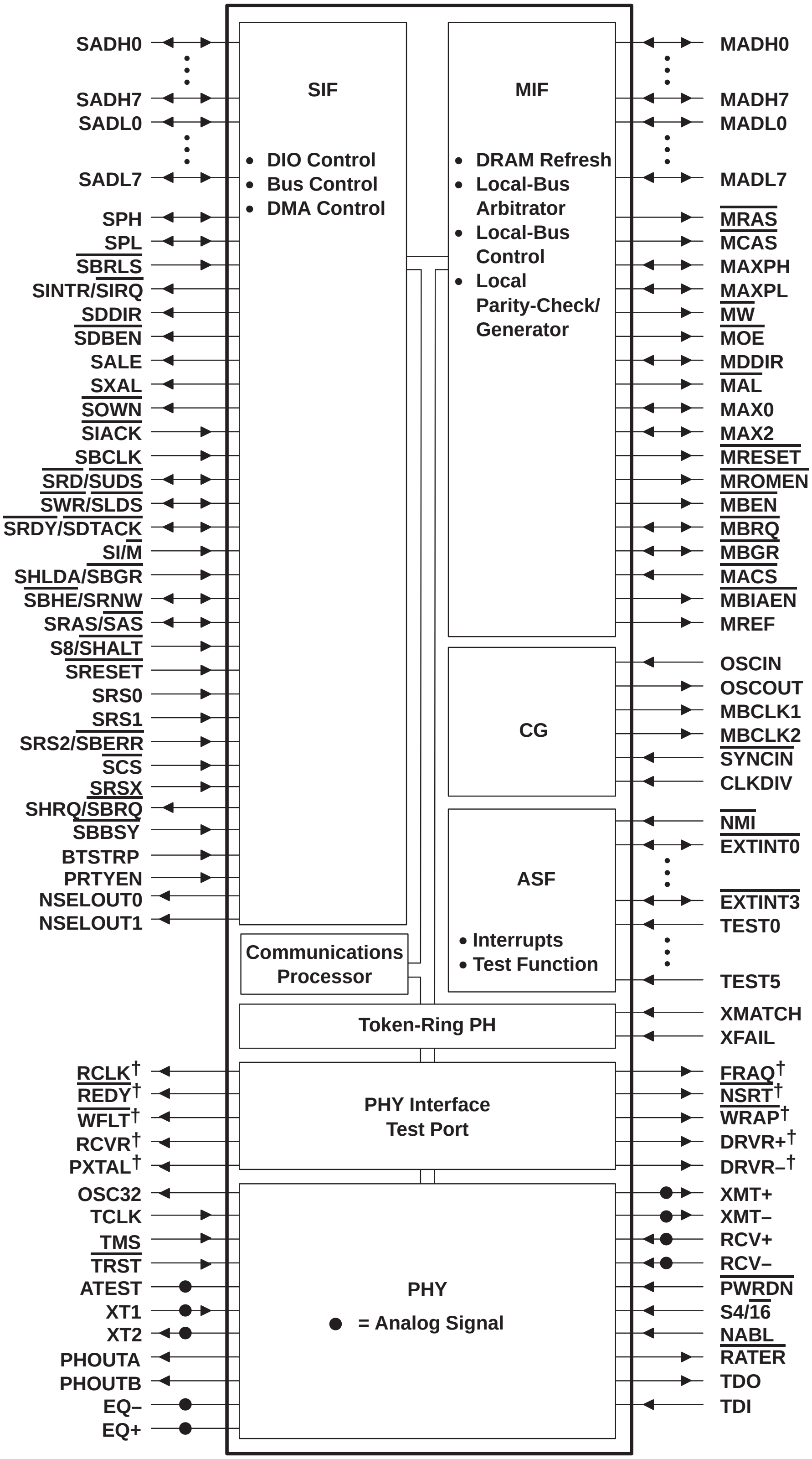
The TI380C30A uses CMOS technology to reduce power consumption to PCMCIA-compatible levels. Power-management features are incorporated to support Green PC compatibility.

In addition to the PLL, all other functions required to interface to an IEEE Std 802.5 token ring are provided. These functions include the phantom drive to control the relays within a trunk-coupling unit and wire-fault detection circuits; an internal-wrap function for self-test; and a watchdog timer to provide fail-safe deinsertion from the ring in the event of a station, microcode, or commprocessor failure.

description (continued)

The major blocks of the TI380C30A include the communications processor (CP), the system interface (SIF), the memory interface (MIF), the protocol handler (PH), the clock generator (CG), the adapter-support function (ASF), and the PHY, as shown in the functional block diagram.

functional block diagram



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† Signals are provided for test-monitoring purposes.

Terminal Functions

TERMINAL		I/O/E[†]	DESCRIPTION
NAME	NO.		
ATEST	128	E	Analog test. ATEST must be left unconnected.
BTSTRP	60	I	Bootstrap. The value on BTSTRP is loaded into the BOOT bit of the SIFACL register at reset (that is, when $\overline{\text{SRESET}}$ is asserted or the $\overline{\text{ARESET}}$ bit in the SIFACL register is set) to form a default value. BTSTRP indicates whether chapters 0 and 31 of the memory map are RAM or ROM. If these chapters are RAM, the TI380C30A is denied access to the local-memory bus until the CPHALT bit in the SIFACL register is cleared. H = Chapters 0 and 31 of local memory are RAM based (see Note 1). L = Chapters 0 and 31 of local memory are ROM based.
CLKDIV	56	I	Clock divider select (see Note 2) H = 64-MHz OSCIN for 4-MHz local bus L = 32-MHz OSCIN for 4-MHz local bus or 48-MHz OSCIN for 6-MHz local bus
DRVR+ DRVR–	169 168	O O	Differential-driver data outputs (reserved)
EQ+ EQ–	152 151	E E	Equalization/gain points. Connections to allow frequency tuning of equalization circuit.
$\overline{\text{EXTINT0}}$ $\overline{\text{EXTINT1}}$ $\overline{\text{EXTINT2}}$ $\overline{\text{EXTINT3}}$	54 53 52 51	I/O	Reserved. $\overline{\text{EXTINT0}}$–$\overline{\text{EXTINT3}}$ must be pulled high (see Note 3).
FRAQ	122	To be resolved	Frequency-acquisition control H = Clock recovery PLL is initialized L = Normal operation
IREF	126	E	Internal reference. IREF allows the internal bias current of analog circuitry to be set by way of an external resistor.
$\overline{\text{MACS}}$	3	I	Reserved. $\overline{\text{MACS}}$ must be tied low (see Note 4).
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	34 33 32 31 28 27 26 25	I/O	Local-memory address, data, and status bus – high byte. For the first quarter of the local-memory cycle, these bus lines carry address bits AX4 and A0–A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits D0–D7. The most significant bit is MADH0 and the least significant bit is MADH7. **Memory Cycle** **1Q** / **2Q** / **3Q** / **4Q** Signal: AX4, A0–A6 / Status / D0–D7 / D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	50 49 48 44 43 42 41 40	I/O	Local-memory address, data, and status bus — low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7–A14; for the second quarter, they carry address bits AX4 and A0–A6; and for the third and fourth quarters, they carry data bits D8–D15. The most significant bit is MADL0 and the least significant bit is MADL7. **Memory Cycle** **1Q** / **2Q** / **3Q** / **4Q** Signal: A7–A14 / AX4, A0–A6 / D8–D15 / D8–D15
$\overline{\text{MAL}}$	2	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0–MADH7, and MADL0–MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched

[†] I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES:
1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
2. The TMS380SRA is supported only with the 4-MHz local bus in either CLKDIV state.
3. Each terminal must be tied individually to V_{DD} with a 1-kΩ pullup resistor.
4. Terminal should be connected to ground.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/E†	DESCRIPTION
MAX0	16	I/O	Local-memory extended-address bit. MAX0 drives AX0 at row-address time and A12 at column-address and data-valid times for all cycles. MAX0 can be latched by $\overline{\text{MRAS}}$. Driving A12 eases interfacing to a burn-in address (BIA) ROM. **Memory Cycle** **1Q 2Q 3Q 4Q** Signal AX0 A12 A12 A12
MAX2	17	I/O	Local-memory extended-address bit. MAX2 drives AX2 at row-address time, which can be latched by $\overline{\text{MRAS}}$, and A14 at column-address and data-valid times for all cycles. Driving A14 eases interfacing to a BIA ROM. **Memory Cycle** **1Q 2Q 3Q 4Q** Signal AX2 A14 A14 A14
MAXPH	35	I/O	Local-memory extended address and parity — high byte. For the first quarter of a memory cycle, MAXPH carries the extended-address bit AX1; for the second quarter of a memory cycle, MAXPH carries the extended-address bit AX0; and for the last half of the memory cycle, MAXPH carries the parity bit for the high data byte. **Memory Cycle** **1Q 2Q 3Q 4Q** Signal AX1 AX0 Parity Parity
MAXPL	39	I/O	Local-memory extended address and parity — low byte. For the first quarter of a memory cycle, MAXPL carries the extended-address bit AX3; for the second quarter of a memory cycle, MAXPL carries extended-address bit AX2; and for the last half of the memory cycle, MAXPL carries the parity bit for the low data byte. **Memory Cycle** **1Q 2Q 3Q 4Q** Signal AX3 AX2 Parity Parity
MBCLK1 MBCLK2	173 174	O	Local-bus clock 1 and local-bus clock 2. MBCLK1 and MBCLK2 are referenced for all local-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. MBCLK1 and MBCLK2 operate according to: **MBCLK1–MBCLK2 OSCIN CLKDIV** 8 MHz 64 MHz H (4-MHz local bus) 8 MHz 32 MHz L (4-MHz local bus) 12 MHz 48 MHz L (6-MHz local bus)
$\overline{\text{MBEN}}$	24	O	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{\text{MBEN}}$ is used with MDDIR, which selects the buffer-output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{\text{MBGR}}$	37	I/O	Reserved. $\overline{\text{MBGR}}$ must be left unconnected.
$\overline{\text{MBIAEN}}$	176	O	Burned-in address enable. $\overline{\text{MBIAEN}}$ is an output signal used to provide an output enable for the ROM containing the adapter's BIA. H = $\overline{\text{MBIAEN}}$ is driven high for any write accesses to the addresses between >00.0000 and >00.000F, or any accesses (read/write) to any other address. L = $\overline{\text{MBIAEN}}$ is driven low for any read from addresses between >00.0000 and >00.000F.
$\overline{\text{MBRQ}}$	36	I/O	Reserved. $\overline{\text{MBRQ}}$ must be pulled high (see Note 3)

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 3. Each terminal must be tied individually to V_{DD} with a 1-kΩ pullup resistor.

Terminal Functions (Continued)

TERMINAL		I/O/E[†]	DESCRIPTION
NAME	NO.		
MCAS	18	O	Column-address strobe for DRAMs. The column address is valid for 3/16ths of the memory cycle following the row-address portion of the cycle. MCAS is driven low every memory cycle while the column address is valid on MADL0–MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: – When the address accessed is in the BIA ROM (>00.0000–>00.000F) – When the address accessed is in the EPROM memory map (that is, when the BOOT bit in the SIFACL register is 0 and an access is made between >00.0010 and >00.FFFF or >1F.0000 and >1F.FFFF) – When the cycle is a refresh cycle, in which case MCAS is driven low at the start of the cycle before MRAS [for DRAMs that have CAS-before-RAS refresh]. For DRAMs that do not support CAS-before-RAS refresh, it may be necessary to disable MCAS with MREF during the refresh cycle.
MDDIR	15	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. MDDIR becomes valid before MBEN becomes active. H = TI380C30A memory-bus write L = TI380C30A memory-bus read
MOE	23	O	Memory-output enable. MOE enables the outputs of the DRAM memory during a read cycle. MOE is high for EPROM or BIA ROM read cycles. H = Disable DRAM outputs L = Enable DRAM outputs
MRAS	20	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16ths of the memory cycle. MRAS is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and ROM cycles. MRAS is also driven low during refresh cycles when the refresh address is valid on MADL0–MADL7.
MREF	1	O	DRAM refresh cycle in progress. MREF indicates that a DRAM refresh cycle is occurring. It is also used for disabling MCAS to all DRAMs that do not use a CAS-before-RAS refresh. H = DRAM refresh cycle in process L = Not a DRAM refresh cycle
MRESET	175	O	Memory-bus reset. MRESET is a reset signal generated when either the ARESET bit in the SIFACL register is set or SRESET is asserted. MRESET is used for resetting external local-bus glue logic. H = External logic not reset L = External logic reset
MROMEN	4	O	ROM enable. During the first 5/16ths of the memory cycle, MROMEN is used to provide a chip select for ROMs when the BOOT bit of the SIFACL is 0 (that is, when code is resident in ROM, and not RAM). MROMEN can be latched by MAL. MROMEN goes low for any read from addresses >00.0010–>00.FFFF or >1F.0000–>1F.FFFF when the BOOT bit in the SIFACL register is 0. MROMEN stays high for writes to these addresses, accesses of other addresses, or accesses of any address when the BOOT bit is 1. During the final three-fourths of the memory cycle, MROMEN outputs the A13 address signal for interfacing to a BIA ROM. This means MBIAEN, MAX0, MROMEN, and MAX2 form a glueless interface for the BIA ROM. H = ROM disabled L = ROM enabled
MW	19	O	Local-memory write. MW is used to specify a write cycle on the local-memory bus. The data on the MADH and MADL buses is valid while MW is low. DRAMs latch data on the falling edge of MW, while SRAMs latch data on the rising edge of MW. H = Not a local-memory write cycle L = Local-memory write cycle
NABL	156	I	Output-enable control. NABL is used in the physical-layer circuitry (see Note 1).
NC	135 166		These NC pins must be left unconnected.
NMI	55	I	Nonmaskable interrupt request. NMI must be left unconnected.

[†] I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/E†	DESCRIPTION
NSELOUT0 NSELOUT1	58 171	O	Network selection outputs. NSELOUT0 and NSELOUT1 are controlled by the host through the corresponding bits of the SIFACL register. The value of NSELOUT0 and NSELOUT1 can be changed only while the TI380C30A is reset. **NSELOUT0 NSELOUT1 Description** L H 16-Mbit/s token ring H H 4-Mbit/s token ring
$\overline{\text{NSRT}}$	121	O	Insert control. $\overline{\text{NSRT}}$ enables the phantom-driver outputs (PHOUTA and PHOUTB) through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB
OSC32	5	O	Oscillator output. OSC32 provides a 32-MHz clock output and can be used to drive OSCIN and one other TTL load.
OSCIN	6	I	External oscillator input. OSCIN provides the clock frequency to the TI380C30A for a 4-MHz or 6-MHz internal bus (see Notes 5, 6, and 8). **CLKDIV OSCIN** H 64 MHz for a 4-MHz local bus L 32 MHz for a 4-MHz local bus or 48 MHz for a 6-MHz local bus
OSCOUT	172	O	Oscillator output **CLKDIV OSCOUT** L OSCIN ÷ 4 (if OSCIN = 32 MHz, OSCOUT = 8 MHz) (if OSCIN = 48 MHz, OSCOUT = 12 MHz) H OSCIN ÷ 8 (if OSCIN = 64 MHz, OSCOUT = 8 MHz)
PHOUTA PHOUTB	139 141	O	Phantom-driver outputs A and B. PHOUTA and PHOUTB cause insertion onto the token ring. PHOUTA and PHOUTB should be connected to the center tap of the transmit transformer secondary winding for phantom-drive generation.
PRTYEN	59	I	Parity enable. The value on PRTYEN is loaded into the PEN bit of the SIFACL register at reset (that is, when $\overline{\text{SRESET}}$ is asserted or the ARESET bit in the SIFACL register is set) to form a default value. PRTYEN enables parity checking for the local memory. H = Local-memory data bus checked for parity (see Note 1) L = Local-memory data bus not checked for parity.
$\overline{\text{PWRDN}}$	154	I	Power-down control (see Note 7) H = Normal operation L = TI380C30A physical-layer circuitry is placed into a power-down state. All TTL outputs of the physical layer are driven to the high-impedance state.
PXTAL	163	O	Reference-clock output. PXTAL is synthesized from the 8-MHz crystal oscillator used for XT1 and XT2. For 16 Mbit/s, it is a 32-MHz clock; for 4 Mbit/s, it is an 8-MHz clock (see Note 8).
$\overline{\text{RATER}}$	158	O	$\overline{\text{RATER}}$ indicates that there are transitions on the RCV+/RCV– input pair (DRVR+/DRVR– if $\overline{\text{WRAP}}$ is asserted low) but that the transition rate is not consistent with the ring speed selected by the S4/$\overline{16}$ pin.
RCLK	161	O	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbit/s operation, it is a 32-MHz clock. For 4-Mbit/s operation, it is an 8-MHz clock.
RCV+ RCV–	149 147	I	Receiver. RCV+ and RCV– are differential inputs that receive the token-ring data by way of isolation transformers.
RCVR	162	O	Recovered data. RCVR contains the data recovered from the token ring.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES:
1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
5. Terminal has an expanded input voltage specification.
6. A maximum of two TI380C30A devices can be connected to any one oscillator.
7. Terminal should be tied to V_{DD} with a 4.7-kΩ pullup resistor.
8. A BUD 35 failure can occur if the rising edge of PXTAL occurs 5 ns to 9 ns after the rising edge of OSCIN. It is a BUD problem only, and does not affect normal operation.

Terminal Functions (Continued)

<table>
<tr><th colspan="2">TERMINAL</th><th rowspan="2">I/O/E[†]</th><th rowspan="2" colspan="2">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td>$\overline{\text{REDY}}$</td><td>124</td><td>O</td><td colspan="2">PLL ready. $\overline{\text{REDY}}$ is normally asserted (active) low. It is cleared following the assertion of FRAQ and reasserted after the data recovery PLL has been reinitialized.
H = Received data not valid (or signal not present)
L = Received data valid
The signal loss indication is in lieu of ring status (SSB_CMD = 0X0001, ring_status bit 0) signal loss indication.</td></tr>
<tr><td>RES</td><td>137</td><td>—</td><td colspan="2">Reserved. RES should be left unconnected.</td></tr>
<tr><td>SADH0
SADH1
SADH2
SADH3
SADH4
SADH5
SADH6
SADH7</td><td>110
109
108
107
106
105
101
100</td><td>I/O</td><td colspan="2">System address/data bus – high byte (see Note 1). These lines make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit (MSB) is SADH0, and the least significant bit (LSB) is SADH7.
Address multiplexing: Bits 31–24 and bits 15–8[‡]
Data multiplexing: Bits 15–8[‡]</td></tr>
<tr><td>SADL0
SADL1
SADL2
SADL3
SADL4
SADL5
SADL6
SADL7</td><td>91
90
89
86
85
84
83
82</td><td>I/O</td><td colspan="2">System address/data bus – low byte (see Note 1). These lines make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0, and the least significant bit is SADL7.
Address multiplexing: Bits 23–16 and bits 7–0[‡]
Data multiplexing: Bits 7–0[‡]</td></tr>
<tr><td>SALE</td><td>80</td><td>O</td><td colspan="2">System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH and SADL buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.</td></tr>
<tr><td>$\overline{\text{SBBSY}}$</td><td>68</td><td>I</td><td colspan="2">System bus busy. The TI380C30A samples the value on $\overline{\text{SBBSY}}$ during arbitration (see Note 1). The sample has one of two values:
H = Not busy. The TI380C30A can become bus master if the grant condition is met.
L = Busy. The TI380C30A cannot become bus master.</td></tr>
<tr><td>SBCLK</td><td>81</td><td>I</td><td colspan="2">System bus clock. The TI380C30A requires the external clock to synchronize its bus timings for all DMA transfers. Valid frequencies are 2 MHz–33 MHz.</td></tr>
<tr><td rowspan="2">$\overline{\text{SBHE}}$/SRNW</td><td rowspan="2">94</td><td rowspan="2">I/O</td><td>Intel™ mode</td><td>$\overline{\text{SBHE}}$ is used for system-byte-high enable. $\overline{\text{SBHE}}$ is a 3-state output driven during DMA; it is an input at all other times.
H = System byte high not enabled (see Note 1)
L = System byte high enabled</td></tr>
<tr><td>Motorola™ mode</td><td>SRNW is used for system read, not write. SRNW serves as a control signal to indicate a read or write cycle.
H = Read cycle (see Note 1)
L = Write cycle</td></tr>
<tr><td>$\overline{\text{SBRLS}}$</td><td>67</td><td>I</td><td colspan="2">System-bus release. $\overline{\text{SBRLS}}$ indicates to the TI380C30A that a higher-priority device requires the system bus. The value on $\overline{\text{SBRLS}}$ is ignored when the TI380C30A is not performing DMA. $\overline{\text{SBRLS}}$ is internally synchronized to SBCLK.
H = The TI380C30A can hold onto the system bus (see Note 1)
L = The TI380C30A should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.</td></tr>
</table>

[†] I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

[‡] Typical bit ordering for Intel™ and Motorola™ processor buses

NOTE 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/E†	DESCRIPTION	
$\overline{SCS}$	66	I	System-chip select. $\overline{SCS}$ activates the system interface of the TI380C30A for a DIO read or write. H = Not selected (see Note 1) L = Selected	
$\overline{SDBEN}$	95	O	System data-bus enable. $\overline{SDBEN}$ signals to the external data buffers to begin driving data. $\overline{SDBEN}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data	
SDDIR	75	O	System data direction. SDDIR provides to the external data buffers a signal indicating the direction in which the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction is into the TI380C30A). During DIO reads and DMA writes, SDDIR is high (data direction is out from the TI380C30A). When the system interface is not involved in a DIO or DMA operation, SDDIR is high by default. **SDDIR** **Data Direction** **DIO** **DMA** H Output Read Write L Input Write Read	
SHLDA/$\overline{SBGR}$	74	I	Intel mode	SHLDA is used for system-hold acknowledge. SHLDA indicates that the system DMA-hold request has been acknowledged. SHLDA is internally synchronized to SBCLK (see Note 1). H = Hold request acknowledged L = Hold request not acknowledged
			Motorola mode	$\overline{SBGR}$ is used for system bus grant. $\overline{SBGR}$ is an active-low bus grant, as defined in the standard 68xxx interface, and is internally synchronized to SBCLK (see Note 1). H = System bus not granted L = System bus granted
SHRQ/$\overline{SBRQ}$	93	O	Intel mode	SHRQ is used for system-hold request. SHRQ is used to request control of the system bus in preparation for a DMA transfer. SHRQ is internally synchronized to SBCLK. H = System bus requested L = System bus not requested
			Motorola mode	$\overline{SBRQ}$ is used for system-bus request. $\overline{SBRQ}$ is used to request control of the system bus in preparation for a DMA transfer. $\overline{SBRQ}$ is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{SIACK}$	61	I	System-interrupt acknowledge. $\overline{SIACK}$ is for the host processor to acknowledge the interrupt request from the TI380C30A. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: The TI380C30A places its interrupt vector onto the system bus.	
SI/$\overline{M}$	72	I	System-Intel/Motorola mode select. The value on SI/$\overline{M}$ specifies the system-interface mode. H = Intel-compatible-interface mode selected. Intel-interface mode can be 8 bit or 16 bit (see S8/$\overline{SHALT}$ description and Note 1). L = Motorola-compatible-interface mode selected. Motorola-interface mode is always 16 bits.	
SINTR/$\overline{SIRQ}$	73	O	Intel mode	SINTR is used for system-interrupt request. TI380C30A activates SINTR to signal an interrupt request to the host processor. H = Interrupt requested by TI380C30A L = No interrupt request
			Motorola mode	$\overline{SIRQ}$ is used for system-interrupt request. TI380C30A activates $\overline{SIRQ}$ to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt requested by TI380C30A

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/E†		DESCRIPTION
$\overline{\text{SOWN}}$	96	O		System bus owned. $\overline{\text{SOWN}}$ indicates to external devices that TI380C30A has control of the system bus. SOWN drives the enable signal of the bus-transceiver chips that drive the address and bus-control signals. H = TI380C30A does not have control of the system bus L = TI380C30A has control of the system bus
SPH	99	I/O		System parity high. SPH is the optional odd-parity bit for each address or data byte transmitted over SADH0–SADH7 (see Note 1).
SPL	92	I/O		System parity low. SPL is the optional odd-parity bit for each address or data byte transmitted over SADL0–SADL7 (see Note 1).
SRAS/$\overline{\text{SAS}}$	76	I/O	Intel mode	SRAS is used for system memory-address strobe (see Note 7). SRAS is used to latch the $\overline{\text{SCS}}$ and SRSX – SRS2 register input signals. In a minimum-chip system, SRAS is tied to the SALE output of the system bus. The latching capability can be defeated since the internal latch for these inputs remains transparent as long as SRAS remains high. This permits SRAS to be pulled high and the signals at $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$ to be applied independently of the SALE strobe from the system bus. During DMA, SRAS remains an input. H = Transparent mode L = Holds latched values of $\overline{\text{SCS}}$, SRSX–SRS2, and $\overline{\text{SBHE}}$ Falling edge = Latches $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$
			Motorola mode	$\overline{\text{SAS}}$ is used for sytem-memory address strobe (see Note 7). $\overline{\text{SAS}}$ is an active-low address strobe that is an input during DIO (although ignored as an address strobe) and an output during DMA. H = Address is not valid L = Address is valid and a transfer operation is in progress
$\overline{\text{SRD}}$/$\overline{\text{SUDS}}$	98	I/O	Intel mode	$\overline{\text{SRD}}$ is used for system-read strobe (see Note 7). $\overline{\text{SRD}}$ is the active-low strobe indicating that a read cycle is performed on the system bus. $\overline{\text{SRD}}$ is an input during DIO and an output during DMA. H = Read cycle is not occurring L = If DMA, host provides data to system bus. If DIO, SIF provides data to system bus
			Motorola mode	$\overline{\text{SUDS}}$ is used for upper-data strobe (see Note 7). $\overline{\text{SUDS}}$ is the active-low upper-data strobe. $\overline{\text{SUDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADH0–SADH7 lines L = Valid data on SADH0–SADH7 lines
$\overline{\text{SRDY}}$/SDTACK	97	I/O	Intel mode	$\overline{\text{SRDY}}$ is used for system bus ready (see Note 7). $\overline{\text{SRDY}}$ indicates to the bus master that a data transfer is complete. $\overline{\text{SRDY}}$ is asynchronous, but during DMA and pseudo-DMA cycles, it is internally synchronized to SBCLK. During DMA cycles, $\overline{\text{SRDY}}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{\text{SRDY}}$ is an output when the TI380C30A is selected for DIO; otherwise, it is an input. H = System bus is not ready L = Data transfer is complete; system bus is ready
			Motorola mode	$\overline{\text{SDTACK}}$ is used for system data-transfer acknowledge (see Note 7). The purpose of SDTACK is to indicate to the bus master that a data transfer is complete. SDTACK is internally synchronized to SBCLK. During DMA cycles, SDTACK must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. SDTACK is an output when the TI380C30A is selected for DIO; otherwise, it is an input. H = System bus is not ready L = Data transfer is complete; system bus is ready

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Terminal should be tied to V_{DD} with a 4.7-kΩ pullup resistor.

Terminal Functions (Continued)

TERMINAL		I/O/E†	DESCRIPTION	
NAME	NO.			
$\overline{\text{SRESET}}$	62	I	System reset. $\overline{\text{SRESET}}$ is activated to place the TI380C30A into a known initial state. Hardware reset puts most of the TI380C30A outputs into the high-impedance state and places all blocks into the reset state. The Intel-mode DMA bus-width selection (S8) is latched on the rising edge of $\overline{\text{SRESET}}$. H = No system reset L = System reset Rising edge = Latch bus width for DMA operations (for Intel-mode applications)	
SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$	65 64 63 70	I	Intel mode	SRSX and SRS0–SRS2 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The MSB is SRSX and the LSB is SRS2 (see Note 1). **MSB** **LSB** Register selected = SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$
			Motorola mode	SRSX, SRS0, and SRS1 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1 (see Note 1). **MSB** **LSB** Register selected = SRSX SRS0 SRS1 $\overline{\text{SBERR}}$ is used for bus error. $\overline{\text{SBERR}}$ corresponds to the bus-error signal of the 68xxx microprocessor. It is internally synchronized to SBCLK. $\overline{\text{SBERR}}$ is driven low during a DMA cycle to indicate to the TI380C30A that the cycle must be terminated (see section 3.4.5.3 of the *TMS380 Second-Generation Token-Ring User's Guide*, literature number SPWU005, for more information).
$\overline{\text{SWR}}$/$\overline{\text{SLDS}}$	77	I/O	Intel mode	$\overline{\text{SWR}}$ is used for system-write strobe (see Note 7). $\overline{\text{SWR}}$ is an active-low write strobe that is an input during DIO and an output during DMA. H = Write cycle is not occurring L = If DMA, data to be driven from SIF to host bus. If DIO, on the rising edge, the data is latched and written to the selected register
			Motorola mode	$\overline{\text{SLDS}}$ is used for lower-data strobe (see Note 7). $\overline{\text{SLDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADL0–SADL7 lines L = Valid data on SADL0–SADL7 lines
SXAL	79	O	System extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry-out of the lower 16 bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.	
$\overline{\text{SYNCIN}}$	12	I	Reserved. $\overline{\text{SYNCIN}}$ must be left unconnected (see Note 1).	
S4/$\overline{\text{16}}$	155	I	Speed switch. S4/$\overline{\text{16}}$ specifies the token-ring data rate for the physical layer (see Note 1). H = 4-Mbit/s data rate L = 16-Mbit/s data rate	

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Terminal should be tied to V_{DD} with a 4.7-kΩ pullup resistor.

Terminal Functions (Continued)

TERMINAL		I/O/E[†]	DESCRIPTION	
NAME	NO.			
S8/$\overline{\text{SHALT}}$	69	I	Intel mode	S8 is used for system 8-/16-bit bus select. S8 selects the bus width used for communications through the system interface. On the rising edge of $\overline{\text{SRESET}}$, the TI380C30A latches the DMA bus width; otherwise, the value on S8 dynamically selects the DIO bus width. H = Selects 8-bit mode (see Note 1) L = Selects 16-bit mode
			Motorola mode	$\overline{\text{SHALT}}$ is used for system halt/bus error retry. If $\overline{\text{SHALT}}$ is asserted along with bus error ($\overline{\text{SBERR}}$), the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68xxx specification. The BERETRY counter is not decremented by $\overline{\text{SBERR}}$ when $\overline{\text{SHALT}}$ is asserted (see section 3.4.5.3 of the *TMS380 Second-Generation Token-Ring User's Guide*, literature number SPWU005, for more information).
TCLK	7	I (see Note 1)	Test ports used during the production test of the device. TCLK, TMS, TDI, and TDO must be left unconnected.	
TMS	8	I (see Note 1)		
TDI	165	I (see Note 1)		
TDO	164	O		
TEST0	116	I	Network select inputs. TEST0–TEST2 are used to select the network speed and type to be used by the TI380C30A. These inputs should be changed only during adapter reset. Connect TEST2 to V_{DDL}. **TEST0 TEST1 TEST2 Description** L NC H 16-Mbit/s token ring H NC H 4-Mbit/s token ring X X L Reserved	
TEST1	115	I		
TEST2	114	I		
TEST3	113	I	Test inputs. TEST3–TEST5 should be left unconnected (see Note 1). Module-in-place test mode is achieved by tying TEST3 and TEST4 to ground. In this mode, all TI380C30A outputs are in the high-impedance state. Internal pullups on all TI380C30A inputs are disabled (except TEST3–TEST5).	
TEST4	112	I		
TEST5	111	I		
$\overline{\text{TRST}}$	9	I	Test-port reset. $\overline{\text{TRST}}$ should be tied to ground for normal operation of the TI380C30A (see Note 1). H = Reserved L = Test ports forced to an idle state	
V_{DD}	14 29 45 87 103 119	—	Positive-supply voltage for commprocessor output buffers. All V_{DD} pins must be attached to the common-system power-supply plane.	
V_{DDA1}	148	—	Positive-supply voltage for receiver circuits	
V_{DDA2}	129	—	Positive-supply voltage for data recovery PLL	
V_{DDA3}	123		Positive-supply voltage for the current-bias generator	
V_{DDD}	157	—	Positive-supply voltage for physical layer output buffers	
V_{DDL}	13 47 71	—	Positive-supply voltage for commprocessor digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.	
V_{DDL1}	134 146	—	Positive-supply voltage for physical layer digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.	
V_{DDO}	133	—	Positive-supply voltage for XTAL oscillator	
V_{DDP}	138	—	Positive-supply voltage for phantom drive	
V_{DDX}	145	—	Positive-supply voltage for transmit output	

[†] I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Terminal Functions (Continued)

TERMINAL		I/O/E[†]	DESCRIPTION
NAME	**NO.**		
V_{SS}	11 30 38 78 104	—	Ground connections for commprocessor output buffers. All V_{SS} pins must be attached to system ground plane.
V_{SSA1}	150	—	Ground reference for receiver circuits
V_{SSA2}	127	—	Ground reference for data-recovery PLL
V_{SSA3}	125		Ground reference for the current-bias generator
V_{SSC}	10 21 57 102	—	Ground reference for commprocessor output buffers (clean ground). All V_{SSC} pins must be attached to the common-system ground plane.
V_{SSC1}	160		Ground reference for physical layer output buffers
V_{SSD}	159	—	Ground reference for physical layer output buffers
V_{SSL}	22 46 88 120	—	Ground reference for digital logic. All V_{SSL} pins must be attached to the common-system ground plane.
V_{SSL1}	136 153	—	Ground reference for internal logic
V_{SSO}	131	—	Ground reference for XTAL oscillator
V_{SSP}	140	—	Ground reference for phantom drive
V_{SSX}	142	—	Ground reference for transmit output
$\overline{\text{WFLT}}$	167	O	Phantom-wire fault. $\overline{\text{WFLT}}$ provides an indication of the presence of a short or open circuit on PHOUTA or PHOUTB. H = No fault L = Open or short. The DC fault condition is present in the phantom-drive lines.
$\overline{\text{WRAP}}$	170	O	Internal wrap mode control. $\overline{\text{WRAP}}$ indicates the TI380C30A has placed the physical layer in the loopback-wrap mode for adapter self test. H = Normal ring operation L = Physical-layer wrap mode selected
XFAIL	117	I	External fail-to-match signal. An EACO device uses XFAIL to indicate to the TI380C30A that it should not copy the frame nor set the address-recognize indicator/frame-copied indicator (ARI/FCI) bits in a token-ring frame due to an external address match.The ARI/FCI bits in a token-ring frame can be set due to an internal address-matched frame. If an EACO device is not used, XFAIL must be left unconnected. XFAIL is ignored when copy-all-frames (CAF) mode is enabled [see table in XMATCH description section (see Note 1)]. H = No address match by external address checker L = External address-checker-armed state
XMATCH	118	I	External match signal. An EACO device uses XMATCH to indicate to the TI380C30A to copy the frame and set the ARI/FCI bits in a token-ring frame. If an EACO device is not used, XMATCH must be left unconnected. XMATCH is ignored when CAF mode is enabled (see Note 1). H = Address match recognized by external address checker L = External address-checker-armed state **XMATCH XFAIL Function** 0 0 Armed (processing frame data) 0 1 Do not externally match the frame (XFAIL takes precedence) 1 0 Copy the frame 1 1 Do not externally match the frame (XFAIL takes precedence) Hi-Z Hi-Z Reset state (adapter not initialized)

[†] I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1. Terminal has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/E†	DESCRIPTION
XMT+ XMT–	143 144	E	Transmit differential outputs. XMT+ and XMT– provide a low-impedance differential source for line drive by way of filtering and transformer isolation.
XT1 XT2	130 132	I E	XTAL connection. An 8-MHz crystal network can be connected here to provide a reference clock for the TI380C30A. Alternatively, an 8-MHz TTL clock source can be connected to XT1.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

architecture

The major blocks of the TI380C30A include the CP, SIF, MIF, PH, CG, ASF, and PHY. The functionality of each block is described in the following sections.

communications processor (CP)

The CP performs the control and monitoring of the other functional blocks in the TI380C30A. The control and monitoring protocols are specified by the software (downloaded or ROM-based) in local memory. Available protocols include:

- Media access control (MAC) software
- Logical link control (LLC) software
- Copy all frames (CAF) software

The CP is a proprietary 16-bit central processing unit (CPU) with data cache and a single prefetch pipe for pipelining of instructions. These features enhance the TI380C30A maximum performance capability to about 8 million instructions per second (MIPS), with an average of about 5 MIPS.

system interface (SIF)

The SIF performs the interfacing of the LAN subsystem to the host system. This interface can require additional logic depending on the application. The system interface can transfer information/data using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) is used to transfer all data to/from host memory from/to local memory. The main uses of DIO are loading the software to local memory and initializing the TI380C30A. DIO also allows command/status interrupts to occur to and from the TI380C30A.

The system interface can be hardware-selected for either of two modes by using SI/$\overline{\mathrm{M}}$. The mode selected determines the memory organizations and control signals used. These modes are:

- The Intel mode (80x8x families): 8-, 16-, and 32-bit bus devices
- The Motorola mode (68xxx microprocessor family): 16- and 32-bit bus devices

The system interface supports host-system memory addressing up to 32 bits (32-bit reach into the host system memory). This allows greater flexibility in using/accessing host-system memory. System designers are allowed to customize the system interface to their particular bus by:

- Programmable burst transfers or cycle-steal DMA operations
- Optional parity protection

These features are implemented in hardware to reduce system overhead, facilitate automatic rearbitration of the bus after a burst, or repeat a cycle when errors occur (parity or bus). Bus retries are also supported.

system interface (SIF) (continued)

The system-interface hardware also includes features to enhance the integrity of the TI380C30A operation and the data. These features include:

- Always internally maintain odd-byte parity regardless of parity being disabled
- Monitor for the presence of a clock failure
- Provide switchable SIF speeds at 2 MHz to 33 MHz

On every cycle, the system interface compares all the system clocks to a reference clock. If any of the clocks becomes invalid, the TI380C30A enters the slow-clock mode, which prevents latch-up of the TI380C30A. If the SBCLK is invalid, any DMA cycle is terminated immediately; otherwise, the DMA cycle is completed and the TI380C30A is placed in slow-clock mode.

When the TI380C30A enters the slow-clock mode, the clock that failed is replaced by a slow free-running clock, and the device is placed into a low-power reset state. When the failed clock(s) return to valid operation, the TI380C30A must be reinitialized.

For DMA with a 16-MHz clock, a continuous transfer rate of 64 MBps [8 megabytes per second (MBps)] can be obtained. For DMA with a 25-MHz clock, a continuous transfer rate of 96 Mbit/s (12 MBps) can be obtained. For DMA with a 33-MHz clock, a continuous transfer rate of 128 Mbit/s (16 MBps) can be obtained. For 8-bit and 16-bit pseudo-DMA, the data rates in Table 2 can be obtained.

Table 2. Pseudo-DMA Data Rates

LOCAL BUS SPEED	8-BIT PDMA	16-BIT PDMA
4 MHz	48 Mbit/s	64 Mbit/s
6 MHz	72 Mbit/s	96 Mbit/s

Since the main purpose of DIO is for downloading and initialization, the DIO transfer rate is not a significant issue.

memory interface (MIF)

The MIF performs memory management to allow the TI380C30A to address 2 Mbytes in local memory. Hardware in the MIF allows the TI380C30A to be connected directly to DRAMs without additional circuitry. This glueless-DRAM connection includes the DRAM-refresh controller. The MIF also handles all internal bus arbitration between these blocks. When required, the MIF arbitrates for the external bus.

The MIF is responsible for the memory mapping of the CPU of a task. The memory maps of DRAMs, EPROMs, burned-in addresses (BIAs), and external devices are addressed appropriately when required by the system interface, the protocol handler, or for a DMA transfer. The memory interface is capable of a 64-Mbit/s continuous transfer rate when using a 4-MHz local bus (64-MHz device crystal) and a 96-Mbit/s continuous transfer rate when using a 6-MHz local bus.

protocol handler (PH)

The PH performs the hardware-based real-time protocol functions for a token-ring LAN. Network type is determined by TEST0–TEST2. The token-ring network speed is determined by software and can be either 16 Mbit/s or 4 Mbit/s. These speeds are fixed by the software, not by the hardware.

The PH converts the parallel-transmit data to serial-network data of the appropriate coding and converts the received serial data to parallel data. The PH data-management state machines direct the transmission/reception of data to/from local memory through the MIF. The PH buffer-management state machines automatically oversee this process, directly sending/receiving linked lists of frames without CPU intervention.

protocol handler (continued)

The PH contains many state machines that perform the following functions:

- Transmit and receive frames
- Capture tokens
- Provide token-priority controls
- Manage the TI380C30A buffer memory
- Provide frame-address recognition (group, specific, functional, and multicast)
- Provide internal parity protection
- Control and verify the physical-layer circuitry-interface signals

Integrity of the transmitted and received data is controlled by cyclic-redundancy checks (CRC), detection of network-data violations, and parity on internal data paths. All data paths and registers are optionally parity-protected to maintain functional integrity.

clock generator (CG)

The CG performs the generation of all internal clocks required by the other functional blocks, including the local memory-bus clocks (MBCLK1, MBCLK2). The CG also generates the reference timer used to sample all input clocks (SBCLK, OSCIN, RCLK, and PXTAL). If no transition is detected within the period of the reference timer on any input clock signal, the CG places the TI380C30A into slow-clock mode. The frequency of the reference timer is in the range of 10 kHz–100 kHz.

adapter-support function (ASF)

The ASF performs support functions not contained in the other blocks. The features are:

- The TI380C30A base timer
- Identification, management, and service of internal and external interrupts
- Test-pin mode control, including the unit-in-place mode for board testing
- Checks for illegal states, such as illegal opcodes and parity

physical-layer interface (PHY)

The major blocks of the TI380C30A PHY include the receiver/equalizer, clock recovery PLL, wrap function, phantom drive with wire-fault detector, and watchdog timer. Figure 2 is the block diagram illustrating these major blocks, and the functionality of each block is described in the following sections.

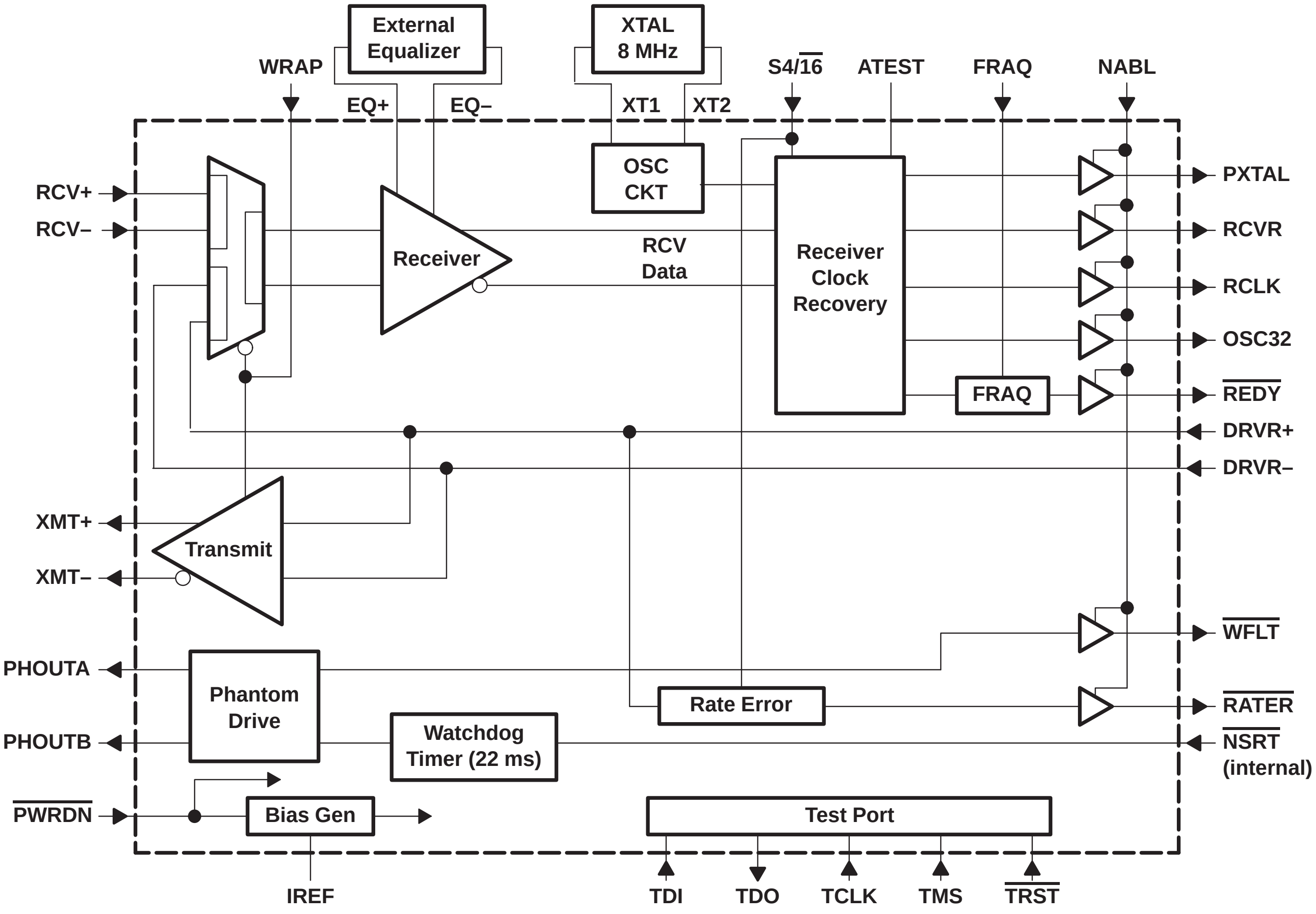


Figure 2. Functional Block Diagram of the PHY

receiver

Figure 3 shows the arrangement of the line-receiver/equalizer circuit. The differential-input pair, RCV+ and RCV–, are designed to be connected to a floating winding of an isolation transformer. Each is equipped with a bias circuit to center the operating point of the differential input at approximately $V_{DD} \div 2$.

The differential-input pair consists of a pair of metal oxide semiconductor field effect transistors (MOSFETs), each with an identical current source in its source terminal that is set to supply a nominal current of 1.5 mA. At low signal levels, the gain of this pair is inversely proportional to the impedance connected between their sources on EQ– and EQ+. A frequency-equalization network can be connected between EQ+ and EQ– to provide equalization for media-signal distortion.

The internal-wrap mode is provided for self-test of the device. When selected by taking $\overline{\text{WRAP}}$ low, the normal input path is disabled by a multiplexer and a path is enabled from the DRVR+/DRVR– input pair. Receiver gain, thresholds, and equalization are unchanged in the internal-wrap mode.

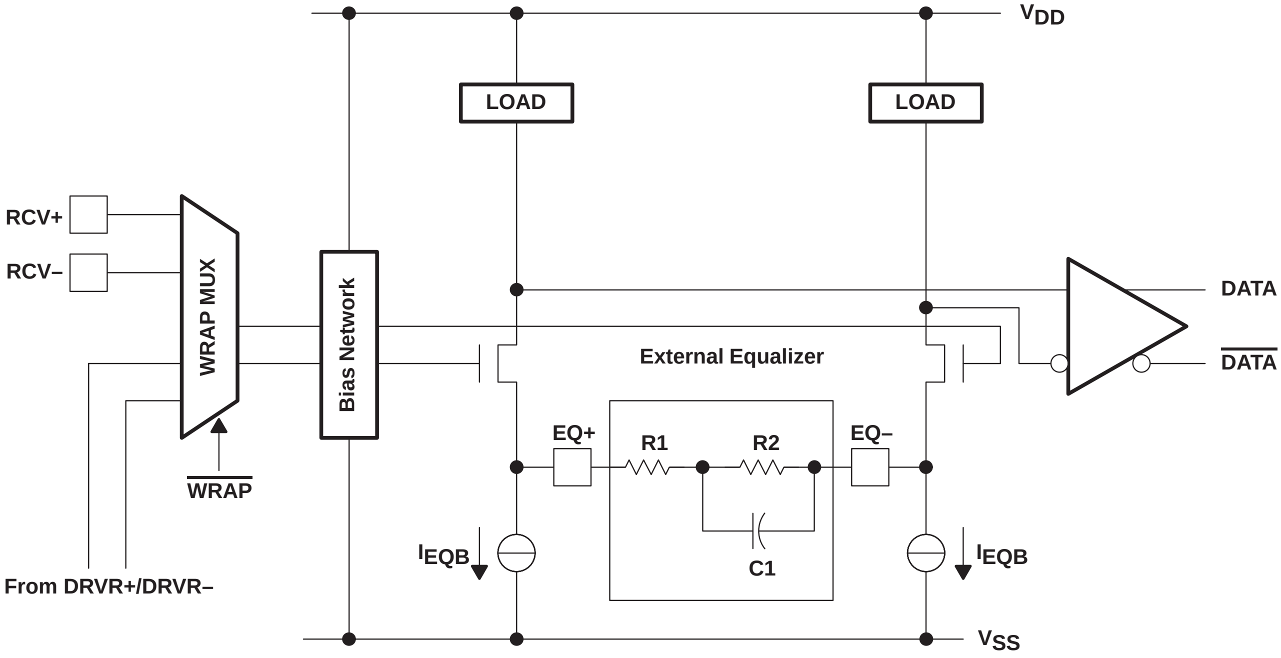
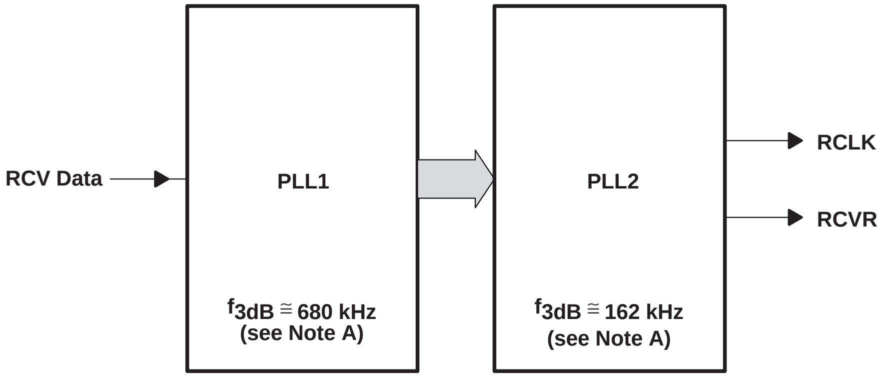


Figure 3. Line Receiver/Equalizer

receiver-clock recovery

The clock and data recovery in the TI380C30A is performed by an advanced, digitally controlled PLL. In contrast to the TMS38054, the PLL of the TI380C30A is digitally controlled and the loop parameters are set by internally programmed digital constants. This results in precise control of loop parameters and requires no external loop-filter components.

The TI380C30A implements an intelligent algorithm to determine the optimum phase position for data sampling and extracted-clock synthesis. The resulting action of the TI380C30A can be modeled as two cascaded PLLs as shown in Figure 4.



NOTE A: f_{3dB} = 3-dB bandwidth of PLL

Figure 4. Dual-PLL Arrangement

receiver-clock recovery (continued)

PLL1 represents the algorithm to recover data from the incoming stream detected by the receiver. It has a relatively high bandwidth to provide good jitter tolerance. Data and embedded-clock-phase information are fed as digital values to PLL2, which generates the extracted clock (RCLK) for the commprocessor. The recovered data is sent to the commprocessor as the RCVR signal in synchronization with RCLK. In addition to sampling the RCVR signal, the commprocessor uses RCLK to retransmit data in most cases. The lower bandwidth of PLL2 greatly reduces the rate of accumulation of data-correlated phase jitter in a token-ring network and provides very good accumulated-phase-slope (APS) characteristics. In addition to RCLK, the token-ring reference clock (PXTAL) and a fixed-frequency 32-MHz clock (OSC32) are also synthesized from the 8-MHz crystal reference.

line driver and wrap function

The line-drive function of the TI380C30A is performed by XMT+/XMT–. Unlike the TMS38054, these pins are low-impedance outputs and require external-series resistance to provide line termination. These pins provide buffering of the differential signal from the PH on DRVR+/DRVR– with action to control skew and asymmetry, and with no retiming in the transmit path.

The wrap function is designed to provide a signal path for system self-test diagnostics. When the PH drives $\overline{\text{WRAP}}$ low, the receiver inputs are ignored and the transmit signal is fed to the receiver input circuitry by way of a multiplexer. In the internal wrap mode, $\overline{\text{WRAP}}$ can be checked by observing the signal amplitude at the equalization pins, EQ+ and EQ–. Equalization is active at this signal level, although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate. During wrap mode, both XMT+/XMT– are driven to a low state to prevent any dc current from flowing into the isolation transformer.

phantom driver and wire-fault detection

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc voltage on both of the phantom-drive outputs, PHOUTA and PHOUTB. To maintain the phantom drive, $\overline{\text{NSRT}}$ is toggled by the TI380C30A at least once every 20 ms. A watchdog timer is included in the TI380C30A to remove the phantom drive if $\overline{\text{NSRT}}$ does not have the required transitions.

The watchdog timer normally is not allowed to expire because it is being reinitialized at least every 20 ms. If there is a problem in the TI380C30A or its microcode, resulting in failure to toggle $\overline{\text{NSRT}}$, the timer expires in a maximum of 22 ms. If this happens, the phantom drive is deasserted and remains so until the next falling edge of $\overline{\text{NSRT}}$. The watchdog timer requires no external-timing components. When the phantom drive is deasserted, the phantom-drive lines are actively pulled low, reaching a level of 1 V or less within 50 ms.

The dc voltage from PHOUTA and PHOUTB is superimposed on the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. This is achieved by connecting the transmit-signal pair to the center of the secondary winding of the transmit-isolation transformer. Since PHOUTA and PHOUTB are connected to the media side of the isolation transformer, they require extensive protection against line surges. A capacitor is connected between the two phantom lines to provide an ac path for the transmit signal, while PHOUTA and PHOUTB independently drive the dc voltage on each of the transmit lines, allowing for independent wire-fault detection on each.

The phantom voltage is detected by the TCU, causing the external wrap path from the transmitter outputs back to the receiver inputs to be broken and the ring to be broken. A signal connection is established from the ring to the receiver inputs and from the transmitter outputs to the ring. The return current from the dc-phantom voltage on the transmit pair is returned to the station by way of the receive pair. This provides some measure of wire-fault detection on the receive lines. The phantom-drive outputs are current limited to prevent damage if short-circuited. They detect either an abnormally high or an abnormally low load current at either output corresponding to a short or an open circuit in the ring or TCU wiring. Either type of fault results in the wire-fault indicator output ($\overline{\text{WFLT}}$) being driven low. The logic state of $\overline{\text{WFLT}}$ is high when the phantom drive is not active.

frequency acquisition and REDY

Unlike its predecessors, the TMS3805x family, the data-recovery PLL of the TI380C30A physical layer does not require constant frequency monitoring; neither is it necessary to recenter its frequency by way of the FRAQ control line. When the commprocessor asserts FRAQ, it initiates a reset of the clock-recovery PLL. The REDY signal is deasserted for the duration of this action and reasserted low when it is complete (a maximum of 3 µs later). This low-going transition of REDY is required by the commprocessor following the setting of FRAQ high to indicate to the PH that any frequency error that it could have detected has been corrected. REDY is not asserted if no incoming transitions are detected by the rate-error function.

rate error (RATER) function

RATER provides an indication that incoming data transitions are present on the RCV+/RCV– pair, but that the rate of transitions is outside the range that is expected for the ring speed selected by S4/16. RATER is not asserted low if no incoming transitions are present. In wrap mode, the rate-error function monitors the transitions on the DRVR+/DRVR– pair.

The rate-error function interprets 16 or more transitions in a 1.5-µs period as valid 16-Mbit/s data. It interprets 15 or fewer transitions in a 1.5-µs period as 4-Mbit/s data. One transition or less in a 1.5-µs period is interpreted as no incoming transitions, in which case, RATER and REDY are not asserted low.

power-down control

The TI380C30A PHY can be disabled by the PWRDN signal. If PWRDN is taken low, all outputs of the PHY are in the high-impedance state and all internal logic is powered down, bringing power consumption to a very low level. Upon taking PWRDN high, the device resets and initializes itself. This process could take up to 2 ms and care should be taken to ensure that the system does not require stable clocks during this period.

user-accessible hardware registers and TI380C30A-internal pointers

Table 3 and Table 4 show how to access internal data by way of pointers and how to address the registers in the host interface. The SIF adapter-control (SIFACL) register, which directly controls device operation, is described in detail. The adapter-internal pointers table is defined only after TI380C30A initialization and until the OPEN command is issued. These pointers are defined by the TI380C30A software (microcode), and this table describes the release 2.x software.

Table 3. Adapter-Internal Pointers for Token Ring[†]

ADDRESS	DESCRIPTION
>00.FFF8[‡]	Pointer to software raw microcode level in chapter 0
>00.FFFA[‡]	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TI380C30A addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A06	Pointer to TI380C30A parameters in chapter 1: Pointer + 0 physical-drop number Pointer + 4 upstream neighbor address Pointer + 10 upstream physical-drop number Pointer + 14 last ring-poll address Pointer + 20 reserved Pointer + 22 transmit access priority Pointer + 24 source class authorization Pointer + 26 last attention code Pointer + 28 source address of the last received frame Pointer + 34 last beacon type Pointer + 36 last major vector Pointer + 38 ring status Pointer + 40 soft-error timer value Pointer + 42 ring-interface error counter Pointer + 44 local ring number Pointer + 46 monitor error code Pointer + 48 last beacon-transmit type Pointer + 50 last beacon-receive type Pointer + 52 last MAC-frame correlator Pointer + 54 last beaconing-station upstream neighbor address (UNA) Pointer + 60 reserved Pointer + 64 last beaconing-station physical-drop number
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter-generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbit/s word flag. If zero, the adapter is set to run at 4 Mbit/s. If nonzero, the adapter is set to run at 16 Mbit/s.
>01.0A0E	Pointer to total TI380C30A RAM found in 1K bytes in RAM allocation test in chapter 1.

[†] This table describes the pointers for release 2.x of the TI380C30A software.
[‡] This address valid only for microcode release 2.x

Table 4. User-Access Hardware Registers

80x8x 16-BIT MODE
(SI/$\overline{\text{M}}$ = 1, S8/$\overline{\text{SHALT}}$ = 0)†

WORD TRANSFERS			NORMAL MODE $\overline{\text{SBHE}}$ = 0, SRS2 = 0		PSEUDO-DMA MODE ACTIVE $\overline{\text{SBHE}}$ = 0, SRS2 = 0	
BYTE TRANSFERS			**$\overline{\text{SBHE}}$ = 0, SRS2 = 1**	**$\overline{\text{SBHE}}$ = 1, SRS2 = 0**	**$\overline{\text{SBHE}}$ = 0, SRS2 = 1**	**$\overline{\text{SBHE}}$ = 1, SRS2 = 0**
SRSX	**SRS0**	**SRS1**				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

† $\overline{\text{SBHE}}$ = 1 and SRS2 = 1 are not defined.

80x8x 8-BIT MODE
(SI/$\overline{\text{M}}$ = 1, S8/$\overline{\text{SHALT}}$ = 1)

SRSX	SRS0	SRS1	SRS2	NORMAL MODE $\overline{\text{SBHE}}$ = X	PSEUDO-DMA MODE ACTIVE $\overline{\text{SBHE}}$ = X
0	0	0	0	SIFDAT LSB	SDMADAT LSB
0	0	0	1	SIFDAT MSB	SDMADAT MSB
0	0	1	0	SIFDAT MSB	DMALEN LSB
0	0	1	1	SIFDAT MSB	DMALEN MSB
0	1	0	0	SIFADR LSB	SDMAADR LSB
0	1	0	1	SIFADR MSB	SDMAADR MSB
0	1	1	0	SIFSTS	SDMAADX LSB
0	1	1	1	SIFCMD	SDMAADX MSB
1	0	0	0	SIFACL LSB	SIFACL LSB
1	0	0	1	SIFACL MSB	SIFACL MSB
1	0	1	0	SIFADR LSB	SIFACL LSB
1	0	1	1	SIFADR MSB	SIFACL MSB
1	1	0	0	SIFADX LSB	SIFADX LSB
1	1	0	1	SIFADX MSB	SIFADX MSB
1	1	1	0	DMALEN LSB	DMALEN LSB
1	1	1	1	DMALEN LSB	DMALEN MSB

Table 4. User-Access Hardware Registers (Continued)

68xxx MODE
(SI/$\overline{\text{M}}$ = 0)[†]

WORD TRANSFERS			NORMAL MODE $\overline{\text{SUDS}}$ = 0, $\overline{\text{SLDS}}$ = 0		PSEUDO-DMA MODE ACTIVE $\overline{\text{SUDS}}$ = 0, $\overline{\text{SLDS}}$ = 0	
BYTE TRANSFERS			**$\overline{\text{SUDS}}$ = 0, $\overline{\text{SLDS}}$ = 1**	**$\overline{\text{SUDS}}$ = 1, $\overline{\text{SLDS}}$ = 0**	**$\overline{\text{SUDS}}$ = 0, $\overline{\text{SLDS}}$ = 1**	**$\overline{\text{SUDS}}$ = 1, $\overline{\text{SLDS}}$ = 0**
SRSX	**SRS0**	**SRS1**				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

[†] 68xxx mode is always a 16-bit mode.

SIF adapter-control (SIFACL) register

The SIFACL register allows the host processor to control, and to some extent, reconfigure the TI380C30A under software control (see Table 5).

SIFACL Register

Bit No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	TEST0	TEST1	TEST2	—	SWHLDA	SWDDIR	SWHRQ	PSDMAEN	ARESET	CPHALT	BOOT	LBP	SINTEN	PEN	NSEL OUT0	NSEL OUT1
	R	R	R		RW –0	R –U	R –0	RS –0	RW –0	RP –b	RP –b	RP –0	RW –1	RP –p	RP –0	RP –1

Legend:
R = Read
W = Write
P = Write during ARESET = 1 only
S = Set only
–n = Value after reset
b = Value on BTSTRP
p = Value on PRTYEN
u = Indeterminate

Table 5. SIFACL Bit Definitions

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>0–2</td><td>TEST0
TEST1
TEST2</td><td>Value on TEST0 and TEST2 pins. These bits are read-only bits and reflect the value on the corresponding device pins. This allows the host software (S/W) to determine speed configuration. If the network speed and type are software-configurable, these bits are used to determine the configurations that are supported by the network hardware.
<table>
<tr><th>TEST0</th><th>TEST1</th><th>TEST2</th><th>Description</th></tr>
<tr><td>L</td><td>NC</td><td>H</td><td>16-Mbit/s token ring</td></tr>
<tr><td>H</td><td>NC</td><td>H</td><td>4-Mbit/s token ring</td></tr>
<tr><td>X</td><td>X</td><td>L</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3</td><td>Reserved</td><td>Read data should be 0.</td></tr>
<tr><td>4</td><td>SWHLDA</td><td>Software-hold acknowledge. Allows the function of SHLDA/$\overline{SBGR}$ to be emulated from software control for pseudo-DMA mode.
<table>
<tr><th>PSDMAEN</th><th>SWHLDA</th><th>SWHRQ</th><th>Result</th></tr>
<tr><td>0[†]</td><td>X</td><td>X</td><td>SWHLDA value in the SIFACL register cannot be set to a 1.</td></tr>
<tr><td>1[†]</td><td>0</td><td>0</td><td>No pseudo-DMA request pending</td></tr>
<tr><td>1[†]</td><td>0</td><td>1</td><td>Indicates a pseudo-DMA request interrupt</td></tr>
<tr><td>1[†]</td><td>1</td><td>X</td><td>Pseudo-DMA process in progress</td></tr>
</table>
[†] The value on SHLDA/$\overline{SBGR}$ is ignored.</td></tr>
<tr><td>5</td><td>SWDDIR</td><td>Current SDDIR signal value. Contains the current value of the pseudo-DMA direction. This enables the host to easily determine the direction of DMA transfers, which allows system DMA to be controlled by system software.
0 = Pseudo DMA from host system to TI380C30A
1 = Pseudo DMA from TI380C30A to host system</td></tr>
<tr><td>6</td><td>SWHRQ</td><td>Current SHRQ signal value. Contains the current value on SHRQ/$\overline{SBRQ}$ when in Intel mode and the inverse of the value on SHRQ/$\overline{SBRQ}$ in Motorola mode. This enables the host to easily determine if a pseudo-DMA transfer is requested.
<table>
<tr><th>Intel Mode (SI/$\overline{M}$ = H)</th><th>Motorola Mode (SI/$\overline{M}$ = L)</th></tr>
<tr><td>0 = System bus not requested</td><td>1 = System bus not requested</td></tr>
<tr><td>1 = System bus requested</td><td>0 = System bus requested</td></tr>
</table></td></tr>
<tr><td>7</td><td>PSDMAEN</td><td>Pseudo-system-DMA enable. Enables pseudo-DMA operation.
0 = Normal bus-master DMA operation is possible.
1 = Pseudo-DMA operation selected. Operations dependent on the values of the SWHLDA and SWHRQ bits in the SIFACL register.</td></tr>
<tr><td>8</td><td>ARESET</td><td>Adapter reset. ARESET is a hardware reset of the TI380C30A. This bit has the same effect as $\overline{SRESET}$ except that the DIO interface to the SIFACL register is maintained. This bit is set to 1 if a clock failure is detected (OSCIN, PXTAL, RCLK, or SBCLK not valid).
0 = TI380C30A operates normally.
1 = TI380C30A is held in the reset condition.</td></tr>
<tr><td>9</td><td>CPHALT</td><td>Communications processor halt. Controls the TI380C30A processor access to the internal TI380C30A buses. This prevents the TI380C30A from executing instructions before the microcode is downloaded.
0 = TI380C30A processor can access the internal TI380C30A buses.
1 = TI380C30A processor cannot access the internal-adapter buses.</td></tr>
<tr><td>10</td><td>BOOT</td><td>Bootstrap CP code. Indicates whether the memory in chapters 0 and 31 of the local-memory space is RAM or ROM/PROM/EPROM. This bit controls the operation of $\overline{MCAS}$ and $\overline{MROMEN}$.
0 = ROM/PROM/EPROM memory in chapters 0 and 31
1 = RAM memory in chapters 0 and 31</td></tr>
<tr><td>11</td><td>LBP</td><td>Local bus priority. Controls the priority levels of devices on the local bus.
0 = No external devices (such as TI380FPA) are used with the TI380C30A.
1 = An external device (such as TI380FPA) is used with the TI380C30A. This allows the external bus master to operate at the necessary priority on the local bus.
If the system uses the TMS380SRA only, the bit must be set to 0. If the system uses both the TMS380SRA and the TI380FPA, the bit must be set to 1.</td></tr>
</table>

Table 5. SIFACL Bit Definitions (Continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>12</td><td>SINTEN</td><td>
<p>System-interrupt enable. Allows the host processor to enable or disable system-interrupt requests from the TI380C30A. The system-interrupt request from the TI380C30A is on SINTR/$\overline{\text{SIRQ}}$. The following equation shows how SINTR/$\overline{\text{SIRQ}}$ is driven:</p>
<p>SINTR/$\overline{\text{SIRQ}}$ = (PSDMAEN * SWHRQ * !SWHLDA) + (SINTEN * SYSTEM_INTERRUPT)</p>
<p>Results of the states are:</p>
<table>
<tr><th>PSDMAEN</th><th>SWHRQ</th><th>SWHLDA</th><th>SINTEN</th><th>System Interrupt (SIFTS Register)</th><th>Result</th></tr>
<tr><td>1†</td><td>1</td><td>1</td><td>X</td><td>X</td><td>Pseudo DMA is active.</td></tr>
<tr><td>1†</td><td>1</td><td>0</td><td>X</td><td>X</td><td>TI380C30A generates a system interrupt for a pseudo DMA.</td></tr>
<tr><td>1†</td><td>0</td><td>0</td><td>X</td><td>X</td><td>Not a pseudo-DMA interrupt</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td><td>TI380C30A generates a system interrupt.</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>1</td><td>0</td><td>TI380C30A does not generate a system interrupt.</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>0</td><td>X</td><td>TI380C30A cannot generate a system interrupt.</td></tr>
</table>
<p>† The value on SHLDA/$\overline{\text{SBGR}}$ is ignored.</p>
</td></tr>
<tr><td>13</td><td>PEN</td><td>
<p>Parity enable. Determines whether data transfers within the TI380C30A are checked for parity.</p>
<p>0 = Data transfers are not checked for parity.
1 = Data transfers are checked for correct odd parity.</p>
</td></tr>
<tr><td>14–15</td><td>NSELOUT0
NSELOUT1</td><td>
<p>Network-selection outputs. Values control NSELOUT0 and NSELOUT1. These bits can be modified only while the ARESET bit is set.</p>
<p>These bits can be used to software-configure a TI380C30A: NSELOUT0 should be connected to TEST0 (TEST1 should be left unconnected and TEST2 should be tied high). NSELOUT0 and NSELOUT1 are used to select network speed as follows:</p>
<table>
<tr><th>NSELOUT0</th><th>NSELOUT1</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>16-Mbit/s token ring</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>4-Mbit/s token ring</td></tr>
</table>
<p>At power up, these bits are set corresponding to 16-Mbit/s token ring (NSELOUT1 = 1, NSELOUT0 = 0). New values are saved only if written in the same cycle that the ARESET bit is cleared.</p>
</td></tr>
</table>

SIFACL control for pseudo-DMA operation

Pseudo-DMA operation is software-controlled by using five bits in the SIFACL register. The logic model for the SIFACL control of pseudo-DMA operation is shown in Figure 5.

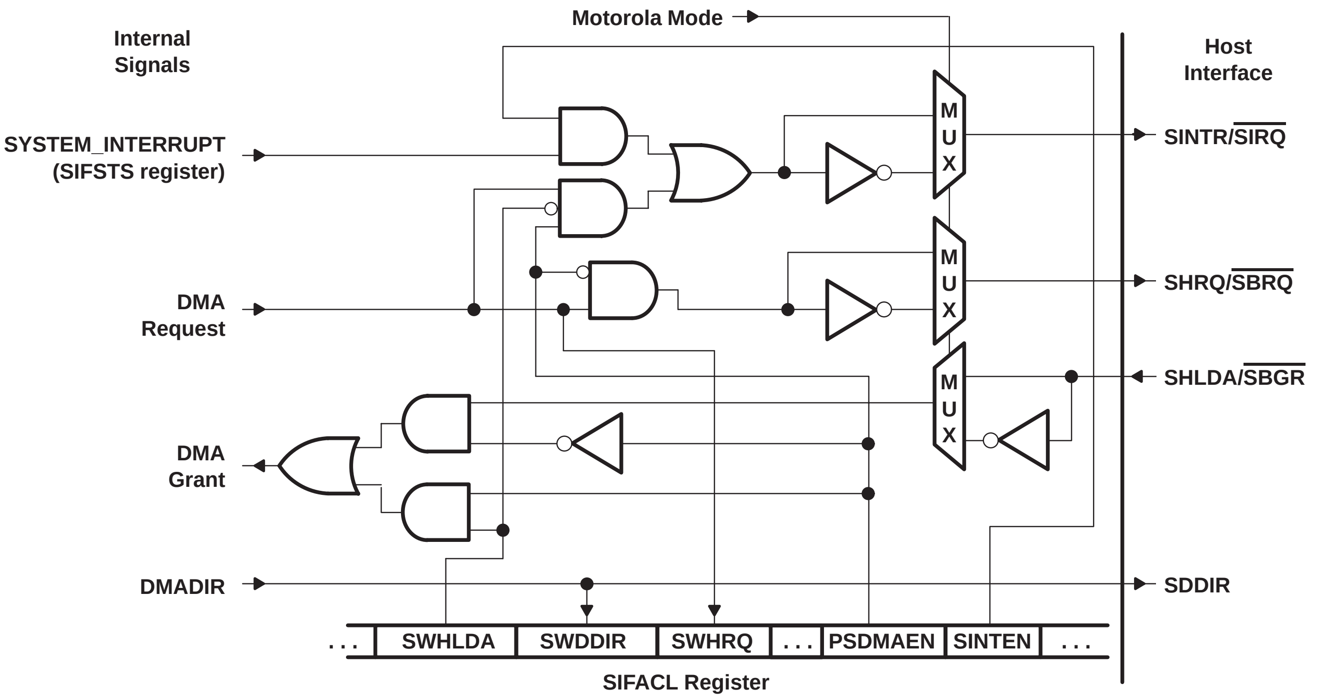


Figure 5. Pseudo-DMA Logic Related to SIFACL Bits

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 8)	–0.5 V to 7 V
Input voltage range (see Note 8)	–0.5 V to 7 V
Output voltage range	–0.5 V to 7 V
Power dissipation	1.25 W
Operating case temperature, T_C	0°C to 95°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 8: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	TTL-level signal	2		V_{DD}+0.3	V
		OSCIN	2.4		V_{DD}+0.3	
		RCLK, PXTAL, RCVR, XT1	2.6		V_{DD}+0.3	
V_{IL}	Low-level input voltage, TTL-level signal (see Note 9)		–0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			–400	µA
I_{OL}	Low-level output current (see Note 10)	TTL outputs			2	mA
T_C	Operating case temperature		0		95	°C

NOTES: 9. The algebraic convention, where the more-negative (less-positive) limit is designated as a minimum, is used for logic-voltage levels only.

10. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 11)		V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal		V_{DD} = MIN,	I_{OL} = MAX			0.6	V
I_{OZ}	High-impedance output current		V_{DD} = MAX,	V_O = 2.4 V			20	µA
			V_{DD} = MAX,	V_O = 0.4 V			–20	
I_I	Input current, any input or input/output		V_I = V_{SS} to V_{DD}				± 20	µA
I_{CC}	Supply current	Normal mode	V_{DD} = MAX			200		mA
		Power-down mode	V_{DD} = 5 V			20		
C_i	Input capacitance, any input		f = 1 MHz,	Others at 0 V			15	pF
C_o	Output capacitance, any output or input/output		f = 1 MHz,	Others at 0 V			15	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

NOTE 11: The following signals require an external pullup resistor: SRAS/$\overline{\text{SAS}}$, $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$, $\overline{\text{SRD}}$/$\overline{\text{SUDS}}$, $\overline{\text{SWR}}$/$\overline{\text{SLDS}}$, $\overline{\text{EXTINT0}}$–$\overline{\text{EXTINT3}}$, and $\overline{\text{MBRQ}}$.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

receiver input (RCV+ and RCV–)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_B	Receiver-input bias voltage	See Note 12	V_{SB}–1	V_{SB}+1	V
V_{T+}	Rising-input threshold voltage	$V_{ICM} = V_{SB}$, R_{tst} = 330 Ω, See Notes 12, 13, and Figure 6		50	mV
V_{T-}	Falling-input threshold voltage	$V_{ICM} = V_{SB}$, R_{tst} = 330 Ω, See Notes 12, 13, and Figure 6	–50		mV
V_{AT}	Asymmetry threshold voltage, $(V_{T+} + V_{T-})/2$	$V_{ICM} = V_{SB}$, R_{tst} = 330 Ω, See Notes 12, 13, and Figure 6	–15	15	mV
$V_{r(CM)}$	Rising-input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	See Notes 12, 13, and Figure 6	–30	30	mV
$V_{f(CM)}$	Falling-input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	See Notes 12, 13, and Figure 6	–30	30	mV
$I_{I(RCVR)}$	Receiver input current	Both inputs at V_{SB}, See Note 12 and Figure 6	–10	10	µA
		Input under test at V_{SB} + 1 V, Other input at V_{SB} – 1 V, See Notes 12 and 13 and Figure 6	10	60	
		R_{tst} = 330 Ω, Input under test at V_{SB} – 1 V, Other input at V_{SB} + 1 V, See Note 12	–10	–60	
I_{EQB}	Equalizer bias current	RCV+ at 4 V, RCV– at 1 V or RCV+ at 1 V, RCV– at 4 V, See Figure 6	1.0	2.2	mA
V_{EQW}	Equalizer wrap voltage	$\overline{\text{WRAP}}$ = low, See Figure 6	300	700	mV

NOTES: 12. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) \div 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} \div 2$.

13. V_{ICM} is the common-mode voltage applied to RCV+ and RCV–.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	4.1		V
		I_{OH} = –2 mA	3.8		V
I_{OS}	Short-circuit output current	V_O = 0 V	–4	–20	mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	1	10	mA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{DD}$	–100	100	µA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0 V	–100	100	µA

wire fault ($\overline{\text{WFLT}}$) (see Notes 14 and 15)

PARAMETER		MIN	MAX	UNIT
R_{LS}	Phantom load resistance detected as short circuit		0.15	kΩ
R_{LO}	Phantom load resistance detected as open circuit	50		kΩ
R_{LN}	Phantom load resistance detected as normal	2.9	5.5	kΩ

NOTES: 14. The wire-fault circuit recognizes a fault condition for any phantom-drive load resistance to ground of greater than R_{LO} or any load resistance less than R_{LS}. Any resistance in the range specified for R_{LN} is not recognized as a wire fault. A fault condition on either PHOUTA or PHOUTB results in the $\overline{\text{WFLT}}$ signal being asserted (low).

15. Resistor (R_{LS}, R_{LO}, R_{LN}) connected from output under test to ground, other output loaded with 4.1 Ω to ground.

PLL characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{FILT}	Reference PLL operating filter voltage	$t_{c(XT1)}$ = 125 ns	1.8	4	V

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

crystal-oscillator characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{SB(XT1)}$	Input self-bias voltage		1.8	4	V
$I_{OH(XT2)}$	Output high-level current	$V_{(XT2)} = V_{SB(XT1)}$, $V_{(XT1)} = V_{SB(XT1)} + 0.5$ V	–2.5	–6.5	mA
$I_{OL(XT2)}$	Output low-level current	$V_{(XT2)} = V_{SB(XT1)}$, $V_{(XT1)} = V_{SB(XT1)} – 0.5$ V	0.4	1.3	mA

timing parameters

The timing parameters for the signals of TI380C30A are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

Table 6 lists signals that are not allowed to change dynamically and therefore have no timing associated with them. They should be strapped high, low, or left unconnected as required.

Table 6. Static Signals and Functions

SIGNAL	FUNCTION
SI/$\overline{\text{M}}$	Host-processor select (Intel/Motorola)
CLKDIV	Clock divider select
BTSTRP	Default-bootstrap mode (RAM/ROM)
PRTYEN	Default-parity select (enabled/disabled)
TEST0	Test pin indicates network type
TEST1	NC
TEST2	Test pin indicates network type
TEST3	Test pin for TI manufacturing test†
TEST4	Test pin for TI manufacturing test†
TEST5	Test pin for TI manufacturing test†

† For unit-in-place test

timing parameter symbology

Some timing parameter symbols have been created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the signal names and other related terminology have been abbreviated as:

DR	DRVR
DRN	$\overline{\text{DRVR}}$
OSC	OSCIN
RS	$\overline{\text{SRESET}}$
SCK	SBCLK
VDD	V_{DDL}, V_{DD}

Lower-case subscripts are defined as:

c	Cycle time
d	Delay time
h	Hold time
r	Rise time
sk	Skew
su	Setup time
t	Transition time
w	Pulse duration

The following additional letters and phrases are defined as:

L	Low
H	High
V	Valid
Z	High impedance
Falling edge	No longer high
Rising edge	No longer low

PARAMETER MEASUREMENT INFORMATION

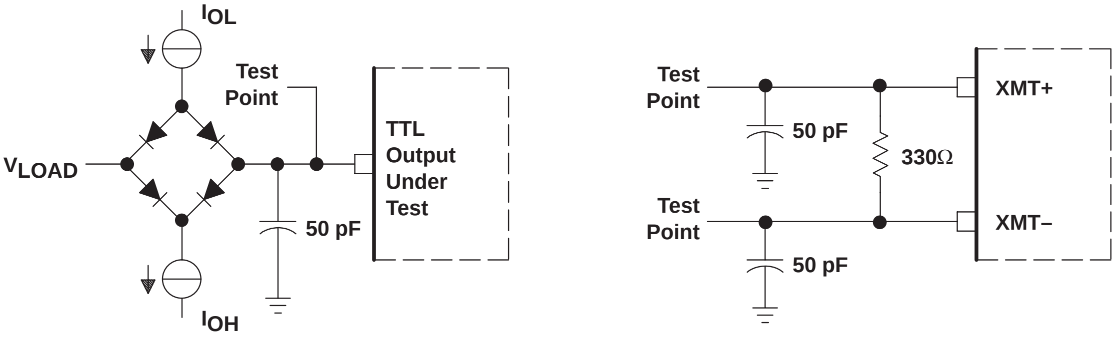
Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which typically are 1.5 ns.

test measurement

The test-load circuit shown in Figure 6 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TI380C30A output signals.



(a) TTL-OUTPUT TEST LOAD

(b) XMT+ and XMT– TEST LOAD

(c) I_{ref} TEST CIRCUIT

(d) EQUALIZER TEST CIRCUIT

Where: V_{LOAD} = 1.5 V, typical dc-level verification or
0.7 V, typical timing verification

Figure 6. Test and Load Circuits

switching characteristics over recommended range of supply voltage (unless otherwise noted)

transmitter drive characteristics (see Figures 6 and 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{PP(XMT)}$	XMT+/XMT– peak-to-peak voltage (see Note 16)	V_{DD} = 4.75 V	8.2		V
		V_{DD} = 5.25 V		10.3	

NOTE 16: $V_{PP(XMT)}$ is determined by: $V_{OH(XMT+)} + V_{OH(XMT–)} – V_{OL(XMT+)} – V_{OL(XMT–)}$

transmitter switching characteristics (see Figures 6 and 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
XMT+/XMT– skew (see Note 17)	$t_{sk(DRV)}$ = – 1 ns	–3	3	ns
	$t_{sk(DRV)}$ = + 1 ns	–3	3	
XMT+/XMT– asymmetry (see Note 18)	$t_{sk(DRV)}$ = –1 ns	–2	2	ns
	$t_{sk(DRV)}$ = + 1 ns	–2	2	

NOTES: 17. XMT+/XMT– skew is determined by: $t_{d(XMT + H)} – t_{d(XMT – L)}$ or $t_{d(XMT + L)} – t_{d(XMT – H)}$

18. XMT+/XMT– asymmetry is determined by:

$$\frac{t_{d(XMT+L)} + t_{d(XMT-H)}}{2} - \frac{t_{d(XMT+H)} + t_{d(XMT-L)}}{2}$$

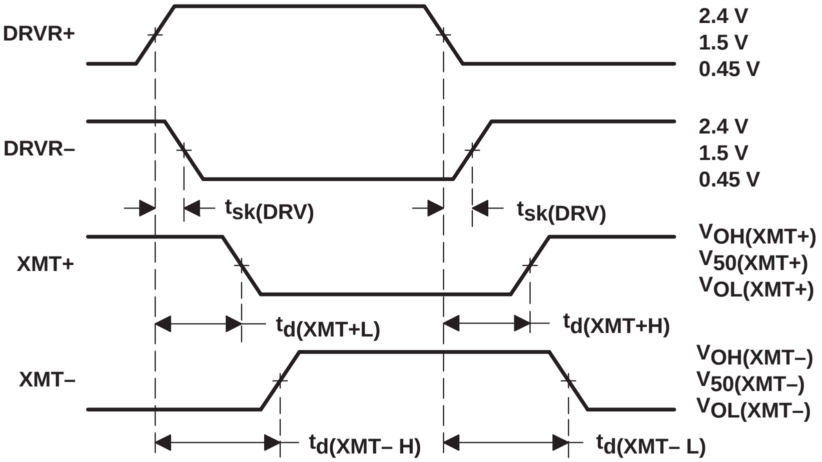


Figure 7. Transmitter

clock and data switching characteristics over recommended range of supply voltage, $t_{c(XT1)}$ = 125 ns (see Figure 8)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(XT1)}$	Cycle time of clock applied to XT1			125		ns
$t_{w(OSC32H)}$	Pulse duration, OSC32 high		10			ns
$t_{w(OSC32L)}$	Pulse duration, OSC32 low		12			ns
$t_{w(PXTALL)}$	Pulse duration, PXTAL low	16-Mbit/s mode	12			ns
		4-Mbit/s mode	46			
$t_{w(PXTALH)}$	Pulse duration, PXTAL high	16-Mbit/s mode	10			ns
		4-Mbit/s mode	46			
$t_{w(RCLKL)}$	Pulse duration, RCLK low	16-Mbit/s mode	12			ns
		4-Mbit/s mode	46			
$t_{w(RCLKH)}$	Pulse duration, RCLK high	16-Mbit/s mode	10			ns
		4-Mbit/s mode	46			
$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge	16-Mbit/s mode	18			ns
$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge	16-Mbit/s mode	1			ns

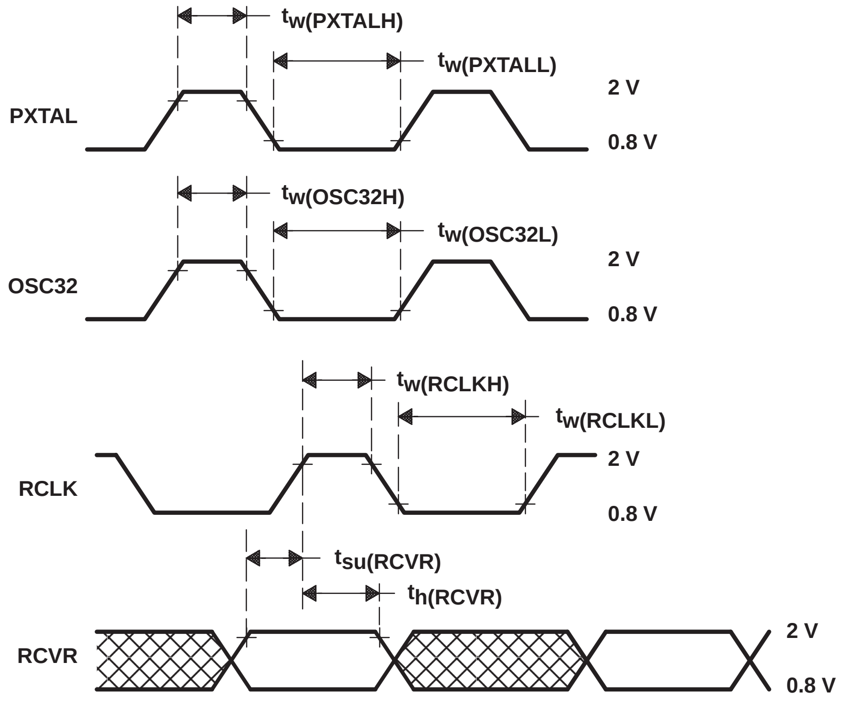


Figure 8. PXTAL, OSC32, RCLK, and RCVR

timing for power-up, SBCLK, OSCIN, MBCLK1, MBCLK2, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$ (see Figure 9)

NO.				MIN	NOM	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level				1	ms
101†‡	$t_{d(VDDH\text{-}SCKV)}$	Delay time, minimum V_{DD}-high level to first valid SBCLK no longer high				1	ms
102†‡	$t_{d(VDDH\text{-}OSCV)}$	Delay time, minimum V_{DD}-high level to first valid OSCIN high				1	ms
103	$t_{c(SCK)}$	Cycle time, SBCLK (see Note 19)		30.3		500	ns
104	$t_{w(SCKH)}$	Pulse duration, SBCLK high		13		500	ns
105	$t_{w(SCKL)}$	Pulse duration, SBCLK low		13		500	ns
106†	$t_{t(SCK)}$	Transition time, SBCLK				2	ns
107	$t_{c(OSC)}$	Cycle time, OSCIN (see Note 20)			1/OSCIN		ns
108	$t_{w(OSCH)}$	Pulse duration, OSCIN high (see Note 21)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
109	$t_{w(OSCL)}$	Pulse duration, OSCIN low (see Note 21)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
110†	$t_{t(OSC)}$	Transition time, OSCIN				3	ns
111†	$t_{d(OSCV\text{-}CKV)}$	Delay time, OSCIN valid to MBCLK1 and MBCLK2 valid				1	ms
117†	$t_{h(VDDH\text{-}RSL)}$	Hold time, $\overline{\text{SRESET}}$ low after V_{DD} reaches minimum high level		5			ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{SRESET}}$ high		14			µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{SRESET}}$ low		14			µs
288†	$t_{su(RST)}$	Setup time, DMA size to $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
289†	$t_{h(RST)}$	Hold time, DMA size from $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
	t_M	One-eighth of a local-memory cycle	CLKDIV = H	$2t_{c(OSC)}$			ns
			CLKDIV = L	$t_{c(OSC)}$			

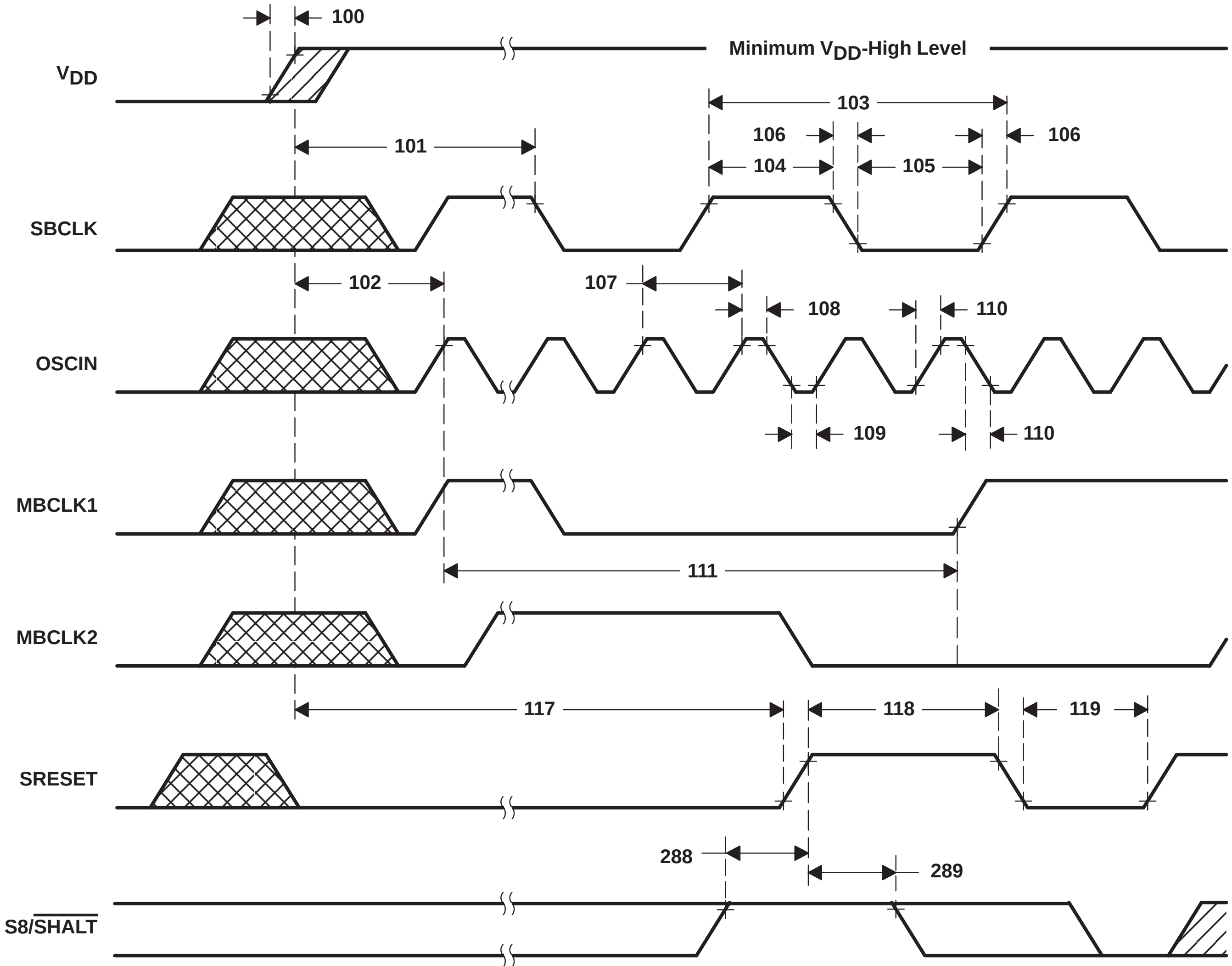
† This specification is provided as an aid to board design.

‡ If parameter 101 or 102 cannot be met, parameter 117 must be extended by the larger difference: real value of parameter 101 or 102 minus the max value listed.

NOTES: 19. SBCLK can be any value between 2 MHz and 33 MHz. This data sheet describes the system interface (SIF) timing parameters for the cases of SBCLK at 25 MHz and 33 MHz.

20. The value of OSCIN can be 64 MHz ±1%, 32 MHz ± 1%, or 48 MHz ± 1%. If OSCIN is used to generate PXTAL, the OSCIN tolerance must be ±0.01%.

21. This maintains a ± 5% duty-cycle crystal, provided that OSCIN meets the recommended operating conditions for V_{IH} and V_{IL}.



NOTE A: To represent the information in one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

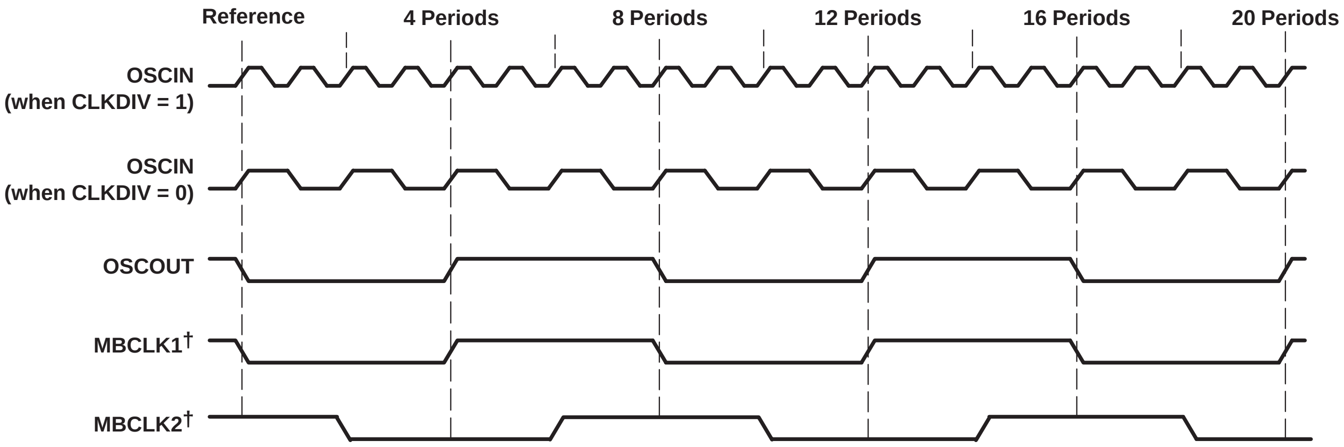
Figure 9. Power-Up, System Clocks, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$

memory-bus timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

local-memory clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and address (see Figures 10 and 11)

NO.		MIN	MAX	UNIT
1	Period of MBCLK1 and MBCLK2	$4t_M$		ns
2	Pulse duration, MBCLK1/MBCLK2 high	$2t_M–9$		ns
3	Pulse duration, MBCLK1/MBCLK2 low	$2t_M–9$		ns
4	Hold time, MBCLK2 low after MBCLK1 high	$t_M–9$		ns
5	Hold time, MBCLK1 high after MBCLK2 high	$t_M–9$		ns
6	Hold time, MBCLK2 high after MBCLK1 low	$t_M–9$		ns
7	Hold time, MBCLK1 low after MBCLK2 low	$t_M–9$		ns
8	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer high	$t_M–9$		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	$t_M–14$		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	$t_M–14$		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	13		ns
12	Setup time, address on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer low	$0.5t_M–9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M–9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M–9$		ns
120	Setup time, $\overline{\text{NMI}}$ valid before MBCLK1 low	30		ns
121	Hold time, $\overline{\text{NMI}}$ valid after MBCLK1 low	0		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	$t_M–7$		ns



† MBCLK1 and MBCLK2 have no timing relationship to OSCOUT. MBCLK1 and MBCLK2 can start on any OSCIN rising edge, depending on when the memory cycle starts execution.

Figure 10. Clock Waveforms After Clock Stabilization

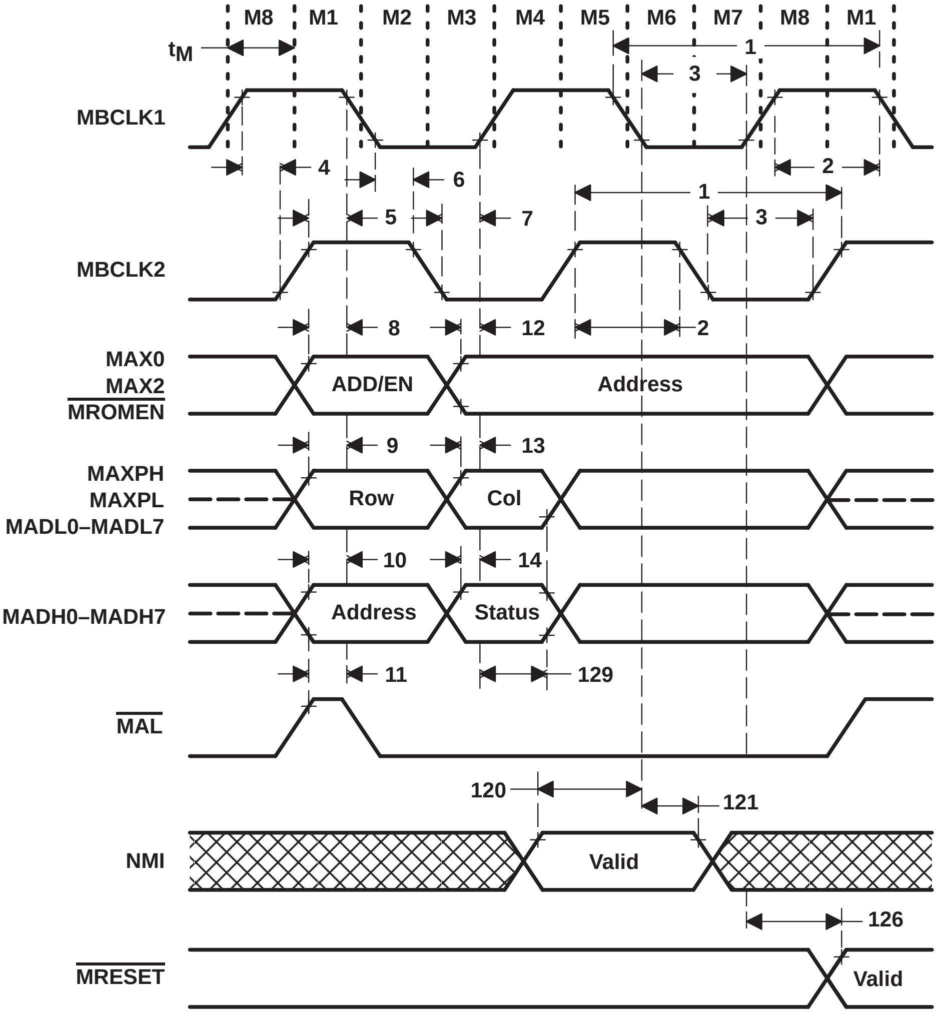


Figure 11. Memory Bus – Local-Memory Clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and Address

memory-bus timing (continued)

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to address (see Figure 12)

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M–11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M–6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M–5$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M–5$		ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M–9$		ns
21	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M–5$		ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M–6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M–9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M–9$		ns
25	Hold time, row address on MAXL0–MAXL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M–9$		ns
26	Setup time, row address on MAXL0–MAXL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M–9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M–9$		ns
28	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MAL}}$ no longer high	$t_M–9$		ns
29	Hold time, address/enable of MAX0, MAX2, and $\overline{\text{MROMEN}}$ after $\overline{\text{MAL}}$ low	$1.5t_M–9$		ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M–9$		ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M–9$		ns

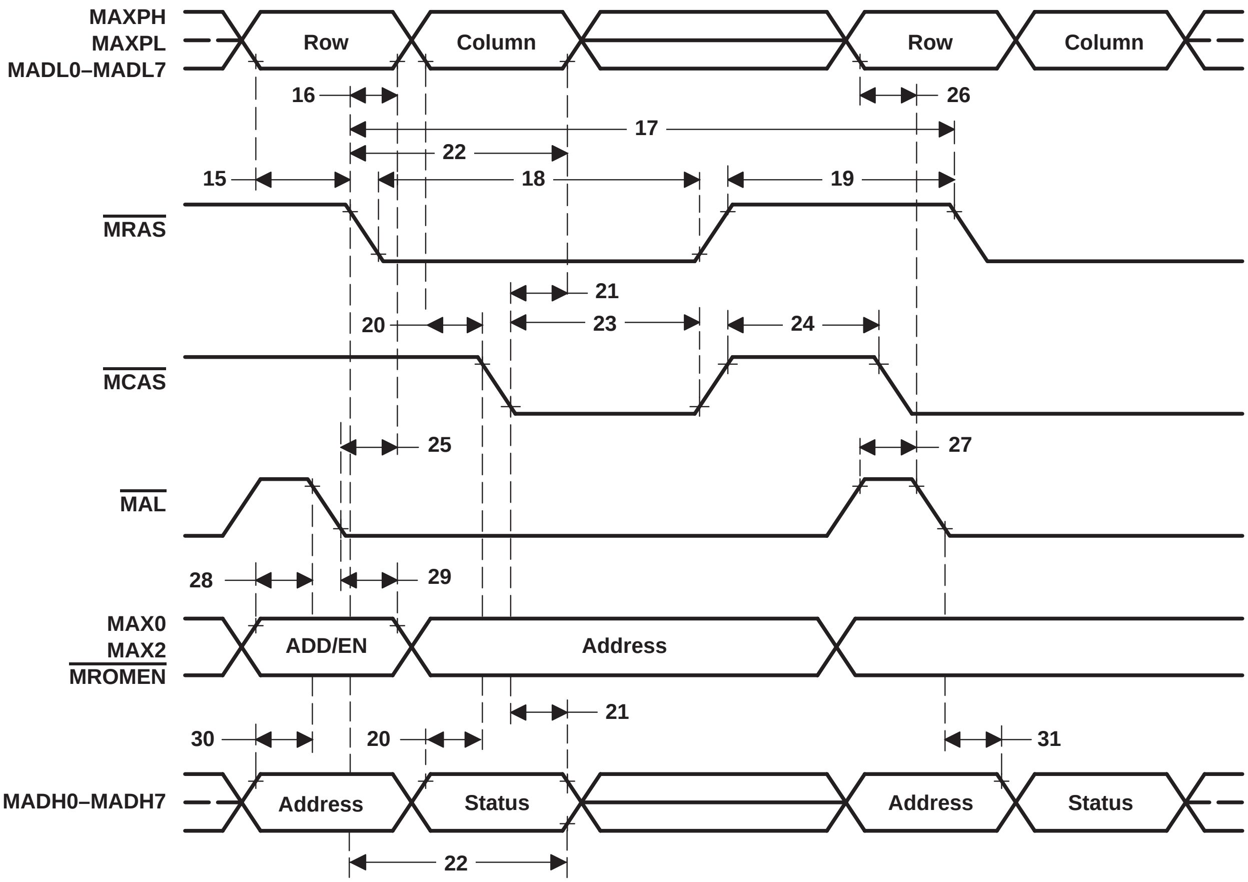


Figure 12. Memory Bus – Clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to Address

memory-bus timing (continued)

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

memory-bus read cycle (see Figure 13)

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ to valid data/parity		6t_M–23	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		6t_M–23	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		4.5t_M–21.5	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{\text{MRAS}}$ high (see Note 22)	2t_M–10.5		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		3t_M–23	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MCAS}}$ high (see Note 22)	2t_M–13		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		t_M+13	ns
42	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		2t_M–20	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	2t_M–9		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	3t_M–9		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MOE}}$ high (see Note 22)	2t_M–15		ns
48	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
48a	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 and before $\overline{\text{MBIAEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		2t_M–25	ns
49a	Access time, $\overline{\text{MBIAEN}}$ low to valid data/parity		2t_M–25	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	2t_M–9		ns
50a	Pulse duration, $\overline{\text{MBIAEN}}$ low	2t_M–9		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
51a	Hold time, valid data/parity after $\overline{\text{MBIAEN}}$ no longer low	0		ns
52	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBEN}}$ high (see Note 22)	2t_M–15		ns
52a	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBIAEN}}$ high	2t_M–15		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	1.5t_M–12		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	3t_M–5		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	3t_M–12		ns

NOTE 22: The data/parity that exists on the address lines most likely will reach the high-impedance state some time later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address, and does not represent the actual high-impedance period on the address bus.

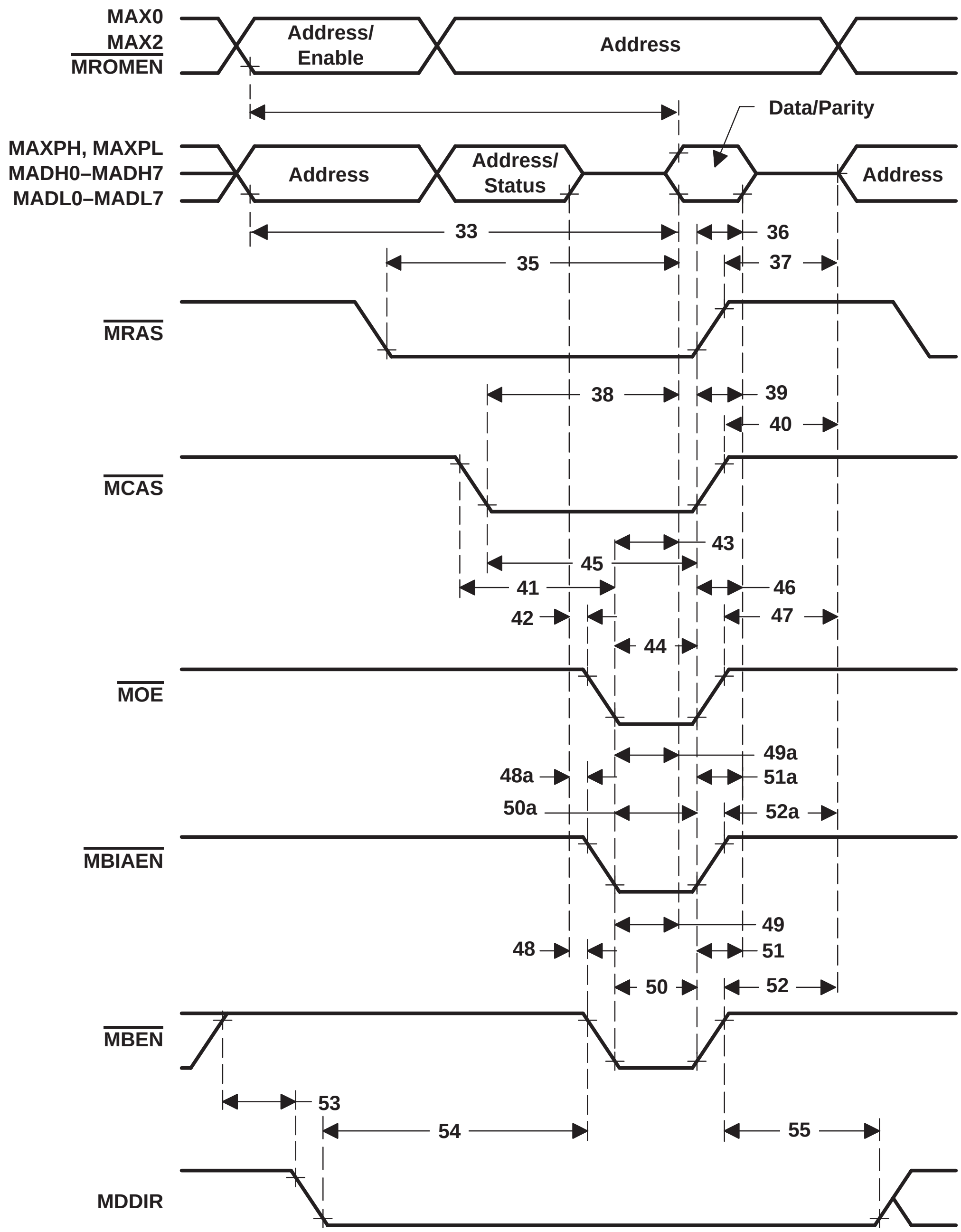


Figure 13. Memory-Bus Read Cycle

memory-bus timing (continued)

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

memory-bus write cycle (see Figure 14)

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{\text{MW}}$ low before $\overline{\text{MRAS}}$ no longer low	t_M		ns
60	Setup time, $\overline{\text{MW}}$ low before $\overline{\text{MCAS}}$ no longer low	$1.5t_M$–6.5		ns
63	Setup time, valid data/parity before $\overline{\text{MW}}$ no longer high	5.1		ns
64	Pulse duration, $\overline{\text{MW}}$ low	$2.5t_M$–9		ns
65	Hold time, data/parity out valid after $\overline{\text{MW}}$ high	$0.5t_M$–10.5		ns
66	Setup time, address valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MW}}$ no longer low	$7t_M$–11.5		ns
67	Hold time, $\overline{\text{MRAS}}$ low to $\overline{\text{MW}}$ no longer low	$5.5t_M$–9		ns
69	Hold time, $\overline{\text{MCAS}}$ low to $\overline{\text{MW}}$ no longer low	$4t_M$–11.5		ns
70	Setup time, $\overline{\text{MBEN}}$ low before $\overline{\text{MW}}$ no longer high	$1.5t_M$–13.5		ns
71	Hold time, $\overline{\text{MBEN}}$ low after $\overline{\text{MW}}$ high	$0.5t_M$–6.5		ns
72	Setup time, MDDIR high before $\overline{\text{MBEN}}$ no longer high	$2t_M$–9		ns
73	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high	$1.5t_M$–12		ns

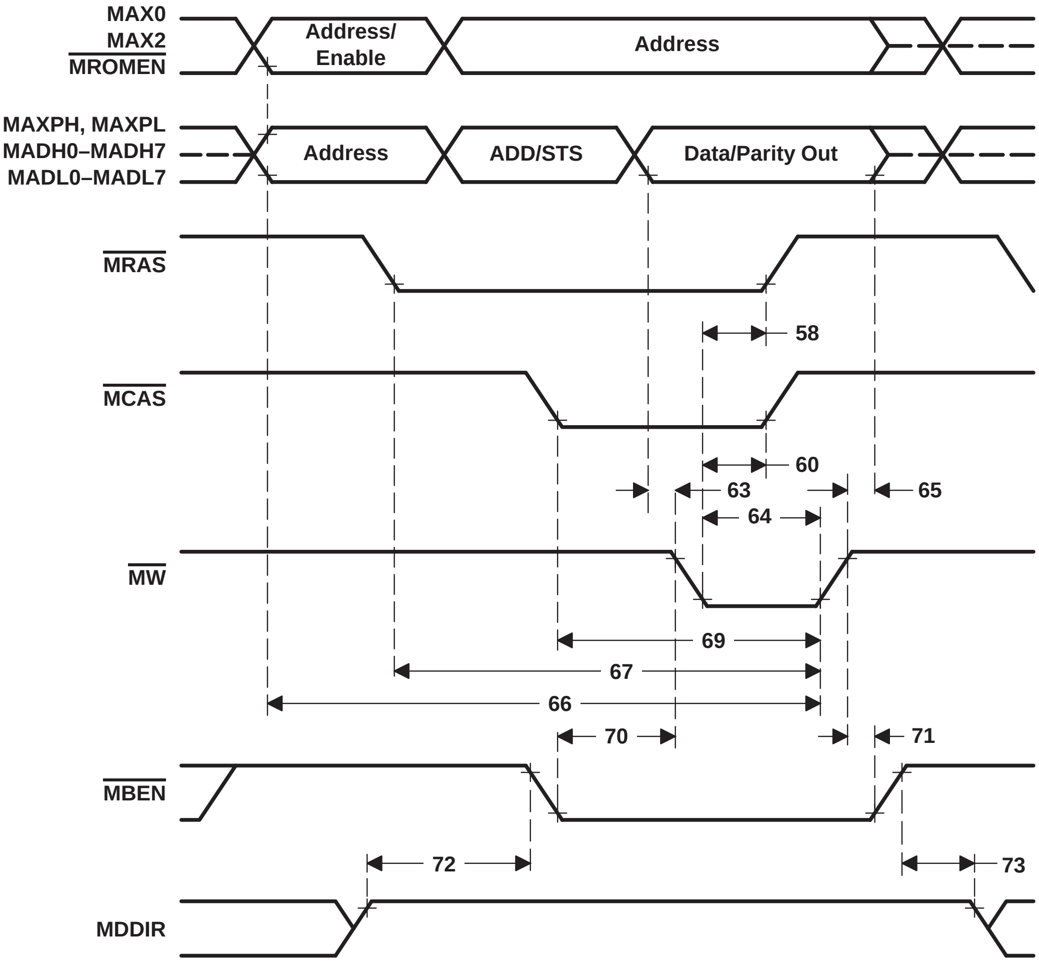


Figure 14. Memory-Bus Write Cycle

memory-bus timing (continued)

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

DRAM-refresh cycle (see Figure 15)

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M$–11.5		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	t_M–6.5		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M$–5		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M$–5		ns
73a	Setup time, $\overline{\text{MCAS}}$ low before $\overline{\text{MRAS}}$ no longer high	$1.5t_M$–11.5		ns
73b	Hold time, $\overline{\text{MCAS}}$ low after $\overline{\text{MRAS}}$ low	$4.5t_M$–6.5		ns
73c	Setup time, MREF high before $\overline{\text{MCAS}}$ no longer high	14		ns
73d	Hold time, MREF high after $\overline{\text{MCAS}}$ high	t_M–9		ns

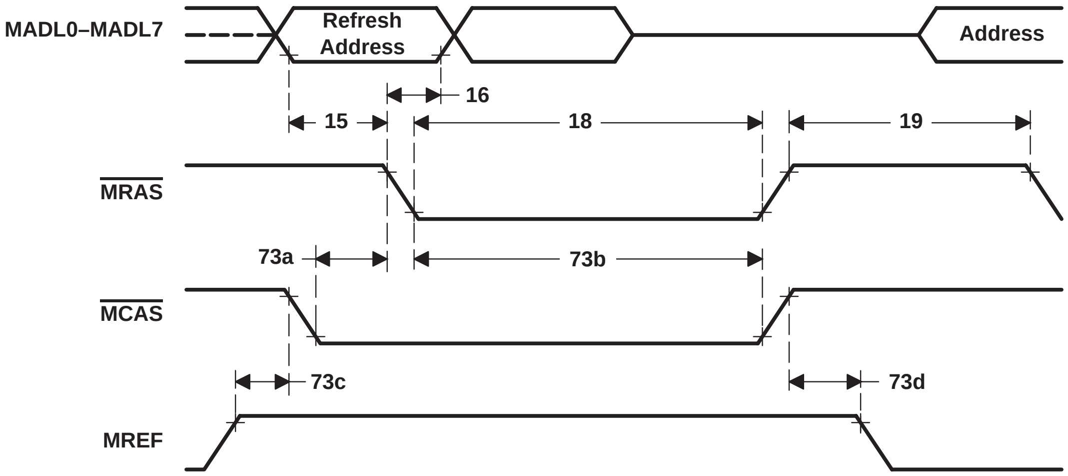


Figure 15. Memory-Bus DRAM-Refresh Cycle

XMATCH and XFAIL timing (see Figure 16)

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.			MIN	MAX	UNIT
127	Delay time, status bit 7 high to XMATCH and XFAIL recognized		$7t_M$		ns
128	Pulse duration, XMATCH or XFAIL high	4-MHz local bus	50		ns
		6-MHz local bus	30		

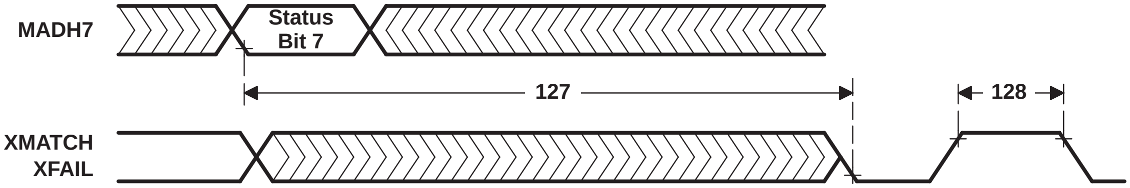


Figure 16. XMATCH and XFAIL

token-ring timing

ring interface (see Figure 17)

NO.			MIN	TYP	MAX	UNIT
153	Period of RCLK (see Note 23)	4 Mbit/s		125		ns
		16 Mbit/s		31.25		
154L	Pulse duration, RCLK low	4 Mbit/s nominal: 62.5 ns	46			ns
		16 Mbit/s nominal: 15.625 ns	15			
154H	Pulse duration, RCLK high	4 Mbit/s nominal: 62.5 ns	35			ns
		16 Mbit/s nominal: 15.625 ns	8			
155	Setup time, RCVR valid before rising edge (1.8 V) of RCLK at 16 Mbit/s		10			ns
156	Hold time, RCVR valid after rising edge (1.8 V) of RCLK at 16 Mbit/s		1			ns
158L	Pulse duration, ring-baud clock low	4 Mbit/s	40			ns
		16 Mbit/s	8			
158H	Pulse duration, ring-baud clock high	4 Mbit/s	40			ns
		16 Mbit/s	8			
165	Period of OSCOUT and PXTAL (see Note 23)	4 Mbit/s		125		ns
		16 Mbit/s (for PXTALIN only)		31.25		
	Tolerance of PXTAL input frequency (see Note 23)				±0.01	%

NOTE 23: This parameter is not tested but is required by the IEEE Std 802.5 specification.

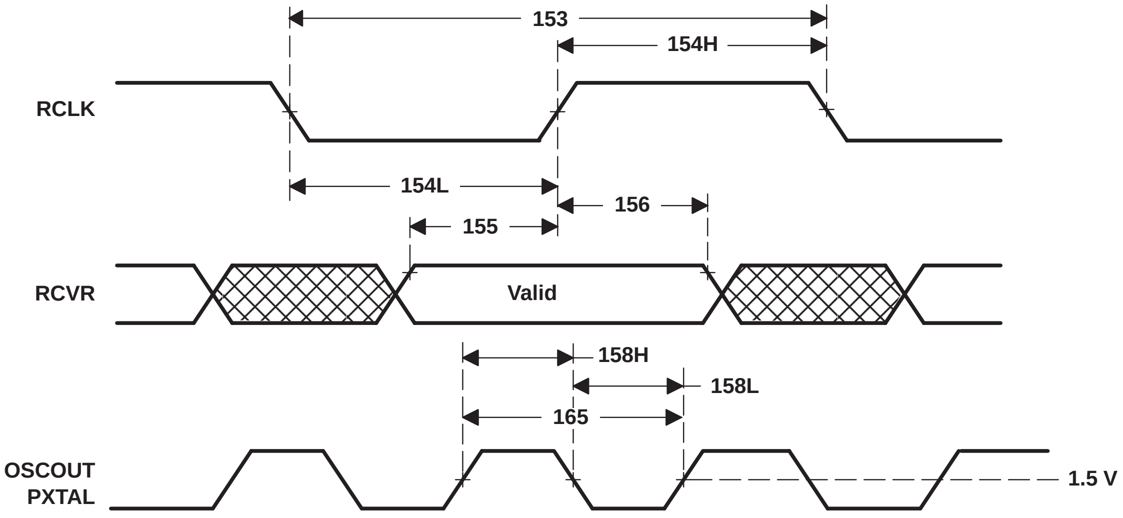


Figure 17. Ring Interface

transmitter timing (see Figure 18)

NO.			MIN	MAX	UNIT
159	$t_{sk(DR)}$	Delay time, DRVR+ rising edge (1.8 V) to DRVR– falling edge (1 V) or DRVR+ falling edge (1 V) to DRVR– rising edge (1.8 V)		±2	ns
160	$t_{d(DR)H}$†	Delay time, RCLK (or PXTAL) falling edge (1 V) to DRVR+ rising edge (1.8 V)	See Note 24		ns
161	$t_{d(DR)L}$†	Delay time, RCLK (or PXTAL) falling edge (1 V) to DRVR+ falling edge (1 V)	See Note 24		ns
162	$t_{d(DRN)H}$†	Delay time, RCLK (or PXTAL) falling edge (1 V) to DRVR– falling edge (1 V)	See Note 24		ns
163	$t_{(DRN)L}$†	Delay time, RCLK (or PXTAL) falling edge (1 V) to DRVR– rising edge (1.8 V)	See Note 24		ns
164	DRVR+/DRVR– asymmetry	$\frac{t_{d(DR)L} + t_{d(DRN)H}}{2} - \frac{t_{d(DR)H} + t_{d(DRN)L}}{2}$		±1.5	ns

† When in active-monitor mode, the clock source is PXTAL; otherwise, the clock source is either RCLK or PXTAL.

NOTE 24: This parameter is not tested to a minimum or a maximum, but is measured and used as a component required for parameter 164.

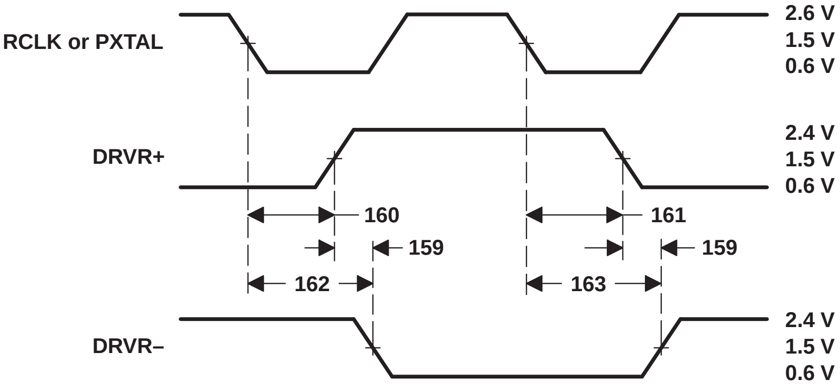


Figure 18. Skew and Asymmetry From RCLK or PXTAL to DRVR+ and DRVR–

80x8x DIO timing

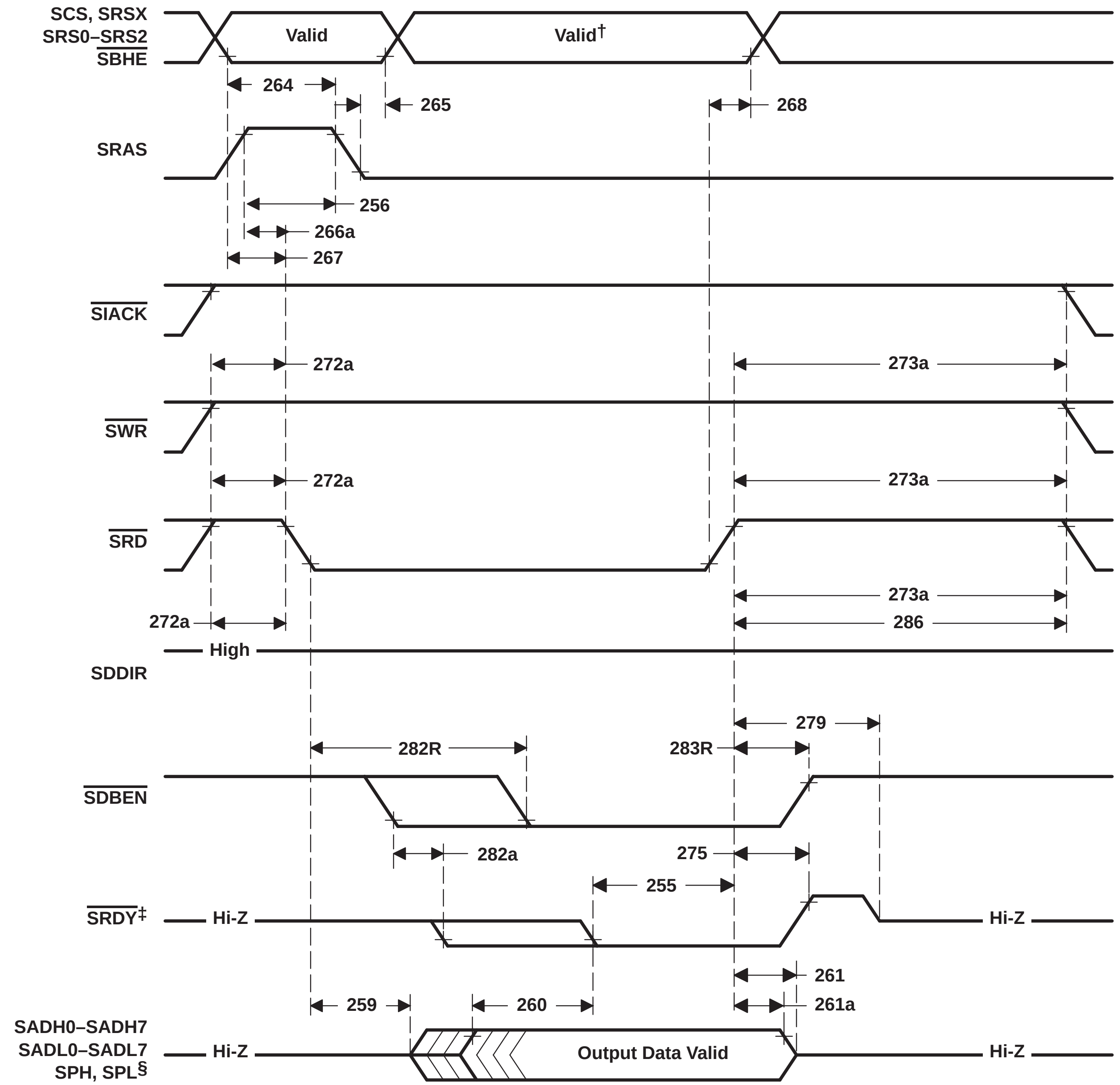
80x8x DIO read cycle (see Figure 19)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SRD}}$ high	15		15		ns
256	Pulse duration, SRAS high	30		30		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SRD}}$ low (see Note 25)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ high to SAD in the high-impedance state (see Note 25)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ high (see Note 25)	0		0		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ valid to SRAS no longer high (see Note 26)	30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ valid after SRAS low	10		10		ns
266a	Setup time, SRAS high to $\overline{\text{SRD}}$ no longer high (see Note 26)	15		15		ns
267‡	Setup time, SRSX, SRS0–SRS2 valid before $\overline{\text{SRD}}$ no longer high (see Note 25)	15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{\text{SRD}}$ no longer low (see Note 26)	0		0		ns
272a	Setup time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high from previous cycle to $\overline{\text{SRD}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high after $\overline{\text{SRD}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$, or $\overline{\text{SCS}}$ high to $\overline{\text{SRDY}}$ high (see Note 25)	0	25	0	25	ns
279†	Delay time, $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$, high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{\text{SRD}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* literature number SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{\text{SRD}}$ high to $\overline{\text{SDBEN}}$ high (see Note 25)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{\text{SRD}}$ high between DIO accesses (see Note 25)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design.
‡ It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

NOTES: 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.

26. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† In 80x8x mode, SRAS can be used to strobe the values of SBHE, SRSX, SRS0–SRS2, and SCS. When used to do so, SRAS must meet parameter 266a; SBHE, SRS0–SRS2, and SCS must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

‡ When the TMS380C30A begins to drive SDBEN inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

§ In 8-bit 80x8x-mode DIO reads, the SADH0–SADH7 contain don't-care data.

Figure 19. 80x8x DIO Read Cycle

80x8x DIO write cycle (see Figure 20)

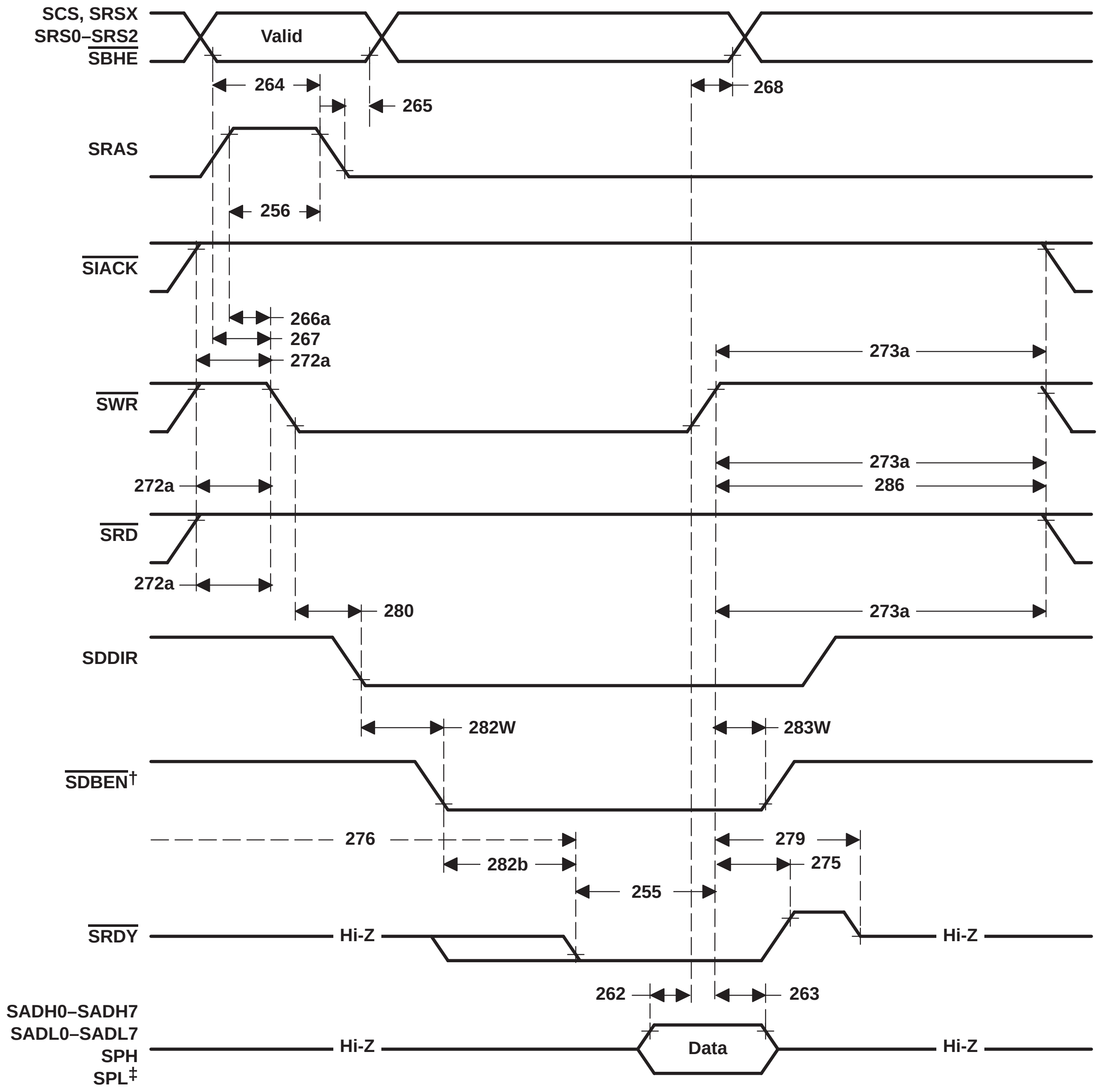
NO.			25-MHZ OPERATION		33-MHZ OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high		15		15		ns
256	Pulse duration, SRAS high		30		30		ns
262	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ no longer low		15		15		ns
263	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high		15		15		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ to SRAS no longer high (see Note 26)		30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ after SRAS low		10		10		ns
266a	Setup time, SRAS high to $\overline{\text{SWR}}$ no longer high (see Note 25)		15		15		ns
267†	Setup time, SRSX, SRS0–SRS2 before $\overline{\text{SWR}}$ no longer high (see Note 25)		15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{\text{SWR}}$ no longer low (see Note 26)		0		0		ns
272a	Setup time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high from previous cycle to $\overline{\text{SWR}}$ no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high after $\overline{\text{SWR}}$ high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
276	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF (see *TMS380 Second-Generation Token-Ring User's Guide*, literature number SPWU005, subsection 3.4.1.1.1)			4000		4000	ns
275	Delay time, $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ high to $\overline{\text{SRDY}}$ high (see Note 25)		0	25	0	25	ns
279‡	Delay time, $\overline{\text{SWR}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{\text{SWR}}$ low to SDDIR low (see Note 25)		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282b	Delay time, SDBEN low to SRDY low (see *TMS380 Second Generation Token-Ring User's Guide,* literature number SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{\text{SDBEN}}$ low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
283W	Delay time, $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high to $\overline{\text{SDBEN}}$ no longer low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{\text{SWR}}$ high between DIO accesses (see Note 25)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

‡ This specification is provided as an aid to board design.

NOTES: 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.

26. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† When the TMS380C30A begins to drive SDBEN inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

‡ In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don’t care.

Figure 20. 80x8x DIO Write Cycle

80x8x interrupt-acknowledge-cycle timing

first $\overline{\text{SIACK}}$ pulse (see Figure 21)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 25)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
287	Pulse duration, $\overline{\text{SIACK}}$ low on first pulse of two pulses	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

NOTE 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.

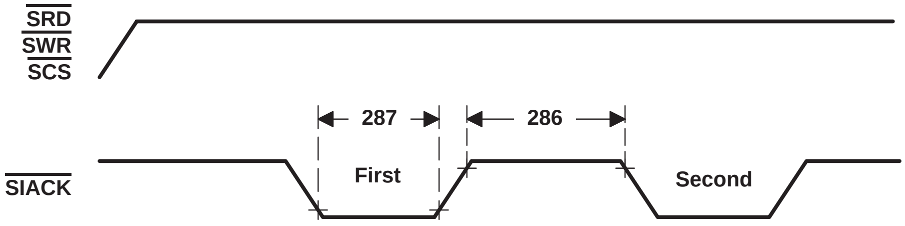


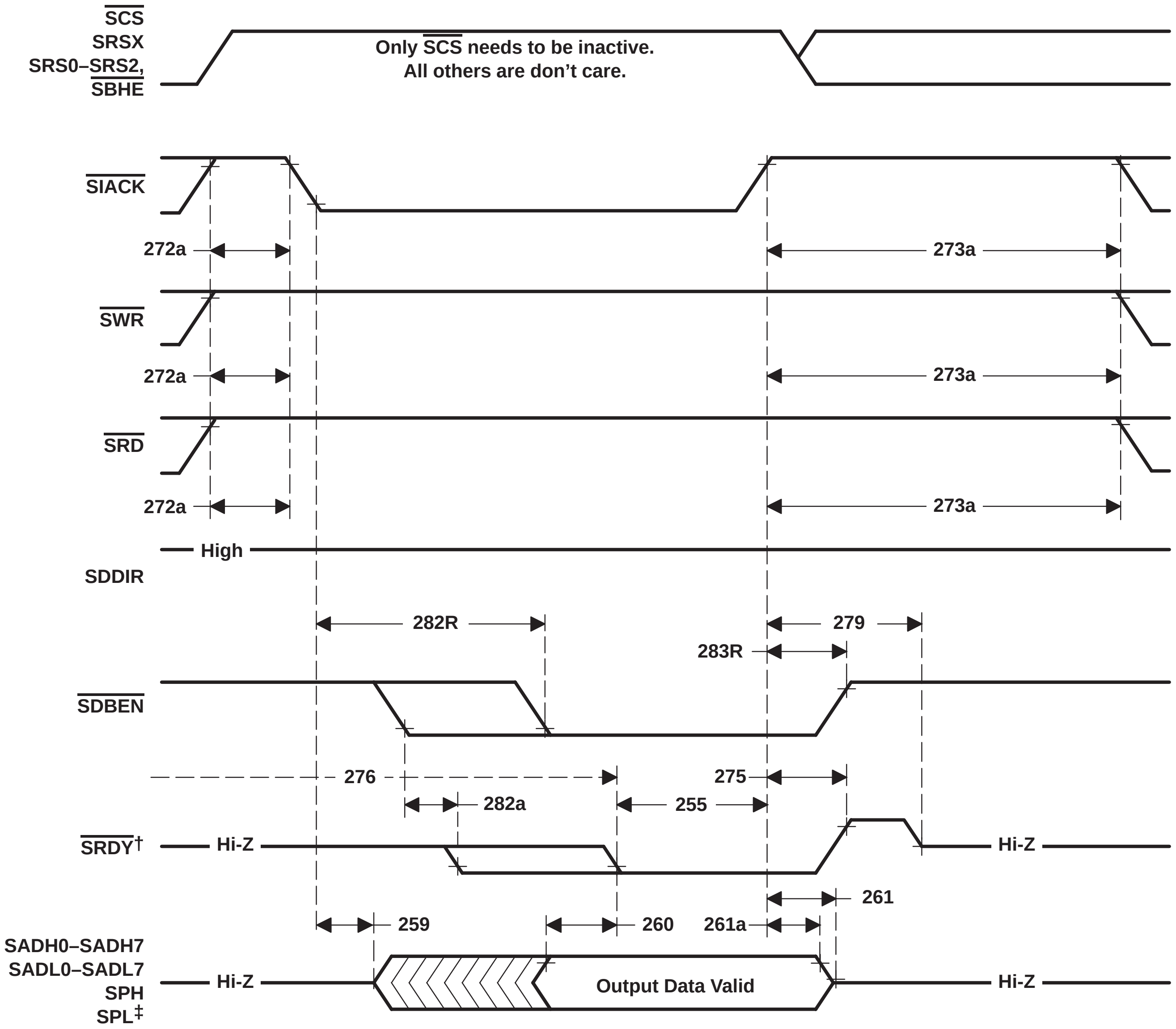
Figure 21. 80x8x Interrupt-Acknowledge Cycle – First $\overline{\text{SIACK}}$ Pulse

second $\overline{\text{SIACK}}$ pulse (see Figure 22)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to $\overline{\text{SCS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ low (see Note 25)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 25)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SIACK}}$ high (see Note 25)	0		0		ns
272a	Setup time, inactive data strobe high to $\overline{\text{SIACK}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive data strobe high after $\overline{\text{SIACK}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ high (see Note 25)	0	25	0	25	ns
276	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* literature number SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 25)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns

† This specification is provided as an aid to board design.

NOTE 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.



† $\overline{\text{SRDY}}$ is an active-low bus-ready signal. It must be asserted before data output.

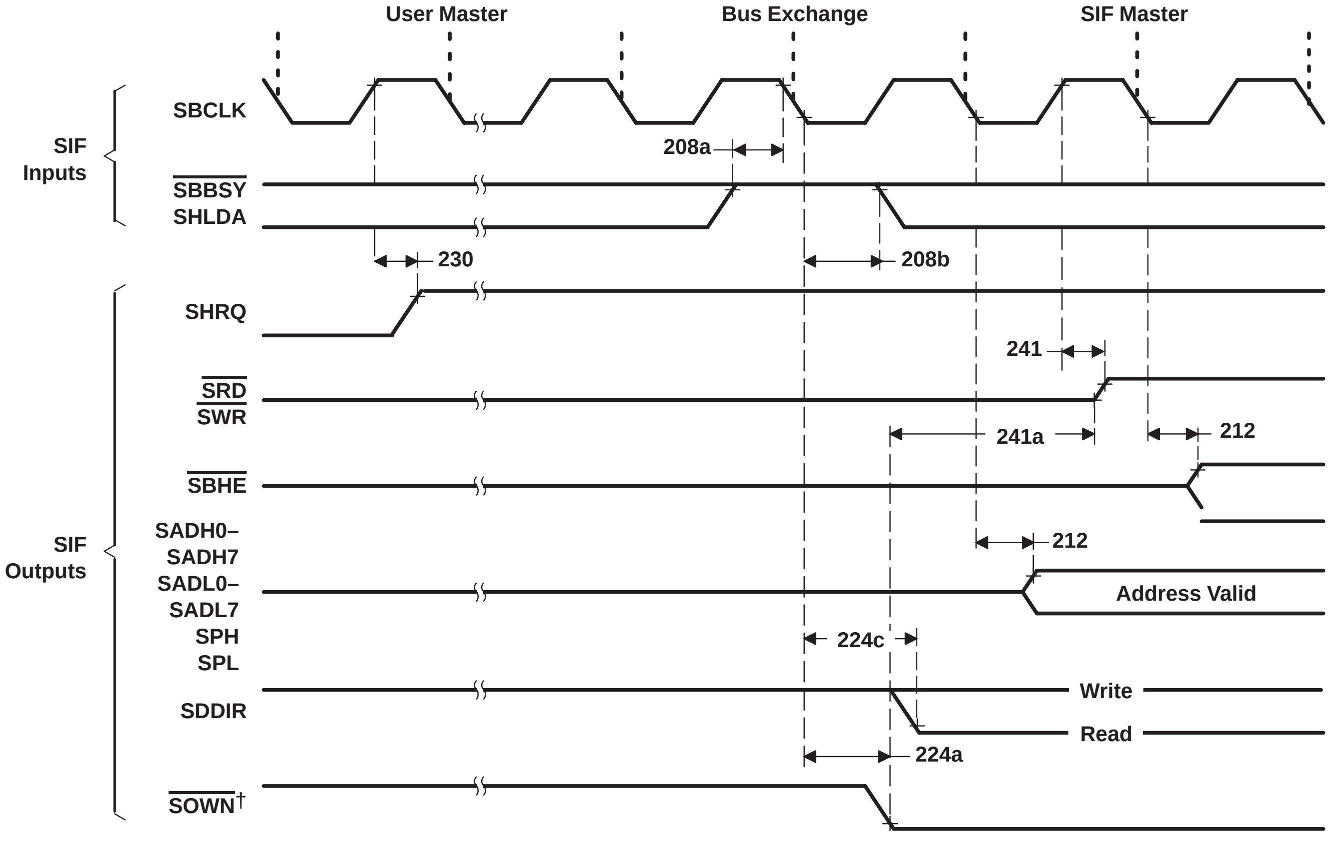
‡ In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 22. 80x8x Interrupt-Acknowledge Cycle – Second $\overline{\text{SIACK}}$ Pulse

80x8x-mode bus-arbitration timing

80x8x-mode bus arbitration – SIF takes control (see Figure 23)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to SHRQ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high, bus acquisition		25		25	ns
241a	Hold time, $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}$–15		$t_{c(SCK)}$–15		ns



† While the system interface DMA controls are active (that is, $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

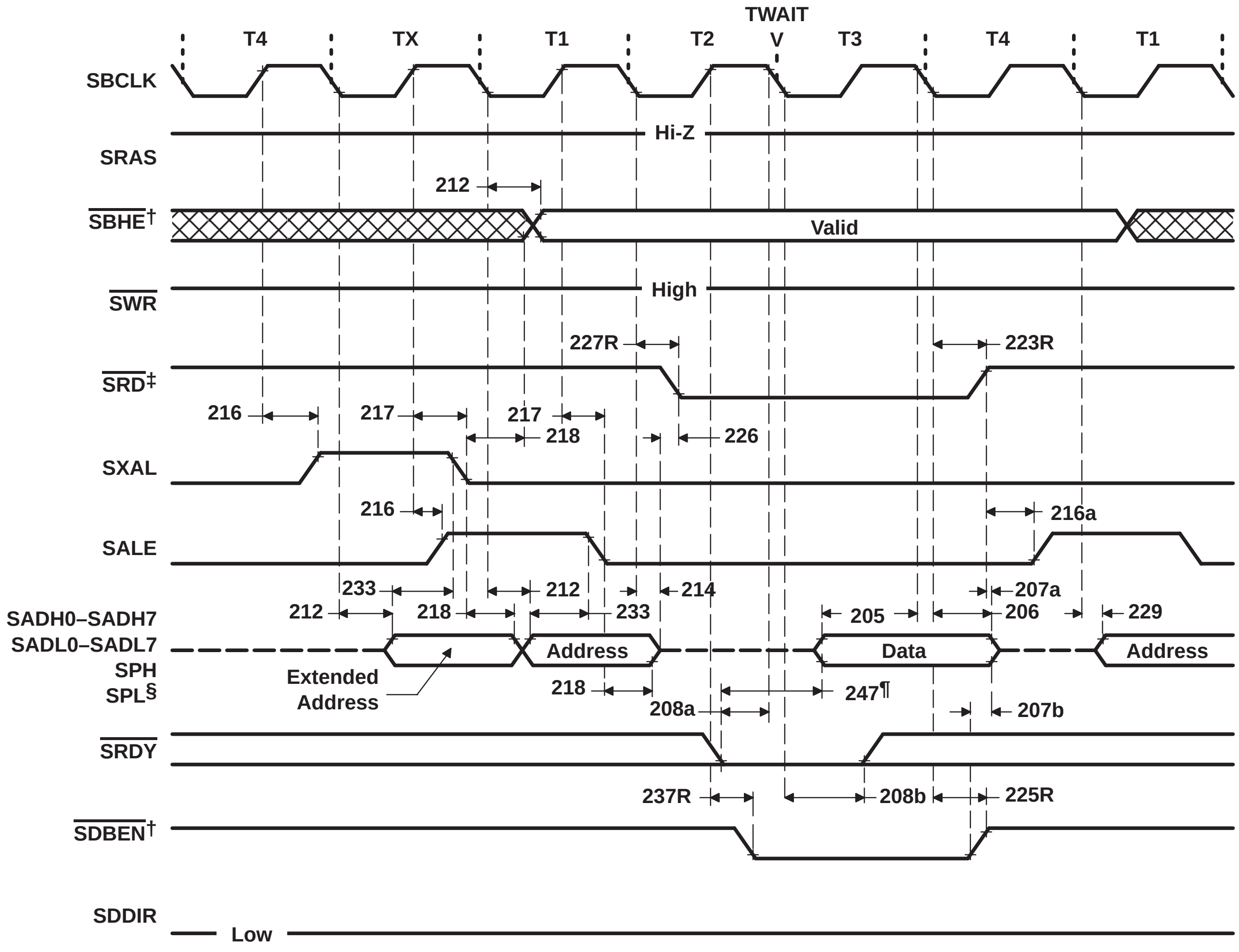
Figure 23. 80x8x-Mode Bus Arbitration – SIF Takes Control

80x8x-mode DMA timing

80x8x-mode DMA read cycle (see Figure 24)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{\text{SRD}}$ high	0		0		ns
207b	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous signal $\overline{\text{SRDY}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SRDY}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid		20		20	ns
214	Delay time, SBCLK low in T1 cycle to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SRD}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after SALE or SXAL low	5		5		ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SRD}}$ high (see Note 27)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
226	Delay time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state to $\overline{\text{SRD}}$ low	0		0		ns
227R	Delay time, SBCLK low in T2 cycle to $\overline{\text{SRD}}$ low	0	15	0	15	ns
229	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state after SBCLK low in T1 cycle	0		0		ns
231	Pulse duration, $\overline{\text{SRD}}$ low	$2t_{c(SCK)}–25$		$2t_{c(SCK)}–25$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237R	Delay time, SBCLK high in the T2 cyle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SRDY}}$ low if parameter 208a not met	0		0		ns

NOTE 27: While the system-interface DMA controls are active (that is, $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.



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† In 8-bit 80x8x mode, $\overline{\text{SBHE}}$/SRNW is a don’t care input during DIO and an inactive (high) output during DMA.

‡ Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.

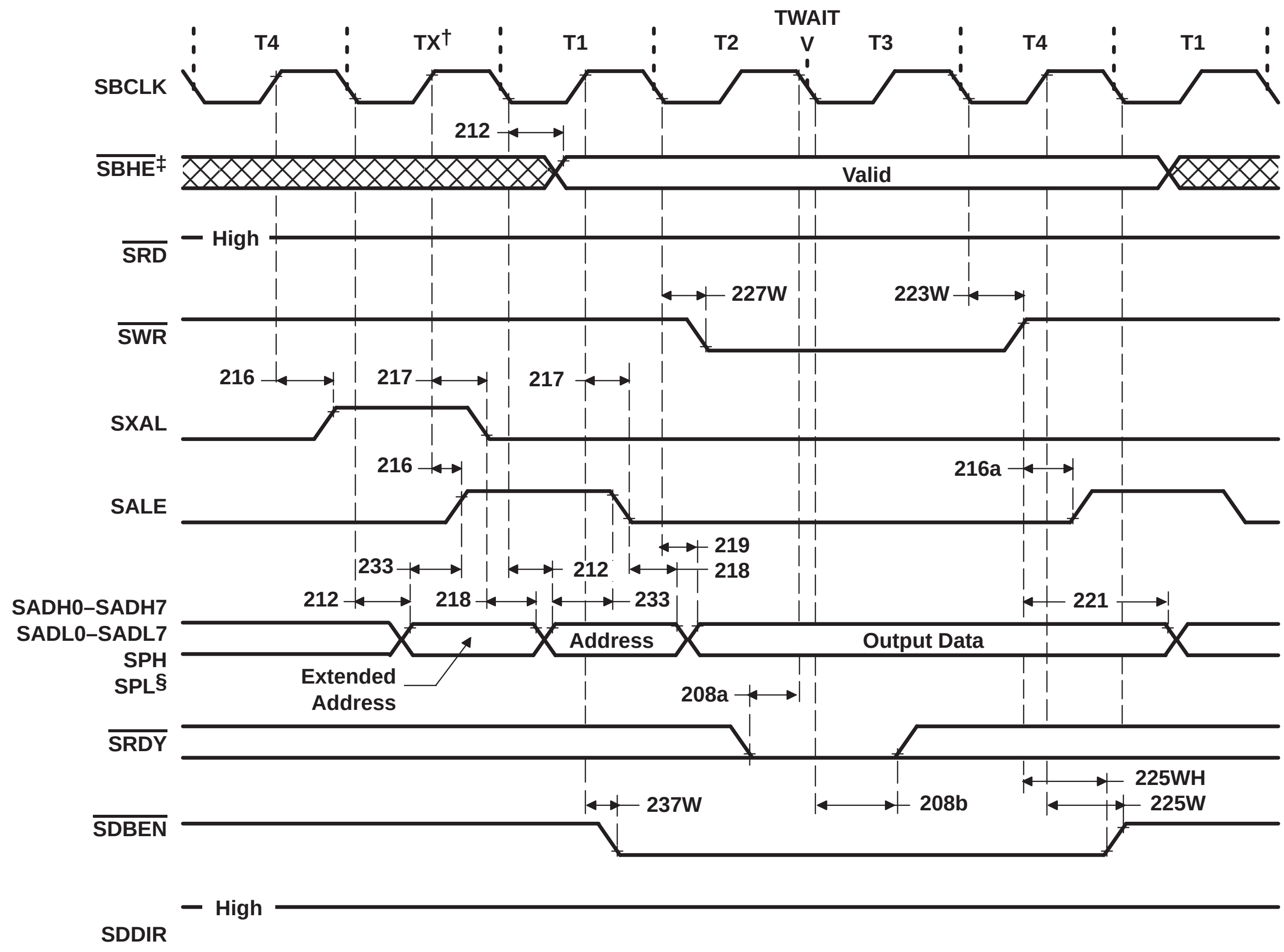
§ In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 221; that is, held after T4 high.

¶ If parameter 208A is not met, then valid data must be present before $\overline{\text{SRDY}}$ goes low.

Figure 24. 80x8x-Mode DMA Read Cycle

80x8x-mode DMA write cycle (see Figure 25)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SRDY}}$ before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SRDY}}$ after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SWR}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	5		5		ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{\text{SWR}}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
223W	Delay time, SBCLK low to $\overline{\text{SWR}}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SWR}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
227W	Delay time, SBCLK low in T2 cycle to $\overline{\text{SWR}}$ low	0	20	0	15	ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns



[†] In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

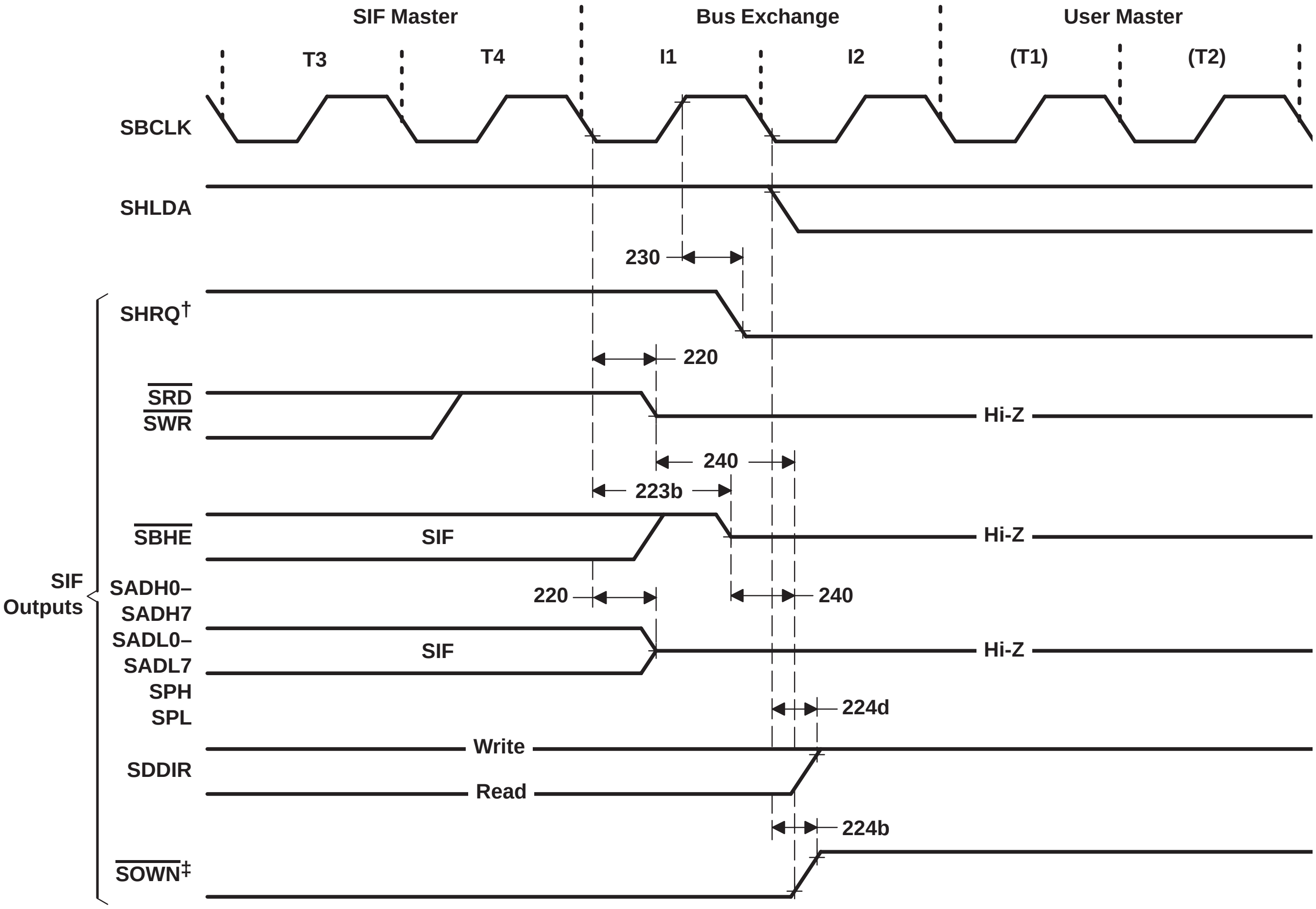
[‡] In 8-bit 80x8x mode, SBHE/SRNW is a don't care input during DIO and an inactive (high) output during DMA.

[§] In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 221; that is, held after T4 high.

Figure 25. 80x8x-Mode DMA Write Cycle

80x8x-mode bus arbitration – SIF returns control (see Figure 26)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220	Delay time, SBCLK low in I1 cycle to SADH0–SADH7, SADL0–SADL7, SPL, SPH, $\overline{\text{SRD}}$, and $\overline{\text{SWR}}$ in the high-impedance state		35		35	ns
223b	Delay time, SBCLK low in I1 cycle to $\overline{\text{SBHE}}$ in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high in cycle I1 to SHRQ low		20		15	ns
240	Setup time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SBHE}}$ in the high-impedance state before $\overline{\text{SOWN}}$ no longer low	0		0		ns

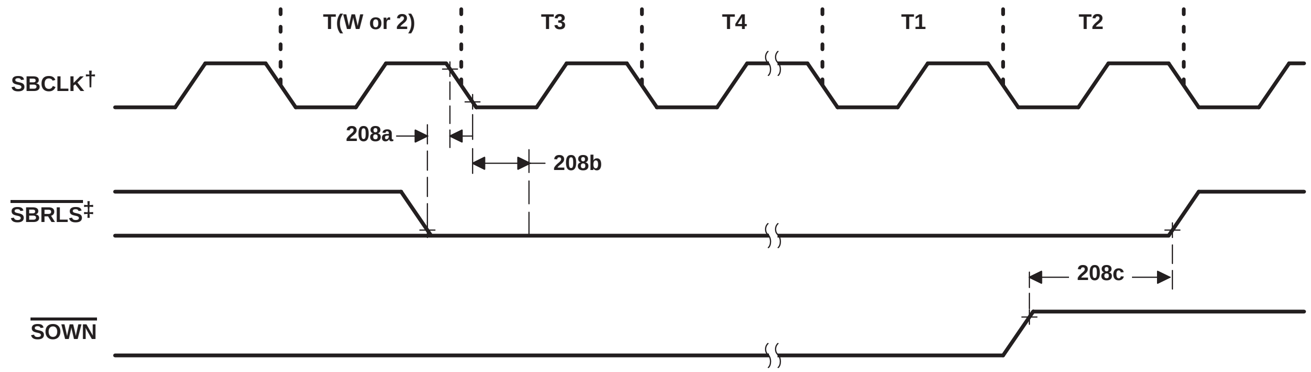


† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.
‡ While the system-interface DMA controls are active (that is, $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.

Figure 26. 80x8x-Mode Bus Arbitration – SIF Returns Control

80x8x-mode bus-release timing (see Figure 27)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBRLS}}$ low before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$ low after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns



† Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

‡ The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has started internally, the system interface releases the bus before starting another.

Figure 27. 80x8x-Mode Bus Release

68xxx DIO timing

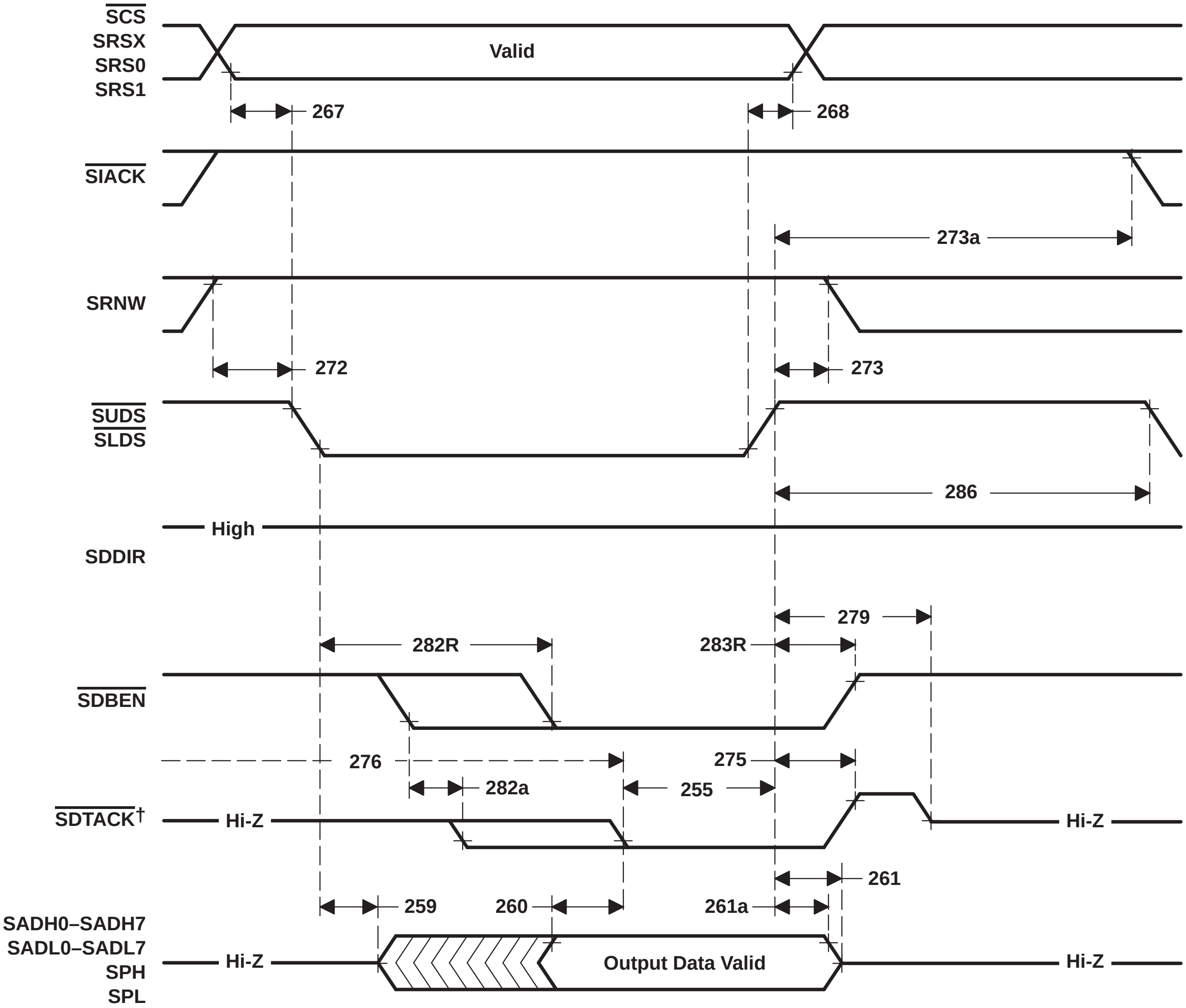
68xxx DIO read cycle (see Figure 28)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low (see Note 25)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SDTACK}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state (see Note 25)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 25)	0		0		ns
267	Setup time, register address before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 25)	15		15		ns
268	Hold time, register address valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 26)	0		0		ns
272	Setup time, SRNW before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 25)	12		12		ns
273	Hold time, SRNW after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high	0		0		ns
273a	Hold time, $\overline{\text{SIACK}}$ high after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ high (see Note 25)	0	25	0	25	ns
276	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SDTACK}}$ low	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* literature number SPWU005, subsection 3.4.1.1.1), provided the previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDBEN}}$ high (see Note 25)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high between DIO accesses (see Note 26)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design.

NOTES: 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.

26. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† $\overline{\text{SDTACK}}$ is an active-low bus-ready signal. It must be asserted before data output.

Figure 28. 68xxx DIO Read Cycle

68xxx DIO write cycle (see Figure 29)

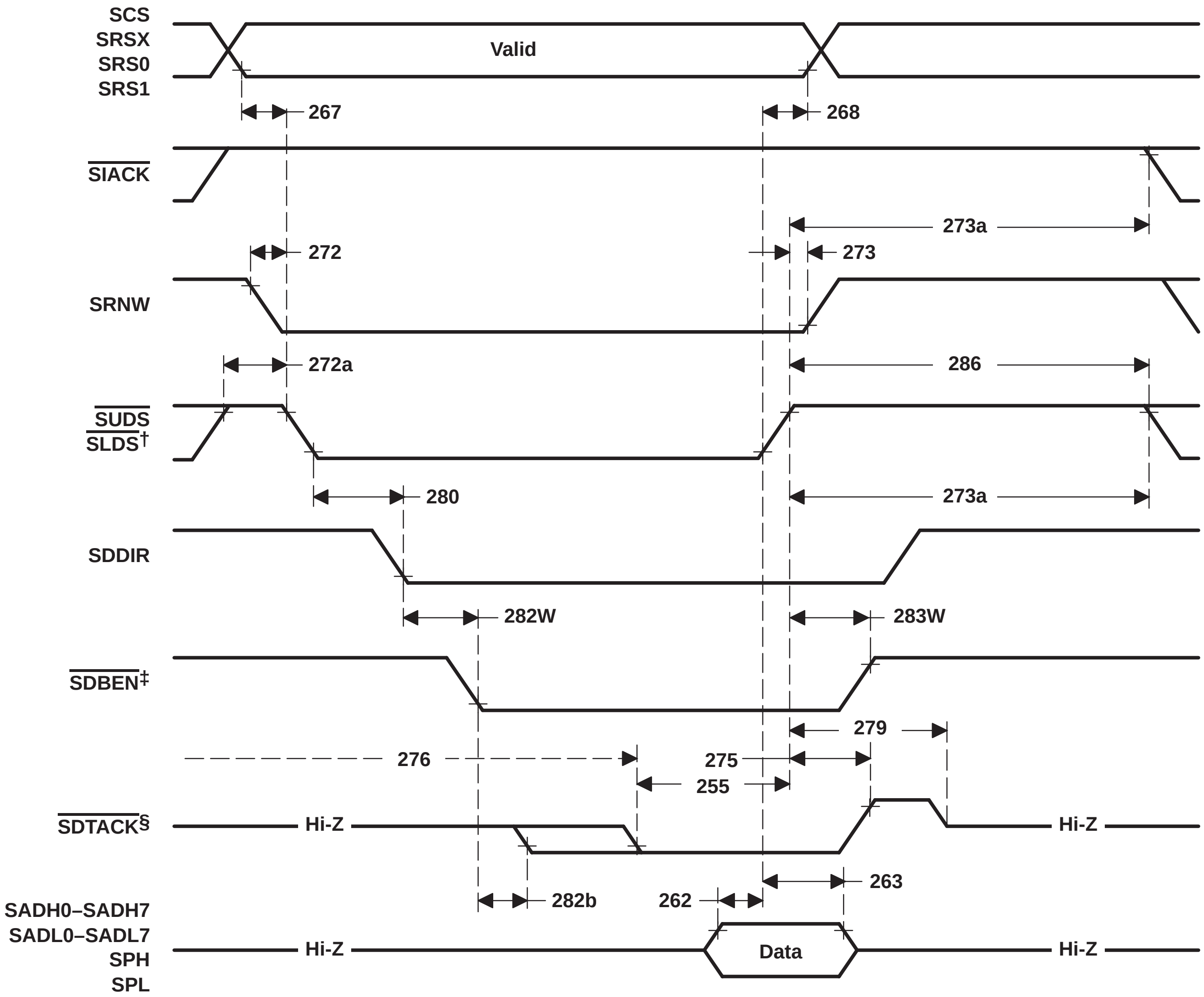
NO.			25-MHZ OPERATION		33-MHZ OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high		15		15		ns
262	Setup time, write data valid before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low		15		15		ns
263	Hold time, write data valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high		15		15		ns
267†	Setup time, register address before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 25)		15		15		ns
268	Hold time, register address valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 26)		0		0		ns
272	Setup time, SRNW before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 25)		12		12		ns
272a	Setup time, inactive $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to active data strobe no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273	Hold time, SRNW after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high		0		0		ns
273a	Hold time, inactive $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high after active data strobe high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ high (see Note 25)		0	25	0	25	ns
276	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF			4000		4000	ns
279‡	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low to SDDIR low (see Note 25)		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282b	Delay time, SDBEN low to SDTACK low (see *TMS380 Second Generation Token-Ring User's Guide,* literaure number SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{\text{SDBEN}}$ low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
283W	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDBEN}}$ no longer low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high between DIO accesses (see Note 25)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

‡ This specification is provided as an aid to board design.

NOTES: 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.

26. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† For 68xxx mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Provided this limitation is observed, all events referenced to a data strobe edge use the later occurring edge. Events defined by two data strobes, edges, such as parameter 286, are measured between latest and earlier edges.

‡ When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

§ $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

Figure 29. 68xxx DIO Write Cycle

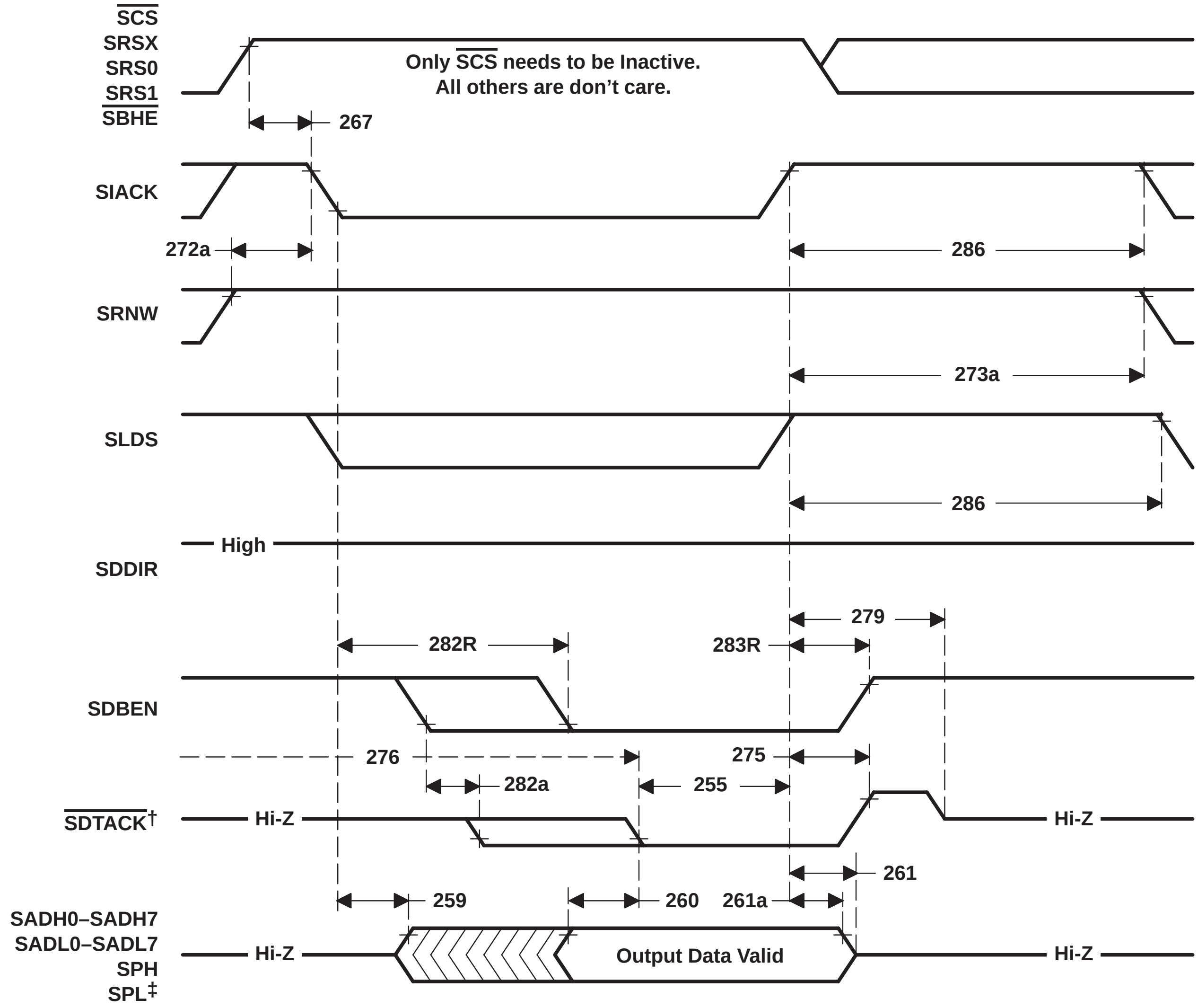
68xxx interrupt-acknowledge-cycle timing (see Figure 30)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SUDS}}$, or $\overline{\text{SIACK}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ no longer high (see Note 25)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SDTACK}}$ no longer high	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 25)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SCS}}$ or $\overline{\text{SIACK}}$ no longer low (see Note 25)	0		0		ns
267‡	Setup time, register address before $\overline{\text{SIACK}}$ no longer high (see Note 25)	15		15		ns
272a	Setup time, inactive high $\overline{\text{SIACK}}$ to active data strobe no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive SRNW high after active data strobe high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$ or SRNW high to $\overline{\text{SDTACK}}$ high (see Note 25)	0	25	0	25	ns
276	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF	0	4000	0	4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SDTACK}}$ low in a read cycle	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* literature number SPWU005, subsection 3.4.1.1.1), provided the previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 25)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 25)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design.

‡ It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

NOTE 25. The inactive chip-select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip-select in interrupt-acknowledge cycles.



† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

‡ Internal logic drives $\overline{\text{SDTACK}}$ high and verifies that it has reached a valid-high level before making it a 3-state signal.

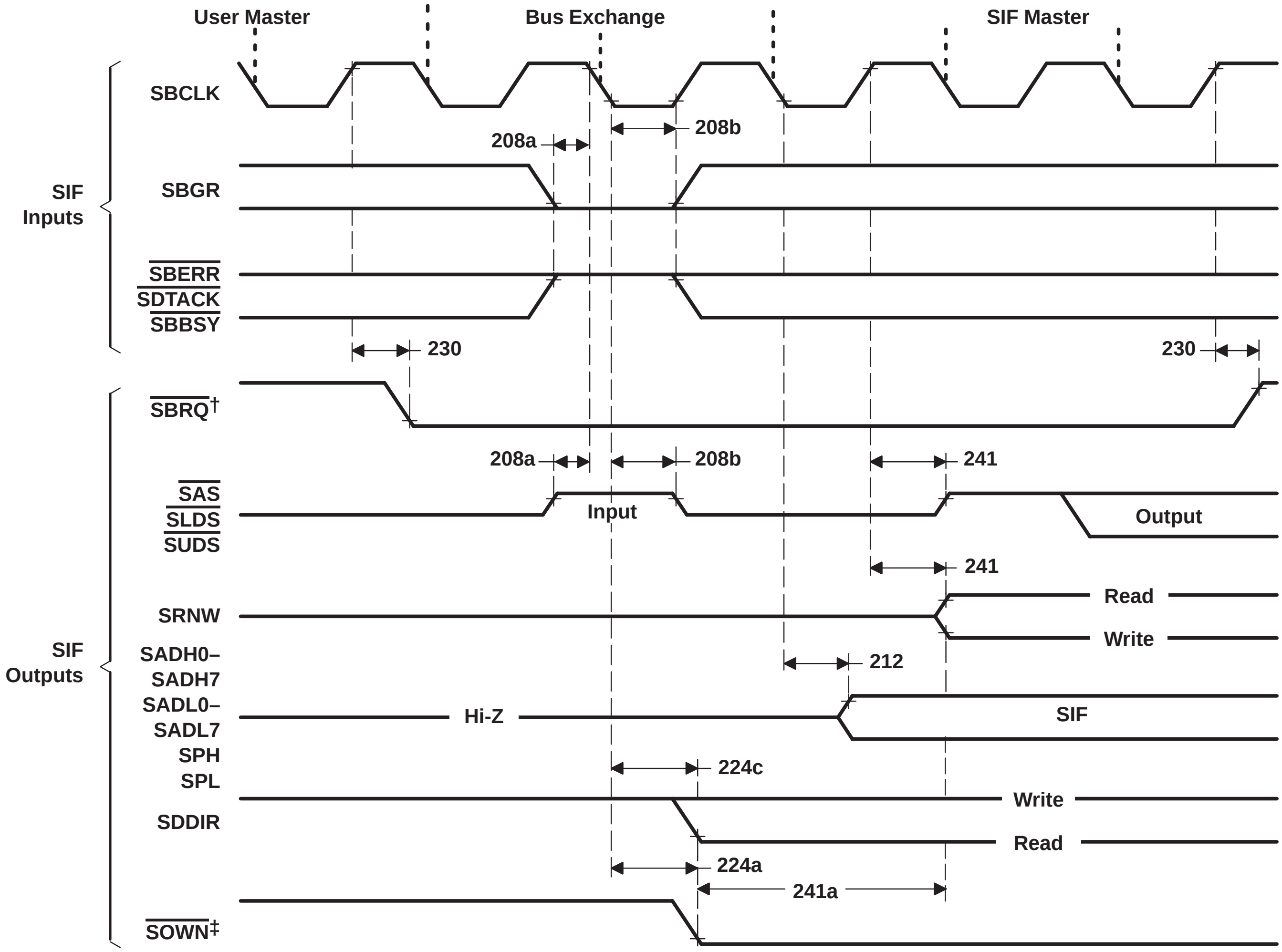
Figure 30. 68xxx Interrupt-Acknowledge Cycle

68xxx-mode bus-arbitration timing

68xxx-mode bus arbitration – SIF takes control (see Figure 31)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBGR}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBGR}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid	0	20	0	20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low (see Note 28)	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high		25		25	ns
241a	Hold time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus aquisition	t_c(SCK–15)		t_c(SCK–15)		ns

NOTE 28. Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.



[†] In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system-bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{\text{SBRQ}}$ on the rising edge of SBCLK in state T2 of the first system-bus transfer it controls.

[‡] While the system-interface DMA controls are active (that is, $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

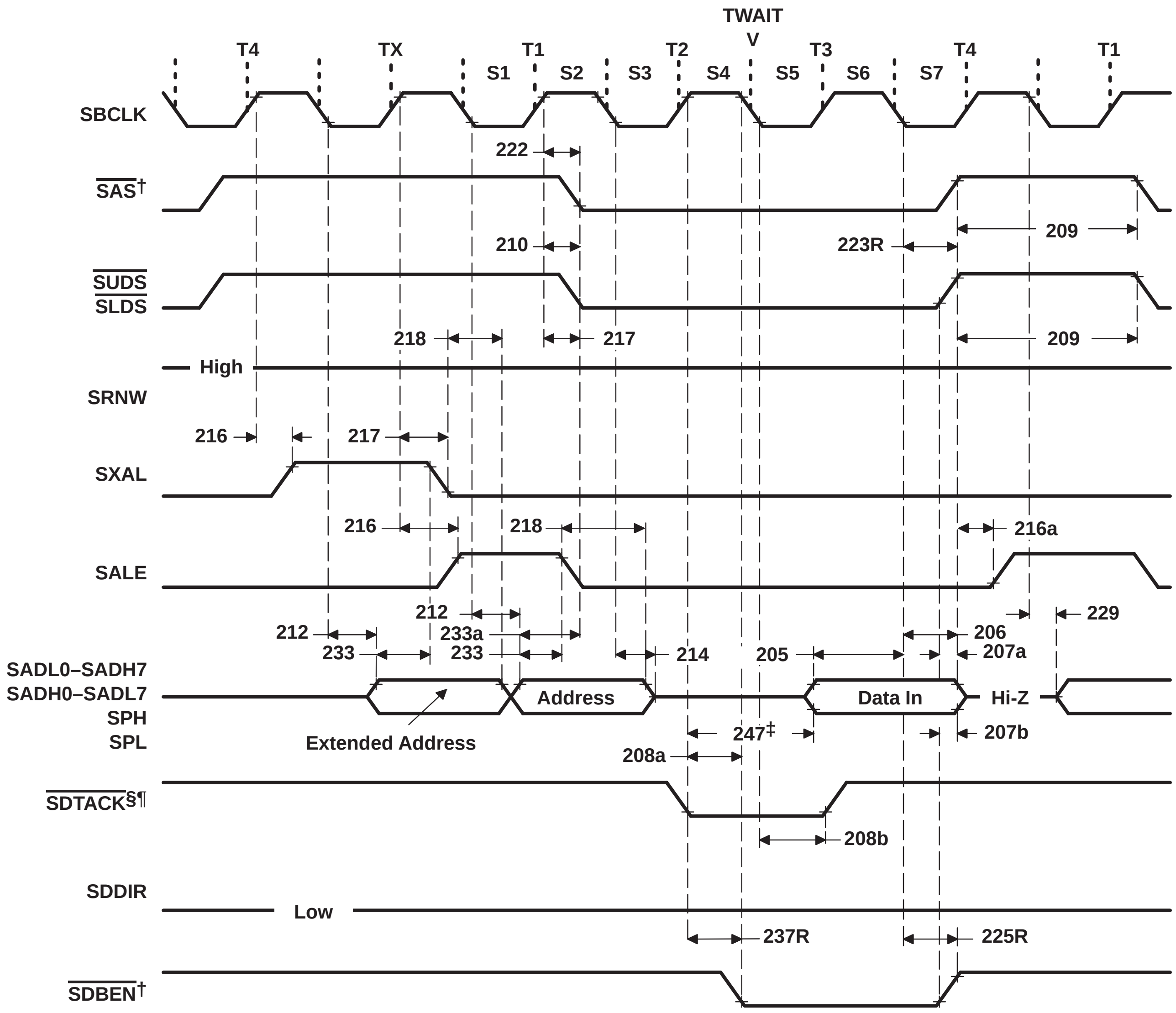
Figure 31. 68xxx-Mode Bus Arbitration – SIF Takes Control

68xxx-mode DMA timing

68xxx-mode DMA read cycle (see Figure 32)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, input data valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, input data valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, input data valid after data strobe no longer low	0		0		ns
207b	Hold time, input data valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
210	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		16		11	ns
212	Delay time, SBCLK low to address valid		20		20	ns
214	Delay time, SBCLK low in T2 cycle to SAD high impedance		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	5		5		ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high (see Note 27)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
229	Hold time, SAD in the high-impedance state after SBCLK low in T4 cycle	0		0		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SDTACK}}$ low if parameter 208a not met	0		0		ns

NOTE 27: While the system-interface DMA controls are active (that is, $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.



† On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data may be removed when either the read strobe or $\overline{\text{SDBEN}}$ becomes inactive.

‡ If parameter 208a is not met, then valid data must be present before $\overline{\text{SDTACK}}$ goes low.

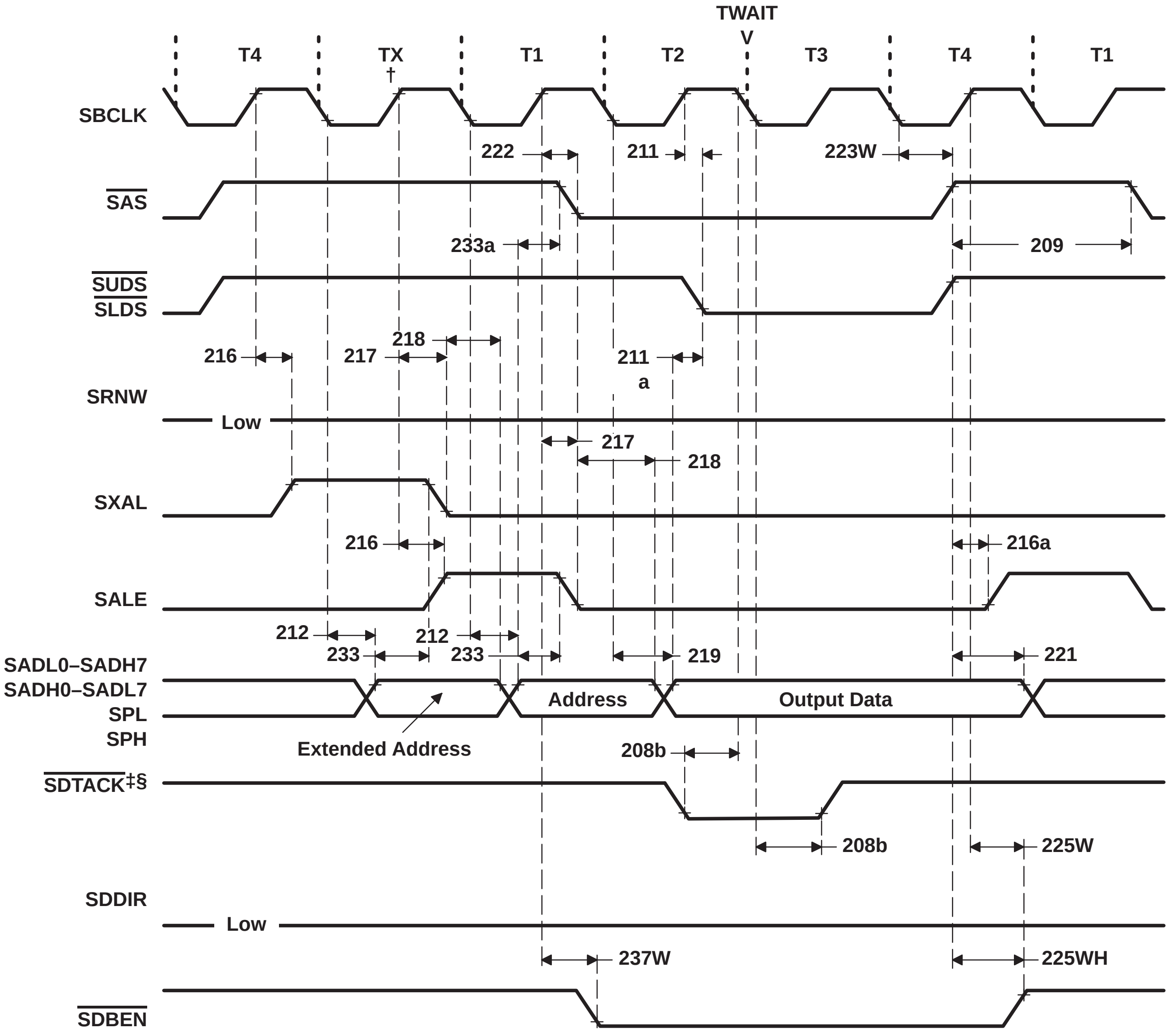
§ Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.

¶ All V_{SS} pins should be routed to minimize inductance to system ground.

Figure 32. 68xxx-Mode DMA Read Cycle

68xxx-mode DMA write cycle (see Figure 33)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+$ $t_{w(SCKL)}-18$		$t_{c(SCK)}+$ $t_{w(SCKL)}-18$		ns
211	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		25		25	ns
211a	Delay time, output data valid to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
212	Delay time, SBCLK low to address valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	5		5		ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, output data, parity valid after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223W	Delay time, SBCLK low to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns



† In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

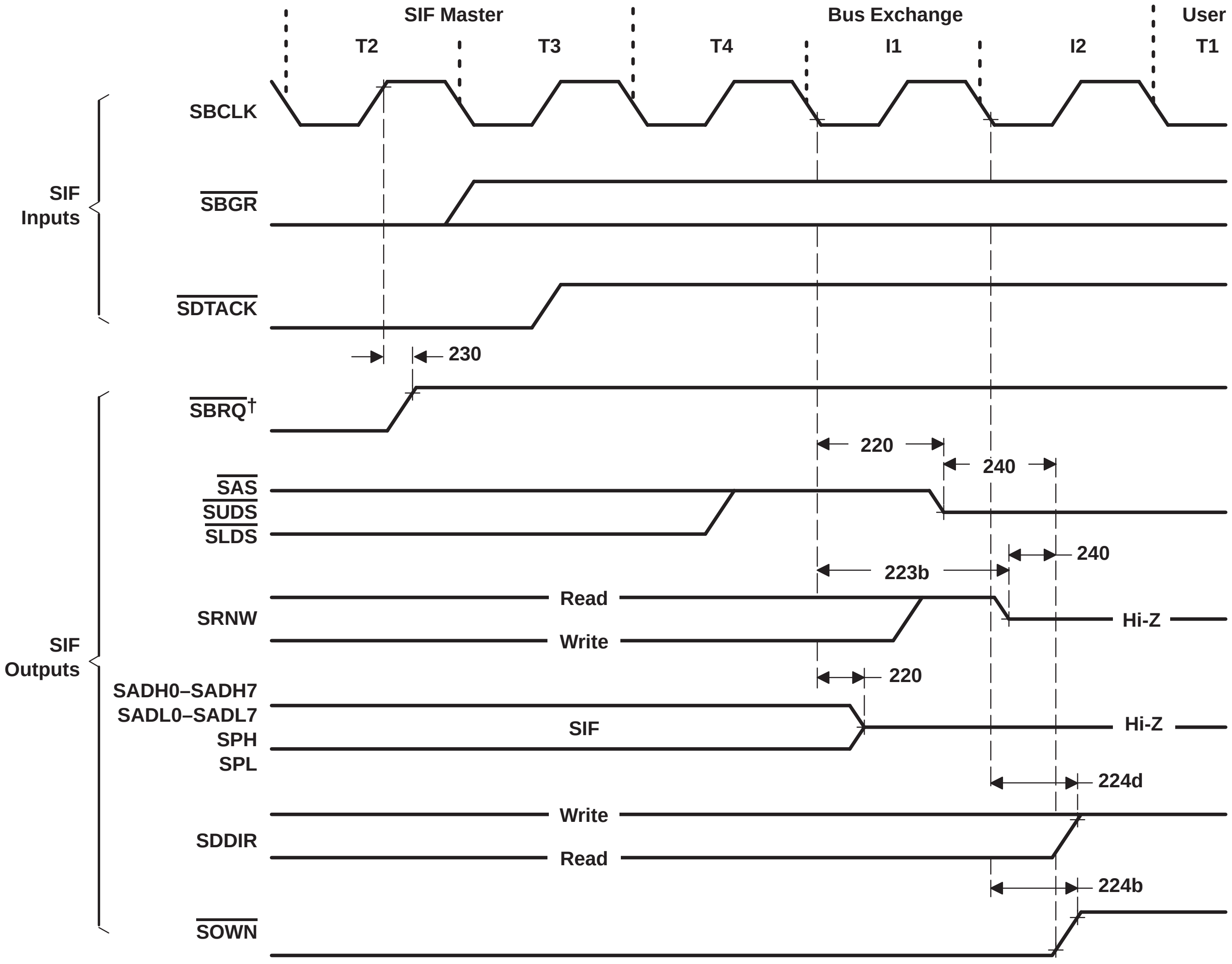
‡ On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or SDBEN becomes inactive.

§ All V_{SS} terminals should be routed to minimize inductance to system ground.

Figure 33. 68xxx-Mode DMA Write Cycle

68xxx-mode bus arbitration – SIF returns control (see Figure 34)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220	Delay time, SBCLK low in I1 cycle to SAD, SPL, SPH, SUDS, and SLDS in the high-impedance state, bus release		35		35	ns
223b	Delay time, SBCLK low in I1 cycle to SBHE/SRNW in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to SOWN high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high to either SHRQ low or SBRQ high		20		15	ns
240	Setup from, SUDS, SLDS, SRNW, and SAS control signals in the high-impedance state before SOWN no longer low	0		0		ns

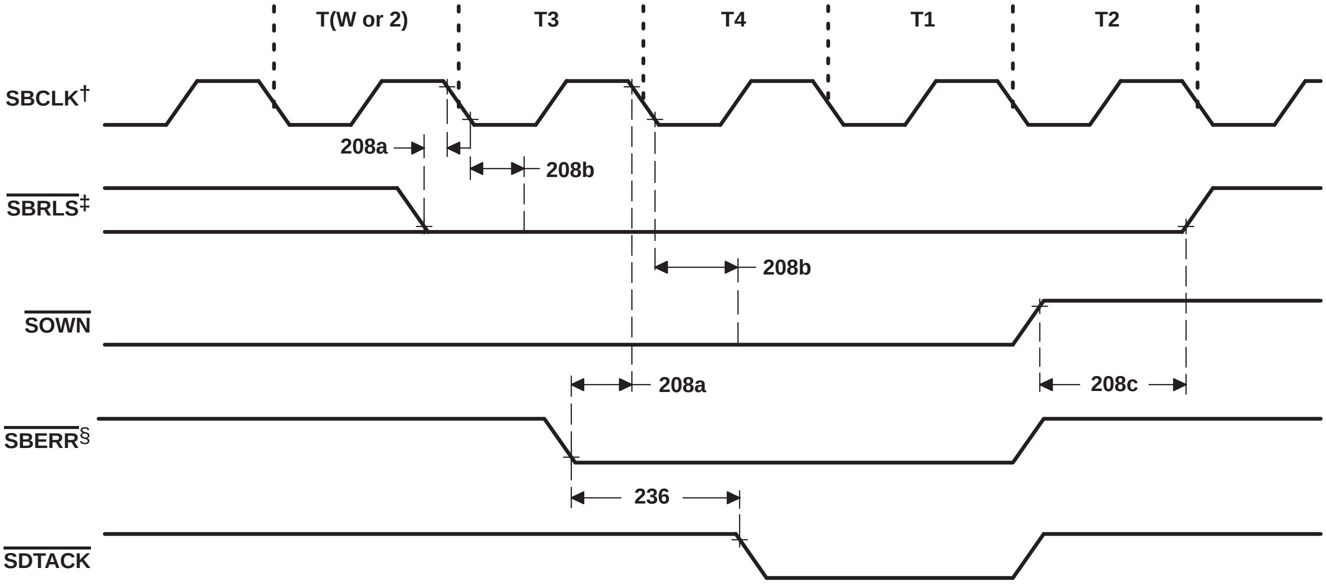


† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system-bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system-bus transfer it controls.

Figure 34. 68xxx-Mode Bus Arbitration – SIF Returns Control

68xxx-mode bus-release and error timing (see Figures 35, 36, and 37)

NO.		25-MHZ OPERATION		33-MHZ OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\mathrm{SBRLS}}$, $\overline{\mathrm{SOWN}}$, or $\overline{\mathrm{SBERR}}$ after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\mathrm{SBRLS}}$ low after $\overline{\mathrm{SOWN}}$ high	0		0		ns
236	Setup time, $\overline{\mathrm{SBERR}}$ low before $\overline{\mathrm{SDTACK}}$ no longer high if parameter 208a not met	30		30		ns



† Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

‡ The system interface ignores the assertion of $\overline{\mathrm{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\mathrm{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has started internally, the system interface releases the bus before starting another.

§ If $\overline{\mathrm{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed, regardless of the value of SDTACK. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface then releases control of the system bus. The system interface ignores the assertion of $\overline{\mathrm{SBERR}}$ if it is not performing a DMA-bus cycle on the system bus. When SBERR is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

Figure 35. 68xxx-Mode Bus Release and Error

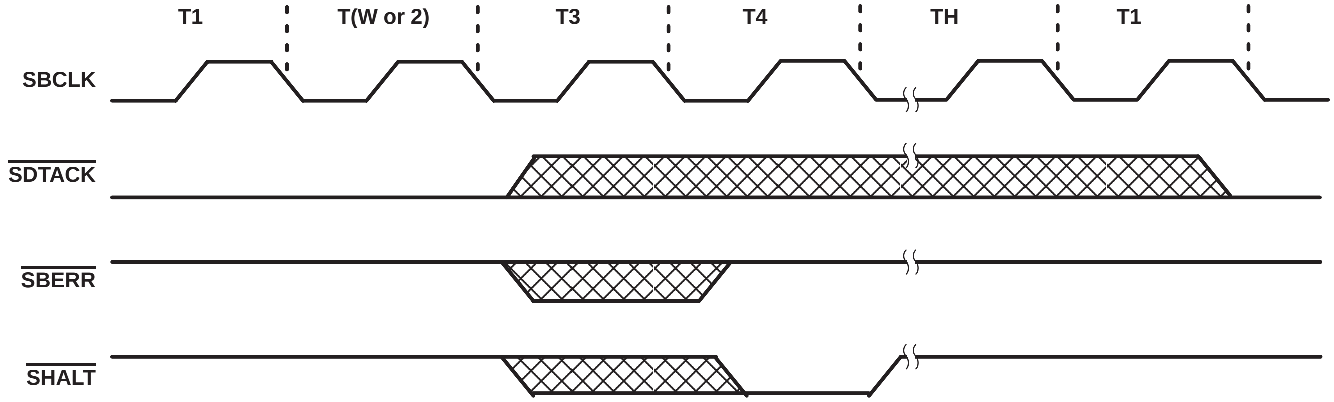


Figure 36. 68xxx-Mode Bus Halt and Retry, Normal Completion With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

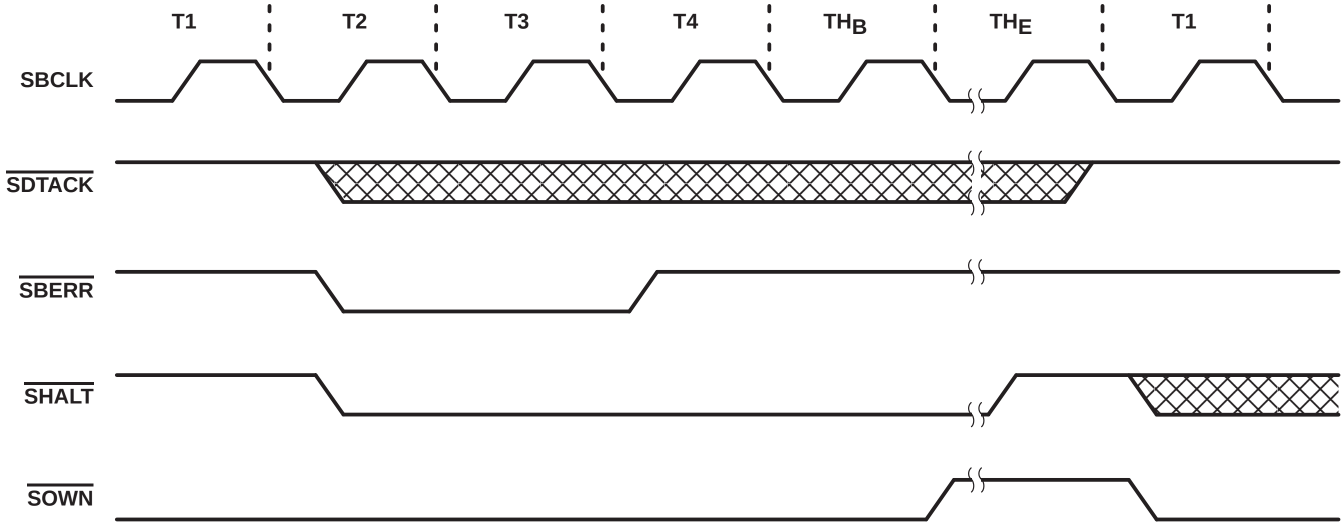
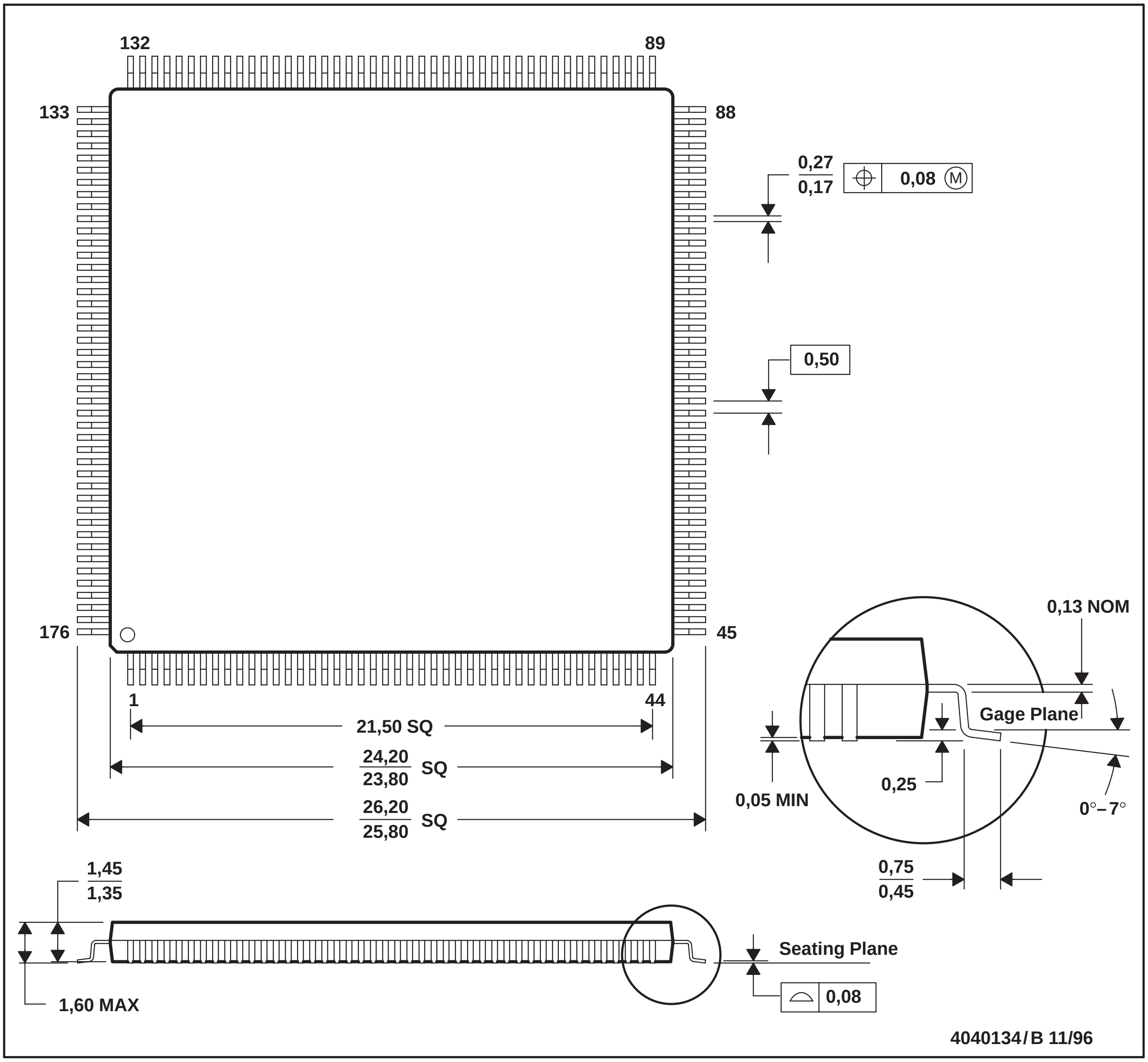


Figure 37. 68xxx-Mode Bus Halt and Retry, Rerun Cycle With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

MECHANICAL DATA

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TI380C30APGF	OBSOLETE	LQFP	PGF	176		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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