

M471B5674EB0
M471B5173EB0
M474B5173EB0
M471B1G73EB0
M474B1G73EB0

204pin Unbuffered SODIMM based on 4Gb E-die

1.35V

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Editor</u>
1.0	- First SPEC Release	Jul. 2014	-	S.H.Kim
1.1	- Addition of 1866(13-13-13) speed from Product line-up	Apr. 2015	-	J.Y.Lee
1.2	- Addition of Module line up (ECC SODMM)	Aug. 2015	-	J.Y.Lee
1.3	- IDD current table typo modification	11th Aug. 2015	-	J.Y.Lee
1.4	- Addition of Module line up (2GB Non-ECC SODIMM)	20th Aug. 2015	-	J.Y.Lee

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1. DDR3L Unbuffered SODIMM Ordering Information

Part Number	Density	Organization	Component Composition ¹	Number of Rank	Height
M471B5674EB0-YK0/MA	2GB	256Mx64	256Mx16(K4B4G1646E-BY##)*4	1	30mm
M471B5173EB0-YK0/MA	4GB	512Mx64	512Mx8(K4B4G0846E-BY##)*8	1	30mm
M474B5173EB0-YK0	4GB	512Mx72	512Mx8(K4B4G0846E-BY##)*9	1	30mm
M471B1G73EB0-YK0/MA	8GB	1Gx64	512Mx8(K4B4G0846E-BY##)*16	2	30mm
M474B1G73EB0-YK0	8GB	1Gx72	512Mx8(K4B4G0846E-BY##)*18	2	30mm

NOTE :

1. "##" - K0/MA

2. K0(1600Mbps 11-11-11) / MA(1866Mbps 13-13-13)

- DDR3-1866(13-13-13) is backward compatible to DDR3-1600(11-11-11)

2. Key Features

Speed	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
	6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	
tCK(min)	2.5	1.875	1.5	1.25	1.071	ns
CAS Latency	6	7	9	11	13	nCK
tRCD(min)	15	13.125	13.5	13.75	13.91	ns
tRP(min)	15	13.125	13.5	13.75	13.91	ns
tRAS(min)	37.5	37.5	36	35	34	ns
tRC(min)	52.5	50.625	49.5	48.75	47.91	ns

- JEDEC standard 1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V) Power Supply
- V_{DDQ} = 1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin, 933MHz f_{CK} for 1866Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 5,6,7,8,9,10,11,13
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600) and 9(DDR3-1866)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm $\pm$ 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq 95^\circ\text{C}$
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
256Mx16(4Gb) based Module	A0-A14	A0-A9	BA0-BA2	A10/AP
512Mx8(4Gb) based Module	A0-A15	A0-A9	BA0-BA2	A10/AP

4. x64 DIMM Pin Configurations (Front side/Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REFDQ}	2	V _{SS}	71	V _{SS}	72	V _{SS}	139	V _{SS}	140	DQ38
3	V _{SS}	4	DQ4	KEY				141	DQ34	142	DQ39
5	DQ0	6	DQ5	73	CKE0	74	CKE1	143	DQ35	144	V _{SS}
7	DQ1	8	V _{SS}	75	V _{DD}	76	V _{DD}	145	V _{SS}	146	DQ44
9	V _{SS}	10	DQS0	77	NC	78	A15 ³	147	DQ40	148	DQ45
11	DM0	12	DQS0	79	BA2	80	A14 ³	149	DQ41	150	V _{SS}
13	V _{SS}	14	V _{SS}	81	V _{DD}	82	V _{DD}	151	V _{SS}	152	DQS5
15	DQ2	16	DQ6	83	A12/B _C	84	A11	153	DM5	154	DQS5
17	DQ3	18	DQ7	85	A9	86	A7	155	V _{SS}	156	V _{SS}
19	V _{SS}	20	V _{SS}	87	V _{DD}	88	V _{DD}	157	DQ42	158	DQ46
21	DQ8	22	DQ12	89	A8	90	A6	159	DQ43	160	DQ47
23	DQ9	24	DQ13	91	A5	92	A4	161	V _{SS}	162	V _{SS}
25	V _{SS}	26	V _{SS}	93	V _{DD}	94	V _{DD}	163	DQ48	164	DQ52
27	DQS1	28	DM1	95	A3	96	A2	165	DQ49	166	DQ53
29	DQS1	30	RESET	97	A1	98	A0	167	V _{SS}	168	V _{SS}
31	V _{SS}	32	V _{SS}	99	V _{DD}	100	V _{DD}	169	DQS6	170	DM6
33	DQ10	34	DQ14	101	CK0	102	CK1	171	DQS6	172	V _{SS}
35	DQ11	36	DQ15	103	CK0	104	CK1	173	V _{SS}	174	DQ54
37	V _{SS}	38	V _{SS}	105	V _{DD}	106	V _{DD}	175	DQ50	176	DQ55
39	DQ16	40	DQ20	107	A10/AP	108	BA1	177	DQ51	178	V _{SS}
41	DQ17	42	DQ21	109	BA0	110	RAS	179	V _{SS}	180	DQ60
43	V _{SS}	44	V _{SS}	111	V _{DD}	112	V _{DD}	181	DQ56	182	DQ61
45	DQS2	46	DM2	113	WE	114	S0	183	DQ57	184	V _{SS}
47	DQS2	48	V _{SS}	115	CAS	116	ODT0	185	V _{SS}	186	DQS7
49	V _{SS}	50	DQ22	117	V _{DD}	118	V _{DD}	187	DM7	188	DQS7
51	DQ18	52	DQ23	119	A13 ³	120	ODT1	189	V _{SS}	190	V _{SS}
53	DQ19	54	V _{SS}	121	S1	122	NC	191	DQ58	192	DQ62
55	V _{SS}	56	DQ28	123	V _{DD}	124	V _{DD}	193	DQ59	194	DQ63
57	DQ24	58	DQ29	125	TEST	126	V _{REFCA}	195	V _{SS}	196	V _{SS}
59	DQ25	60	V _{SS}	127	V _{SS}	128	V _{SS}	197	SA0	198	NC
61	V _{SS}	62	DQS3	129	DQ32	130	DQ36	199	V _{DDSPD}	200	SDA
63	DM3	64	DQS3	131	DQ33	132	DQ37	201	SA1	202	SCL
65	V _{SS}	66	V _{SS}	133	V _{SS}	134	V _{SS}	203	V _{TT}	204	V _{TT}
67	DQ26	68	DQ30	135	DQS4	136	DM4				
69	DQ27	70	DQ31	137	DQS4	138	V _{SS}				

NOTE :

1. NC = No Connect, NU = Not Used, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

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5. x72 DIMM Pin Configurations (Front side/Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REFDQ}	2	V _{SS}	71	CB1	72	CB4	139	$\overline{\text{DQS}}_4$	140	DM4
3	V _{SS}	4	DQ4	KEY				141	DQS4	142	DQ38
5	DQ0	6	DQ5	73	V _{SS}	74	CB5	143	V _{SS}	144	DQ39
7	DQ1	8	V _{SS}	75	$\overline{\text{DQS}}_8$	76	DM8	145	DQ34	146	V _{SS}
9	V _{SS}	10	$\overline{\text{DQS}}_0$	77	DQS8	78	V _{SS}	147	DQ35	148	DQ44
11	DM0	12	DQS0	79	V _{SS}	80	CB6	149	V _{SS}	150	DQ45
13	DQ2	14	V _{SS}	81	CB2	82	CB7	151	DQ40	152	V _{SS}
15	DQ3	16	DQ6	83	CB3	84	V _{REFCA}	153	DQ41	154	$\overline{\text{DQS}}_5$
17	V _{SS}	18	DQ7	85	V _{DD}	86	V _{DD}	155	V _{SS}	156	DQS5
19	DQ8	20	V _{SS}	87	CKE0	88	A15	157	DM5	158	V _{SS}
21	DQ9	22	DQ12	89	CKE1	90	A14	159	DQ42	160	DQ46
23	V _{SS}	24	DQ13	91	BA2	92	A9	161	DQ43	162	DQ47
25	$\overline{\text{DQS}}_1$	26	V _{SS}	93	V _{DD}	94	V _{DD}	163	V _{SS}	164	V _{SS}
27	DQS1	28	DM1	95	A12/ $\overline{\text{BC}}$	96	A11	165	DQ48	166	DQ52
29	V _{SS}	30	$\overline{\text{RESET}}$	97	A8	98	A7	167	DQ49	168	DQ53
31	DQ10	32	V _{SS}	99	A5	100	A6	169	V _{SS}	170	V _{SS}
33	DQ11	34	DQ14	101	V _{DD}	102	V _{DD}	171	$\overline{\text{DQS}}_6$	172	DM6
35	V _{SS}	36	DQ15	103	A3	104	A4	173	DQS6	174	DQ54
37	DQ16	38	V _{SS}	105	A1	106	A2	175	V _{SS}	176	DQ55
39	DQ17	40	DQ20	107	A0	108	BA1	177	DQ50	178	V _{SS}
41	V _{SS}	42	DQ21	109	V _{DD}	110	V _{DD}	179	DQ51	180	DQ60
43	$\overline{\text{DQS}}_2$	44	DM2	111	CK0	112	Par_in, NC, CK1	181	V _{SS}	182	DQ61
45	DQS2	46	V _{SS}	113	$\overline{\text{CK}}_0$	114	Err_out, NC, $\overline{\text{CK}}_1$	183	DQ56	184	V _{SS}
47	V _{SS}	48	DQ22	115	V _{DD}	116	V _{DD}	185	DQ57	186	$\overline{\text{DQS}}_7$
49	DQ18	50	DQ23	117	A10/AP	118	$\overline{\text{S}}_3$	187	V _{SS}	188	DQS7
50	DQ19	52	V _{SS}	119	BA0	120	$\overline{\text{S}}_2$	189	DM7	190	V _{SS}
53	V _{SS}	54	DQ28	121	$\overline{\text{WE}}$	122	$\overline{\text{RAS}}$	191	DQ58	192	DQ62
55	DQ24	56	DQ29	123	V _{DD}	124	V _{DD}	193	DQ59	194	DQ63
57	DQ25	58	V _{SS}	125	$\overline{\text{CAS}}$	126	ODT0	195	V _{SS}	196	V _{SS}
59	DM3	60	$\overline{\text{DQS}}_3$	127	$\overline{\text{S}}_0$	128	ODT1	197	SA0	198	$\overline{\text{EVENT}}$
61	V _{SS}	62	DQS3	129	$\overline{\text{S}}_1$	130	A13	199	V _{DDSPD}	200	SDA
63	DQ26	64	V _{SS}	131	V _{DD}	132	V _{DD}	201	SA1	202	SCL
65	DQ27	66	DQ30	133	DQ32	134	DQ36	203	V _{TT}	204	V _{TT}
67	V _{SS}	68	DQ31	135	DQ33	136	DQ37				
69	CB0	70	V _{SS}	137	V _{SS}	138	V _{SS}				

NOTE :

1. NC = No Connect, NU = Not Usable, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

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6. Pin Description

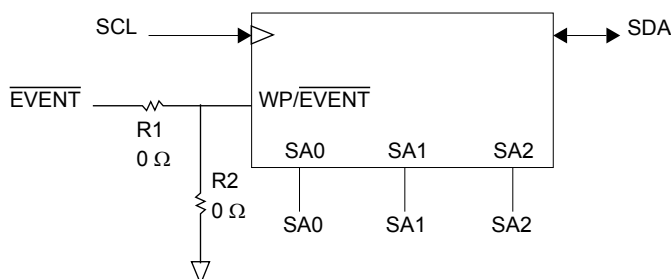
Pin Name	Description	Number	Pin Name	Description	Number
CK0, CK1	Clock Inputs, positive line	2	DQ0-DQ63	Data Input/Output	64
$\overline{\text{CK}}0, \overline{\text{CK}}1$	Clock Inputs, negative line	2	DM0-DM7	Data Masks/ Data strobes, Termination data strobes	8
CKE0, CKE1	Clock Enables	2	DQS0-DQS7	Data strobes	8
$\overline{\text{RAS}}$	Row Address Strobe	1	$\overline{\text{DQS}}0\text{-}\overline{\text{DQS}}7$	Data strobes complement	8
$\overline{\text{CAS}}$	Column Address Strobe	1	$\overline{\text{RESET}}$	Reset Pin	1
$\overline{\text{WE}}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{\text{S}}0, \overline{\text{S}}1$	Chip Selects	2	V _{DD}	Core and I/O Power	18
A0-A9, A11, A13-A15	Address Inputs	14	V _{SS}	Ground	52
A10/AP	Address Input/Autoprecharge	1	V _{REFDQ} V _{REFCA}	Input/Output Reference	2
A12/ $\overline{\text{BC}}$	Address Input/Burst chop	1	V _{DDSPD}	SPD and Temp sensor Power	1
BA0-BA2	SDRAM Bank Addresses	3	V _{TT}	Termination Voltage	2
ODT0, ODT1	On-die termination control	2	NC	Reserved for future use	3
SCL	Serial Presence Detect (SPD) Clock Input	1		Total	204
SDA	SPD Data Input/Output	1			
SA0-SA1	SPD Address	2			

NOTE:

*The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs.

7. SPD and Thermal Sensor for ECC UDIMMs

On DIMM thermal sensor will provide DRAM temperature readout through a integrated thermal sensor.


NOTE :

1. Raw Cards D (1Rx8 ECC) and E (2Rx8 ECC) support a thermal sensor.
2. When the SPD and the thermal sensor are placed on the module, R1 is placed but R2 is not. When only the SPD is placed on the module, R2 is placed but R1 is not.

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

8. Input/Output Functional Description

Symbol	Type	Function
CK0-CK1 CK0-CK1	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$ - $\overline{S1}$	Input	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0-BA2	Input	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT0-ODT1	Input	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
A0-A9, A10/AP, A11 A12/ $\overline{BC}$ A13-A15	Input	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the fly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ0-DQ63	I/O	Data Input/Output pins.
DM0-DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0-DQS7 $\overline{DQS0}$ - $\overline{DQS7}$	I/O	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.
V_{DD} , V_{DDSPD} , V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ} , V_{REFCA}	Supply	Reference voltage for SSTL15 inputs.
SDA	I/O	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0-SA1	Input	Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	I/O	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules
$\overline{RESET}$	Input	$\overline{RESET}$ In Active Low This signal resets the DDR3 SDRAM

8.1 Address Mirroring Feature

There is a via grid located under the DRAMs for wiring the CA signals (address, bank address, command, and control lines) to the DRAM pins. The length of the traces from the vias to the DRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.

The pins on the DRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 DRAM pins are wired straight, with no mismatch between the connector pin assignment and the DRAM pin assignment. Some of the Rank 1 DRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

8.1.1 DRAM Pin Wiring Mirroring

Connector Pin	DRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

Figure 1 illustrates the wiring in both the mirrored and non-mirrored case. The lengths of the traces to the DRAM pins, is obviously shorter. The via grid is smaller as well.

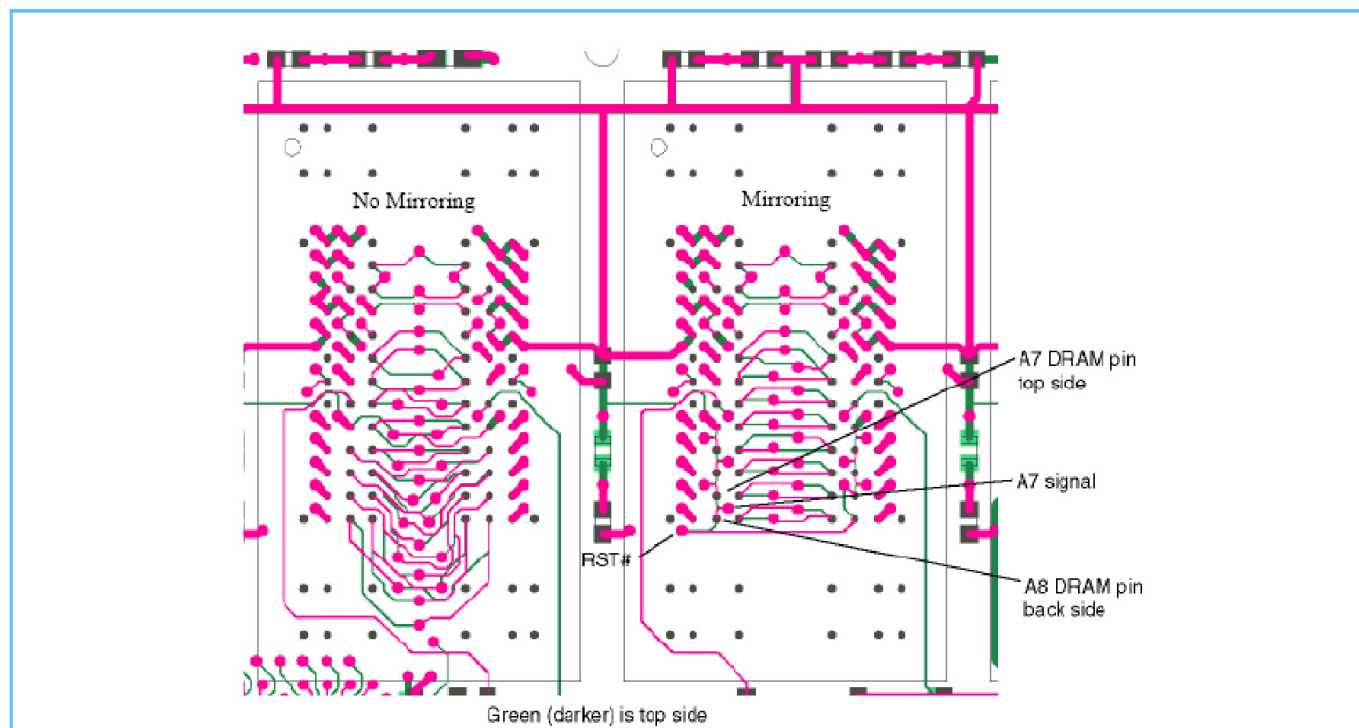
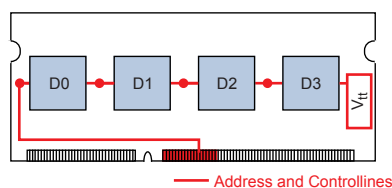
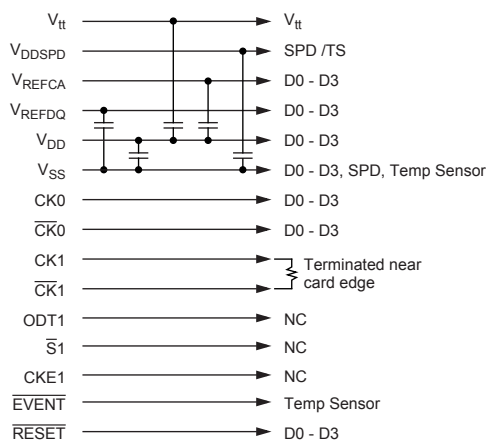
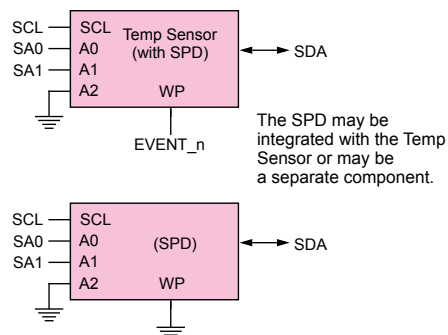
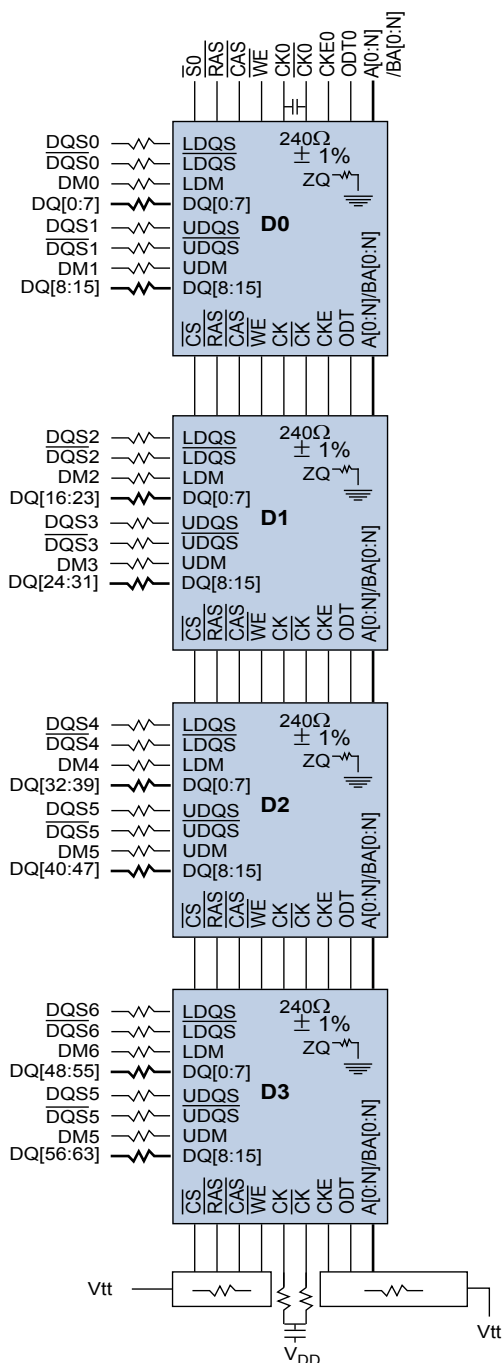


Figure 1. Wiring Differences for Mirrored and Non-Mirrored Addresses

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank. SAMSUNG DDR3 dual rank UDIMM R/C B(2Rx8) and R/C E(2Rx8) Modules are using Mirrored Addresses mode.

9. Function Block Diagram:

9.1 2GB, 256Mx64 Module (Populated as 1 rank of x16 DDR3 SDRAMs)

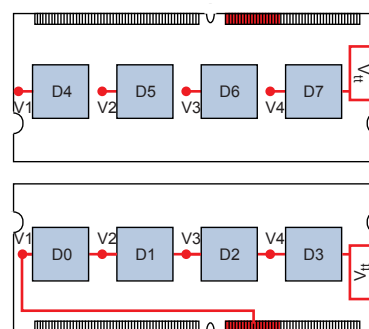
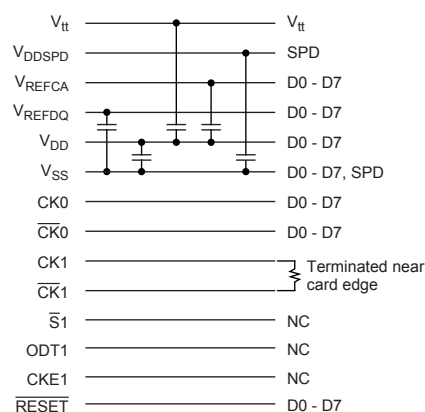
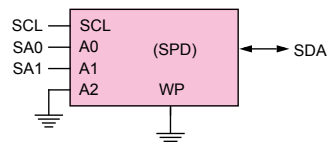
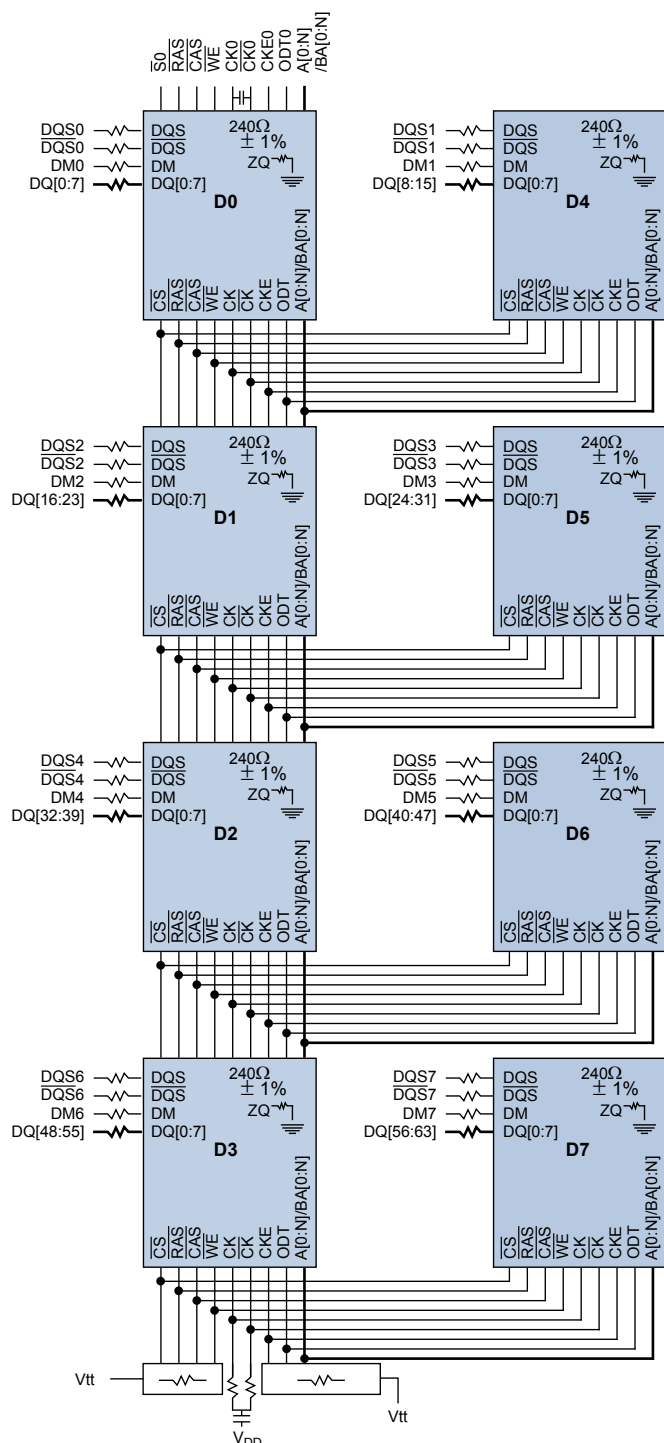


NOTE :

1. DQ wiring may differ from that shown however ,DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

Rank0

9.2 4GB, 512Mx64 Module (Populated as 1 rank of x8 DDR3 SDRAMs)



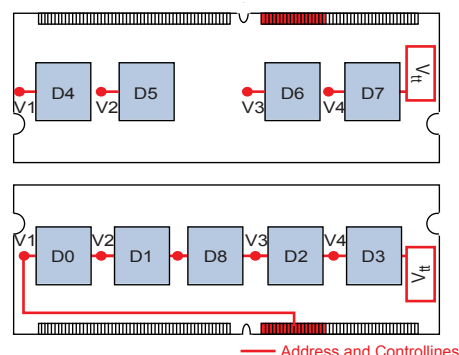
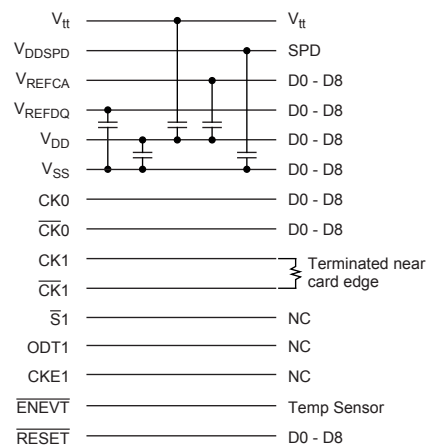
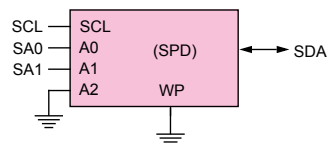
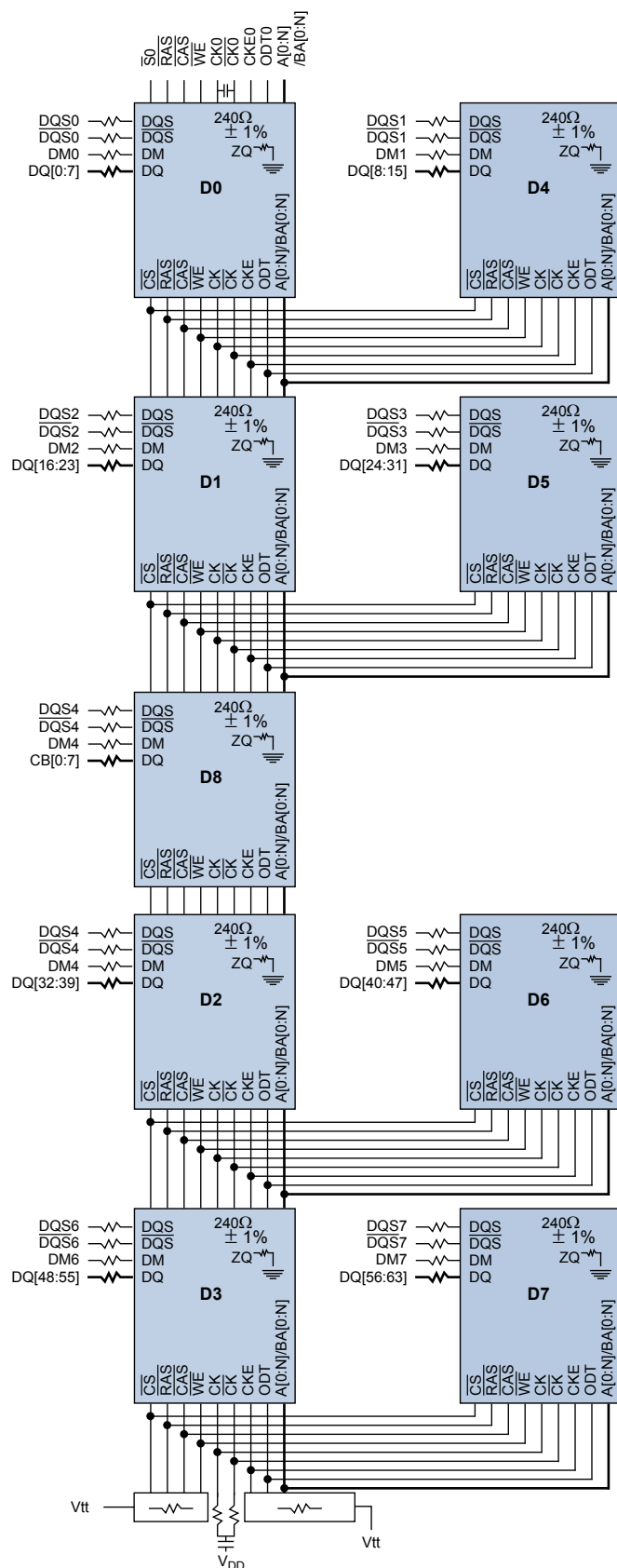
Address and Control lines

NOTE :

1. DQ wiring may differ from that shown however, DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

Rank0

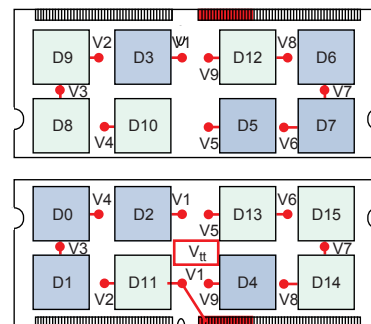
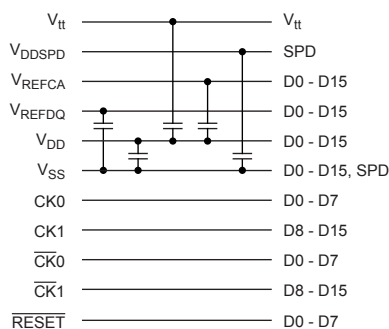
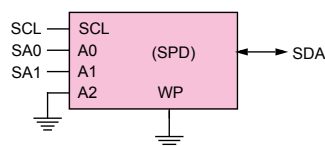
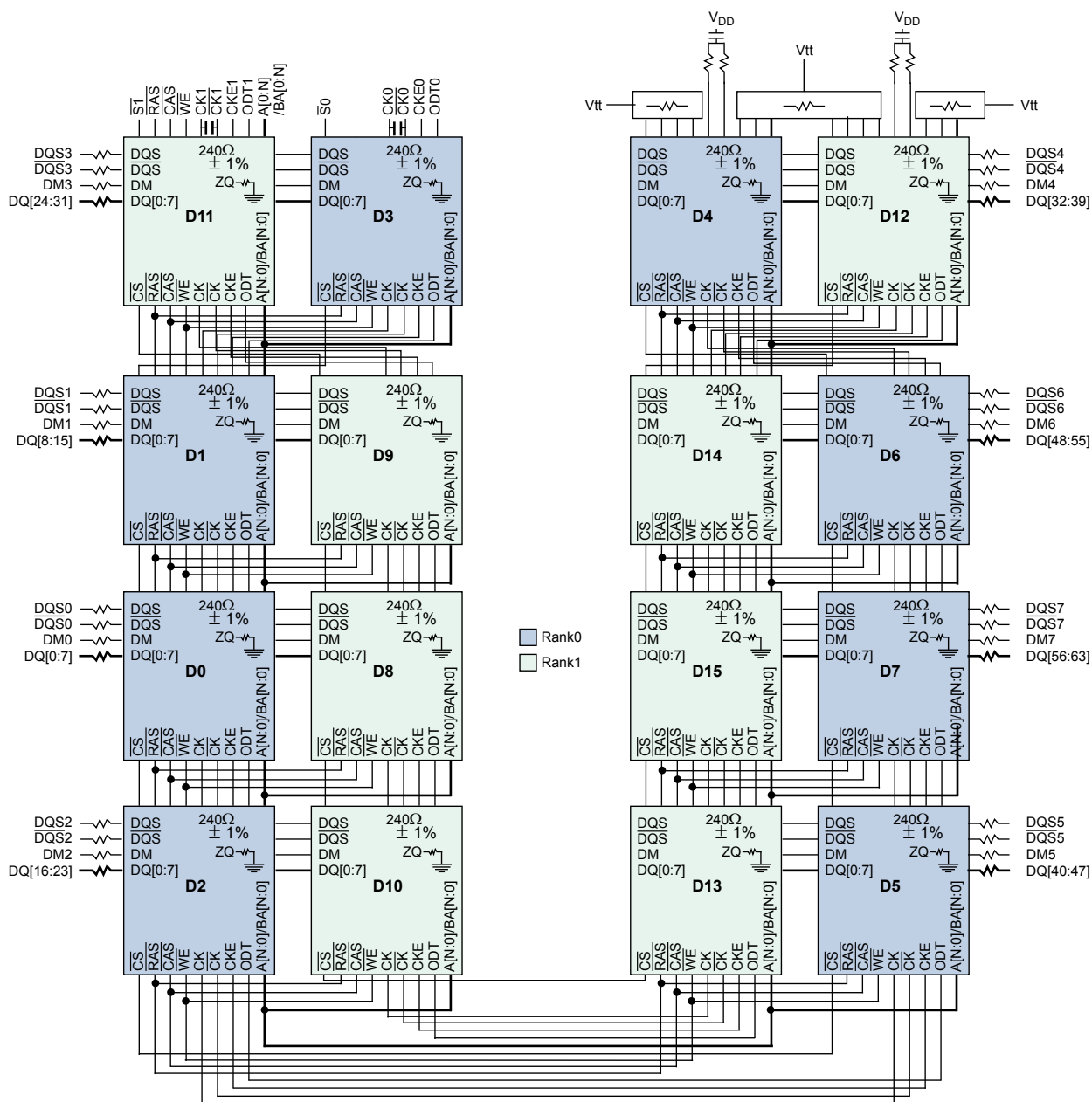
9.3 4GB, 512Mx72 Module (Populated as 1 rank of x8 DDR3 SDRAMs)

**NOTE :**

1. DQ wiring may differ from that shown however, DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

Rank0

9.4 8GB, 1Gx64 Module (Populated as 2 ranks of x8 DDR3 SDRAMs)

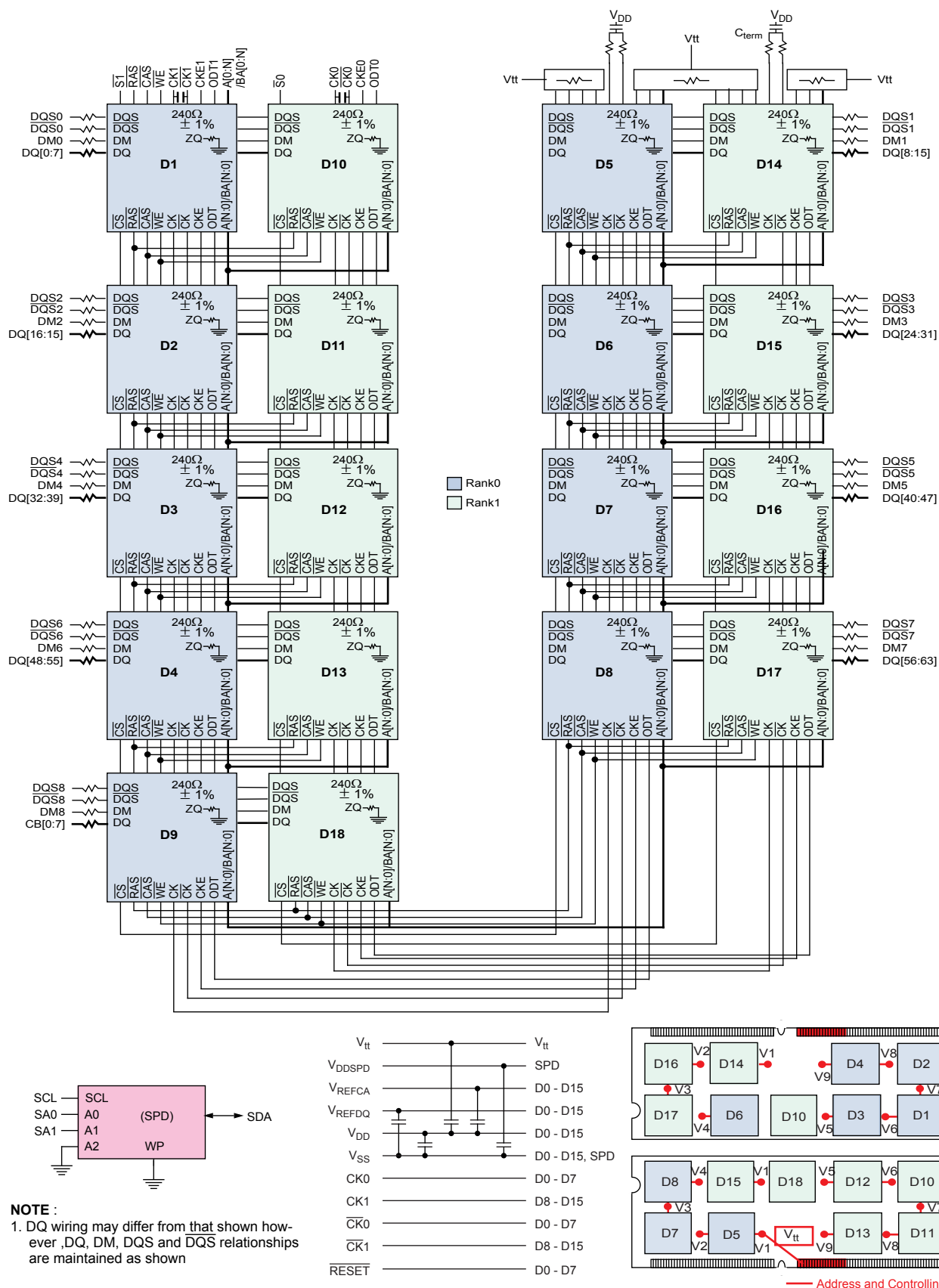


— Address and Control Lines

NOTE :

1. DQ wiring may differ from that shown however, DQ, DM, DQS and DQS relationships are maintained as shown

9.5 8GB, 1Gx72 Module (Populated as 2 ranks of x8 DDR3 SDRAMs)



10. Absolute Maximum Ratings

10.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ -1.80 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ -1.80 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ -1.80 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

10.2 DRAM Component Operating Temperature Range

Symbol	Parameter	rating	Unit	NOTE
T_{OPER}	Operating Temperature Range	0 to 95	°C	1, 2, 3

NOTE :

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
- Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the refresh interval $tREFI$ to 3.9us.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case $IDD6$ current can be increased around 10~20% than normal Temperature range.

11. AC & DC Operating Conditions

11.1 Recommended DC Operating Conditions

Symbol	Parameter	Operation Voltage	Rating			Units	NOTE
			Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.35V	1.283	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3
V_{DDQ}	Supply Voltage for Output	1.35V	1.283	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3

NOTE:

- Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together.
- V_{DD} & V_{DDQ} rating are determined by operation voltage.

12. AC & DC Input Measurement Levels

12.1 AC & DC Logic Input Levels for Single-ended Signals

[Table 2] Single Ended AC and DC input levels for Command and Address(1.35V)

Symbol	Parameter	DDR3L-800/1066/1333/1600		DDR3L-1866		Unit	NOTE
		Min.	Max.	Min.	Max.		
1.35V							
V _{IH,CA} (DC90)	DC input logic high	V _{REF} + 90	V _{DD}	V _{REF} + 90	V _{DD}	mV	1
V _{IL,CA} (DC90)	DC input logic low	V _{SS}	V _{REF} - 90	V _{SS}	V _{REF} - 90	mV	1
V _{IH,CA} (AC160)	AC input logic high	V _{REF} + 160	Note 2	-	-	mV	1,2,5
V _{IL,CA} (AC160)	AC input logic low	Note 2	V _{REF} - 160	-	-	mV	1,2,5
V _{IH,CA} (AC135)	AC input logic high	V _{REF} +135	Note 2	V _{REF} +135	Note 2	mV	1,2,5
V _{IL,CA} (AC135)	AC input logic lowM	Note 2	V _{REF} -135	Note 2	V _{REF} -135	mV	1,2,5
V _{REFCA} (DC)	Reference Voltage for ADD, CMD inputs	0.49*V _{DD}	0.51*V _{DD}	V _{REF} + 125	Note 2	V	3,4

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFCA}(DC)$
- See "Overshoot and Undershoot specifications" on Component Datasheet.
- The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV).
- For reference: approx. $V_{DD}/2 \pm 13.5$ mV
- These levels apply for 1.35 Volt operation only. If the device is operated at 1.5 V, the respective levels in JESD79-3 ($V_{IH/L,CA}(DC100)$, $V_{IH/L,CA}(AC175)$, $V_{IH/L,CA}(AC150)$, $V_{IH/L,CA}(AC135)$, $V_{IH/L,CA}(AC125)$ etc.) apply. The 1.5 V levels ($V_{IH/L,CA}(DC100)$, $V_{IH/L,CA}(AC175)$, $V_{IH/L,CA}(AC150)$, $V_{IH/L,CA}(AC135)$, $V_{IH/L,CA}(AC125)$ etc.) do not apply when the device is operated in the 1.35 voltage range.

[Table 3] Single-ended AC & DC input levels for Command and Address(1.5V)

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866		Unit	NOTE
		Min.	Max.	Min.	Max.		
1.5V							
V _{IH,CA} (DC100)	DC input logic high	V _{REF} + 100	V _{DD}	V _{SS}	V _{REF} - 100	mV	1,5
V _{IL,CA} (DC100)	DC input logic low	V _{SS}	V _{REF} - 100	-	-	mV	1,6
V _{IH,CA} (AC175)	AC input logic high	V _{REF} + 175	Note 2	-	-	mV	1,2,7
V _{IL,CA} (AC175)	AC input logic low	Note 2	V _{REF} - 175	-	-	mV	1,2,8
V _{IH,CA} (AC150)	AC input logic high	V _{REF} +150	Note 2	-	-	mV	1,2,7
V _{IL,CA} (AC150)	AC input logic low	Note 2	V _{REF} -150	V _{REF} + 135	Note 2	mV	1,2,8
V _{REFCA} (DC)	Reference Voltage for ADD, CMD inputs	0.49*V _{DD}	0.51*V _{DD}	Note 2	V _{REF} - 135	V	3,4,9

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFCA}(DC)$
- See "Overshoot and Undershoot specifications" on Component Datasheet.
- The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
- For reference: approx. $V_{DD}/2 \pm 15$ mV.
- $V_{IH}(dc)$ is used as a simplified symbol for $V_{IH,CA}(DC100)$
- $V_{IL}(dc)$ is used as a simplified symbol for $V_{IL,CA}(DC100)$
- $V_{IH}(ac)$ is used as a simplified symbol for $V_{IH,CA}(AC175)$, $V_{IH,CA}(AC150)$, $V_{IH,CA}(AC135)$, and $V_{IH,CA}(AC125)$; $V_{IH,CA}(AC175)$ value is used when Vref + 0.175V is referenced, $V_{IH,CA}(AC150)$ value is used when Vref + 0.150V is referenced, $V_{IH,CA}(AC135)$ value is used when Vref + 0.135V is referenced, and $V_{IH,CA}(AC125)$ value is used when Vref + 0.125V is referenced.
- $V_{IL}(ac)$ is used as a simplified symbol for $V_{IL,CA}(AC175)$, $V_{IL,CA}(AC150)$, $V_{IL,CA}(AC135)$ and $V_{IL,CA}(AC125)$; $V_{IL,CA}(AC175)$ value is used when Vref - 0.175V is referenced, $V_{IL,CA}(AC150)$ value is used when Vref - 0.150V is referenced, $V_{IL,CA}(AC135)$ value is used when Vref - 0.135V is referenced, and $V_{IL,CA}(AC125)$ value is used when Vref - 0.125V is referenced.
- VrefCA(DC) is measured relative to VDD at the same point in time on the same device

[Table 4] Single Ended AC and DC input levels for DQ and DM(1.35V)

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
1.35V									
V _{IH,DQ} (DC90)	DC input logic high	V _{REF} + 90	V _{DD}	V _{REF} + 90	V _{DD}	V _{REF} + 90	V _{DD}	mV	1
V _{IL,DQ} (DC90)	DC input logic low	V _{SS}	V _{REF} - 90	V _{SS}	V _{REF} - 90	V _{SS}	V _{REF} - 90	mV	1
V _{IH,DQ} (AC160)	AC input logic high	V _{REF} + 160	Note 2	-	-	-	-	mV	1,2,5
V _{IL,DQ} (AC160)	AC input logic low	Note 2	V _{REF} - 160	-	-	-	-	mV	1,2,5
V _{IH,DQ} (AC135)	AC input logic high	V _{REF} + 135	Note 2	V _{REF} + 135	Note 2	-	-	mV	1,2,5
V _{IL,DQ} (AC135)	AC input logic low	Note 2	V _{REF} - 135	Note 2	V _{REF} - 135	-	-	mV	1,2,5
V _{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49*V _{DD}	0.51*V _{DD}	0.49*V _{DD}	0.51*V _{DD}	V _{REF} + 130	Note 2	V	3,4

NOTE :

- For input only pins except $\overline{\text{RESET}}$, V_{REF} = V_{REFDQ}(DC)
- See "Overshoot and Undershoot specifications" on Component Datasheet.
- The ac peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFDQ}(DC) by more than +/-1% V_{DD} (for reference: approx. +/- 13.5 mV).
- For reference: approx. V_{DD}/2 +/- 13.5 mV.
- These levels apply for 1.35 Volt operation only. If the device is operated at 1.5 V, the respective levels in JESD79-3 (V_{IH/L.DQ}(DC100), V_{IH/L.DQ}(AC175), V_{IH/L.DQ}(AC150), V_{IH/L.DQ}(AC135), etc.) apply. The 1.5 V levels (V_{IH/L.DQ}(DC100), V_{IH/L.DQ}(AC175), V_{IH/L.DQ}(AC150), V_{IH/L.DQ}(AC135), etc.) do not apply when the device is operated in the 1.35 voltage range.

[Table 5] Single-ended AC & DC input levels for DQ and DM (1.5V)

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
1.5V									
V _{IH.DQ} (DC100)	DC input logic high	V _{REF} + 100	V _{DD}	V _{REF} + 100	V _{DD}	V _{REF} + 100	V _{DD}	mV	1,5
V _{IL.DQ} (DC100)	DC input logic low	V _{SS}	V _{REF} - 100	V _{SS}	V _{REF} - 100	V _{SS}	V _{REF} - 100	mV	1,6
V _{IH.DQ} (AC175)	AC input logic high	V _{REF} + 175	NOTE 2	-	-	-	-	mV	1,2,7
V _{IL.DQ} (AC175)	AC input logic low	NOTE 2	V _{REF} - 175	-	-	-	-	mV	1,2,8
V _{IH.DQ} (AC150)	AC input logic high	V _{REF} + 150	NOTE 2	V _{REF} + 150	NOTE 2	-	-	mV	1,2,7
V _{IL.DQ} (AC150)	AC input logic low	NOTE 2	V _{REF} - 150	NOTE 2	V _{REF} - 150	-	-	mV	1,2,8
V _{IH.DQ} (AC135)	AC input logic high	V _{REF} + 135	NOTE 2	V _{REF} + 135	NOTE 2	V _{REF} + 135	NOTE 2	mV	1,2,7,10
V _{IL.DQ} (AC135)	AC input logic low	NOTE 2	V _{REF} - 135	NOTE 2	V _{REF} - 135	NOTE 2	V _{REF} - 135	mV	1,2,8,10
V _{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49*V _{DD}	0.51*V _{DD}	0.49*V _{DD}	0.51*V _{DD}	0.49*V _{DD}	0.51*V _{DD}	V	3,4,9

NOTE :

- For input only pins except $\overline{\text{RESET}}$, V_{REF} = V_{REFDQ}(DC)
- See "Overshoot and Undershoot specifications" on Component Datasheet.
- The ac peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REFDQ}(DC) by more than +/-1% V_{DD} (for reference: approx. +/- 15 mV).
- For reference: approx. V_{DD}/2 +/- 15 mV.
- V_{IH}(dc) is used as a simplified symbol for V_{IH.DQ}(DC100)
- V_{IL}(dc) is used as a simplified symbol for V_{IL.DQ}(DC100)
- V_{IH}(ac) is used as a simplified symbol for V_{IH.DQ}(AC175), V_{IH.DQ}(AC150), and V_{IH.DQ}(AC135); V_{IH.DQ}(AC175) value is used when V_{REF} + 0.175V is referenced, V_{IH.DQ}(AC150) value is used when V_{REF} + 0.150V is referenced, and V_{IH.DQ}(AC135) value is used when V_{REF} + 0.135V is referenced.
- V_{IL}(ac) is used as a simplified symbol for V_{IL.DQ}(AC175), V_{IL.DQ}(AC150), and V_{IL.DQ}(AC135); V_{IL.DQ}(AC175) value is used when V_{REF} - 0.175V is referenced, V_{IL.DQ}(AC150) value is used when V_{REF} - 0.150V is referenced, and V_{IL.DQ}(AC135) value is used when V_{REF} - 0.135V is referenced.
- V_{REFDQ}(DC) is measured relative to V_{DD} at the same point in time on the same device
- Optional in DDR3 SDRAM for DDR3-800/1066/1333/1600: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support this option

12.2 V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 2. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements of V_{REF} . Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

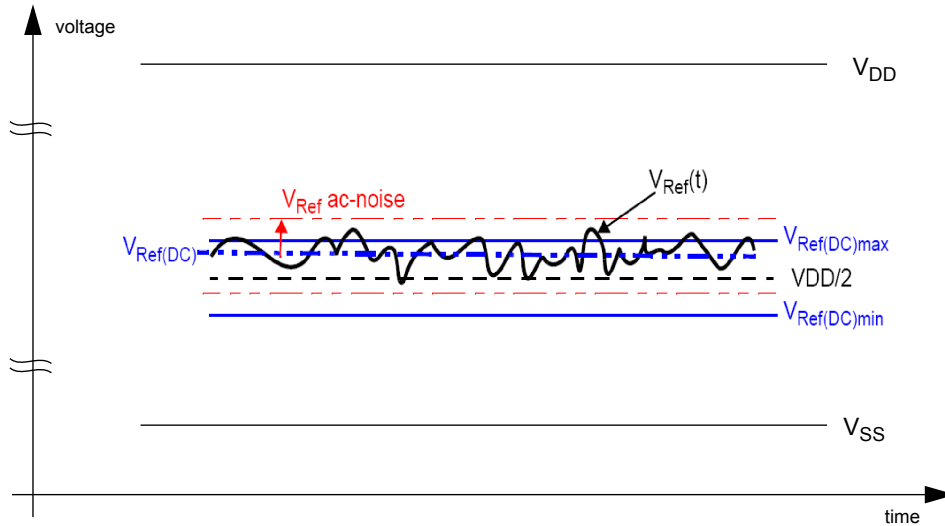


Figure 2. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure 2.

This clarifies, that dc-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} ac-noise. Timing and voltage effects due to ac-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

12.3 AC and DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition

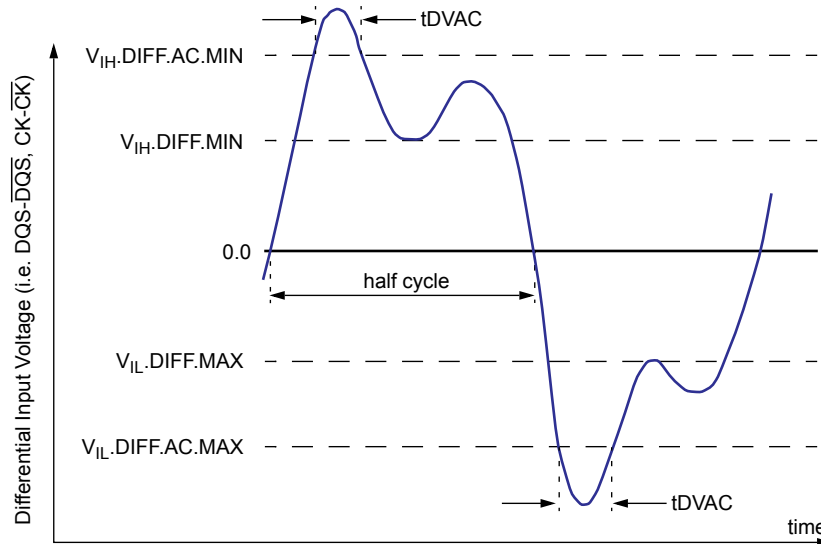


Figure 3. Definition of differential ac-swing and "time above ac level" tDVAC

12.3.2 Differential Swing Requirement for Clock (CK - CK-bar) and Strobe (DQS - DQS-bar)

Symbol	Parameter	DDR3-800/1066/1333/1600/1866				unit	NOTE
		1.35V		1.5V			
		min	max	min	max		
V _{IHdiff}	differential input high	+0.18	NOTE 3	+0.20	NOTE 3	V	1
V _{ILdiff}	differential input low	NOTE 3	-0.18	NOTE 3	-0.20	V	1
V _{IHdiff} (AC)	differential input high ac	2 x (V _{IH} (AC) - V _{REF})	NOTE 3	2 x (V _{IH} (AC) - V _{REF})	NOTE 3	V	2
V _{ILdiff} (AC)	differential input low ac	NOTE 3	2 x (V _{IL} (AC) - V _{REF})	NOTE 3	2 x (V _{IL} (AC) - V _{REF})	V	2

NOTE :

- Used to define a differential signal slew-rate.
- for CK - CK-bar use $V_{IH}/V_{IL}(AC)$ of ADD/CMD and V_{REFCA} ; for DQS - DQS-bar use $V_{IH}/V_{IL}(AC)$ of DQs and V_{REFDQ} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however they single-ended signals CK, CK-bar, DQS, DQS-bar need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "overshoot and Undersheet Specification"

[Table 6] Allowed time before ringback (tDVAC) for CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$ (1.35V)

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600				DDR3L-1866					
	tDVAC [ps] @ $ V_{IH}/L_{diff}(AC) = 320\text{mV}$		tDVAC [ps] @ $ V_{IH}/L_{diff}(AC) = 270\text{mV}$		tDVAC [ps] @ $ V_{IH}/L_{diff}(ac) = 270\text{mV}$		tDVAC [ps] @ $ V_{IH}/L_{diff}(ac) = 250\text{mV}$		tDVAC [ps] @ $ V_{IH}/L_{diff}(ac) = 260\text{mV}$	
	min	max	min	max	min	max	min	max	min	max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	note	-	44	-	5	-	22	-	24	-
1.0	note	-	note	-	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

NOTE: Rising input signal shall become equal to or greater than $V_{IH}(ac)$ level and Falling input signal shall become equal to or less than $V_{IL}(ac)$ level.

[Table 7] Allowed time before ringback (tDVAC) for CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$ (1.5V)

Slew Rate [V/ns]	DDR3-800/1066/1333/1600						DDR3-1866			
	tDVAC [ps] @ $V_{IH}/L_{diff}(AC) = 350\text{mV}$		tDVAC [ps] @ $V_{IH}/L_{diff}(AC) = 300\text{mV}$		tDVAC [ps] @ $V_{IH}/L_{diff}(ac) = 270\text{mV}$ (DQS - DQS#) only (Optional)		tDVAC [ps] @ $V_{IH}/L_{diff}(AC) = 270\text{mV}$		tDVAC [ps] @ $V_{IH}/L_{diff}(AC) = 250\text{mV}$ (CK - CK#) only	
	min	max	min	max	min	max	min	max	min	max
> 4.0	75	-	175	-	214	-	134	-	139	-
4.0	57	-	170	-	214	-	134	-	139	-
3.0	50	-	167	-	191	-	112	-	118	-
2.0	38	-	119	-	146	-	67	-	77	-
1.8	34	-	102	-	131	-	52	-	63	-
1.6	29	-	81	-	113	-	33	-	45	-
1.4	22	-	54	-	88	-	9	-	23	-
1.2	note	-	19	-	56	-	note	-	note	-
1.0	note	-	note	-	11	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

NOTE: Rising input differential signal shall become equal to or greater than $V_{IHdiff}(ac)$ level and Falling input differential signal shall become equal to or less than $V_{ILdiff}(ac)$ level.

12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, $\overline{\text{CK}}$, $\overline{\text{DQS}}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{\text{CK}}$ have to approximately reach V_{SEHmin} / V_{SELmax} (approximately equal to the ac-levels ($V_{IH}(AC) / V_{IL}(AC)$) for ADD/CMD signals) in every half-cycle.

DQS have to reach V_{SEHmin} / V_{SELmax} (approximately the ac-levels ($V_{IH}(AC) / V_{IL}(AC)$) for DQ signals) in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if $V_{IH150}(AC)/V_{IL150}(AC)$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{\text{CK}}$.

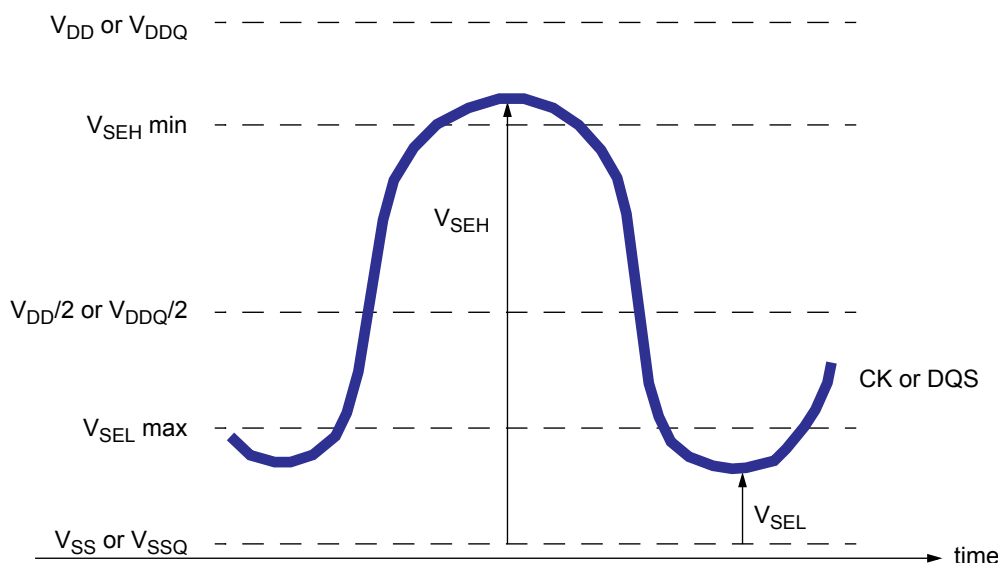


Figure 4. Single-ended requirement for differential signals

Note that while ADD/CMD and DQ signal requirements are with respect to V_{REF} , the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SELmax} , V_{SEHmin} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 8] Single ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

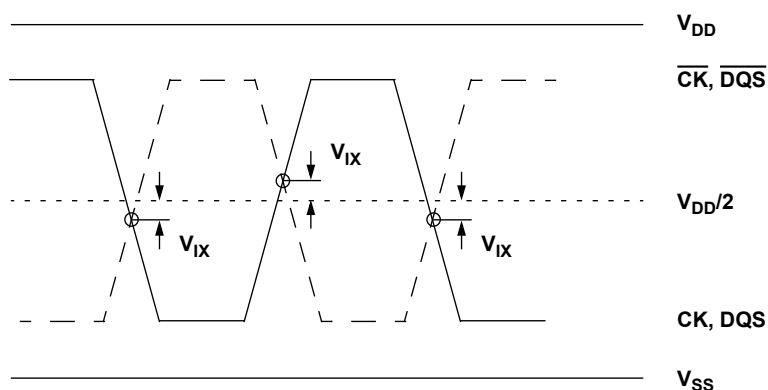
Symbol	Parameter	DDR3-800/1066/1333/1600/1866		Unit	NOTE
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	$(V_{DD}/2)+0.175$	NOTE 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	$(V_{DD}/2)+0.175$	NOTE 3	V	1, 2
V_{SEL}	Single-ended low-level for strobes	NOTE 3	$(V_{DD}/2)-0.175$	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	$(V_{DD}/2)-0.175$	V	1, 2

NOTE :

- For CK, $\overline{CK}$ use $V_{IH}/V_{IL}(AC)$ of ADD/CMD; for strobes (DQS, $\overline{DQS}$) use $V_{IH}/V_{IL}(AC)$ of DQs.
- $V_{IH}(AC)/V_{IL}(AC)$ for DQs is based on V_{REFDQ} ; $V_{IH}(AC)/V_{IL}(AC)$ for ADD/CMD is based on V_{REFCA} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
- These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specification"

12.3.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid level between of V_{DD} and V_{SS} .

Figure 5. V_{IX} Definition

[Table 9] Cross point voltage for differential input signals (CK, DQS) : 1.35V

Symbol	Parameter	DDR3L-800/1066/1333/1600/1866		Unit	NOTE
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, $\overline{CK}$	-150	150	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, $\overline{DQS}$	-150	150	mV	

NOTE :

1. The relation between V_{ix} Min/Max and V_{SEL}/V_{SEH} should satisfy following.

$$(V_{DD}/2) + V_{ix}(\text{Min}) - V_{SEL} \geq 25\text{mV}$$

$$V_{SEH} - ((V_{DD}/2) + V_{ix}(\text{Max})) \geq 25\text{mV}$$

[Table 10] Cross point voltage for differential input signals (CK, DQS) : 1.5V

Symbol	Parameter	DDR3-800/1066/1333/1600/1866		Unit	NOTE
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, $\overline{DQS}$	-150	150	mV	

NOTE :

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2 \pm 250\text{ mV}$, and the differential slew rate of CK- $\overline{CK}$ is larger than 3 V / ns.

12.4 Slew Rate Definition for Single Ended Input Signals

See "Address / Command Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

12.5 Slew rate definition for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) are defined and measured as shown in below.

[Table 11] Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{\text{ILdiffmax}}$	$V_{\text{IHdiffmin}}$	$[V_{\text{IHdiffmin}} - V_{\text{ILdiffmax}}] / \Delta \text{TRdiff}$
Differential input slew rate for falling edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{\text{IHdiffmin}}$	$V_{\text{ILdiffmax}}$	$[V_{\text{IHdiffmin}} - V_{\text{ILdiffmax}}] / \Delta \text{TFdiff}$

NOTE : The differential signal (i.e. CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$) must be linear between these thresholds

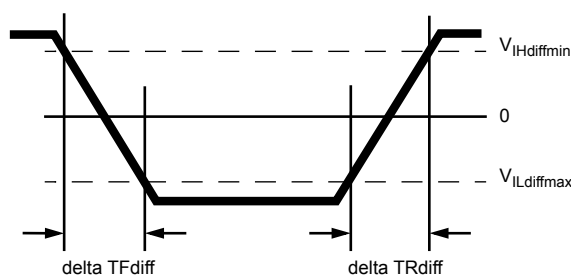


Figure 6. Differential input slew rate definition for DQS, $\overline{\text{DQS}}$ and CK, $\overline{\text{CK}}$

13. AC & DC Output Measurement Levels

13.1 Single Ended AC and DC Output Levels

[Table 12] Single Ended AC and DC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600/1866	Units	NOTE
$V_{\text{OH}}(\text{DC})$	DC output high measurement level (for IV curve linearity)	$0.8 \times V_{\text{DDQ}}$	V	
$V_{\text{OM}}(\text{DC})$	DC output mid measurement level (for IV curve linearity)	$0.5 \times V_{\text{DDQ}}$	V	
$V_{\text{OL}}(\text{DC})$	DC output low measurement level (for IV curve linearity)	$0.2 \times V_{\text{DDQ}}$	V	
$V_{\text{OH}}(\text{AC})$	AC output high measurement level (for output SR)	$V_{\text{TT}} + 0.1 \times V_{\text{DDQ}}$	V	1
$V_{\text{OL}}(\text{AC})$	AC output low measurement level (for output SR)	$V_{\text{TT}} - 0.1 \times V_{\text{DDQ}}$	V	1

NOTE :

1. The swing of $\pm 0.1 \times V_{\text{DDQ}}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{\text{TT}} = V_{\text{DDQ}}/2$.

13.2 Differential AC and DC Output Levels

[Table 13] Differential AC and DC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600/1866	Units	NOTE
$V_{\text{OHdiff}}(\text{AC})$	AC differential output high measurement level (for output SR)	$+0.2 \times V_{\text{DDQ}}$	V	1
$V_{\text{OLdiff}}(\text{AC})$	AC differential output low measurement level (for output SR)	$-0.2 \times V_{\text{DDQ}}$	V	1

NOTE :

1. The swing of $\pm 0.2 \times V_{\text{DDQ}}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{\text{TT}} = V_{\text{DDQ}}/2$ at each of the differential outputs.

13.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single ended signals as shown in below.

[Table 14] Single ended Output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)] / \Delta TR_{se}$
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)] / \Delta TF_{se}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 15] Single ended output slew rate

Parameter	Symbol	Operation Voltage	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	1.35V	1.75	5 ¹⁾	1.75	5 ¹⁾	1.75	5 ¹⁾	1.75	5 ¹⁾	1.75	5 ¹⁾	V/ns
		1.5V	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

se : Single-ended Signals

For Ron = RZQ/7 setting

NOTE : 1) In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
- Case_2 is defined for a single DQ signal in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

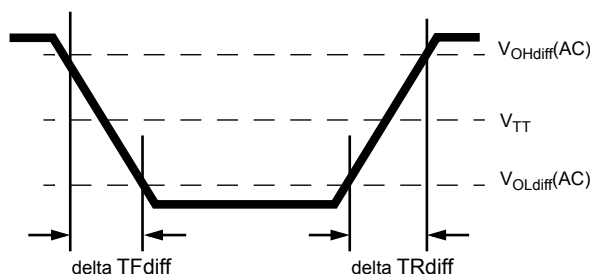


Figure 7. Single-ended output slew rate definition

13.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in below.

[Table 16] Differential Output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)] / \Delta TF_{diff}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 17] Differential Output slew rate

Parameter	Symbol	Operation Voltage	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	1.35V	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns
		1.5V	5	10	5	10	5	10	5	10	5	12	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

diff : Differential Signals

For Ron = RZQ/7 setting

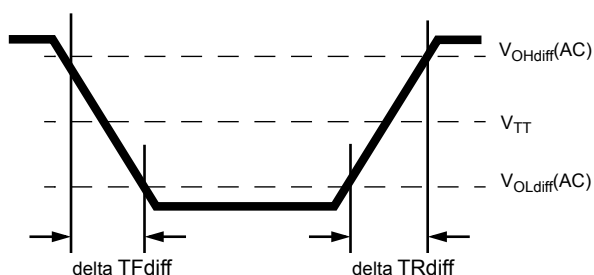


Figure 8. Differential output slew rate definition

14. IDD specification definition

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N	Precharge Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit ³⁾
IDD2P1	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit ³⁾
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one ; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD6	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled ⁴⁾ ; Self-Refresh Temperature Range (SRT): Normal ⁵⁾ ; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$, Command, Address, Bank Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: FLOATING
IDD6ET	Self-Refresh Current: Extended Temperature Range (optional)⁶⁾ TCASE: 0 - 95°C; Auto Self-Refresh (ASR): Disabled ⁴⁾ ; Self-Refresh Temperature Range (SRT): Extended ⁵⁾ ; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: 0; $\overline{CS}$, Command, Address, Bank Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: FLOATING
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern ; BL: 8 ¹⁾ ; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8	RESET Low Current RESET : Low; External clock : off; CK and $\overline{CK}$: LOW; CKE : FLOATING ; $\overline{CS}$, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING

NOTE :

- 1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
- 2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
- 3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
- 4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
- 5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
- 6) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
- 7) IDD current measure method and detail patterns are described on DDR3 component datasheet
- 8) VDD and VDDQ are merged on module PCB.
- 9) DIMM IDD SPEC is measured with Qoff condition
(IDDQ values are not considered)

15. IDD SPEC Table

M471B5674EB0 : 2GB (256Mx64) Module

Symbol	DDR3-1600		DDR3-1866		Unit	NOTE
	1.35V	1.5V	1.35V	1.5V		
	11-11-11	11-11-11	13-13-13	13-13-13		
IDD0	140	160	150	170	mA	
IDD1	220	230	220	240	mA	
IDD2P0(slow exit)	50	60	50	60	mA	
IDD2P1(fast exit)	50	60	50	60	mA	
IDD2N	70	80	70	80	mA	
IDD2Q	70	80	70	80	mA	
IDD3P	80	90	80	90	mA	
IDD3N	120	130	120	130	mA	
IDD4R	420	460	480	520	mA	
IDD4W	400	440	440	480	mA	
IDD5B	840	880	840	880	mA	
IDD6	60	60	60	60	mA	
IDD7	680	720	700	740	mA	
IDD8	50	60	50	60	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 18.
2. IDD current measure method and detail patterns are described on DDR3 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

M471B5173EB0 : 4GB (512Mx64) Module

Symbol	DDR3-1600		DDR3-1866		Unit	NOTE
	1.35V	1.5V	1.35V	1.5V		
	11-11-11	11-11-11	13-13-13	13-13-13		
IDD0	200	230	240	240	mA	
IDD1	280	320	350	360	mA	
IDD2P0(slow exit)	60	90	60	90	mA	
IDD2P1(fast exit)	60	90	60	90	mA	
IDD2N	90	100	110	110	mA	
IDD2Q	80	100	100	100	mA	
IDD3P	80	90	90	90	mA	
IDD3N	170	180	180	180	mA	
IDD4R	510	570	620	640	mA	
IDD4W	510	570	610	640	mA	
IDD5B	1520	1600	1560	1600	mA	
IDD6	100	120	100	120	mA	
IDD7	970	1040	1080	1130	mA	
IDD8	120	120	120	120	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 18.
2. IDD current measure method and detail patterns are described on DDR3 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

M474B5173EB0 : 4GB (512Mx72) Module

Symbol	DDR3-1600	Unit	NOTE
	1.35V		
	11-11-11		
IDD0	230	mA	
IDD1	320	mA	
IDD2P0(slow exit)	70	mA	
IDD2P1(fast exit)	70	mA	
IDD2N	100	mA	
IDD2Q	90	mA	
IDD3P	90	mA	
IDD3N	190	mA	
IDD4R	570	mA	
IDD4W	560	mA	
IDD5B	1710	mA	
IDD6	110	mA	
IDD7	1040	mA	
IDD8	140	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 18.
2. IDD current measure method and detail patterns are described on DDR3 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

M471B1G73EB0 : 8GB (1Gx64) Module

Symbol	DDR3-1600		DDR3-1866		Unit	NOTE
	1.35V	1.5V	1.35V	1.5V		
	11-11-11	11-11-11	13-13-13	13-13-13		
IDD0	290	330	350	360	mA	
IDD1	370	420	460	470	mA	
IDD2P0(slow exit)	130	180	130	180	mA	
IDD2P1(fast exit)	130	180	130	180	mA	
IDD2N	180	210	220	220	mA	
IDD2Q	160	190	210	210	mA	
IDD3P	160	180	180	180	mA	
IDD3N	340	370	370	370	mA	
IDD4R	600	670	730	750	mA	
IDD4W	590	670	720	750	mA	
IDD5B	1610	1700	1670	1710	mA	
IDD6	190	240	190	240	mA	
IDD7	1060	1140	1190	1240	mA	
IDD8	240	240	240	240	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 18.
2. IDD current measure method and detail patterns are described on DDR3 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

M474B1G73EB0 : 8GB (1Gx72) Module

Symbol	DDR3-1600	Unit	NOTE
	1.35V		
	11-11-11		
IDD0	330	mA	
IDD1	420	mA	
IDD2P0(slow exit)	140	mA	
IDD2P1(fast exit)	140	mA	
IDD2N	200	mA	
IDD2Q	180	mA	
IDD3P	180	mA	
IDD3N	380	mA	
IDD4R	670	mA	
IDD4W	660	mA	
IDD5B	1810	mA	
IDD6	220	mA	
IDD7	1140	mA	
IDD8	270	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N. Please refer to Table 18.
2. IDD current measure method and detail patterns are described on DDR3 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

[Table 18] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
IDD0	IDD0	IDD2N
IDD1	IDD1	IDD2N
IDD2P slow	IDD2P slow	IDD2P slow
IDD2P fast	IDD2P fast	IDD2P fast
IDD2N	IDD2N	IDD2N
IDD2Q	IDD2Q	IDD2Q
IDD3P	IDD3P	IDD3P
IDD3N	IDD3N	IDD2N
IDD4R	IDD4R	IDD2N
IDD4W	IDD4W	IDD2N
IDD5B	IDD5B	IDD2N
IDD6	IDD6	IDD6
IDD7	IDD7	IDD2N
IDD8	IDD8	IDD8

16. Input/Output Capacitance

[Table 19] Input/Output Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
1.35V											
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	1.4	2.5	1.4	2.5	1.4	2.3	1.5	2.2	pF	1,2,3
Input capacitance (CK and $\overline{CK}$)	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
Input capacitance delta (CK and $\overline{CK}$)	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	pF	2,3,6
Input/Output capacitance delta (DQS and $\overline{DQS}$)	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-only pins)	CDI_ADD_CMD	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2, 3, 12
1.5V											
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	1.4	3.0	1.4	2.7	1.4	2.5	1.4	2.3	pF	1,2,3
Input capacitance (CK and $\overline{CK}$)	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
Input capacitance delta (CK and $\overline{CK}$)	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	2,3,6
Input capacitance delta (DQS and $\overline{DQS}$)	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-only pins)	CDI_ADD_CMD	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2, 3, 12

NOTE : This parameter is Component Input/Output Capacitance so that is different from Module level Capacitance.

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS

2. This parameter is not subject to production test. It is verified by design and characterization.

The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET and ODT as necessary). $V_{DD}=V_{DDQ}=1.5V$ or 1.35V, $V_{BIAS}=V_{DD}/2$ and on-die termination off.

3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

4. Absolute value of CCK- $\overline{CCK}$

5. Absolute value of CIO(DQS)-CIO($\overline{DQS}$)

6. CI applies to ODT, $\overline{CS}$, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.

7. CDI_CTRL applies to ODT, $\overline{CS}$ and CKE

8. $CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI(\overline{CLK}))$

9. CDI_ADD_CMD applies to A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$

10. $CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI(\overline{CLK}))$

11. $CDIO=CI(O,DQ,DM) - 0.5*(CI(O,DQS)+CI(\overline{DQS}))$

12. Maximum external load capacitance on ZQ pin: 5pF

17. Electrical Characteristics and AC timing

[0 °C < T_{CASE} ≤ 95 °C, V_{DDQ} = 1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V); V_{DD} = 1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)]

17.1 Refresh Parameters by Device Density

Parameter	Symbol	1Gb	2Gb	4Gb	8Gb	Units	NOTE
All Bank Refresh to active/refresh cmd time	tRFC	110	160	260	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T _{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	μs
		85 °C < T _{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	μs 1

NOTE :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

17.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Units	NOTE
Bin (CL - tRCD - tRP)	6-6-6	7-7-7	9-9-9	11-11-11	13-13-13		
Parameter	min	min	min	min	min		
CL	6	7	9	11	13	tCK	
tRCD	15	13.13	13.5	13.75	13.91	ns	
tRP	15	13.13	13.5	13.75	13.91	ns	
tRAS	37.5	37.5	36	35	34	ns	
tRC	52.5	50.63	49.5	48.75	47.91	ns	
tRRD	10	7.5	6.0	6.0	5.0	ns	
tFAW	40	37.5	30	30	27	ns	

17.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

DDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

[Table 20] DDR3-800 Speed Bins

Speed			DDR3-800		Units	NOTE
CL-nRCD-nRP			6 - 6 - 6			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15	20	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	15	-	ns	
ACT to ACT or REF command period		tRC	52.5	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,9,10
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3
Supported CL Settings			5,6		nCK	
Supported CWL Settings			5		nCK	

[Table 21] DDR3-1066 Speed Bins

Speed			DDR3-1066		Units	NOTE
CL-nRCD-nRP			7 - 7 - 7			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.125	20		ns	
ACT to internal read or write delay time	tRCD	13.125	-		ns	
PRE command period	tRP	13.125	-		ns	
ACT to ACT or REF command period	tRC	50.625	-		ns	
ACT to PRE command period	tRAS	37.5	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,5,9,10
	CWL = 6	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,5
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,8
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3
Supported CL Settings			5,6,7,8		nCK	
Supported CWL Settings			5,6		nCK	

[Table 22] DDR3-1333 Speed Bins

Speed			DDR3-1333		Units	NOTE
CL-nRCD-nRP			9 - 9 - 9			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.5 (13.125) ⁸	20		ns	
ACT to internal read or write delay time	tRCD	13.5 (13.125) ⁸	-		ns	
PRE command period	tRP	13.5 (13.125) ⁸	-		ns	
ACT to ACT or REF command period	tRC	49.5 (49.125) ⁸	-		ns	
ACT to PRE command period		tRAS	36	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,6,9,10
	CWL = 6,7	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,8
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3
Supported CL Settings			5,6,7,8,9,10		nCK	
Supported CWL Settings			5,6,7		nCK	

[Table 23] DDR3-1600 Speed Bins

Speed			DDR3-1600		Units	NOTE
CL-nRCD-nRP			11-11-11			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.75 (13.125) ⁸	20		ns	
ACT to internal read or write delay time	tRCD	13.75 (13.125) ⁸	-		ns	
PRE command period	tRP	13.75 (13.125) ⁸	-		ns	
ACT to ACT or REF command period	tRC	48.75 (48.125) ⁸	-		ns	
ACT to PRE command period		tRAS	35	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,7,9,10
	CWL = 6,7,8	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,7
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 7, 8	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
Supported CL Settings			5,6,7,8,9,10,11		nCK	
Supported CWL Settings			5,6,7,8		nCK	

[Table 24] DDR3-1866 Speed Bins

Speed			DDR3-1866		Units	NOTE
CL-nRCD-nRP			13-13-13			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.91 (13.125) ¹³	20		ns	
ACT to internal read or write delay time	tRCD	13.91 (13.125) ¹³	-		ns	
PRE command period	tRP	13.91 (13.125) ¹³	-		ns	
ACT to ACT or REF command period	tRC	47.91 (47.125) ¹³	-		ns	
ACT to PRE command period	tRAS	34	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,8
	CWL = 6,7,8,9	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	2.5	ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
CL = 8	CWL = 8,9	tCK(AVG)	Reserved		ns	4
	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	1.875	ns	1,2,3,4,8
CL = 9	CWL = 8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	4
	CWL = 5,6	tCK(AVG)	Reserved		ns	4
CL = 10	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
CL = 11	CWL = 8	tCK(AVG)	1.25	1.5	ns	1,2,3,4,8
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
CL = 12	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
CL = 13	CWL = 9	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
	Supported CL Settings		5,6,7,8,9,10,11,13		nCK	
Supported CWL Settings			5,6,7,8,9		nCK	

17.3.1 Speed Bin Table Notes

Absolute Specification [T_{OPER} ; $V_{\text{DDQ}} = V_{\text{DD}} = 1.35\text{V}(1.28\text{V} \sim 1.45\text{V})$ & $1.5\text{V}(1.425\text{V} \sim 1.575\text{V})$];

NOTE :

1. The CL setting and CWL setting result in $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ and $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ requirements. When making a selection of $t_{\text{CK}}(\text{AVG})$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{\text{CK}}(\text{AVG})$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating $\text{CL} [\text{ns}] = t_{\text{AA}} [\text{ns}] / t_{\text{CK}}(\text{AVG}) [\text{ns}]$, rounding up to the next "Supported CL".
3. $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ limits: Calculate $t_{\text{CK}}(\text{AVG}) = t_{\text{AA}}_{\text{MAX}} / \text{CL SELECTED}$ and round the resulting $t_{\text{CK}}(\text{AVG})$ down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ corresponding to CL SELECTED.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. For devices supporting optional downshift to CL=7 and CL=9, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RP}}$ min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte 16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-1866(CL13) devices supporting downshift to DDR3-1600(CL11) or DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-2133(CL14) devices supporting downshift to DDR3-1866(CL13) or DDR3-1600(CL11) or DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). Once t_{RP} (Byte 20) is programmed to 13.125ns, t_{RCmin} (Byte 21,23) also should be programmed accordingly. For example, 49.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 36\text{ns} + 13.125\text{ns}$) for DDR3-1333(CL9) and 48.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 35\text{ns} + 13.125\text{ns}$) for DDR3-1600(CL11).
11. DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
12. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
13. For devices supporting optional down binning to CL=11, CL=9 and CL=7, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RPmin}}$ must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for t_{AAmin} (byte16), t_{RCDmin} (Byte18) and t_{RPmin} (byte20). Once t_{RP} (Byte20) is programmed to 13.125ns, t_{RCmin} (Byte21,23) also should be programmed accordingly. For example, 47.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 34\text{ns} + 13.125\text{ns}$)

18. Timing Parameters by Speed Grade

[Table 25] Timing Parameters by Speed Bin(Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OF F)	8	-	8	-	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table										ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	-70	70	-60	60	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	-70	70	-60	60	-50	50	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		140		120		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180		160		140		120		100		ps	
Cumulative error across 2 cycles	tERR(2per)	- 147	147	- 132	132	- 118	118	-103	103	-88	88	ps	
Cumulative error across 3 cycles	tERR(3per)	- 175	175	- 157	157	- 140	140	-122	122	-105	105	ps	
Cumulative error across 4 cycles	tERR(4per)	- 194	194	- 175	175	- 155	155	-136	136	-117	117	ps	
Cumulative error across 5 cycles	tERR(5per)	- 209	209	- 188	188	- 168	168	-147	147	-126	126	ps	
Cumulative error across 6 cycles	tERR(6per)	- 222	222	- 200	200	- 177	177	-155	155	-133	133	ps	
Cumulative error across 7 cycles	tERR(7per)	- 232	232	- 209	209	- 186	186	-163	163	-139	139	ps	
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	-169	169	-145	145	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	-175	175	-150	150	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	-180	180	-154	154	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	-184	184	-158	158	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	-188	188	-161	161	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max										ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing													
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	-	85	ps	13
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-800	400	-600	300	-500	250	-450	225	-390	195	ps	13,14, f
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	400	-	300	-	250	-	225	-	195	ps	13,14, f
Data setup time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels	1.35V												
	tDS(base) AC160	90	-	40	-	-	-	-	-	-	-	ps	d, 17
	tDS(base) AC135	140	-	90	-	45	-	25	-	-	-	ps	d, 17
	tDS(base) AC125	-	-	-	-	-	-	-	-	10	-	ps	d, 17
	1.5V												
	tDS(base) AC175	75	-	25	-	-	-	-	-	-	-	ps	d, 17
	tDS(base) AC150	125	-	75	-	30	-	10	-	-	-	ps	d, 17
	tDS(base) AC135	-	-	-	-	-	-	-	-	-	68	-	ps
Data hold time from DQS, $\overline{DQS}$ referenced to $V_{IH}(DC)V_{IL}(DC)$ levels	1.35V												
	tDH(base) DC90	160	-	110	-	75	-	55	-	30	-	ps	d, 17
	1.5V												
tDH(base) DC100	150	-	100	-	65	-	45	-	20	-	ps	d, 17	
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	320	-	ps	28

[Table 25] Timing Parameters by Speed Bin (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Data Strobe Timing													
DQS, $\overline{\text{DQS}}$ differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	NOTE 19	tCK(avg)	13, 19, g
DQS, $\overline{\text{DQS}}$ differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	NOTE 11	tCK(avg)	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	tQSH	0.38	-	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential output low time	tQSL	0.38	-	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS, $\overline{\text{DQS}}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	tDQSK	-400	400	-300	300	-255	255	-225	225	-195	195	ps	13,f
DQS, $\overline{\text{DQS}}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	-450	225	-390	195	ps	13,14,f
DQS, $\overline{\text{DQS}}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	-	195	ps	12,13,14
DQS, $\overline{\text{DQS}}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	29, 31
DQS, $\overline{\text{DQS}}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	30, 31
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.27	0.27	tCK(avg)	c
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)	c, 32
DQS, $\overline{\text{DQS}}$ falling edge hold time to CK, $\overline{\text{CK}}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)	c, 32
Command and Address Timing													
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5n s)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5 ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5n s)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 7.5 ns)	-		e, 18
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK, 15 ns)	-	max (12nCK, 15 ns)	-	max (12nCK, 15 ns)	-	max (12nCK, 15 ns)	-	max (12nCK, 15 ns)	-		
CAS to $\overline{\text{CAS}}$ command delay	tCCD	4	-	4	-	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))										nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin"										ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK, 10n s)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	max (4nCK, 5ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK, 10n s)	-	max (4nCK, 10n s)	-	max (4nCK, 7.5n s)	-	max (4nCK, 7.5 ns)	-	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	27	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	35	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to $V_{IH}(AC)$ / $V_{IL}(AC)$ levels	1.35V												
	tIS(base) AC160	215	-	140	-	80	-	60	-	-	-	ps	b, 16
	tIS(base) AC135	365	-	290	-	205	-	185	-	-	-	ps	b, 16, 27
	tIS(base) AC125	-	-	-	-	-	-	-	-	75	-	ps	b, 16, 27
	1.5V												
	tIS(base) AC175	200	-	125	-	65	-	45	-	-	-	ps	b, 16
	tIS(base) AC150	350	-	275	-	190	-	170	-	-	-	ps	b, 16, 27
	tIS(base) AC135	-	-	-	-	-	-	-	-	65	-	ps	b, 16
tIS(base) AC125	-	-	-	-	-	-	-	-	150	-	ps	b, 16, 27	

[Table 25] Timing Parameters by Speed Bin(Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing													
Command and Address hold time from CK, $\overline{CK}$ referenced to $V_{IH}(DC)$ / $V_{IL}(DC)$ levels	1.35V												
	tIH(base) DC90	285	-	210	-	150	-	130	-	110	-	ps	b,16
	1.5V												
	tIH(base) DC100	275		200		140		120	-	100	-	ps	b,16
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	560	-	535	-	ps	28
Calibration Timing													
Power-up and RESET calibration time	tZQinitl	512	-	512	-	512	-	512	-	max(512nCK,640ns)	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	256	-	max(256nCK,320ns)	-	nCK	
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	64	-	max(64nCK,80ns)	-	nCK	23
Reset Timing													
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-		
Self Refresh Timing													
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Power Down Timing													
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	max(3nCK, 6ns)	-	max(3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max(3nCK, 7.5ns)	-	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK(avg)	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing													
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	6	-	nCK	

[Table 25] Timing Parameters by Speed Bin

Speed		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ODT Timing													
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	-195	195	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing													
First DQS/DQS rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	tCK(avg)	3
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	tCK(avg)	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	tWLS	325	-	245	-	195	-	165	-	140	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	165	-	140	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	ns	

18.1 Jitter Notes

- Specific Note a** Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
- Specific Note b** These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/ $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note c** These parameters are measured from a data strobe signal (DQS, $\overline{DQS}$) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note d** These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, $\overline{DQS}$) crossing.
- Specific Note e** For these parameters, the DDR3 SDRAM device supports $t_{nPARAM} [nCK] = RU \{ t_{PARAM} [ns] / tCK(avg) [ns] \}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP} = RU \{ t_{RP} / tCK(avg) \}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support $t_{nRP} = RU \{ t_{RP} / tCK(avg) \} = 6$, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
- Specific Note f** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where $2 \leq m \leq 12$. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where $2 \leq n \leq 12$, and tERR(mper),act,max is the maximum measured value of tERR(nper) where $2 \leq n \leq 12$.
- Specific Note g** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

18.2 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation & Timing Diagram Datasheet"
8. For definition of RTT turn-off time tAOF see "Device Operation & Timing Diagram Datasheet".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See "Device Operation & Timing Diagram Datasheet".
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter 8 and chapter 9 for definition and measurement method.
15. tREFI depends on T_{OPER}
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{\text{CK}}$ differential slew rate, Note for DQ and DM signals, $V_{\text{REF}}(\text{DC}) = V_{\text{REFDQ}}(\text{DC})$. For input only pins except $\overline{\text{RESET}}$, $V_{\text{REF}}(\text{DC}) = V_{\text{REFCA}}(\text{DC})$. See "Address/Command Setup, Hold and Derating" on component datasheet.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{\text{DQS}}$ differential slew rate. Note for DQ and DM signals, $V_{\text{REF}}(\text{DC}) = V_{\text{REFDQ}}(\text{DC})$. For input only pins except $\overline{\text{RESET}}$, $V_{\text{REF}}(\text{DC}) = V_{\text{REFCA}}(\text{DC})$. See "Data Setup, Hold and Slew Rate Derating" on component datasheet.
18. Start of internal write transaction is defined as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation & Timing Diagram Datasheet"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation & Timing Diagram Datasheet".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
One method for calculating the interval between ZQCS commands, given the temperature (Tdrrate) and voltage (Vdrrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdrrate}) + (\text{VSens} \times \text{Vdrrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdrrate = 1°C / sec and Vdrrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

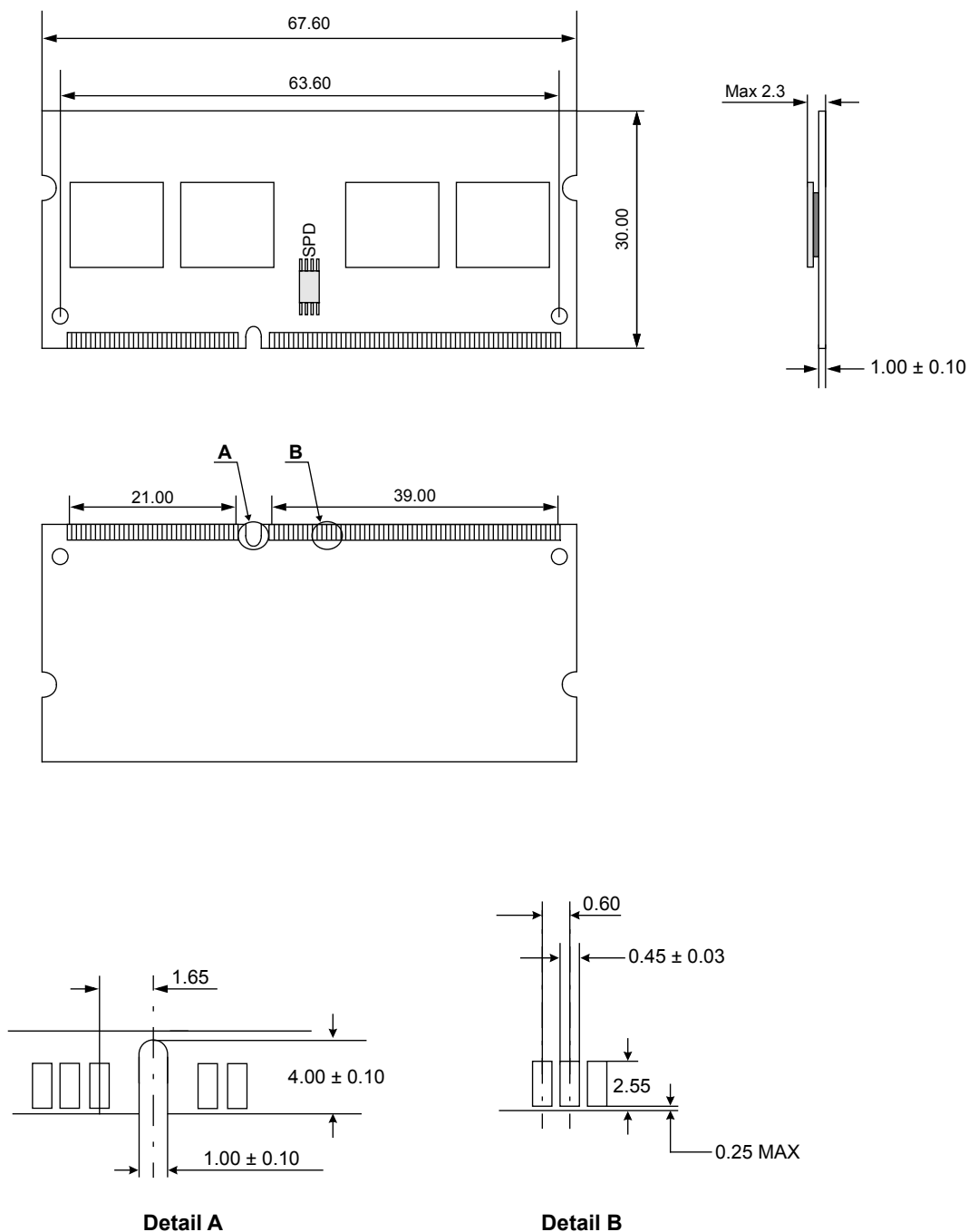
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of $V_{\text{REF}}(\text{DC})$ and the consecutive crossing of $V_{\text{REF}}(\text{DC})$
29. tDQSL describes the instantaneous differential input low pulse width on DQS- $\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS- $\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

19. Physical Dimensions :

19.1 256Mbx16 based 256Mx64 Module (1 Rank) - M471B5674EB0

Units : Millimeters

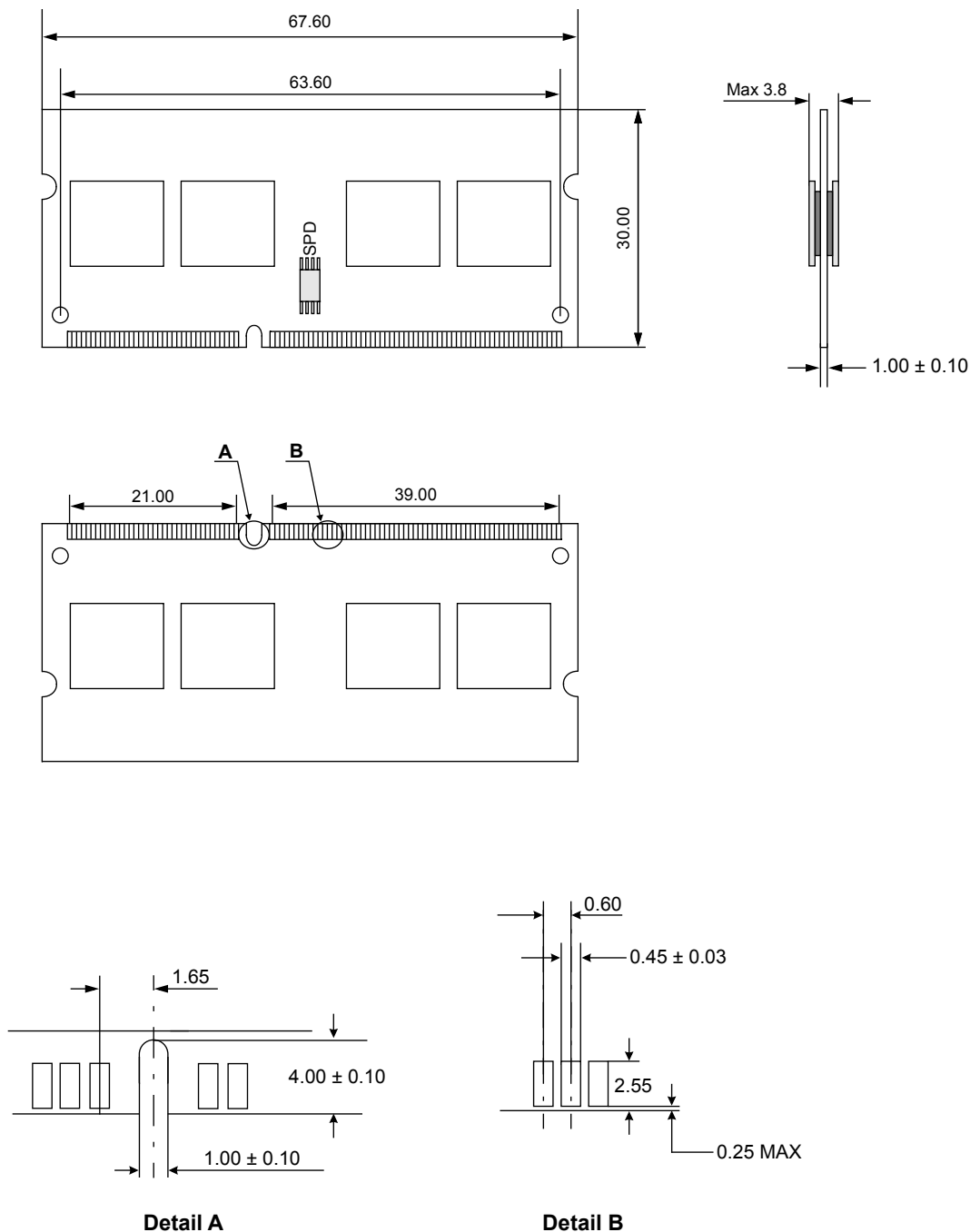


The used device is 256M x16 DDR3 SDRAM, Flip-Chip.
DDR3 SDRAM Part NO : K4B4G1646E - BY**

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

19.2 512Mbx8 based 512Mx64 Module (1 Rank) - M471B5173EB0

Units : Millimeters

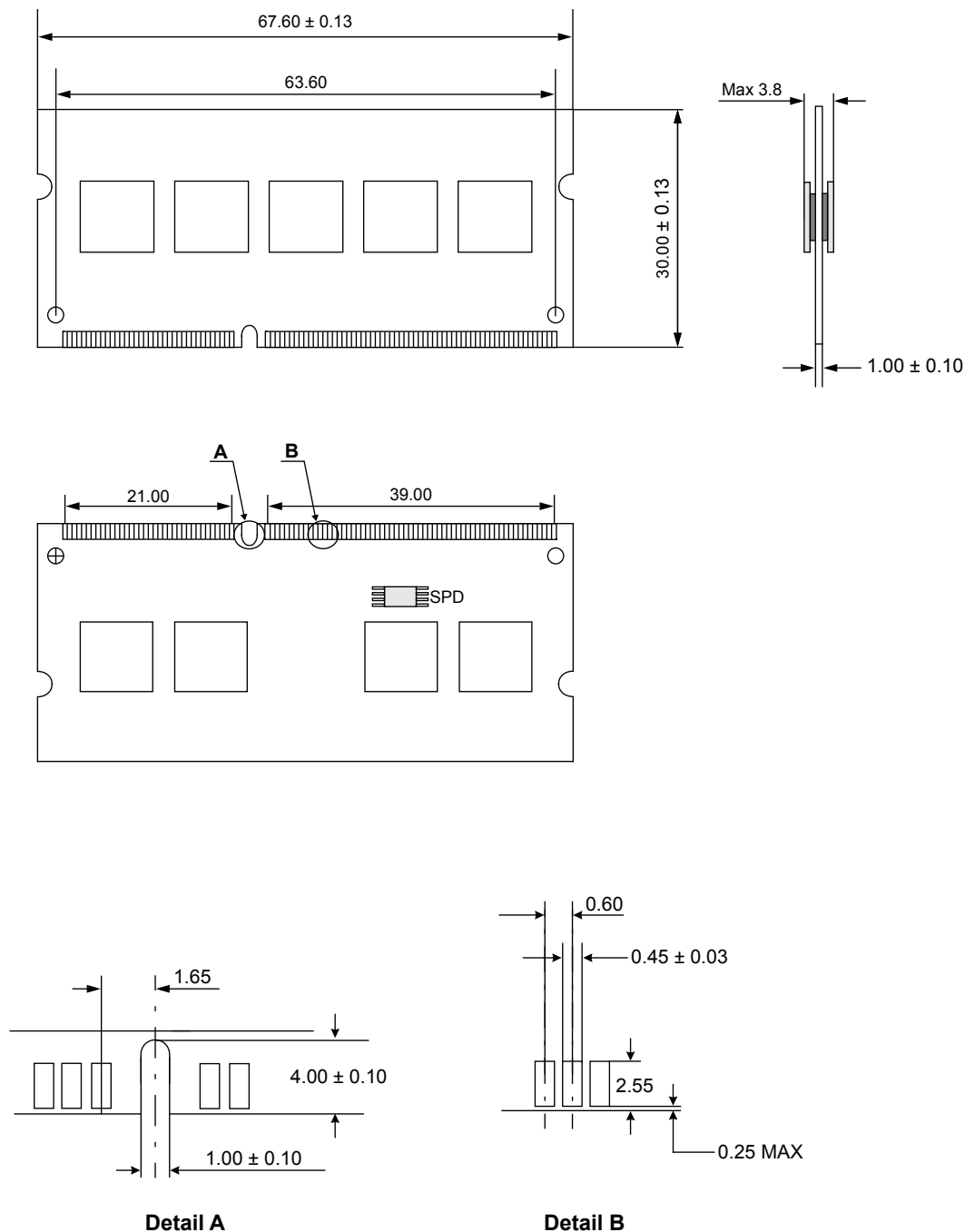


The used device is 512M x8 DDR3 SDRAM, Flip-Chip.
DDR3 SDRAM Part NO : K4B4G0846E - BY**

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

19.3 512Mbx8 based 512Mx72 Module (1 Rank) - M474B5173EB0

Units : Millimeters

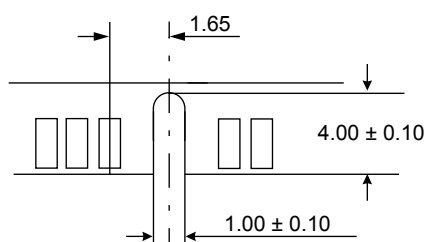
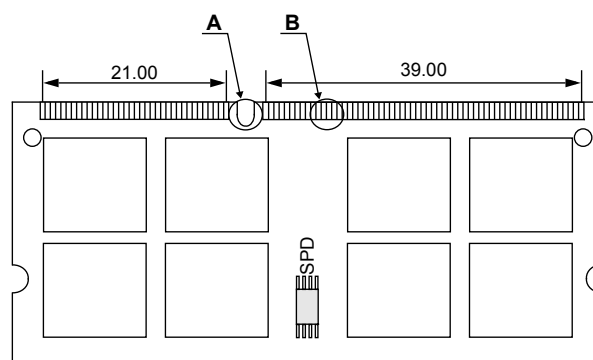
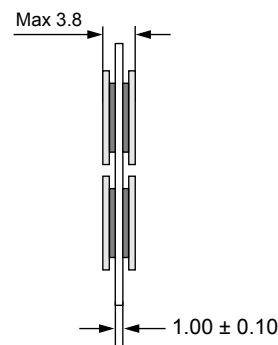
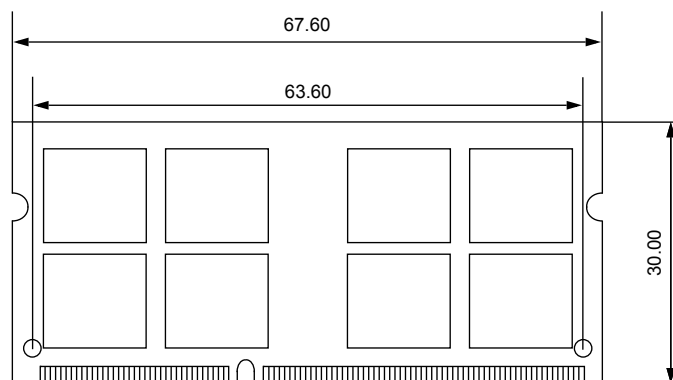


The used device is 512M x8 DDR3 SDRAM, Flip-Chip.
 DDR3 SDRAM Part NO : K4B4G0846E - BY**

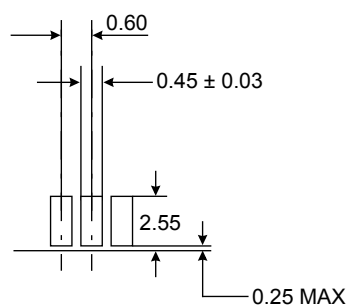
* NOTE : Tolerances on all dimensions ± 0.15 unless otherwise specified.

19.4 512Mx8 based 1Gx64 Module (2 Ranks) - M471B1G73EB0

Units : Millimeters



Detail A



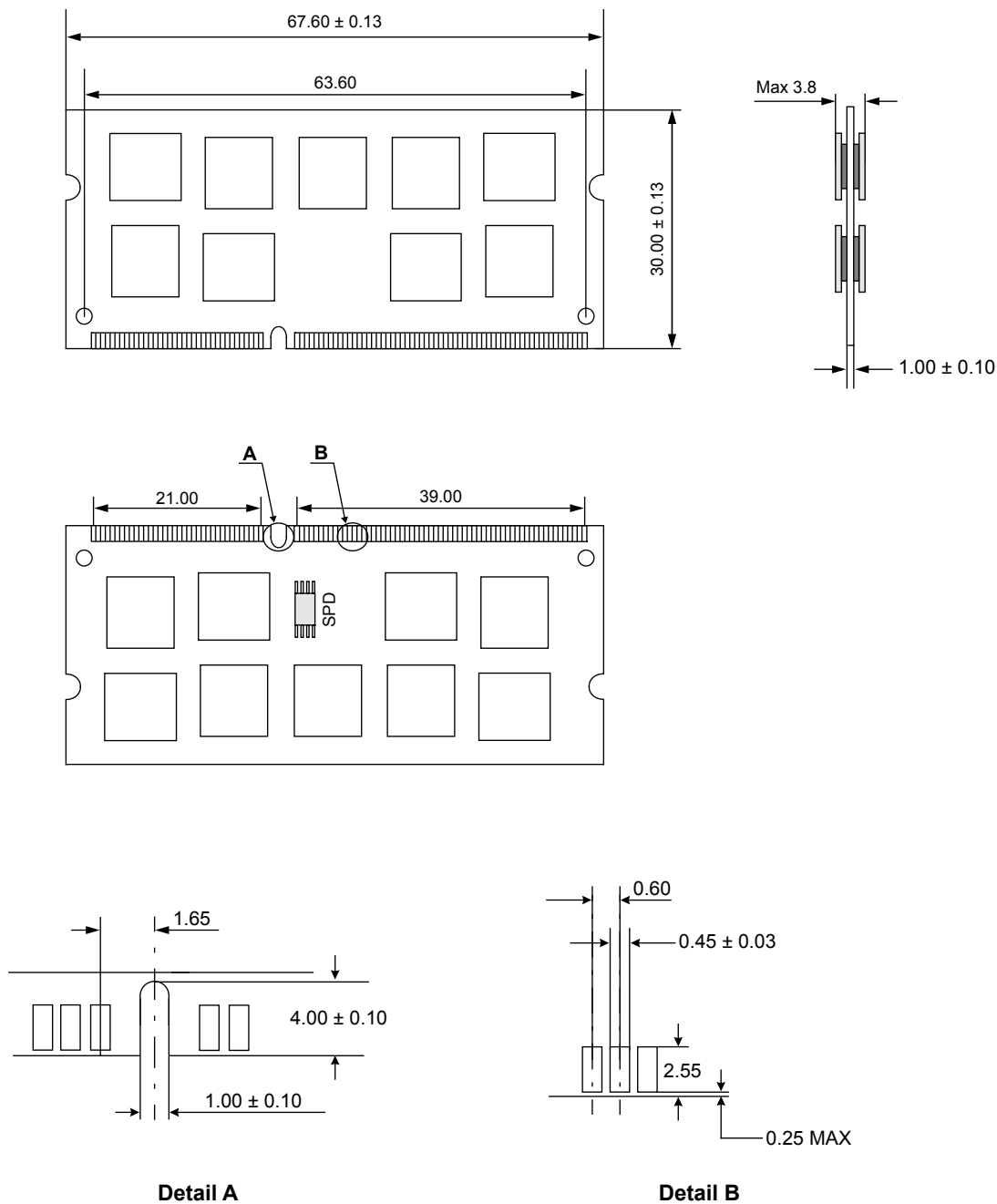
Detail B

The used device is 512M x8 DDR3 SDRAM, Flip-Chip.
DDR3 SDRAM Part NO : K4B4G0846E - BY**

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

19.5 512Mbx8 based 1Gx72 Module (2 Ranks) - M474B1G73EB0

Units : Millimeters



The used device is 512M x8 DDR3 SDRAM, Flip-Chip.
 DDR3 SDRAM Part NO : K4B4G0846E - BY**

* NOTE : Tolerances on all dimensions ± 0.15 unless otherwise specified.