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## PTP & SyncE Network Synchronizers with up to 5 Channels, 10 Inputs, 20 Outputs Product Brief

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### Features

#### Highlights

- Up to five independent clock channels
- Any-to-any frequency conversion per channel
- Inputs: up to 10, differential or single-ended
- Outputs: up to 10 differential, up to 20 CMOS
- Output jitter  $100 f_{s_{RMS}}$  typical for 156.25 MHz  
12 kHz to 20 MHz
- Core power consumption <0.9W
- MiToDSync™ 1-wire time-of-day interface in/out
- MiToDBasic™ 3-wire time-of-day interface out

#### Frequency and Phase over Packet Networks

- Packet and/or physical-layer frequency, phase and time synchronization
- Physical-layer compliance with ITU-T G.8262, G.8262.1, G.813, G.812, Telcordia GR-1244, GR-253
- Packet-timing compliance with ITU-T G.8261, G.8263, G.8273.2 (class A,B,C,D), G.8273.4
- Enables 5G wireless applications with sub-100 ns time/phase alignment requirements

#### Input Clocks

- Accepts up to 10 differential or CMOS inputs
- Any input frequency from 0.5 Hz to 1250 MHz
- Per-input activity and frequency monitoring
- Automatic or manual reference switching
- Revertive or nonrevertive switching
- Any input can be a 0.5 Hz to 8 kHz Sync input for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution

#### Up to 8 DPLLs

- Hitless reference switching
- High-resolution holdover averaging
- Per-DPLL phase adjustment, 1 ps resolution
- Programmable bandwidth, tracking range, phase-slope limiting, frequency-change limiting and other advanced features
- Locking to gapped-clock input signals
- Fast lock to 1 Hz inputs, 3 to 60 seconds, depending on test conditions

#### Output Clocks

- Any frequency 0.5 Hz to 750 MHz
- Each OUTP/N pair can be LVDS, LVPECL, 2xC-MOS, Low- $V_{CM}$ , or programmable differential
- In 2xC-MOS mode, the P and N pins can be different frequencies (e.g. 125 MHz and 25 MHz)
- VDD per output pair, CMOS voltages 1.8V to 3.3V
- Per-synth phase adjustment, 1 ps resolution
- Per-output duty cycle adjustment
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

#### Local Oscillator

- Operates from a single oscillator 9.72 MHz to 400 MHz
- Very-low-jitter applications can connect a TCXO or OCXO as the stability reference and a low-jitter XO as the jitter reference

#### General Features

- Automatic self-configuration at power-up from internal Flash memory, 7 configurations
- Input-to-output alignment <100 ps
- Numerically controlled oscillator behavior in each DPLL and each synthesizer
- Easy-to-configure design requires no external VCXO or loop filter components
- 5 GPIO pins with many possible behaviors, each REF can be GPI, each OUT can be GPO
- SPI or I<sup>2</sup>C processor Interface
- 1.8V and 3.3V core VDD voltages
- Easy-to-use evaluation/programming software

#### Applications

- Central system timing ICs for SyncE, SyncE+1588, routers, switches, OTN, and other carrier-grade systems
- Wireless base stations (3G, W-CDMA, 4G/LTE, LTE-A, 5G)
- Remote Radio Unit (RRU), Remote Access Networks (RAN), small cells, wireless backhaul, wireless repeaters

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## 1.0 BLOCK DIAGRAM

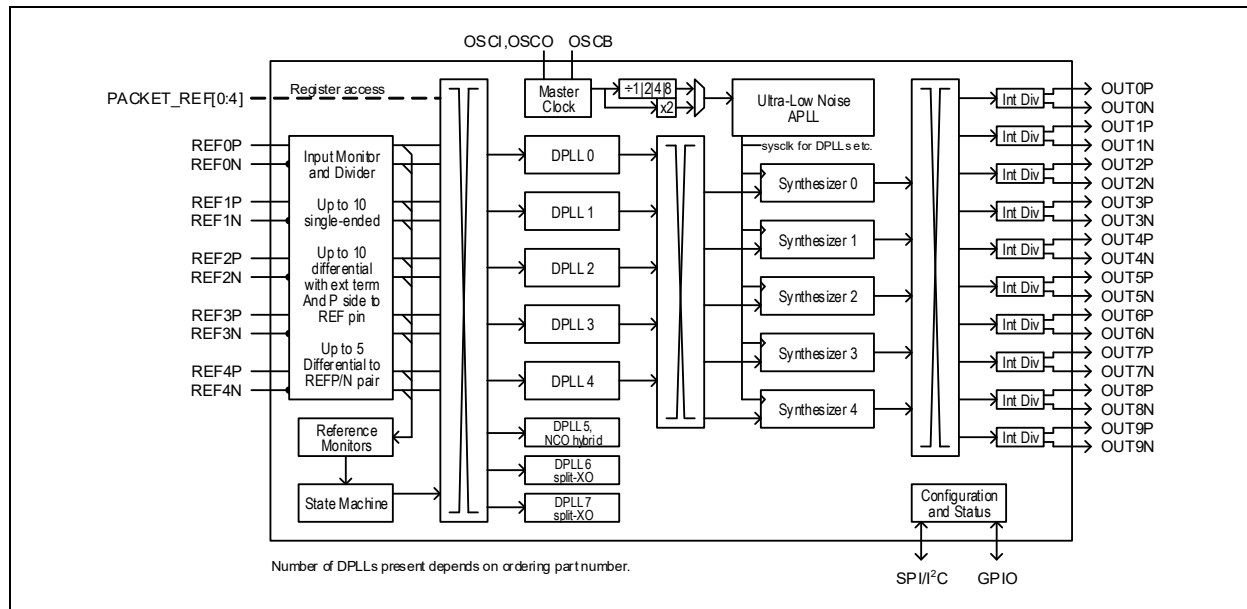


FIGURE 1-1: Functional Block Diagram.

## 2.0 APPLICATION EXAMPLE

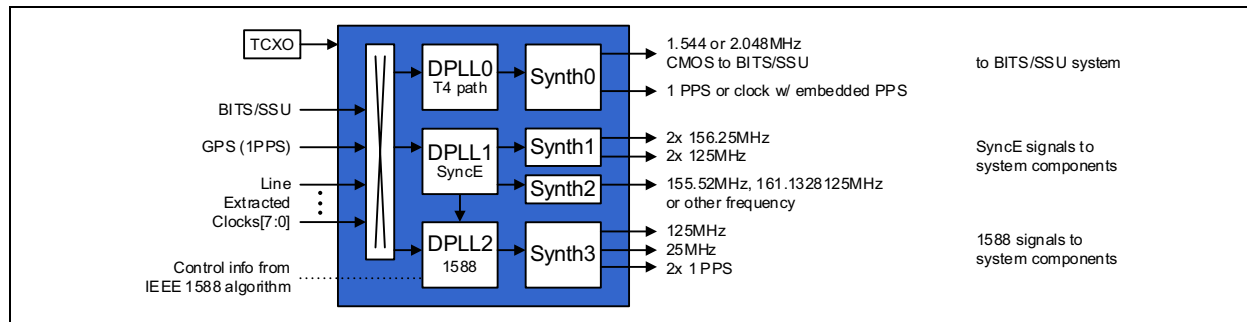


FIGURE 2-1: Synchronous Ethernet and IEEE 1588 Central Timing Application.

## 3.0 DETAILED FEATURES

### 3.1 General

- Up to five independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - $\geq 48$  MHz for lowest jitter
  - 9.72 MHz to 400 MHz total frequency range
- Configurable via SPI or I<sup>2</sup>C interface
- Internal nonvolatile memory
  - Factory-configurable power-on configuration
  - Multiple time writeable/re-writeable
- Default settings can be overridden using SPI/I<sup>2</sup>C

## 3.2 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair
- Any input can be a SYNC signal (0.5 Hz to 8 kHz) for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync signal (0.5 Hz to 1 kHz, duty cycle distortion for Sync)
- Any input can be a MiToDSync signal carrying one to three channels of frequency/phase/ToD information
- Input clocks can be any frequency from 0.5 Hz up to 1250 MHz (300 MHz max for CMOS inputs)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO or GPI assertion to react to LOS signals from PHYs
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution
- Each REF pin can be a GPI (general-purpose input)

## 3.3 DPLL Features

- Up to eight DPLLs: up to five for clock I/O channels, one for NCO-hybrid mode (SyncE assist), and two for locking to OCXOs for split-XO configuration
- Very high-resolution DPLL architecture
- State machine automatically transitions among freerun, tracking, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1 mHz to 470 Hz
- Less than 0.1 dB gain peaking
- Fast frequency/phase/time lock capability for 1PPS or clock+1PPS input references
- Programmable phase-slope limiting (PSL)
- Programmable frequency rate-of-change limiting (FCL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching
- Per-DPLL phase adjustment, 1 ps resolution
- High-resolution frequency and phase measurement (4e-15 and 1 ps)
- Fast detection of input clock failure and transition to holdover mode
- High-resolution holdover frequency averaging
  - Initial offset better than 10 ppb when using < 10 Hz filter
  - Initial offset better than 1 ppb when using < 0.1 Hz filter
  - Initial offset better than 0.1 ppb when using < 0.01 Hz filter
  - Initial offset better than 0.01 ppb when using < 0.001 Hz filter (translates to 864 ns over 24 hours)
- Supports holdover compensation for oscillator aging and temperature changes by learning oscillator characteristics during locked operation
- Time-of-Day registers: 48-bit seconds, 32-bit nanoseconds, writeable on input PPS edge

## 3.4 Synthesizer Features

- Five next-generation low-jitter, low-power, any-frequency synthesizers
- A total of five output frequency families
- Any-to-any frequency conversion with 0 ppm error
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Jitter suitable for OC-192, STM-64, and 1G, 10G, 40G, 100G, and 400G Ethernet jitter requirements

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## 3.5 Output Clock Features

- Up to 20 single-ended outputs, up to 10 differential outputs, from any synthesizer
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5 Hz to 750 MHz (250 MHz max for CMOS)
- Output jitter  $100 f_{s_{RMS}}$  typical for 156.25 MHz and many other frequencies (12 kHz to 20 MHz)
- In CMOS mode, the OUTxN frequency can be an integer divisor of the OUTxP frequency (Example 1: OUT3P 125 MHz, OUT3N 25 MHz. Example 2: OUT2P 25 MHz, OUT2N 1 Hz)
- Outputs directly interface (DC-coupled) with LVDS, LVPECL, HCSL, and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs, and other components
- Can produce PCIe Gen 1 to 5 clocks
- Each output pair can have clock plus embedded Sync signal (0.5 Hz to clock div 4)
- Each output pair can be MiToDSync signals carrying one to three channels of frequency/phase/ToD information
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1 ps resolution
- Per-output phase adjustment to accommodate trace delays or compensate for system routing paths
- Per-output duty cycle/pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)
- Each OUT pin can be a GPO (general-purpose output)
- Each OUT pin can be a MiToDBasic data signal which can be combined with a MHz clock output and a 4 kHz sync output to form a 3-wire MiToDBasic interface carrying one channel of frequency/phase/ToD information

## 3.6 Local Oscillator

- Operates from a single oscillator (jitter reference for the device). Acceptable frequencies: 9.72 MHz to 400 MHz. Best jitter:  $\geq 48$  MHz.
- Very-low-jitter applications can connect a TCXO or OCXO (any frequency, any output jitter) as the stability reference and a low-cost low-jitter XO as the jitter reference
- This ability to have separate jitter and stability references greatly reduces the cost of the TCXO or OCXO (no jitter requirement, no high-frequency-requirement) and allows reuse of already-qualified TCXO and OCXO components
- Supports redundant TCXOs or OCXOs connected to two REF pins

## 3.7 General Features

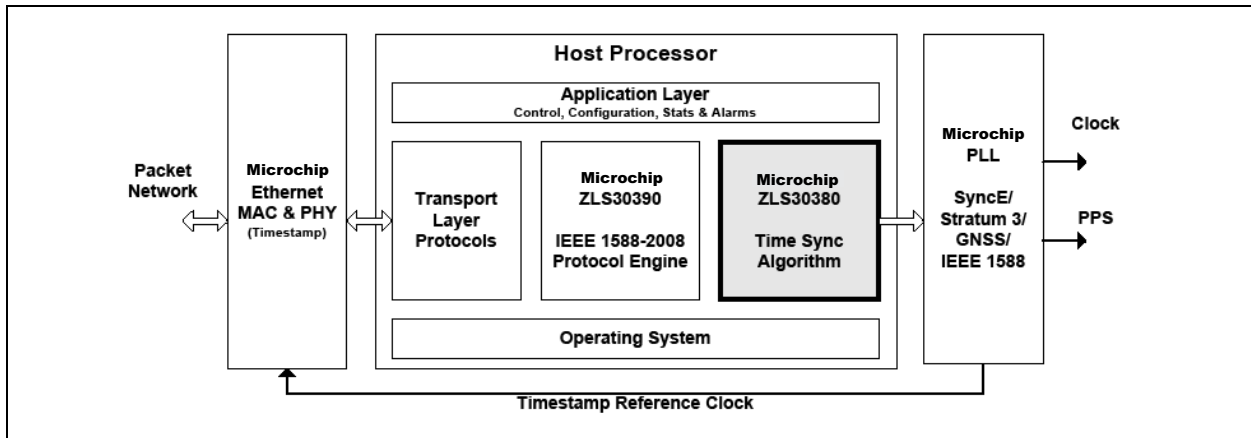
- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment  $< 200$  ps with external feedback
- Fast Ref-Sync locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Generates output SYNC signals: 1PPS (IEEE 1588), 2 kHz or 8 kHz (SONET/SDH), or other frequency
- JESD204B clocking: clock and SYSREF signal generation with skew adjustment
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or synthesizer frequency with resolution better than 0.005 ppt
- Spread-spectrum modulation available in each synthesizer (PCIe compliant)
- Five general-purpose I/O pins each with many possible status and control options
- SPI or I<sup>2</sup>C serial microprocessor interface

## 3.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts
- Works with or without an evaluation board

## 4.0 SOFTWARE FEATURES

The following figure shows the Time Synchronization Algorithm system environment. The subsections below list the features of the Time Synchronization Algorithm.



**FIGURE 4-1:** Time Synchronization Algorithm System Environment.

### 4.1 Time Synchronization Algorithm

The Time Synchronization Algorithm is responsible to accurately synchronize the local clock to a selected Server. The Time Synchronization Algorithm is synchronizing the Client to the Server to meet a variety of specifications or applications related to frequency accuracy (FFO), frequency (MTIE, TDEV), phase (1 Hz or 1PPS) and time (UTC & GNSS/GPS).

The Time Synchronization Algorithm can run on a variety of host processor architectures, whether embedded into an SoC or on a dedicated small scale CPU (such as Microchip's SmartFusion2 SoC FPGA). The Time Synchronization Algorithm interconnects with a wide array of software-programmable clock generators (such as Microchip's Network Synchronizer PLLs), protocol engines (such as Microchip's ZLS30390 IEEE 1588-2008 Protocol Engine), and underlying Ethernet MACs and PHYs that perform hardware timestamping.

### 4.2 End Application Target Performance

The Time Synchronization Algorithm is suitable for many end application targets, including:

- Frequency offset accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell, and macrocell applications, with target performance less than  $\pm 15$  ppb.
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC, and CES interface specifications.
- Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD, LTE-A, LTE-A Pro, and 5G NR femtocell, small cell (residential, urban, rural, enterprise), picocell, and macrocell applications with target performance less than  $\pm 1$   $\mu$ s phase alignment.
- Time Synchronization for TAI, UTC-traceability, and GNSS/GPS replacement.

### 4.3 Packet Networks

The Time Synchronization Algorithm is suitable for high performance over a variety of packet networks including:

- ITU-T G.8261 Appendix VI
- ITU-T G.8261.1 network limit compliant
- ITU-T G.8271.1 network limit compliant without SyncE
- ITU-T G.8271.2 network limit compliant
- Native Ethernet (switched) & IP (routed) networks
- xDSL
- Microwave
- Fully aware, partially aware, and unaware timing supported networks

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- Networks including intermediate Boundary Clocks and Transparent Clocks
- Networks with and without SyncE or frequency physical layer support

## 4.4 Clock Specifications

The Time Synchronization Algorithm meets the performance requirements from ITU-T packet clock specifications, or draft packet clock specifications, including:

- ITU-T G.8261 Appendix VI
- ITU-T G.8263 PEC-S
- ITU-T G.8273.2 T-BC full on-path without SyncE
- ITU-T G.8273.2 T-BC full on-path with SyncE
- ITU-T G.8273.2 T-TSC full on-path without SyncE
- ITU-T G.8273.2 T-TSC full on-path with SyncE
- ITU-T G.8273.4 T-BC-A (draft)
- ITU-T G.8273.4 T-BC-P (draft)
- ITU-T G.8273.4 T-TSC-A (draft)
- ITU-T G.8273.4 T-TSC-P (draft)

## 4.5 Profiles

The Time Synchronization Algorithm is suitable for use in a wide variety of markets and applications, including the following IEEE 1588-2008 Profiles:

- IEEE 1588 Annex J.3 Delay Request-Response Default Profile (2008)
- IEEE 1588 Annex J.4 Peer-to-peer Default Profile (2008)
- ITU-T G.8265.1 Telecom Profile for Frequency Synchronization (Edition 1)
- ITU-T G.8275.1 Telecom Profile for Phase with Full Timing Support Networks (Edition 1)
- ITU-T G.8275.1 Telecom Profile for Phase with Full Timing Support Networks (Edition 2)
- ITU-T G.8275.2 Telecom Profile for Phase with Partial Timing Support Networks (Edition 1)
- CableLabs CM-SP-RDTI Remote DTI Profile (Edition I0x)
- AES 67 Standard for Audio Applications of Networks – High-Performance Streaming Audio-over-IP interoperability: PTP Profile for Media Applications
- SMPTE 2059-2 Profile for Use of IEEE-1588 Precision Time Protocol in Professional Broadcast Applications
- AES R16 Project Report – PTP parameters for AES67 and SMPTE ST 2059-2 interoperability
- IEEE C37.238 Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications (Edition 2011)
- IEEE C37.238 Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications (Edition 2017)
- IEC 61850-9-3 Precision time protocol profile for power utility automation (Edition 1.0)
- IEC 62439-3 PTP profiles for high-availability automation networks (Edition 3.0)
- IEEE802.1as AVB-TSN gPTP
- IEEE 1588-2018 Annex J.5 High Accuracy Profile (based on White Rabbit)
- IETF TICTOC Enterprise Profile

## 4.6 Monitoring & Redundancy

The Time Synchronization Algorithm includes monitoring and redundancy for high availability synchronization, including:

- Synchronization to the best available server
- Client monitoring of secondary server references
  - Monitoring includes full time synchronization reporting of secondary server
  - Supports a programmable number of secondary server connections
- Hitless reference switching between multiple servers
- Holdover when server packet connectivity is lost
- TIE-clear option to build out, or clear, phase offsets between server references

## 4.7 General

The Time Synchronization Algorithm includes many advanced features to aide in the high-accuracy & high-stability applications, including:

- Full PLL state machine (Freerun, Holdover, Frequency Lock Acquiring, Frequency Lock Acquired, Phase Lock Acquired), with programmable thresholds for state transitions
- Programmable, non-linear packet selection with PDV suppression
- Programmable bandwidth configurability from sub-mHz to 100s of mHz.
- Programmable packet rates from 1 packet/second to over 128 packets/second
- Programmable phase slope limiting, down to 1 ns/s
- Programmable frequency change limiting, down to 1 ppb/s
- Warm-start to initialize or seed the Time Synchronization Algorithm from a stored or last-known-good frequency offset to improve convergence
- Programmable thresholds for management of phase errors: when to adjust with frequency offsets and when to adjust with phase jumps
- User ability to manually add frequency offsets due to temperature or aging (especially during holdover state)

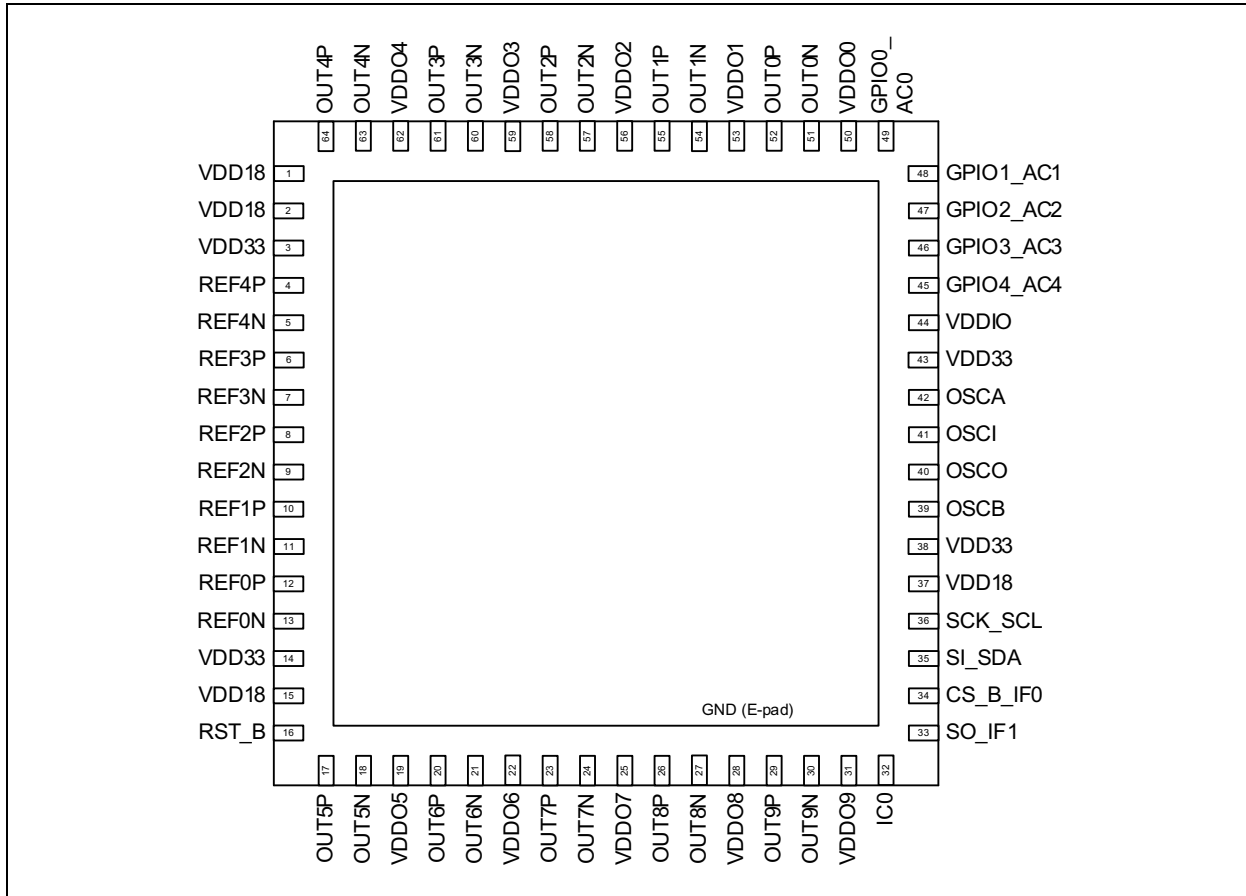
## 4.8 Reporting

The Time Synchronization Algorithm includes user reporting to aide in performance debugging, including:

- Set of user notifications about packet network events, such as packet loss, small transient phase jumps, large transient phase jumps, outliers, network path re-routes
- Set of metrics related to the synchronization, such as frequency stability and phase stability
- Independent reporting of the forward path and reverse path lock status
- Oscillator stability analysis for excessive aging or temperature variation
- Server tracking impairments such as pull-in range exceeded

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## 5.0 PIN DIAGRAM



**FIGURE 1:** 64-Lead 9 mm x 9 mm VQFN (0.5 mm pitch) for ZL30731, ZL30732, ZL30733, ZL30734, ZL30735.



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