ADC08D500 High Performance, Low Power, Dual 8-Bit, 500 MSPS A/D Converter

Check for Samples: ADC08D500

FEATURES

- **Internal Sample-and-Hold**
- **Single +1.9V ±0.1V Operation**
- **Choice of SDR or DDR Output Clocking**
- **Interleave Mode for 2x Sampling Rate**
- **Multiple ADC Synchronization Capability**
- **Ensured No Missing Codes**
- **Serial Interface for Extended Control**
- **Fine Adjustment of Input Full-Scale Range and Offset**
- **Duty Cycle Corrected Sample Clock**

APPLICATIONS

- **Direct RF Down Conversion**
- **Digital Oscilloscopes**
- **Satellite Set-Top Boxes**
- **Communications Systems**
- **Test Instrumentation**

KEY SPECIFICATIONS

- **Resolution 8 Bits**
- **Max Conversion Rate 500 MSPS (min)**
- **Bit Error Rate 10^{-18} (typ)**
- **ENOB @ 250 MHz Input 7.5 Bits (typ)**
- **DNL ±0.15 LSB (typ)**
- **Power Consumption**
  - **Operating 1.4 W (typ)**
  - **Power Down Mode 3.5 mW (typ)**

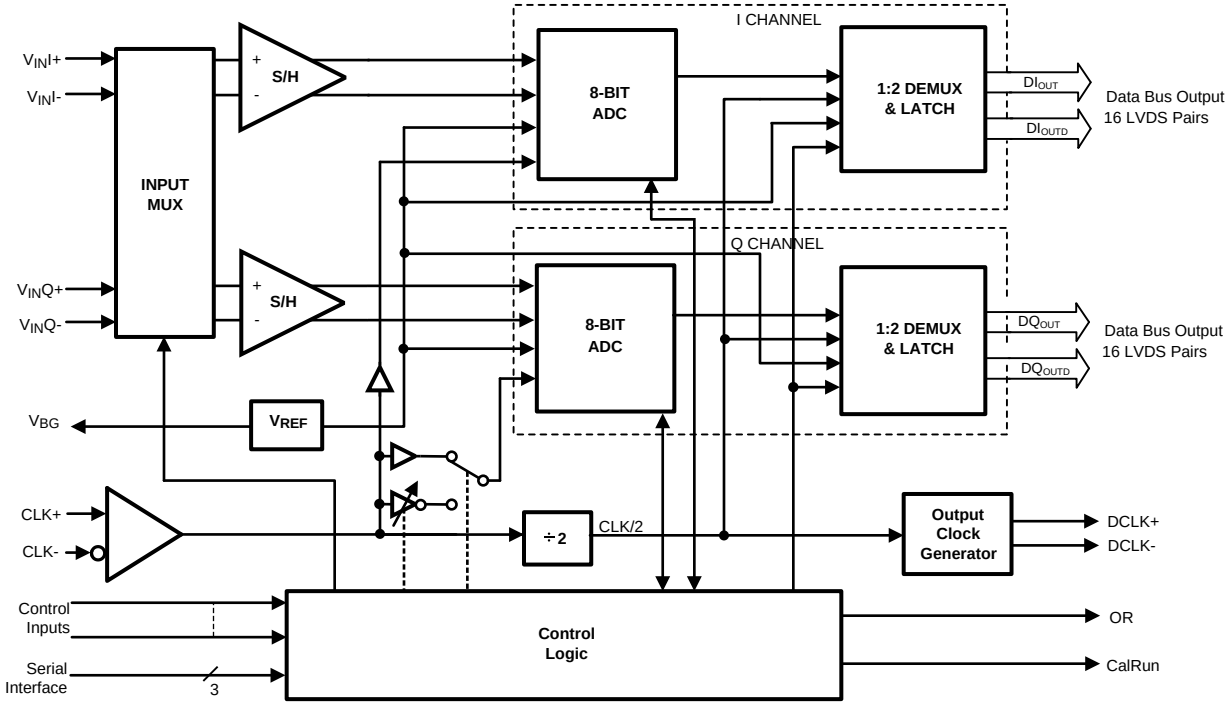
DESCRIPTION

The ADC08D500 is a dual, low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 500 MSPS. Consuming a typical 1.4 Watts at 500 MSPS from a single 1.9 Volt supply, this device is ensured to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.5 ENOB with a 250 MHz input signal and a 500 MHz sample rate while providing a 10^{-18} B.E.R. Output formatting is offset binary and the LVDS digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V.

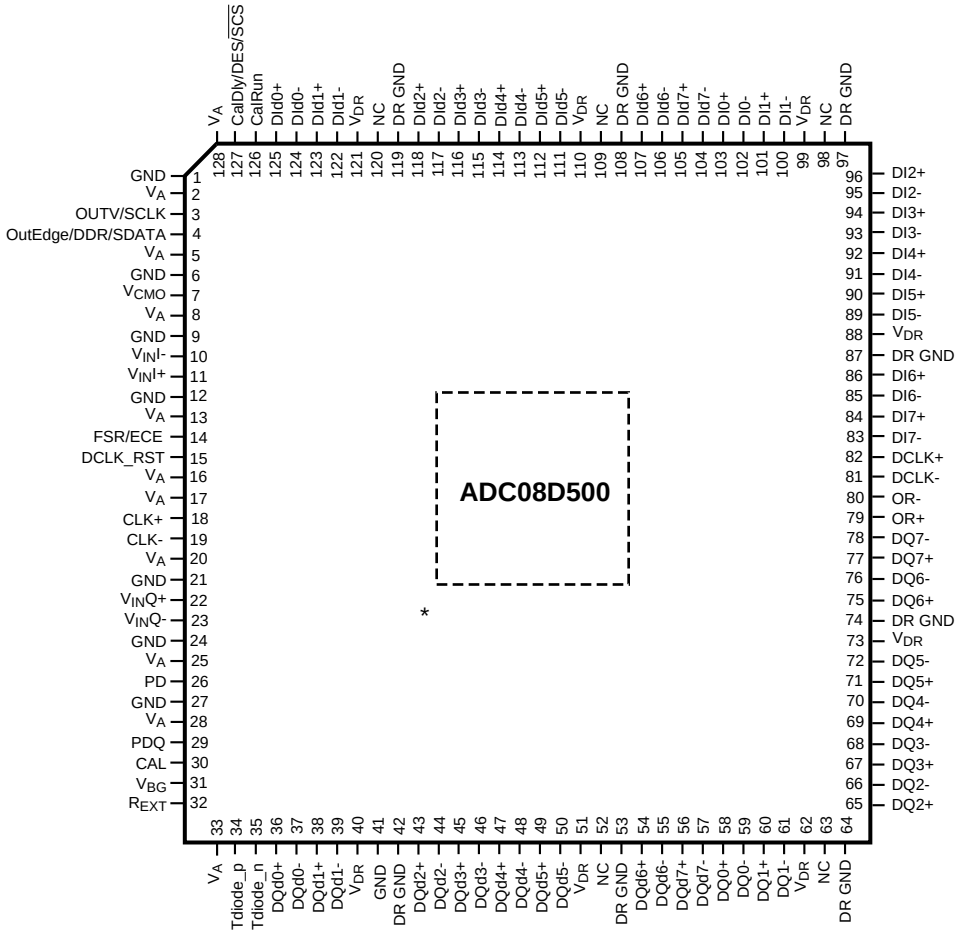
Each converter has a 1:2 demultiplexer that feeds two LVDS buses and reduces the output data rate on each bus to half the sampling rate. The two converters can be interleaved and used as a single 1 GSPS ADC.

The converter typically consumes less than 3.5 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad HLQFP and operates over the Industrial ($-40°C \le T_A \le +85°C$) temperature range.

Block Diagram

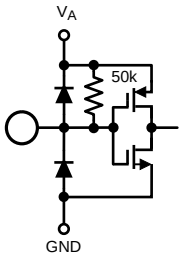
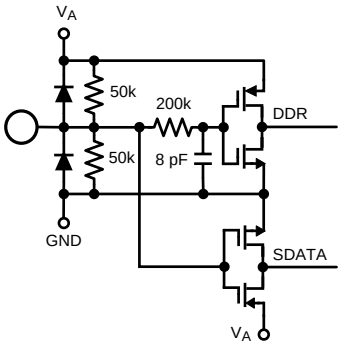
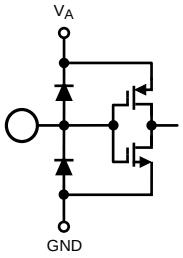
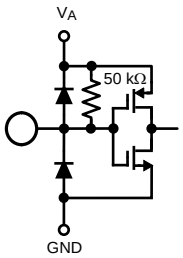
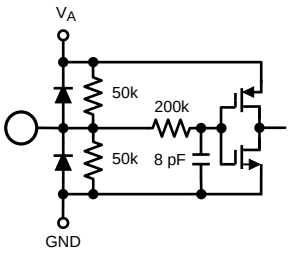


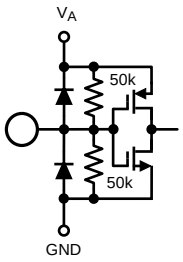
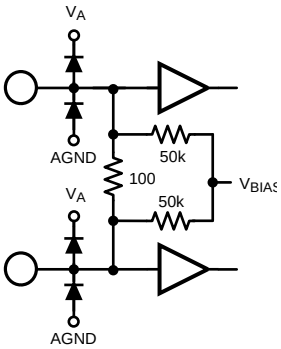
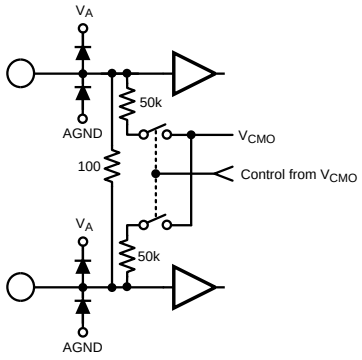
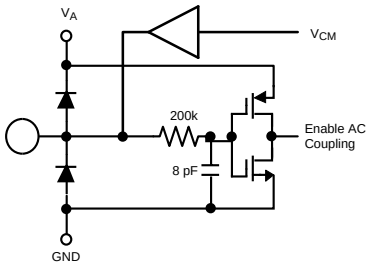
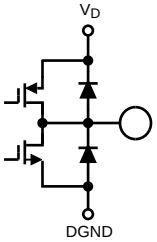
Pin Configuration

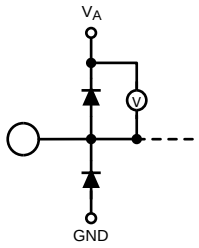
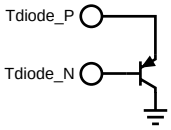
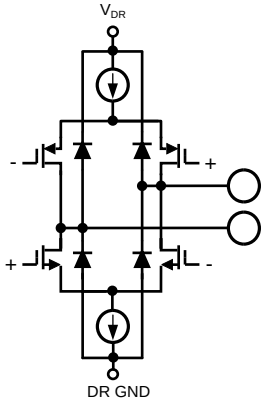


* Exposed pad on back of package must be soldered to ground plane to ensure rated performance.

Pin Descriptions and Equivalent Circuits

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
3	OutV / SCLK		Output Voltage Amplitude and Serial Interface Clock. Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. See The LVDS Outputs. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface.
4	OutEdge / DDR / SDATA		DCLK Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the output edge of DCLK+ at which the output data transitions. (See OutEdge Setting). When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface.
15	DCLK_RST		DCLK Reset. A positive pulse on this pin is used to reset and synchronize the DCLK outs of multiple converters. See MULTIPLE ADC SYNCHRONIZATION for detailed description.
26	PD		Power Down Pins. A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL		Calibration Cycle Initiate. A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the self calibration sequence. See Self Calibration for an overview of self-calibration and On-Command Calibration for a description of on-command calibration.
29	PDQ		A logic high on the PDQ pin puts only the "Q" ADC into the Power Down mode.
14	FSR/ECE		Full Scale Range Select and Extended Control Enable. In non-extended control mode, a logic low on this pin sets the full-scale differential input range to 650 mV_{P-P}. A logic high on this pin sets the full-scale differential input range to 870 mV_{P-P}. See The Analog Inputs. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. See NORMAL/EXTENDED CONTROL for information on the extended control mode.

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
127	CalDly / DES / $\overline{SCS}$		Calibration Delay, Dual Edge Sampling and Serial Interface Chip Select. With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of clock cycles after power up before calibration begins (See Self-Calibration). With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes 0b (short delay with no provision for a long power-up calibration delay). When this pin is floating or connected to a voltage equal to $V_A/2$, DES (Dual Edge Sampling) mode is selected where the "I" input is sampled at twice the clock rate and the "Q" input is ignored. See Dual-Edge Sampling.
18 19	CLK+ CLK-		LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+. See Acquiring the Input for a description of acquiring the input and THE CLOCK INPUTS for an overview of the clock inputs.
11 10 . 22 23	$V_{IN}I+$ $V_{IN}I-$. $V_{IN}Q+$ $V_{IN}Q-$		Analog signal inputs to the ADC. The differential full-scale input range is 650 mV_{P-P} when the FSR pin is low, or 870 mV_{P-P} when the FSR pin is high.
7	V_{CMO}		Common Mode Voltage. This pin is the common mode output in d.c. coupling mode and also serves as the a.c. coupling mode select pin. When d.c. coupling is used, the voltage output at this pin is required to be the common mode input voltage at $V_{IN}+$ and $V_{IN}-$ when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog inputs. This pin is capable of sourcing or sinking 100 µA. See THE ANALOG INPUT.
31	V_{BG}		Bandgap output voltage capable of 100 µA source/sink.
126	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running.

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
32	R_{EXT}		External bias resistor connection. Nominal value is 3.3k-Ohms (±0.1%) to ground. See Self-Calibration.
34 35	Tdiode_P Tdiode_N		Temperature Diode Positive (Anode) and Negative (Cathode). These pins may be used for die temperature measurements, however no specified accuracy is implied or ensured. Noise coupling from adjacent output data signals has been shown to affect temperature measurements using this feature. See Thermal Management.
83 / 78 84 / 77 85 / 76 86 / 75 89 / 72 90 / 71 91 / 70 92 / 69 93 / 68 94 / 67 95 / 66 96 / 65 100 / 61 101 / 60 102 / 59 103 / 58	DI7− / DQ7− DI7+ / DQ7+ DI6− / DQ6− DI6+ / DQ6+ DI5− / DQ5− DI5+ / DQ5+ DI4− / DQ4− DI4+ / DQ4+ DI3− / DQ3− DI3+ / DQ3+ DI2− / DQ2− DI2+ / DQ2+ DI1− / DQ1− DI1+ / DQ1+ DI0− / DQ0− DI0+ / DQ0+		I and Q channel LVDS Data Outputs that are not delayed in the output demultiplexer. Compared with the DId and DQd outputs, these outputs represent the later time samples. These outputs should always be terminated with a 100Ω differential resistor.
104 / 57 105 / 56 106 / 55 107 / 54 111 / 50 112 / 49 113 / 48 114 / 47 115 / 46 116 / 45 117 / 44 118 / 43 122 / 39 123 / 38 124 / 37 125 / 36	DId7− / DQd7− DId7+ / DQd7+ DId6− / DQd6− DId6+ / DQd6+ DId5− / DQd5− DId5+ / DQd5+ DId4− / DQd4− DId4+ / DQd4+ DId3− / DQd3− DId3+ / DQd3+ DId2− / DQd2− DId2+ / DQd2+ DId1− / DQd1− DId1+ / DQd1+ DId0− / DQd0− DId0+ / DQd0+		I and Q channel LVDS Data Outputs that are delayed by one CLK cycle in the output demultiplexer. Compared with the DI/DQ outputs, these outputs represent the earlier time sample. These outputs should always be terminated with a 100Ω differential resistor.
79 80	OR+ OR-		Out Of Range output. A differential high at these pins indicates that the differential input is out of range (outside the range ±325 mV or ±435 mV as defined by the FSR pin).
82 81	DCLK+ DCLK-		Differential Clock outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. This signal is at 1/2 the input clock rate in SDR mode and at 1/4 the input clock rate in the DDR mode. The DCLK outputs are not active during a calibration cycle, therefore this is not recommended as a system clock.
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		Analog power supply pins. Bypass these pins to ground.

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
40, 51 ,62, 73, 88, 99, 110, 121	V_{DR}		Output Driver power supply pins. Bypass these pins to DR GND.
1, 6, 9, 12, 21, 24, 27, 41	GND		Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		Ground return for V_{DR}.
52, 63, 98, 109, 120	NC		No Connection. Make no connection to these pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_A, V_{DR})		2.2V
Supply Difference V_{DR} - V_A		0V to 100 mV
Voltage on Any Input Pin (Except V_{IN}+, V_{IN}-)		−0.15V to (V_A +0.15V)
Voltage on V_{IN}+, V_{IN}- (Maintaining Common Mode)		-0.15V to 2.5V
Ground Difference |GND - DR GND|		0V to 100 mV
Input Current at Any Pin (3)		±25 mA
Package Input Current (3)		±50 mA
Power Dissipation at T_A = 85°C		2.0 W
ESD Susceptibility (4)	Human Body Model	2500V
	Machine Model	250V
Soldering Temperature, Infrared, 10 seconds		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no ensure of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.
(4) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Operating Ratings (1) (2)

Ambient Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±50mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no ensure of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Operating Ratings (1) (2) (continued)

V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	0V to 2.15V (100% duty cycle) 0V to 2.5V (10% duty cycle)
Ground Difference (|GND - DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

Package Thermal Resistance (1)

Package	θ_{JA}	$\theta_{JC\ (Top\ of\ Package)}$	$\theta_{J\text{-}PAD\ (Thermal\ Pad)}$
128-Lead Exposed Pad HLQFP	25°C / W	10°C / W	2.8°C / W

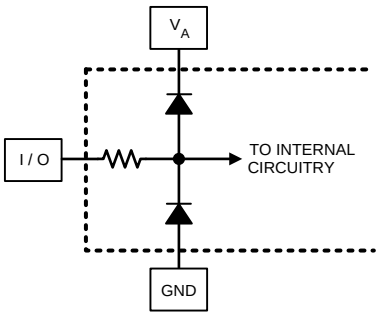
(1) *Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to* www.ti.com/packaging.

Converter Electrical Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity	DC Coupled, 1MHz Sine Wave Over ranged	±0.3	**±0.9**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Over ranged	±0.15	**±0.6**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		-0.45	**−1.5** **0.5**	LSB (min) LSB (max)
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error (4)		−0.6	**±25**	mV (max)
NFSE	Negative Full-Scale Error (4)		−1.31	**±25**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS
NORMAL MODE (non DES) DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth	Normal (non DES) Mode	1.7		GHz

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(2) To ensure accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).
(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Figure 2. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
B.E.R.	Bit Error Rate		10^{-18}		Error/Sample
	Gain Flatness	d.c. to 500 MHz	±0.5		dBFS
ENOB	Effective Number of Bits	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	7.5		Bits
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	7.5	**7.1**	Bits (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	7.5	**7.1**	Bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	47		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	47	**44.5**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	47	**44.5**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	48		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	48	**45.3**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	47.5	**45.3**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	-55		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	-55	**−47.5**	dB (max)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	-55	**−47.5**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	−65		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	−65		dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−65		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 50 MHz, V_{IN} = FSR − 0.5 dB	55		dB
		f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	55	**47.5**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	55	**47.5**	dB (min)
IMD	Intermodulation Distortion	f_{IN1} = 121 MHz, V_{IN} = FSR − 7 dB f_{IN2} = 126 MHz, V_{IN} = FSR − 7 dB	-50		dB
	Out of Range Output Code (In addition to OR Output high)	(V_{IN}+) − (V_{IN}−) > + Full Scale		**255**	
		(V_{IN}+) − (V_{IN}−) < − Full Scale		**0**	
INTERLEAVE MODE (DES Pin 127=Float) - DYNAMIC CONVERTER CHARACTERISTICS					
FPBW (DES)	Full Power Bandwidth	Dual Edge Sampling Mode	900		MHz
ENOB	Effective Number of Bits	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	7.4	**7.0**	Bits (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	7.4	**7.0**	Bits (min)
SINAD	Signal to Noise Plus Distortion Ratio	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	46.3	**43.9**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	46.3	**43.9**	dB (min)
SNR	Signal to Noise Ratio	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	46.7	**44.1**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	46.7	**44.1**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	-58	**-49**	dB (min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	-58	**-49**	dB (min)
2nd Harm	Second Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	-60		dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	-60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR − 0.5 dB	-64		dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	-64		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	57	**47**	dB(min)
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	57	**47**	dB dB (min(min)

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low	650	**570**	mV_{P-P} (min)
				730	mV_{P-P} (max)
		FSR pin 14 High	870	**790**	mV_{P-P} (min)
				950	mV_{P-P} (max)
V_{CMI}	Analog Input Common Mode Voltage		V_{CMO}	**V_{CMO} − 50** **V_{CMO} + 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance, Normal operation (5) (6)	Differential	0.02		pF
		Each input pin to ground	1.6		pF
	Analog Input Capacitance, DES Mode (5) (6)	Differential	0.08		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**94**	Ω (min)
				106	Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage		1.26	**0.95** **1.45**	V (min) V (max)
V_{CMO_LVL}	V_{CMO} input threshold to set DC Coupling mode	V_A = 1.8V	0.60		V
		V_A = 2.0V	0.66		V
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = −40°C to +85°C	118		ppm/°C
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance			80	pF
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.20** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −40°C to +85°C, I_{BG} = ±100 µA	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference Load Capacitance			80	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25°C	71.23		mV
		192 µA vs. 12 µA, T_J = 85°C	85.54		mV
CHANNEL-TO-CHANNEL CHARACTERISTICS					
	Offset Error Match		1		LSB
	Positive Full-Scale Error Match	Zero offset selected in Control Register	1		LSB
	Negative Full-Scale Error Match	Zero offset selected in Control Register	1		LSB
	Phase Matching (I, Q)	F_{IN} = 1.0 GHz	< 1		Degree
X-TALK	Crosstalk from I (Aggressor) to Q (Victim) Channel	Aggressor = 867 MHz F.S. Victim = 100 MHz F.S.	−71		dB
X-TALK	Crosstalk from Q (Aggressor) to I (Victim) Channel	Aggressor = 867 MHz F.S. Victim = 100 MHz F.S.	-71		dB

(5) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(6) This parameter is specified by design and is not tested in production.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
CLOCK INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0 or $V_{IN} = V_A$	±1		µA
C_{IN}	Input Capacitance (7) (8)	Differential	0.02		pF
		Each input to ground	1.5		pF
DIGITAL CONTROL PIN CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	See (9)		**0.85 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	See (9)		**0.15 x V_A**	V (max)
C_{IN}	Input Capacitance (8) (10)	Each input to ground	1.2		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OD}	LVDS Differential Output Voltage	Measured differentially, OutV = V_A, V_{BG} = Floating, (11)	710	**400**	mV_{P-P} (min)
				920	mV_{P-P} (max)
		Measured differentially, OutV = GND, V_{BG} = Floating, (11)	510	**280**	mV_{P-P} (min)
				720	mV_{P-P} (max)
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage, see Figure 1	V_{BG} = Floating	800		mV
V_{OS}	Output Offset Voltage, see Figure 1	$V_{BG} = V_A$ (11)	1200		mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output- connected to 0.8V	−4		mA
Z_O	Differential Output Impedance		100		Ohms
V_{OH}	Cal_Run High level output	I_{OH} = -400uA (9)	1.65	**1.5**	V
V_{OL}	Cal_Run Low level output	I_{OH} = 400uA (9)	0.15	**0.3**	V
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High	561 340 1.8	**665** **408**	mA (max) mA mA
I_{DR}	Output Driver Supply Current	PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High	200 112 0.012	**275** **157**	mA (max) mA (max) mA
P_D	Power Consumption	PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High	1.4 0.8 3.5	**1.78** **1.0**	W (max) W mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in Full Scale Error with change in V_A from 1.8V to 2.0V	30		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, $50mV_{P-P}$ riding on V_A	51		dB

(7) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(8) This parameter is specified by design and is not tested in production.
(9) This parameter is specified by design and/or characterization and is not tested in production.
(10) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(11) Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions		Typical (3)	Limits (3)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS						
f_{CLK1}	Maximum Input Clock Frequency	Normal Mode (non DES) or DES Mode			**500**	MHz (min)
f_{CLK2}	Minimum Input Clock Frequency	Normal Mode (non DES)		200		MHz
f_{CLK2}	Minimum Input Clock Frequency	DES Mode		450		MHz
	Input Clock Duty Cycle	200 MHz ≤ Input clock frequency ≤ 500 MHz **(Normal Mode)** (12)		50	20 80	% (min) % (max)
	Input Clock Duty Cycle	450 MHz ≤ Input clock frequency ≤ 500 MHz **(DES Mode)** (12)		50	20 80	% (min) % (max)
t_{CL}	Input Clock Low Time	See (12)		500	**400**	ps (min)
t_{CH}	Input Clock High Time	See (12)		500	**400**	ps (min)
	DCLK Duty Cycle	See (12)		50	**45** **55**	% (min) % (max)
t_{RS}	Reset Setup Time	See (12)		150		ps
t_{RH}	Reset Hold Time	See (12)		250		ps
t_{SD}	Synchronizing Edge to DCLK Output Delay	f_{CLKIN} = 500 MHz f_{CLKIN} = 200 MHz		3.53 3.85		ns
t_{RPW}	Reset Pulse Width	See (13)			**4**	Clock Cycles (min)
t_{LHT}	Differential Low to High Transition Time	10% to 90%, C_L = 2.5 pF		250		ps
t_{HLT}	Differential High to Low Transition Time	10% to 90%, C_L = 2.5 pF		250		ps
t_{OSK}	DCLK to Data Output Skew	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode, 0° DCLK (12)		±50		ps (max)
t_{SU}	Data to DCLK Set-Up Time	DDR Mode, 90° DCLK (12)		2		ns
t_H	DCLK to Data Hold Time	DDR Mode, 90° DCLK (12)		2		ns
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data		1.3		ns
t_{AJ}	Aperture Jitter			0.4		ps rms
t_{OD}	Input Clock to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition		3.1		ns
	Pipeline Delay (Latency) (13) (14)	DI Outputs			**13**	Clock Cycles
		DId Outputs			**14**	
		DQ Outputs	Normal Mode		**13**	
			DES Mode		**13.5**	
		DQd Outputs	Normal Mode		**14**	
			DES Mode		**14.5**	
	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion		1		Input Clock Cycle
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)			500		ns
f_{SCLK}	Serial Clock Frequency	See (12)		100		MHz
t_{SSU}	Data to Serial Clock Setup Time	See (12)		2.5		ns (min)

(12) This parameter is specified by design and/or characterization and is not tested in production.
(13) This parameter is specified by design and is not tested in production.
(14) Each of the two converters of the ADC08D500 has two LVDS output buses, which each clock data out at one half the sample rate. The data at each bus is clocked out at one half the sample rate. The second bus (D0 through D7) has a pipeline latency that is one clock cycle less than the latency of the first bus (Dd0 through Dd7)

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $870mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Input Clock, f_{CLK} = 500 MHz at $0.5V_{P-P}$ with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
t_{SH}	Data to Serial Clock Hold Time	See (12)	1		ns (min)
	Serial Clock Low Time			**4**	ns (min)
	Serial Clock High Time			**4**	ns (min)
t_{CAL}	Calibration Cycle Time		1.4×10^5		Clock Cycles
t_{CAL_L}	CAL Pin Low Time	See Figure 9 (13)		80	Clock Cycles (min)
t_{CAL_H}	CAL Pin High Time	See Figure 9 (13)		80	Clock Cycles (min)
t_{CalDly}	Calibration delay determined by pin 127	See Self-Calibration, Figure 9, (15)		2^{25}	Clock Cycles (min)
t_{CalDly}	Calibration delay determined by pin 127	See Self-Calibration, Figure 9, (15)		2^{31}	Clock Cycles (max)

(15) Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the “hold” mode the aperture delay time (t_{AD}) after the clock goes low.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

Bit Error Rate (B.E.R.) is the probability of error and is defined as the probable number of errors per unit of time divided by the number of bits seen in that amount of time. A B.E.R. of 10^{-18} corresponds to a statistical error in one bit about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 500 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Pos. Gain Error = Offset Error − Pos. Full-Scale Error

Neg. Gain Error = −(Offset Error − Neg. Full-Scale Error)

Gain Error = Neg. Full-Scale Error − Pos. Full-Scale Error = Pos. Gain Error + Neg. Gain Error

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$V_{FS} / 2^n$

where V_{FS} is the differential full-scale amplitude of 650 mV or 870 mV as set by the FSR input and "n" is the ADC resolution in bits, which is 8 for the ADC08D500.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the difference between the V_D+ & V_D- outputs; each measured with respect to Ground.

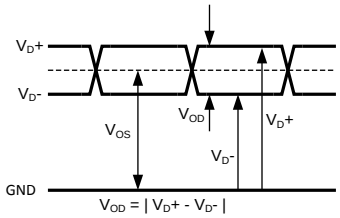


Figure 1.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage; i.e., $[(V_D+) + (V_D-)]/2$.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the last code transition is from the ideal 1/2 LSB above a differential −870 mV with the FSR pin high, or 1/2 LSB above a differential −650 mV with the FSR pin low. For the ADC08D500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 127.5.

OUTPUT DELAY (t_{OD}) is the time delay after the falling edge of DCLK before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +870 mV with the FSR pin high, or 1-1/2 LSB below a differential +650 mV with the FSR pin low. For the ADC08D500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

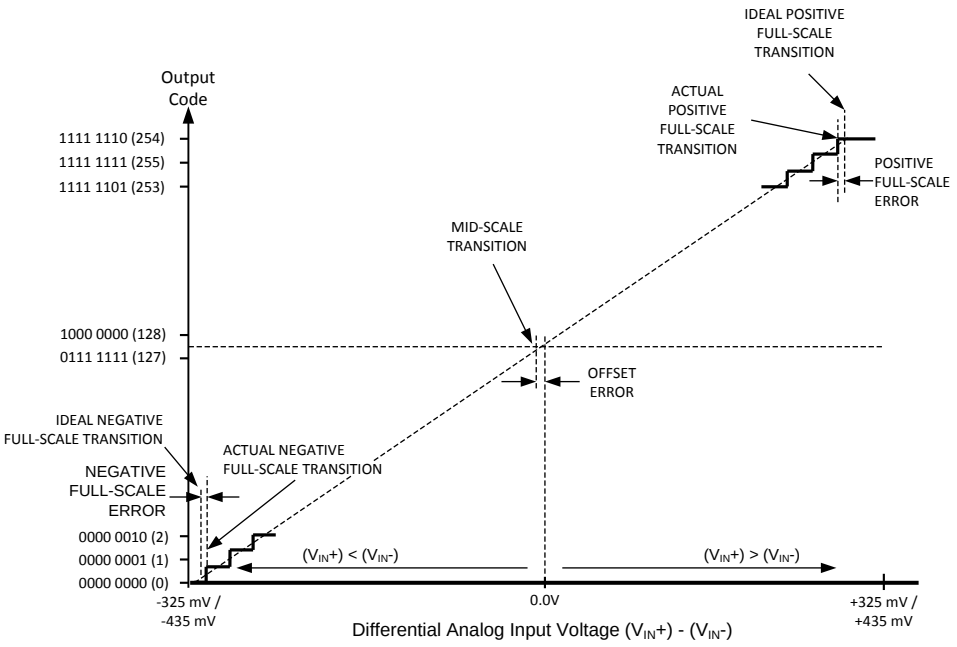


Figure 2. Input / Output Transfer Characteristic

Timing Diagrams

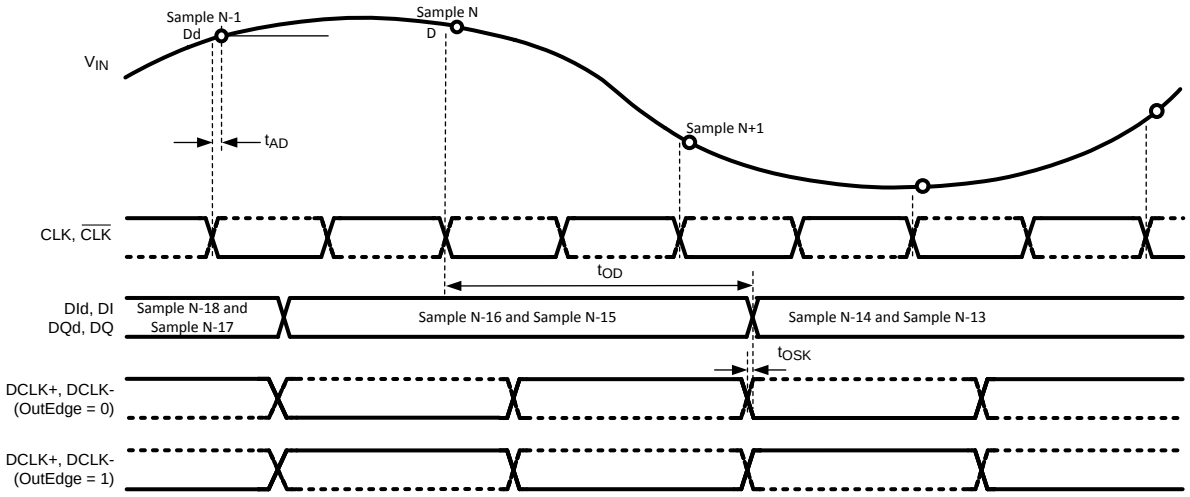


Figure 3. ADC08D500 Timing — SDR Clocking

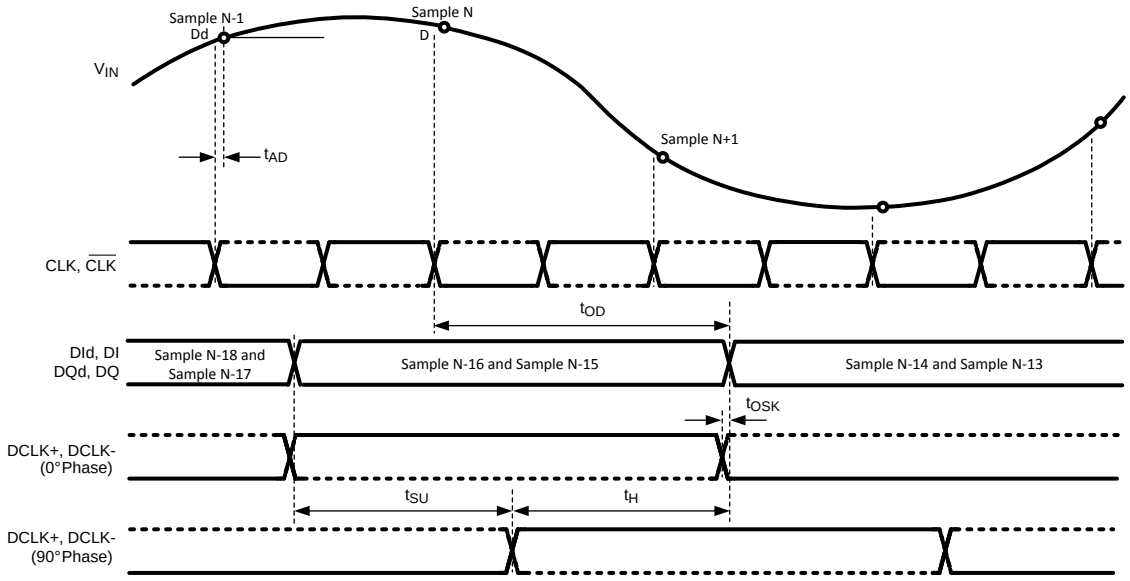


Figure 4. ADC08D500 Timing — DDR Clocking

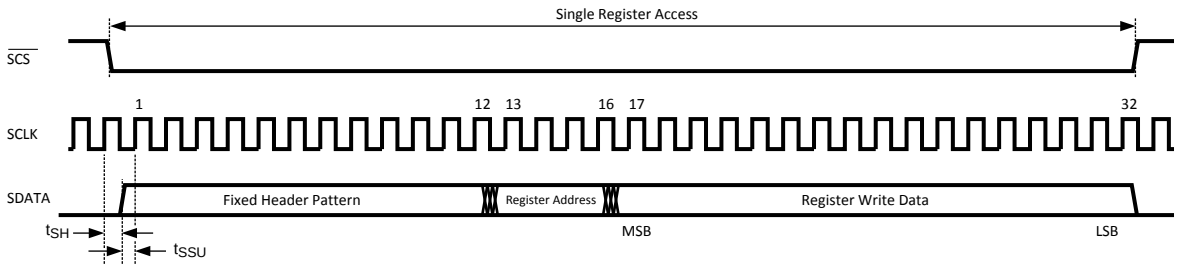


Figure 5. Serial Interface Timing

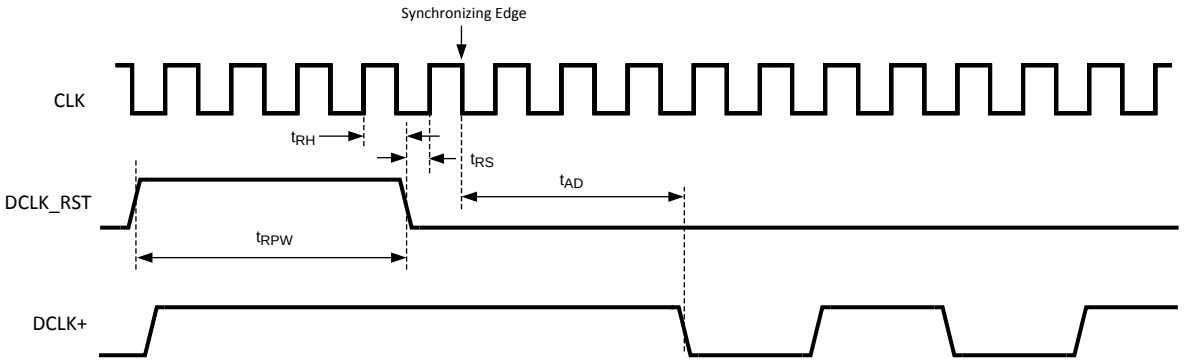


Figure 6. Clock Reset Timing in DDR Mode

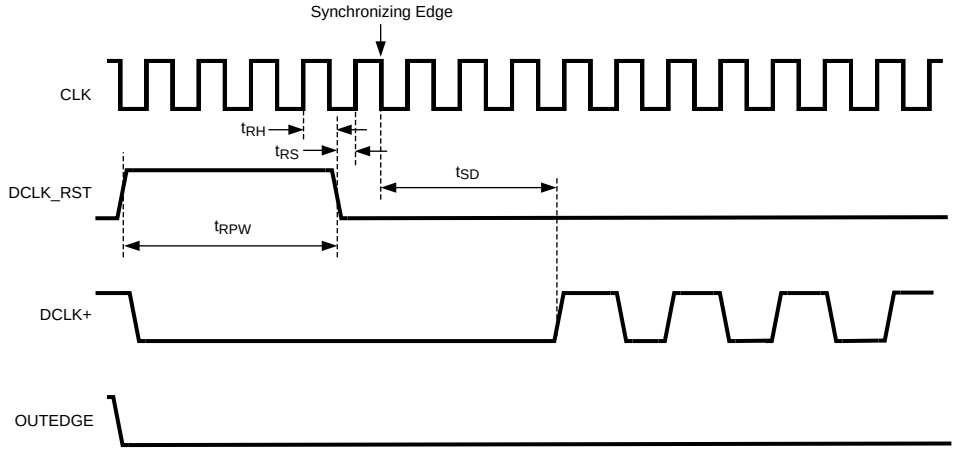


Figure 7. Clock Reset Timing in SDR Mode with OUTEDGE Low

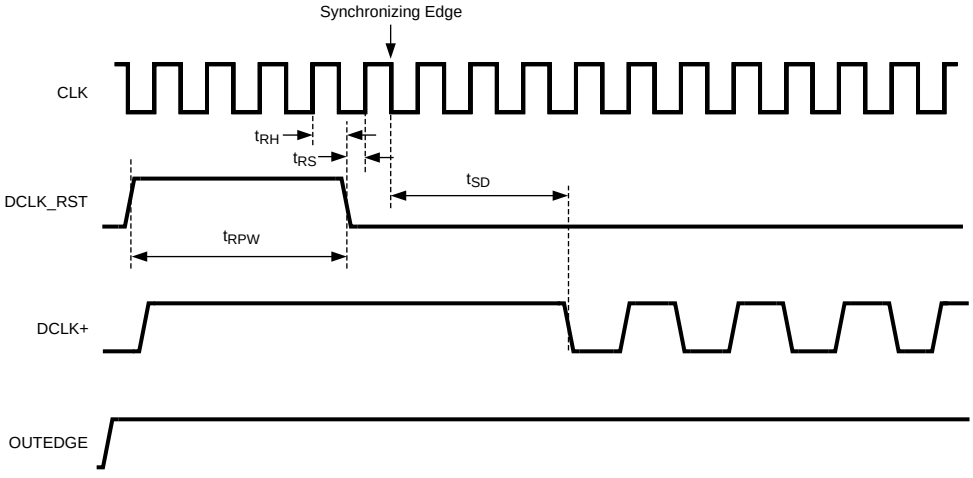


Figure 8. Clock Reset Timing in SDR Mode with OUTEDGE High

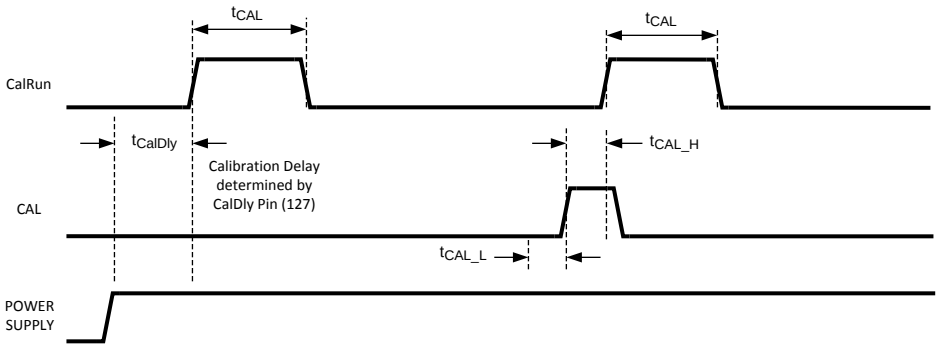


Figure 9. Self Calibration and On-Command Calibration Timing

Typical Performance Characteristics

V_A=V_{DR}=1.9V, F_{CLK}=500MHz, T_A=25°C unless otherwise stated.

INL vs. CODE

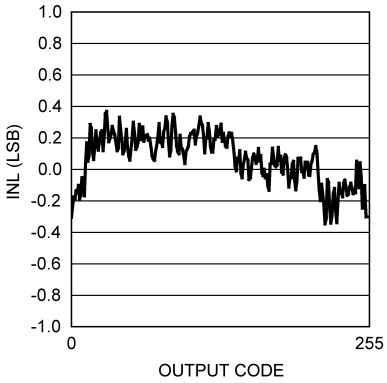


Figure 10.

INL vs. TEMPERATURE

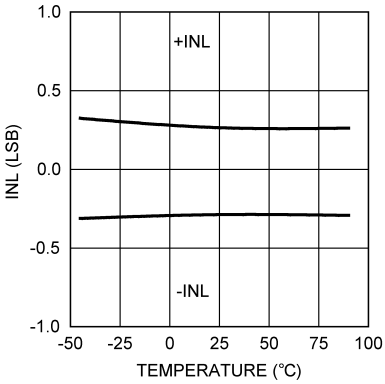


Figure 11.

DNL vs. CODE

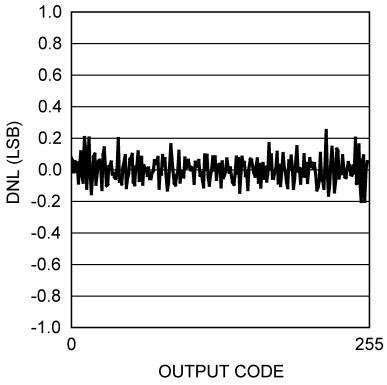


Figure 12.

DNL vs. TEMPERATURE

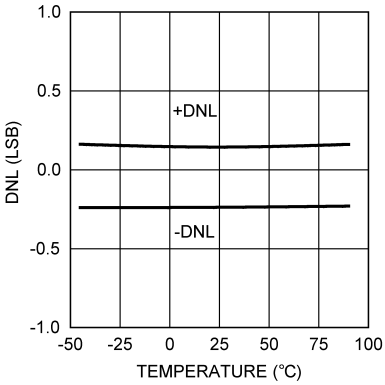


Figure 13.

ENOB vs. TEMPERATURE

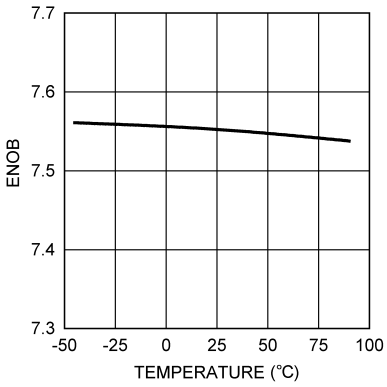


Figure 14.

ENOB vs. SUPPLY VOLTAGE

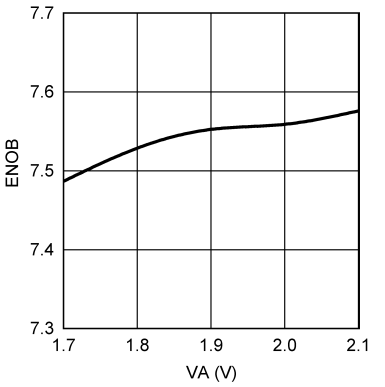


Figure 15.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, F_{CLK}=500MHz, T_A=25°C unless otherwise stated.

ENOB vs. INPUT FREQUENCY

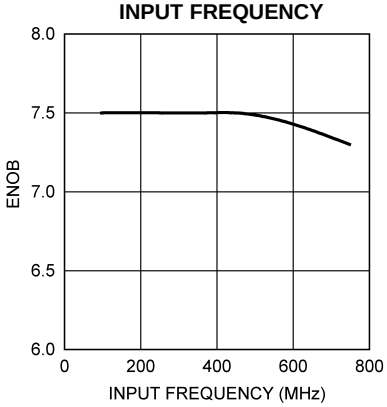


Figure 16.

SNR vs. TEMPERATURE

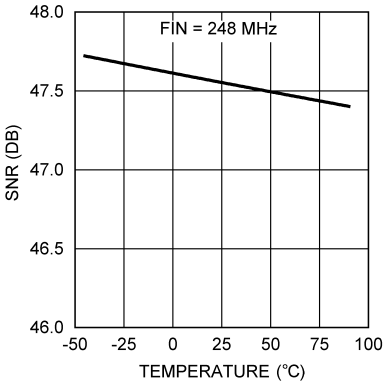


Figure 17.

SNR vs. SUPPLY VOLTAGE

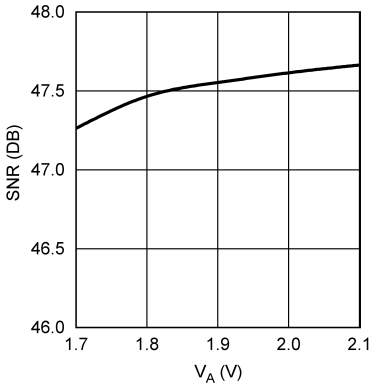


Figure 18.

SNR vs. INPUT FREQUENCY

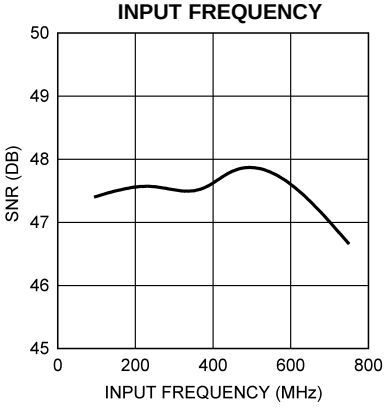


Figure 19.

THD vs. TEMPERATURE

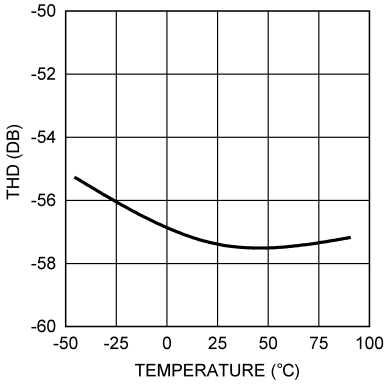


Figure 20.

THD vs. SUPPLY VOLTAGE

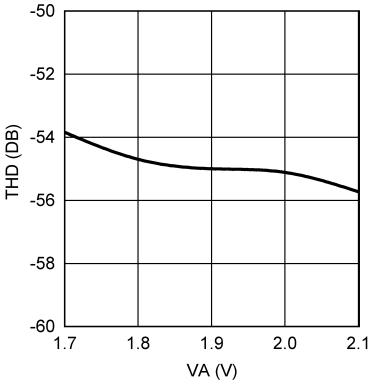


Figure 21.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, F_{CLK}=500MHz, T_A=25°C unless otherwise stated.

THD vs. INPUT FREQUENCY

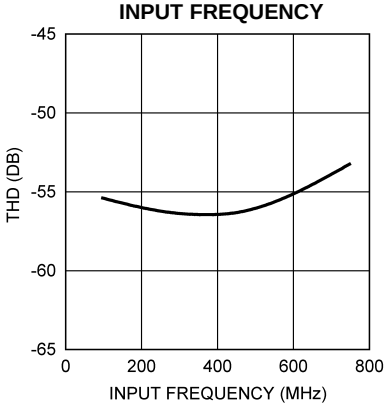


Figure 22.

SFDR vs. TEMPERATURE

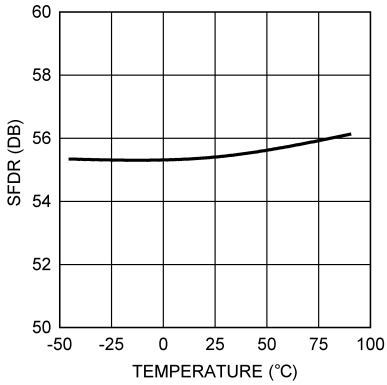


Figure 23.

SFDR vs. SUPPLY VOLTAGE

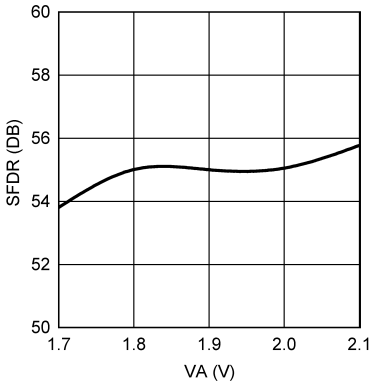


Figure 24.

SFDR vs. INPUT FREQUENCY

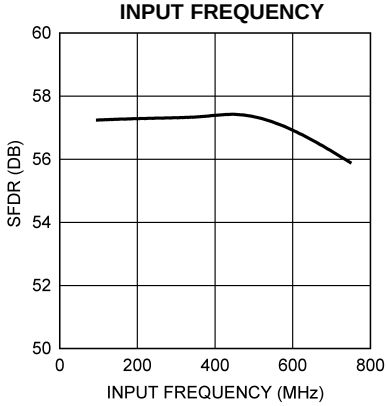


Figure 25.

Spectral Response at FIN = 98 MHz

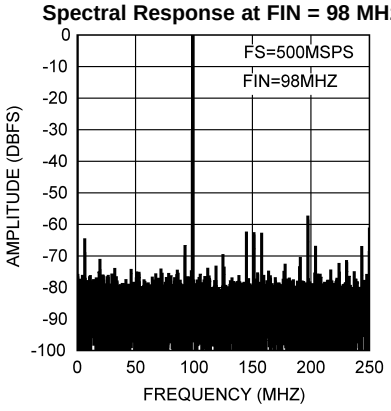


Figure 26.

Spectral Response at FIN = 248 MHz

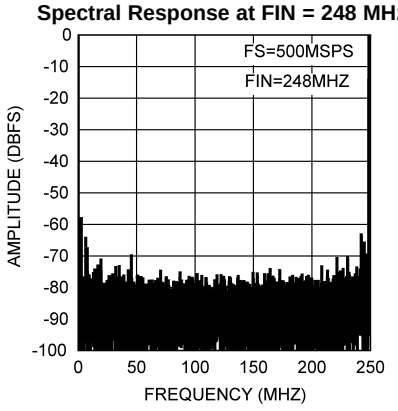


Figure 27.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, F_{CLK}=500MHz, T_A=25°C unless otherwise stated.

CROSSTALK vs. SOURCE FREQUENCY

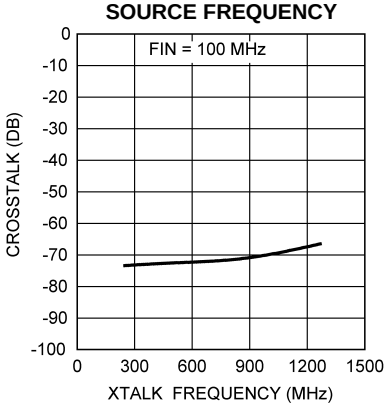


Figure 28.

FULL POWER BANDWIDTH

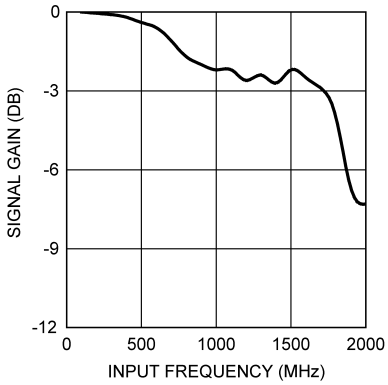


Figure 29.

FUNCTIONAL DESCRIPTION

The ADC08D500 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 4, 14 and 127 of the ADC08D500 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

OVERVIEW

The ADC08D500 uses a calibrated folding and interpolating architecture that achieves over 7.5 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 500 MSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at either the "I" or "Q" input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from one or both of the channels is below negative full scale or above positive full scale.

Each of the two converters has a 1:2 demultiplexer that feeds two LVDS output buses. The data on these buses provide an output word rate on each bus at half the ADC sampling rate and must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

Self-Calibration

A self-calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the self calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, self calibration must be re-run whenever the sense of the FSR pin is changed. For best performance, we recommend that self calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, according to the particular system design requirements. See On-Command Calibration for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Power Down for information on the interaction between Power Down and Calibration.

During the calibration process, the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This external resistor is located between pin 32 and ground. R_{EXT} must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used. In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 clock cycles, then hold it high for at least another 80 clock cycles. The time taken by the calibration procedure is specified in the A.C. Characteristics Table. Holding the CAL pin high upon power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 clock cycles low followed by 80 clock cycles high.

CalDly (pin 127) is used to select one of two delay times after the application of power to the start of calibration. This calibration delay is 2^{25} clock cycles (about 67.2 ms at 500 MSPS) with CalDly low, or 2^{31} clock cycles (about 4.3 seconds at 500 MSPS) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 18) and the digital equivalent of that data is available at the digital outputs 13 clock cycles later for the DI and DQ output buses and 14 clock cycles later for the DId and DQd output buses. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC08D500 will convert as long as the clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables a very flat SINAD/ENOB response beyond 500 MHz. The ADC08D500 output data signaling is LVDS and the output format is offset binary.

Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC08D500 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and CalDly/DES (pin 127). See NORMAL/EXTENDED CONTROL for details on the Extended Control mode.

The Analog Inputs

The ADC08D500 must be driven with a differential input signal. Operation with a single-ended signal is not recommended. It is important that the inputs either be a.c. coupled to the inputs with the V_{CMO} pin grounded or d.c. coupled with the V_{CMO} pin not grounded and an input common mode voltage equal to the V_{CMO} output.

Two full-scale range settings are provided with pin 14 (FSR). A high on pin 14 causes an input full-scale range setting of 870 mV_{P-P}, while grounding pin 14 causes an input full-scale range setting of 650 mV_{P-P}. The full-scale range setting operates equally on both ADCs.

In the Extended Control mode, the full-scale input range can be set to values between 560 mV_{P-P} and 840 mV_{P-P} through a serial interface. See THE ANALOG INPUT.

Clocking

The ADC08D500 must be driven with an a.c. coupled, differential clock signal. THE CLOCK INPUTS describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever receives that data.

The ADC08D500 offers options for input and output clocking. These options include a choice of Dual Edge Sampling (DES) or interleaved mode where the ADC08D500 performs as a single device converting at twice the input clock rate and a choice of which DCLK edge the output data transitions on and choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs.

The ADC08D500 also has the option to use a duty cycle corrected clock receiver as part of the input clock circuit. This feature is enabled by default and provides improved ADC clocking, especially in the Dual-Edge Sampling mode (DES). This circuitry allows the ADC to be clocked with a signal source having a duty cycle ratio of 80 / 20 % (worst case) for both the normal and the Dual Edge Sampling modes.

Dual-Edge Sampling

The DES mode allows one of the ADC08D500's inputs (I or Q Channel) to be sampled by both ADCs. One ADC samples the input on the positive edge of the input clock and the other ADC samples the same input on the other edge of the input clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the input clock frequency, or 1 GSPS with a 500 MHz clock.

In this mode the outputs are interleaved such that the data is effectively demultiplexed 1:4. Since the sample rate is doubled, each of the 4 output buses have a 250 MSPS output rate with a 500 MHz input clock. All data is available in parallel. The four bytes of parallel data that is output with each clock is in the following sampling order, from the earliest to the latest: DQd, DId, DQ, DI. Table 1 indicates what the outputs represent for the various sampling possibilities.

In the non-extended mode of operation only the "I" input can be sampled in the DES mode. In the extended mode of operation the user can select which input is sampled.

The ADC08D500 also includes an automatic clock phase background calibration feature which can be used in DES mode to automatically and continuously adjust the clock phase of the I and Q channel. This feature removes the need to adjust the clock phase setting manually and provides optimal Dual-Edge Sampling ENOB performance.

NOTE

The background calibration feature in DES mode does not replace the requirement for On-Command Calibration which should be run before entering DES mode, or if a large swing in ambient temperature is experienced by the device.

Table 1. Input Channel Samples Produced at Data Outputs

Data Outputs (Always sourced with respect to fall of DCLK)	Normal Sampling Mode	Dual-Edge Sampling Mode	
		I-Channel Selected	Q-Channel Selected (1)
DI	"I" Input Sampled with Fall of CLK 13 cycles earlier.	"I" Input Sampled with Fall of CLK 13 cycles earlier.	"Q" Input Sampled with Fall of CLK 13 cycles earlier.
DId	"I" Input Sampled with Fall of CLK 14 cycles earlier.	"I" Input Sampled with Fall of CLK 14 cycles earlier.	"Q" Input Sampled with Fall of CLK 14 cycles earlier.
DQ	"Q" Input Sampled with Fall of CLK 13 cycles earlier.	"I" Input Sampled with Rise of CLK 13.5 cycles earlier.	"Q" Input Sampled with Rise of CLK 13.5 cycles earlier.
DQd	"Q" Input Sampled with Fall of CLK 14 cycles after being sampled.	"I" Input Sampled with Rise of CLK 14.5 cycles earlier.	"Q" Input Sampled with Rise of CLK 14.5 cycles earlier.

(1) In DES + normal mode, only the I Channel is sampled. In DES + extended control mode, I or Q channel can be sampled.

OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input (pin 4). A high on the OutEdge input causes the output data to transition on the rising edge of DCLK, while grounding this input causes the output to transition on the falling edge of DCLK. See Output Edge Synchronization.

Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. With single data rate the clock frequency is the same as the data rate of the two output buses. With double data rate the clock frequency is half the data rate and data is sent to the outputs on both DCLK edges. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK, are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 14) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC08D500 is used is noisy, it may be necessary to tie the OutV pin high. The LVDS data output have a typical common mode voltage of 800mV when the V_{BG} pin is unconnected and floating. This common mode voltage can be increased to 1.2V by tying the V_{BG} pin to V_A if a higher common mode is required.

NOTE

Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage by up to 40mV.

Power Down

The ADC08D500 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device power consumption is reduced to a minimal level. A high on the PDQ pin will power down the "Q" channel and leave the "I" channel active. There is no provision to power down the "I" channel independently of the "Q" channel. Upon return to normal operation, the pipeline will contain meaningless information.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state. Calibration will function with the "Q" channel powered down, but that channel will not be calibrated if PDQ is high. If the "Q" channel is subsequently to be used, it is necessary to perform a calibration after PDQ is brought low.

NORMAL/EXTENDED CONTROL

The ADC08D500 may be operated in one of two modes. In the simpler "normal" control mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through a serial interface and a set of 8 registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 2 shows how several of the device features are affected by the control mode chosen.

Table 2. Features and Modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	Selected with pin 4	Selected with DE bit in the Configuration Register (1h).
DDR Clock Phase	Not Selectable (0° Phase Only)	Selected with DCP bit in the Configuration Register (1h). See REGISTER DESCRIPTION
SDR Data transitions with rising or falling DCLK edge	Selected with pin 4	Selected with the OE bit in the Configuration Register (1h).
LVDS output level	Selected with pin 3	Selected with the OV bit in the Configuration Register (1h).
Power-On Calibration Delay	Delay Selected with pin 127	Short delay only.
Full-Scale Range	Options (650 mV_{P-P} or 870 mV_{P-P}) selected with pin 14. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range of 560 mV to 840 mV. Separate range selected for I- and Q-Channels. Selected using registers 3h and Bh.
Input Offset Adjust	Not possible	Separate ±45 mV adjustments in 512 steps for each channel using registers 2h and Ah.
Dual Edge Sampling Selection	Enabled with pin 127	Enabled through DES Enable Register (1h).
Dual Edge Sampling Input Channel Selection	Only I-Channel Input can be used	Either I- or Q-Channel input may be sampled by both ADCs

Table 2. Features and Modes (continued)

DES Sampling Clock Adjustment	The Clock Phase is adjusted automatically	Automatic Clock Phase control can be selected by setting bit 14 in the DES Enable register (Dh). The clock phase can also be adjusted manually through the Coarse & Fine registers Eh and Fh.

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 3.

Table 3. Extended Control Mode Operation (Pin 14 Floating)

Feature	Extended Control Mode Default State
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0° phase)
LVDS Output Amplitude	Normal amplitude ($710\ mV_{P-P}$)
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel
Dual Edge Sampling (DES)	Not enabled

THE SERIAL INTERFACE

NOTE

During the initial write using the serial interface, all 8 user registers must be written with desired or default values. In addition, the first write to the DES Enable register (Dh) must load the default value (0x3FFFh). Once all registers have been written once, other desired settings, including enabling DES can be loaded.

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$) Eight write only registers are accessible through this serial interface.

$\overline{SCS}$: This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted with the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram.

Each Register access consists of 32 bits, as shown in Figure 5 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a 0b is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 4.

Refer to the REGISTER DESCRIPTION for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

NOTE

The Serial Interface should not be used when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

Table 4. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after Fixed Header Pattern, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	"I" Ch Offset
0	0	1	1	3h	"I" Ch Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	"Q" Ch Offset
1	0	1	1	Bh	"Q" Ch Full-Scale Voltage Adjust
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	DES Enable
1	1	1	0	Eh	DES Coarse Adjust
1	1	1	1	Fh	DES Fine Adjust

REGISTER DESCRIPTION

Eight write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Table 5. Configuration Register

Addr: 1h (0001b)	**W only (0xB2FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	0	1	DCS	DCP	nDE	OV	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

IMPORTANT: The Configuration Register should not be written if the DES Enable bit = 1. The DES Enable bit should first be changed to 0, then the Configuration Register can be written. Failure to follow this procedure can cause the internal DES clock generation circuitry to stop.	
Bit 15	Must be set to 1b
Bit 14	Must be set to 0b
Bit 13	Must be set to 1b
Bit 12	DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.

Bit 11	DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90° Phase"), using the one-half speed DCLK shown in Figure 4 as the phase reference.
	POR State: 0b
Bit 10	nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK, as determined by the OutEdge bit.
	POR State: 0b
Bit 9	OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude of 710 mV_{P-P} is used. When this bit is set to 0b, the reduced output amplitude of 510 mV_{P-P} is used.
	POR State: 1b
Bit 8	OE: Output Edge. This bit selects the DCLK edge with which the data words transition in the SDR mode and has the same effect as the OutEdge pin in the normal control mode. When this bit is 1b, the data outputs change with the rising edge of DCLK+. When this bit is 0b, the data output change with the falling edge of DCLK+.
	POR State: 0b
Bits 7:0	Must be set to 1b.

Table 6. I-Channel Offset

Addr: 2h (0010b)	**W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Offset Value				(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8	Offset Value. The input offset of the I-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.
	POR State: 0000 0000b
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset.
	POR State: 0b
Bit 6:0	Must be set to 1b

Table 7. I-Channel Full-Scale Voltage Adjust

Addr: 3h (0011b)	**W only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Adjust Value				

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage of the I-Channel ADC is adjusted linearly and monotonically from the nominal 700 mV_{P-P} differential by the value in this field.	
	0000 0000 0	560mV_{P-P}
	1000 0000 0	700mV_{P-P}
	1111 1111 1	840mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation .A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b (no adjustment)	
Bits 6:0	Must be set to 1b	

Table 8. Q-Channel Offset

Addr: Ah (1010b)	**W only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Offset Value						(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bit 15:8	Offset Value. The input offset of the Q-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides about 0.176 mV of offset.
	POR State: 0000 0000b
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset.
	POR State: 0b
Bit 6:0	Must be set to 1b

Table 9. Q-Channel Full-Scale Voltage Adjust

Addr: Bh (1011b)	**W only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage of the Q-Channel ADC is adjusted linearly and monotonically from the nominal 700 mV_{P-P} differential by the value in this field.	
	0000 0000 0	560mV_{P-P}
	1000 0000 0	700mV_{P-P}
	1111 1111 1	840mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation .A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b (no adjustment)	
Bits 6:0	Must be set to 1b	

Table 10. DES Enable

Addr: Dh (1101b)	W only (0x3FFF)

D15	D14	D13	D12	D11	D10	D9	D8
DEN	ACP	1	1	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	DES Enable. Setting this bit to 1b enables the Dual Edge Sampling mode. In this mode the ADCs in this device are used to sample and convert the same analog input in a time-interleaved manner, accomplishing a sampling rate of twice the input clock rate. When this bit is set to 0b, the device operates in the normal dual channel mode.
	POR State: 0b
Bit 14	Automatic Clock Phase (ACP) Control. Setting this bit to 1b enables the Automatic Clock Phase Control. In this mode the DES Coarse and Fine manual controls are disabled. A phase detection circuit continually adjusts the I and Q sampling edges to be 180 degrees out of phase. When this bit is set to 0b, the sample (input) clock delay between the I and Q channels is set manually using the DES Coarse and Fine Adjust registers. (See Dual Edge Sampling for important application information)**Using the ACP Control option is recommended over the manual DES settings**.
	POR State: 0b
Bits 13:0	Must be set to 1b

Table 11. DES Coarse Adjust

Addr: Eh (1110b)	W only (0x07FF)

D15	D14	D13	D12	D11	D10	D9	D8
IS	ADS	CAM			1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	Input Select. When this bit is set to 0b the "I" input is operated upon by both ADCs. When this bit is set to 1b the "Q" input is operated on by both ADCs.
	POR State: 0b
Bit 14	Adjust Direction Select. When this bit is set to 0b, the programmed delays are applied to the "I" channel sample clock while the "Q" channel sample clock remains fixed. When this bit is set to 1b, the programmed delays are applied to the "Q" channel sample clock while the "I" channel sample clock remains fixed.
	POR State: 0b
Bits 13:11	Coarse Adjust Magnitude. Each code value in this field delays either the "I" channel or the "Q" channel sample clock (as determined by the ADS bit) by approximately 20 picoseconds. A value of 000b in this field causes zero adjustment.
	POR State: 000b
Bits 10:0	Must be set to 1b

Table 12. DES Fine Adjust

Addr: Fh (1111b)	W only (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	FAM						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bits 15:7	Fine Adjust Magnitude. Each code value in this field delays either the "I" channel or the "Q" channel sample clock (as determined by the ADS bit of the DES Coarse Adjust Register) by approximately 0.1 ps. A value of 0000 0000 0b in this field causes zero adjustment. Note that the amount of adjustment achieved with each code will vary with the device conditions as well as with the Coarse Adjustment value chosen.
	POR State: 0000 0000 0b
Bit 6:0	Must be set to 1b

Note Regarding Extended Mode Offset Correction

When using the I or Q channel Offset Adjust registers, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

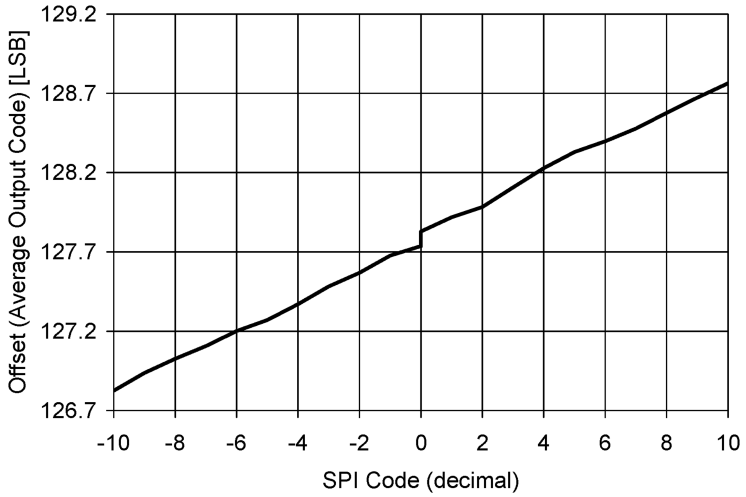


Figure 30. Extended Mode Offset Behavior

MULTIPLE ADC SYNCHRONIZATION

The ADC08D500 has the capability to precisely reset its sampling clock input to DCLK output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all use for sampling.

The DCLK_RST signal must observe some timing requirements that are shown in Figure 6, Figure 7, and Figure 8 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These times are specified in the AC Electrical Characteristics Table.

The DCLK_RST signal can be asserted asynchronous to the input clock If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to Figure 6, Figure 8, and Figure 8 for the DCLK reset conditions). Therefore depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the DCLK output with those of other ADC08D500s in the system. The DCLK output is enabled again after a constant delay which is equal to the CLK input to DCLK output delay (t_{AD}). The device always exhibits this delay characteristic in normal operation.

The DCLK-RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

Applications Information

THE REFERENCE VOLTAGE

The voltage reference for the ADC08D500 is derived from a 1.254V bandgap reference which is made available at pin 31, V_{BG} for user convenience and has an output current capability of ±100 µA and should be buffered if more current than this is required.

The internal bandgap-derived reference voltage has a nominal value of 650 mV or 870 mV, as determined by the FSR pin and described in The Analog Inputs.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in NORMAL/EXTENDED CONTROL.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See Out Of Range (OR) Indication.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1200mV the V_{BG} pin can be connected directly to the supply rails.

THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin to be 650 mV_{P-P} or 870 mV_{P-P}, or can be adjusted to values between 560 mV_{P-P} and 840 mV_{P-P} in the Extended Control mode through the Serial Interface. For best performance, it is recommended that the full-scale range be kept between 595 mV_{P-P} and 805 mV_{P-P} in the Extended Control mode.

Table 13 gives the input to output relationship with the FSR pin high and the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 13 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 13. Differential Input To Output Relationship (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 217.5mV	V_{CM} + 217.5mV	0000 0000
V_{CM} − 109mV	V_{CM} + 109mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 109 mV	V_{CM} − 109mV	1100 0000
V_{CM} + 217.5mV	V_{CM} − 217.5mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when a.c. input coupling is used and the input signal is a.c. coupled to the ADC.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in Figure 31. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50k-Ohm resistors.

NOTE

An Analog input channel that is not used (e.g. in DES Mode) should be left floating when the inputs are a.c. coupled. Do not connect an unused analog input to ground.

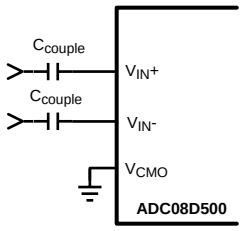


Figure 31. Differential Input Drive

When the d.c. coupled mode is used, a common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

NOTE

An analog input channel that is not used (e.g. in DES Mode) should be tied to the V_{CMO} voltage when the inputs are d.c. coupled. Do not connect unused analog inputs to ground.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

If d.c. coupling is used, it is best to servo the input common mode voltage with V_{CMO} to maintain optimum performance. An example of this type of circuit is shown in Figure 32.

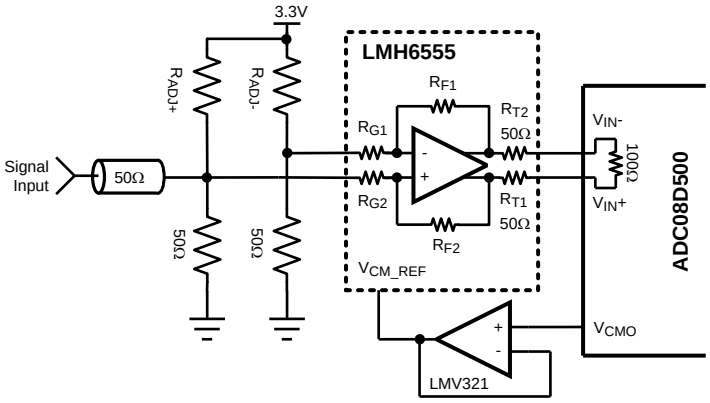


Figure 32. Example of Servoing the Analog Input with V_{CMO}

One such circuit should be used in front of the V_{IN}+ input and another in front of the V_{IN}− input. In that figure, R_{D1}, R_{D2} and R_{D3} are used to divide the V_{CMO} potential so that, after being gained up by the amplifier, the input common mode voltage is equal to V_{CMO} from the ADC. R_{D1} and R_{D2} are split to allow the bypass capacitor to isolate the input signal from V_{CMO}. R_{IN}, R_{D2} and R_{D3} will divide the input signal, if necessary. Capacitor "C" in Figure 32 should be chosen to keep any component of the input signal from affecting V_{CMO}.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 µA.

The Input impedance in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor between V_{IN}+ and V_{IN}− and a capacitance from each of these inputs to ground. In the a.c. coupled mode the input appears the same except there is also a resistor of 50K between each analog input pin and the V_{CMO} potential.

Driving the inputs beyond full scale will result in a saturation or clipping of the reconstructed output.

Handling Single-Ended Input Signals

There is no provision for the ADC08D500 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected transformer, as shown in Figure 33.

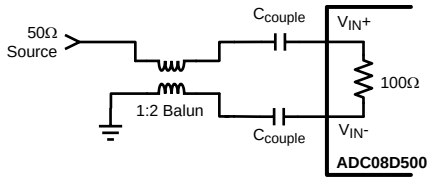


Figure 33. Single-Ended to Differential signal conversion with a balun-connected transformer

The 100 Ohm external resistor placed across the output terminals of the balun in parallel with the ADC08D1000's on-chip 100 Ohm resistor makes a 50 Ohms differential impedance at the balun output. Or, 25 Ohms to virtual ground at each of the balun output terminals.

Looking into the balun, the source sees the impedance of the first coil in series with the impedance at the output of that coil. Since the transformer has a 1:1 turns ratio, the impedance across the first coil is exactly the same as that at the output of the second coil, namely 25 Ohms to virtual ground. So, the 25 Ohms across the first coil in series with the 25 Ohms at its output gives 50 Ohms total impedance to match the source.

Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh.

Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08D500 is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the ADC08D500 such that the differential full-scale input range at the analog inputs is 870 mV_{P-P} with the FSR pin high, or is 650 mV_{P-P} with FSR pin low. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low.

THE CLOCK INPUTS

The ADC08D500 has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with a differential, a.c. coupled clock signal as indicated in Figure 34. Although the ADC08D500 is tested and its performance is specified with a differential 500 MHz clock, it typically will function well with clock frequencies indicated in the Electrical Characteristics Table. The clock inputs are internally terminated and biased.

Operation up to the sample rates indicated in the Electrical Characteristics Table is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Thermal Management.

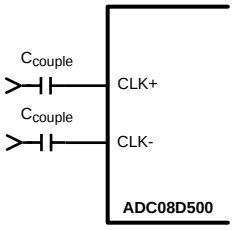


Figure 34. Differential (LVDS) Clock Connection

The differential Clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The clock line should be as short and as direct as possible. The ADC08D500 clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient clock levels will result in poor dynamic performance. Excessively high clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the clock level within the range specified in the Electrical Characteristics Table.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08D1000 features a duty cycle clock correction circuit which can maintain performance over temperature even in DES mode. The ADC will meet its performance specification if the input clock high and low times are maintained within the range (20/80% ratio) as specified in the Electrical Characteristics Table.

High speed, high performance ADCs such as the ADC08D500 require a very stable clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)} / V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (1)$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, to the ADC analog input.

Note that the maximum jitter described above is the arithmetic sum of the jitter from all sources, including that in the ADC clock, that added by the system to the ADC clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Clock amplitudes above those specified in the Electrical Characteristics Table may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC08D500 and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

Full-Scale Input Range Setting

The input full-scale range can be selected to be either 650 mV_{P-P} or 870 mV_{P-P}, as selected with the FSR control input (pin 14) in the Normal Mode of operation. In the Extended Control Mode, the input full-scale range may be set to be anywhere from 560 mV_{P-P} to 840 mV_{P-P}. See THE ANALOG INPUT for more information.

Self Calibration

The ADC08D500 self-calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is a clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that DCLK outputs are not active during a calibration cycle, therefore it is not recommended as a system clock.

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC08D500 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration.

The internal power-on calibration circuitry comes up in an unknown logic state. If the clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

On-Command Calibration

An on-command calibration may be run at any time in **NORMAL (non-DES)** mode only. Do not run a calibration while operating the ADC in Auto DES Mode.

If the ADC is operating in Auto DES mode and a calibration cycle is required then the controlling application should bring the ADC into normal (non DES) mode before an On Command calibration is initiated. Once calibration has completed, the ADC can be put back into Auto DES mode.

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed. When an on-command calibration is executed, the CAL pin must be held low for 80 input clock cycles and then low for 80 input clock cycles before the CalRun pin is activated to indicate that a calibration is taking place. When the CalRun pin is activated, all outputs including the DCLK outputs are deactivated and enter a high impedance state. After the calibration cycle is finished and the CalRun pin is low, the outputs, including DCLK, are active again but require a short settling period, typically around 100ns. Because the DCLK outputs are not activated during a calibration cycle, they are not recommended for use as a system clock.

The minimum 80 input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in Self-Calibration for best performance, a self calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly according to the particular system performance requirements. ENOB drops slightly as junction temperature increases and executing a new self calibration cycle will essentially eliminate the change.

Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in Self-Calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these clock signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that clock signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC08D500 is capable, slight differences in the lengths of the clock and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the FSR input low. If the LVDS lines are long and/or the system in which the ADC08D500 is used is noisy, it may be necessary to tie the FSR pin high.

Dual Edge Sampling

NOTE

When using the ADC in Extended Control Mode, the Configuration Register must only be written when the DES Enable bit = 0. Writing to the Configuration Register when the DES Enable bit = 1 can cause the internal DES clock generation circuitry to stop.

The Dual Edge Sampling (DES) feature causes one of the two input pairs to be routed to both ADCs. The other input pair is deactivated. One of the ADCs samples the input signal on one clock edge, the other samples the input signal on the other clock edge. The result is a 1:4 demultiplexed output with a sample rate that is twice the input clock frequency.

To use this feature in the non-enhanced control mode, allow pin 127 to float and the signal at the "I" channel input will be sampled by both converters. The Calibration Delay will then only be a short delay.

In the enhanced control mode, either input may be used for dual edge sampling. See Dual-Edge Sampling.

NOTE

1) For the Extended Control Mode - When using the Automatic Clock Phase Control feature in dual edge sampling mode, it is important that the automatic phase control is disabled (set bit 14 of DES Enable register Dh to 0) before the ADC is powered up. Not doing so may cause the device not to wake up from the power down state.

2) For the Non-Extended Control Mode - When the ADC08D1000 is powered up and DES mode is required, ensure that pin 127 (CalDly/DES/$\overline{SCS}$) is initially pulled low during or after the power up sequence. The pin can then be allowed to float or be tied to V_A / 2 to enter the DES mode. This will ensure that the part enters the DES mode correctly.

3) The automatic phase control should also be disabled if the input clock is interrupted or stopped for any reason. This is also the case if a large abrupt change in the clock frequency occurs.

4) If a calibration of the ADC is required in Auto DES mode, the device must be returned to the Normal Mode of operation before performing a calibration cycle. Once the Calibration has been completed, the device can be returned to the Auto DES mode and operation can resume.

Power Down Feature

The Power Down pins (PD and PDQ) allow the ADC08D500 to be entirely powered down (PD) or the "Q" channel to be powered down and the "I" channel to remain active. See Power Down for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

THE DIGITAL OUTPUTS

The ADC08D1000 demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters, the results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that, the word rate at each LVDS bus is 1/2 the ADC08D1000 input clock rate and the two buses must be multiplexed to obtain the entire 1 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 200 MSPS (normal non DES mode), the effective rate can be reduced to as low as 100 MSPS by using the results available on just one of the the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS output clock pair (DCLK+/-) available for use to latch the LVDS outputs on all buses. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in Output Edge Synchronization.

DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See LVDS Output Level Control.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}− will produce an output code of all ones, a full-scale input level with V_{IN}− positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}− are equal, the output code will vary between codes 127 and 128.

POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08D500 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC08D500. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

Supply Voltage

The ADC08D500 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08D500 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08D500. The circuit of Figure 35 will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08D500, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of Figure 35, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

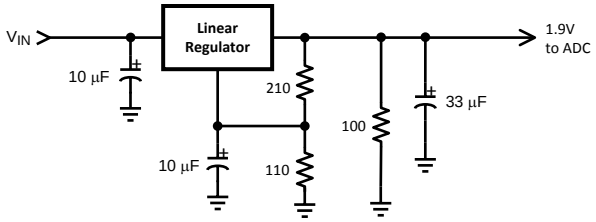


Figure 35. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage and should never spice to a voltage greater than (V_A + 100 mV).

If the power is applied to the device without a clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08D500 gets reset through clocked logic and its initial state is random. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the clock is established.

Thermal Management

The ADC08D500 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +85°C as specified in the Operating Ratings section.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the ADC08D500 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional HLQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

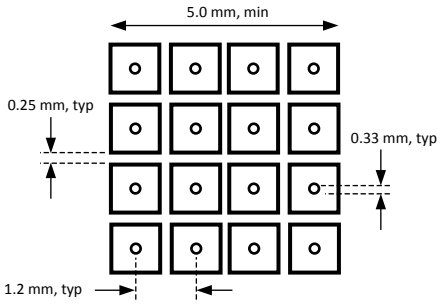


Figure 36. Recommended Package Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of Figure 36.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. .Allow for a thermal gradient between the temperature sensor and the ADC08D500 die of $\theta_{J\text{-}PAD}$ times typical power consumption = 2.8 x 1.6 = 4.5°C. Allowing for a 5.5°C (including an extra 1°C) temperature drop from the die to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 124.5°C will ensure that the die temperature does not exceed 130°C, assuming that the exposed pad of the ADC08D500 is properly soldered down and the thermal vias are adequate. (The inaccuracy of the temperature sensor is in addition to the above calculation).

LAYOUT AND GROUNDING

Proper grounding and routing of all signals are essential to ensure accurate conversion. A single ground plane should be used instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08D500. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

DYNAMIC PERFORMANCE

The ADC08D500 is a.c. tested and its dynamic performance is specified. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in THE CLOCK INPUTS.

It is good practice to keep the ADC clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

USING THE SERIAL INTERFACE

The ADC08D500 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 14 and Table 15 describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the full-scale range, single-ended or differential input and input coupling (a.c. or d.c.) are all controlled with pin settings. The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. Table 14 indicates the pin functions of the ADC08D500 in the non-extended control mode.

Table 14. Non-Extended Control Mode Operation (Pin 14 High or Low)

Pin	Low	High	Floating
3	0.51 V_{P-P} Output	0.71 V_{P-P} Output	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
127	CalDly Low	CalDly High	DES
14	650 mV_{P-P} input range	870 mV_{P-P} input range	Extended Control Mode

Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See NORMAL/EXTENDED CONTROL for more information.

Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See Output Edge Synchronization for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see Double Data Rate) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

Pin 127, if it is high or low in the non-extended control mode, sets the calibration delay. If pin 127 is floating, the calibration delay is the same as it would be with this pin low and the converter performs dual edge sampling (DES).

Table 15. Extended Control Mode Operation (Pin 14 Floating)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)

Table 15. Extended Control Mode Operation (Pin 14 Floating) (continued)

Pin	Function
127	$\overline{SCS}$ (Serial Interface Chip Select)

COMMON APPLICATION PITFALLS

Failure to write all register locations when using extended control mode. When using the serial interface, all 8 user registers must be written at least once with the default or desired values before calibration and subsequent use of the ADC. In addition, the first write to the DES Enable register (Dh) must load the default value (0x3FFFh). Once all registers have been written once, other desired settings, including enabling DES can be loaded.

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should not go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08D500. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in The Analog Inputs and THE ANALOG INPUT, the Input common mode voltage must remain within 50 mV of the V_{CMO} output, which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC08D500 as many high speed amplifiers will have higher distortion than will the ADC08D500, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in THE REFERENCE VOLTAGE, the reference voltage is intended to be fixed to provide one of two different full-scale values (650 mV_{P-P} and 870 mV_{P-P}). Over driving this pin will not change the full scale value, but can otherwise upset operation.

Driving the clock input with an excessively high level signal. The ADC clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate clock levels. As described in THE CLOCK INPUTS, insufficient clock levels can result in poor performance. Excessive clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Thermal Management, it is important to provide adequate heat removal to ensure device reliability. This can either be done with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	43

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08D500CIYB/NOPB	ACTIVE	HLQFP	NNB	128	60	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC08D500 CIYB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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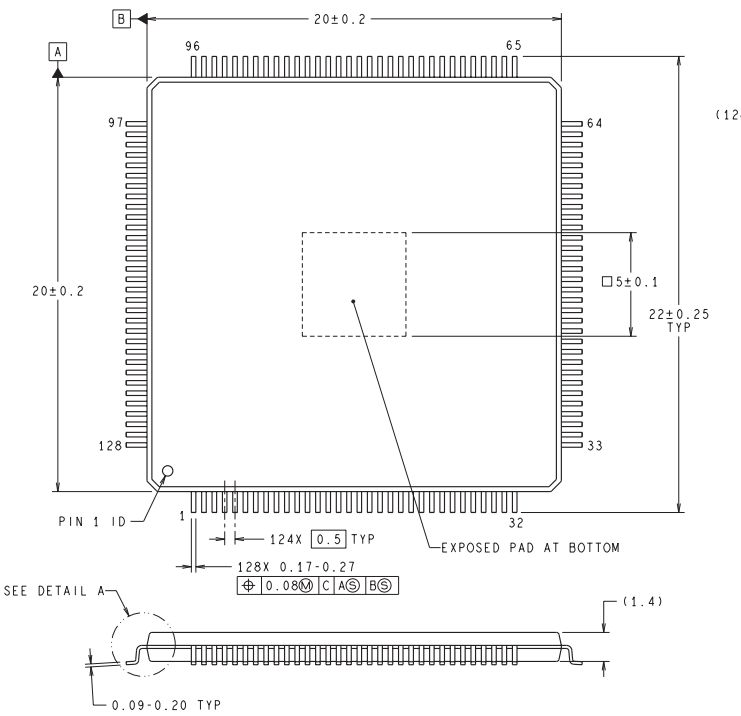
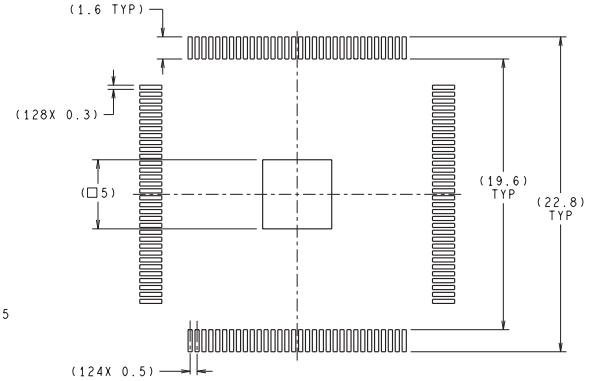
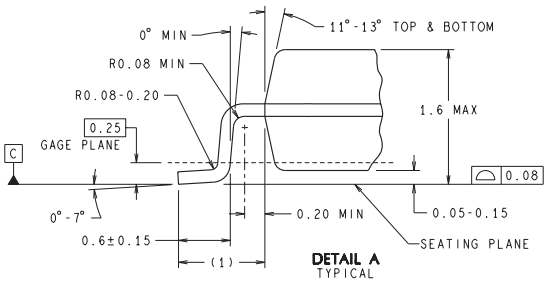


DIMENSIONS ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

VNX128A (Rev B)

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