Features

- Up to 150 Mbps Data Rate
- 3.75 kV RMS Isolation Rating (SOP8)
- 9.6 kV Surge Capability (SOP8)
- ±150 kV/μs typ CMTI
- Low Power Consumption, typ 3 mA/ch @1 Mbps
- Low Propagation Delay: 12 ns Typical
- Wide Supply Range: 2.25 V to 5.5 V
- Default Output Low (TPT7720F) and High (TPT7720)
- Wide Temperature Range: –40°C to +125°C
- SOP8 and Wide-SOIC (WSOP16, WSOP8)
- ESD Protection Exceeds JESD 22
  - ±6kV Human-Body Model
  - ±1.5kV Charged-Device Model
- Safety-Related Certifications (on processing):
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01
  - 3000 Vrms (SOP8) Isolation Rating per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 60601-1 End Equipment Standards
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - CQC Certification per GB4943.1-2011

Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Isolated interface and general purpose isolation

Description

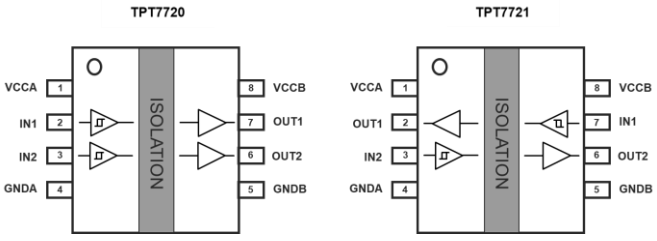
The TPT772x devices are high-performance, dual channel digital isolators with 5000 V_{RMS} (WSOP packages), 3750 V_{RMS} (SOP package), isolation ratings per UL 1577. These devices are also to be certified by VDE, UL, CSA, and CQC.

The TPT772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. The TPT7720 device has both channels in the same direction while the TPT7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is *low* for devices UVLOsuffix F and for *high* devices without suffix F.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as RS-485, RS-232, and CAN, from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the TPT772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

TPT772x family is available in SOP8, WSOP8 and WSOP16 package, and is characterized from –40°C to +125°C.

Functional block



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Revision History

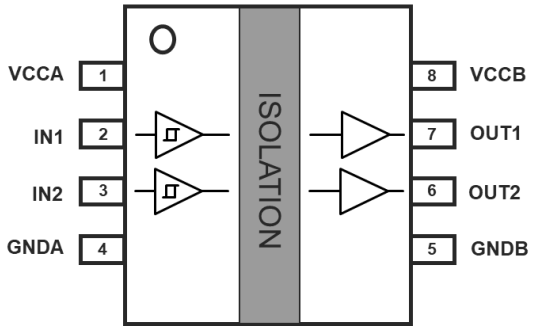
Date	Revision	Notes
2020/05/05	Rev. Pre.0	Definition Version Pre.0
2020/12/15	Rev. Pre.1	Add electrical data
2021/01/12	Rev. Pre.2	Add characteristics data
2021/03/05	Rev. Pre.3	Update characteristics data

Order Information

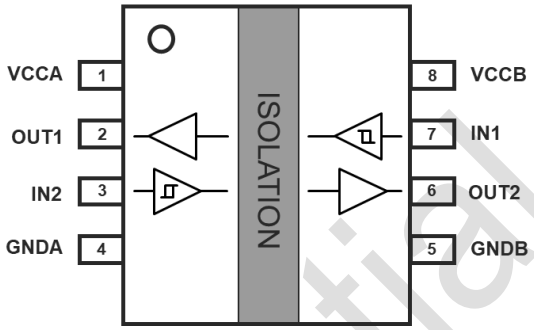
Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT7720-SO1R	-40 to 125°C	8-Pin SOP	T7720	3	Tape and Reel, 4000
TPT7720F-SO1R	-40 to 125°C	8-Pin SOP	7720F	3	Tape and Reel, 4000
TPT7721-SO1R	-40 to 125°C	8-Pin SOP	T7721	3	Tape and Reel, 4000
TPT7721F-SO1R	-40 to 125°C	8-Pin SOP	7721F	3	Tape and Reel, 4000

Pin Configuration and Functions

TPT7720
SOP8
WSOP8



TPT7721
SOP8
WSOP8



Pin Functions

Table 1.

Pin			I/O	Description
Name	TPT7720	TPT7721		
VCCA	1	1	—	Power supply, VCCA
IN1	2	7	I	Input, channel 1
IN2	3	3	I	Input, channel 2
GNDA	4	4	—	Ground connection for VCCA
GNDB	5	5	—	Ground connection for VCCB
OUT2	6	6	O	Output, channel 2
OUT1	7	2	O	Output, channel 1
VCCB	8	8	—	Power supply, VCCB

Absolute Maximum Ratings

Table 2.

Parameter	Description	Min	Max	Unit
V_{CC}	Supply voltage, V_{CCA}, V_{CCB} (2)	–0.5	6	V
V_{IO}	Voltage at IN1, IN2, OUT1, OUT2	–0.5	VCC + 0.5	V
IO	Output current	–15	15	mA
T_J	Operating virtual junction temperature		150	°C
Tstg	Storage temperature	–65	150	°C

* Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(1) This data was taken with the JEDEC low effective thermal conductivity test board.
(2) This data was taken with the JEDEC standard multilayer test boards.

Recommended Operating Conditions

Table 3.

Parameter	Description	Min	Typ	Max	Unit
V_{CCX}	Supply voltage, V_{CCA}, V_{CCB} (1)	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising(2)		2	2.25	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is falling(2)	1.7	1.85		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	60	150		mV
V_{IH}	High-level input voltage (data input)	2		VCC	V
V_{IL}	Low-level input voltage (data input)	0		0.8	V
f_{data}	Data rate(3)	0		100	Mbps
T_A	Operating ambient temperature	-40	25	125	°C

(1) V_{CCA} is input side V_{CC}; V_{CCB} is output side V_{CC};
(2) $V_{CC(UVLO+)}$, $V_{CC(UVLO+)}$, $V_{HYS(UVLO)}$ are same to V_{CCA} and V_{CCB};
(3) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

ESD, Electrostatic Discharge Protection

Table 4.

		Value	Unit
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	All Pin	6	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	1.5	kV
IEC, per IEC 61000-4-2; Isolation barrier withstand test	All Side (1)	6	kV

Note:IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

Thermal Information

Table 5.

Package Type	θJA	θJC	Unit
8-Pin SOP	130	48	°C/W

Insulation Specifications

Table 6. SOP8 SPEC

Symbol	Parameter	Conditions	VALUE	Unit
CLR	External clearance	Shortest terminal-to-terminal distance through air	>3.7	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>22	um
CTI	Comparative tracking index		>600	V
	Material group		I	
	Installation Classification	For Rated Mains Voltage ≤ 300Vrms	I-III	
	Climatic Classification		55/125/21	
	Pollution degree		2	
C_{IO}	Isolation capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance	V_{IO}=500V	>10^9	Ω
Isolation voltage(1)				
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; TDDB Test	450	V_{RMS}
		DC voltage	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	5500	V_{PK}
q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	⩽5	mA
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	⩽5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	⩽5	

(1) All pins on each side of the barrier tied together creating a two-terminal device.

(2) Testing must be carried out in oil.

Electrical Characteristics

VCCA=VCCB=2.25V ~ 5.5V, TA = -40°C ~ +125°C. Typical value is in VCC = 3.3V, TA = +25°C.

Table 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V_{IH}	Logic Input High Voltage	Input signal, IN1, IN2	2.0			V
V_{IL}	Logic Input Low Voltage	Input signal, IN1, IN2			0.8	V
V_{IT+}	Rising input threshold voltage	Input signal, IN1, IN2		1.6	2	V
V_{IT-}	Falling input threshold voltage	Input signal, IN1, IN2	0.8	1.2		V
V_{HYS}	Input threshold voltage hysteresis			0.4		V
I_{IH}	High-level input current	VIH = V_{CCA} at IN1, IN2(1)		2.5	10	μA
I_{IL}	Low-level input current	VIL = 0 V at IN1, IN2(1)	–10	-2.5		μA
I_{OH}	High-level output current	V_{CCB}=5V±10%			4	mA
		V_{CCB}=3.3V±10%			2	
		V_{CCB}=2.5V±10%			1	
I_{OL}	Low-level output current	V_{CCB}=5V±10%			4	
		V_{CCB}=3.3V±10%			2	
		V_{CCB}=2.5V±10%			1	
V_{OH}	High-level output voltage	V_{CCB}=5V±10%,I_{OH} = –4 mA; Test OUT1, OUT2, Figure 10	V_{CCB}– 0.4	V_{CCB} – 0.2		mV
		V_{CCB}=3.3V±10%,I_{OH} = –2 mA; Test OUT1, OUT2, Figure 10	V_{CCB}– 0.3	V_{CCB} – 0.15		
		V_{CCB}=2.5V±10%,I_{OH} = –1 mA; Test OUT1, OUT2, Figure 10	V_{CCB}– 0.2	V_{CCB} – 0.1		
V_{OL}	Low-level output voltage	V_{CCB}=5V±10%,I_{OL}= 4 mA; Test OUT1, OUT2, Figure 10		0.2	0.4	V
		V_{CCB}=3.3V±10%,I_{OL}= 2 mA; Test OUT1, OUT2, Figure 10		0.15	0.3	
		V_{CCB}=2.5V±10%,I_{OL} = 1 mA; Test OUT1, OUT2, Figure 10		0.1	0.2	
CMTI	Common-mode transient immunity	Static CMTI, See Figure12		150		kV/μs
		Dynamic CMTI, See Figure12		120		kV/μs
Ci	Input capacitance (1)			2		pF

*Note: (1). Provided by bench test and design simulation

Timing Specifications—5V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND

Table 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				150	Mpbs
t_{PLH}	Propagation delay time	See Figure 10		11.5	18	ns
t_{PLH}	Propagation delay time	See Figure 10		12	18	ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5	ns
$t_{sk(CC)}$	Channel-to-channel output skew time(2)	Same direction channels			4	ns
$t_{sk(PP)}$	Channel-to-channel output skew time(2)	Same direction channels			5	ns
t_r	Output signal rise time	See Figure 10		0.7	4	ns
t_f	Output signal fall time	See Figure 10		0.7	4	ns
Jitter	eye jitter p-p	f_{data} = 100Mbps		800		ps
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V. See Figure 16		30	52	ns
t_{ie}	Time interval error	216 – 1 PRBS data at 100 Mbps (1)		2.4		ns
t_{su}	Setup time			28	60	us

*Note:

(1). Provided by bench test and design simulation.

(2). $t_{sk(CC)}$ & $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics—5V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND.

Table 9.

Parameter	Conditions		Supply current	Min	Typ	Max	Unit
Supply current - DC signal	V_I = 0V , VO = 0 V (TPT7720F)		I_{CCA}		0.95	1.5	mA
			I_{CCB}		2.4	4.4	
	V_I = VCCA, VO = 0 V (TPT7720F)		I_{CCA}		8.2	10.9	
			I_{CCB}		2.1	3.8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		4.4	5.9	
			I_{CCB}		2.4	4.3	
		10 Mbps	I_{CCA}		4.6	6	
			I_{CCB}		3.7	6.2	
		100 Mbps	I_{CCA}		6.3	8.4	
			I_{CCB}		16.4	22	

*Note:(1). Provided by bench test and design simulation

Timing Specifications—3.3V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND.

Table 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				100	Mpbs
t_{PLH}	Propagation delay time	See Figure 10		12.5	18	ns
t_{PLH}	Propagation delay time	See Figure 10		12.2	18	ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	5	ns
$t_{sk(CC)}$	Channel-to-channel output skew time(2)	Same direction channels			4	ns
$t_{sk(PP)}$	Channel-to-channel output skew time(2)	Same direction channels			5	ns
t_r	Output signal rise time	See Figure 10		0.7	4	ns
t_f	Output signal fall time	See Figure 10		0.7	4	ns
Jitter	eye jitter p-p	f_{data} = 100Mbps		800		ps
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V. See Figure 16		30	52	ns
t_{ie}	Time interval error	216 – 1 PRBS data at 100 Mbps		2.4		ns
t_{su}	Setup time			28	60	us

*Note:

(1). Provided by bench test and design simulation.

(2). $t_{sk(CC)}$& $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics—3.3V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND.

Table 11.

Parameter	Conditions		Supply current	Min	Typ	Max	Unit
TPT7720							
Supply current - DC signal	V_I = 0V , VO = 0 V (TPT7720F)		I_{CCA}		0.92	1.5	mA
			I_{CCB}		2.4	4.4	
	V_I = VCCA, VO = 0 V (TPT7720F)		I_{CCA}		8.2	10.8	
			I_{CCB}		2.1	4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		4.3	6.4	
			I_{CCB}		2.3	4.3	
		10 Mbps	I_{CCA}		4.4	6.5	
			I_{CCB}		3.2	6.2	
		100 Mbps	I_{CCA}		5.5	8.2	
			I_{CCB}		11	18	

*Note:(1). Provided by bench test and design simulation

Timing Specifications—2.5V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND.

Table 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{data}	Translation data rate				100	Mpbs
t_{PLH}	Propagation delay time	See Figure 10		13.5	20	ns
t_{PLH}	Propagation delay time	See Figure 10		12.2	20	ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			1.3	5	ns
$t_{sk(CC)}$	Channel-to-channel output skew time(2)	Same direction channels			4	ns
$t_{sk(PP)}$	Channel-to-channel output skew time(2)	Same direction channels			5	ns
t_r	Output signal rise time	See Figure 10		0.7	4	ns
t_f	Output signal fall time	See Figure 10		0.7	4	ns
Jitter	eye jitter p-p	f_{data} = 100Mbps		800		ps
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7 V. See Figure 16		30	52	ns
t_{ie}	Time interval error	216 – 1 PRBS data at 100 Mbps		2.4		ns
t_{su}	Setup time			28	60	us

*Note:

(1). Provided by bench test and design simulation.

(2). $t_{sk(CC)}$& $t_{sk(PP)}$ is the shew of delay time between different channel of a single device or different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Supply Current Characteristics—2.5V Supply

VCCA=VCCB=5V±10%, TA = -40°C ~ +125°C. Typical value is in VCC = 5V, TA = +25°C, CL = 15PF to GND.

Table 13.

Parameter	Conditions		Supply current	Min	Typ	Max	Unit
TPT7720							
Supply current - DC signal	V_I = 0V , VO = 0 V (TPT7720F)		I_{CCA}		0.9	1.5	mA
			I_{CCB}		2.4	4.4	
	V_I = VCCA, VO = 0 V (TPT7720F)		I_{CCA}		8.2	10.8	
			I_{CCB}		2.1	4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CCA}		4.3	5.9	
			I_{CCB}		2.3	4.3	
		10 Mbps	I_{CCA}		4.3	6.1	
			I_{CCB}		3	6.2	
		100 Mbps	I_{CCA}		4.6	6.2	
			I_{CCB}		8.9	12.5	

*Note:(1). Provided by bench test and design simulation

Typical Characteristics

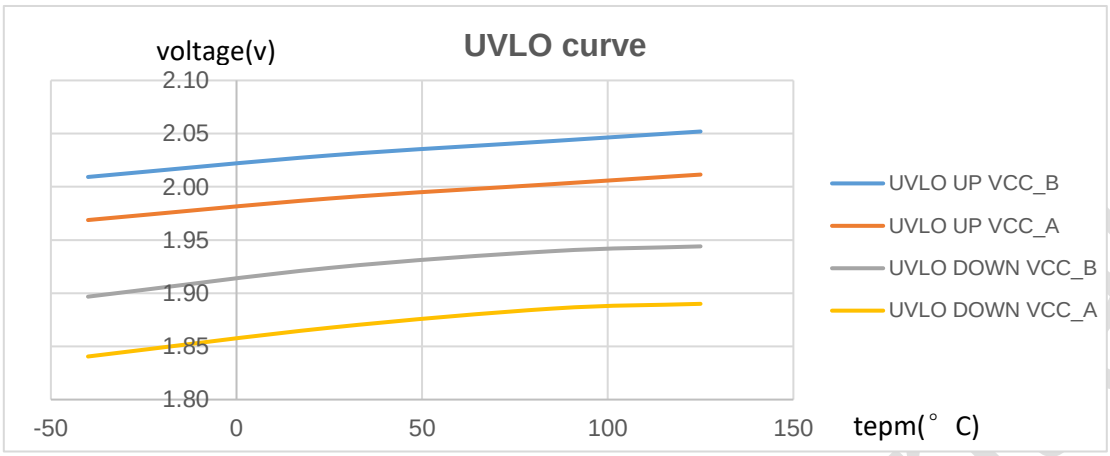


Figure 2. UVLO characterization by temperature

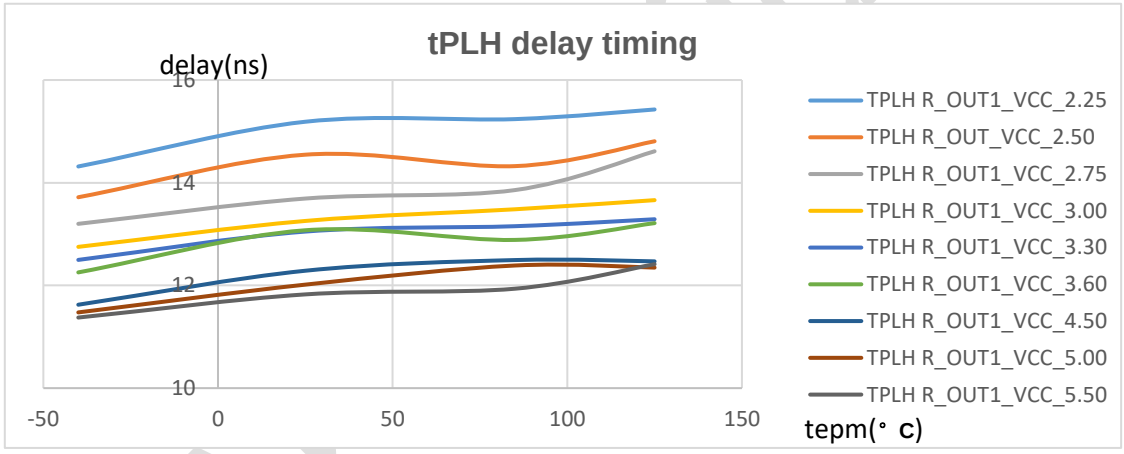


Figure 3. tPLH delay timing

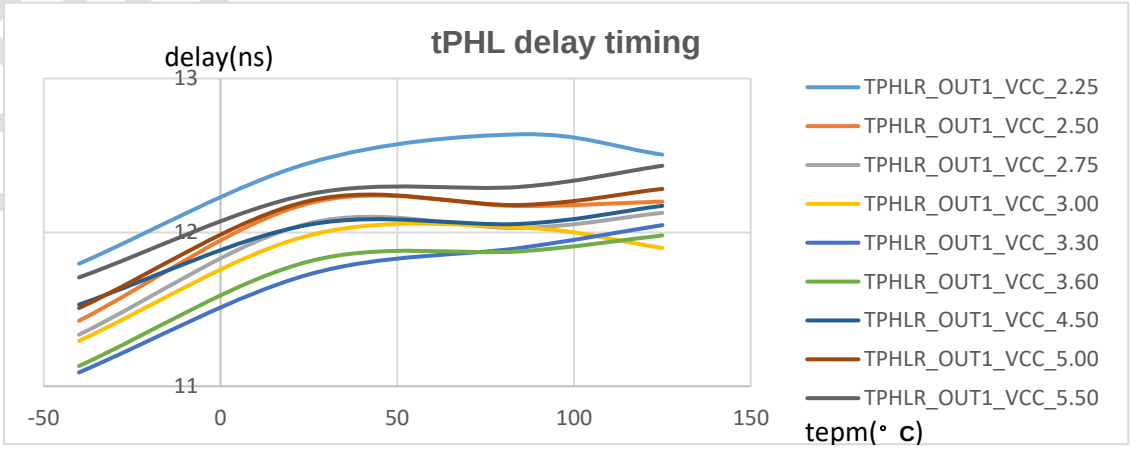


Figure 4. tPHL delay timing

Typical Characteristics (Continue)

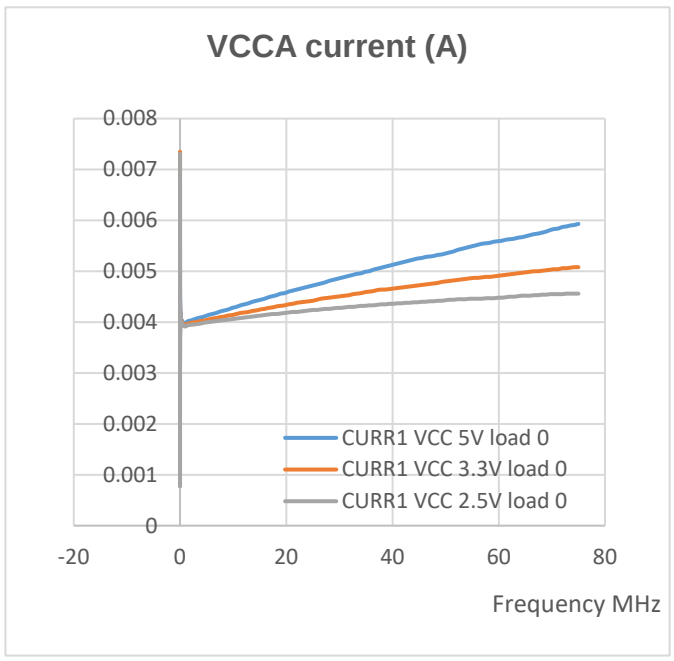


Figure 5. Supply Current vs Data Rate (With 15-pF Load)

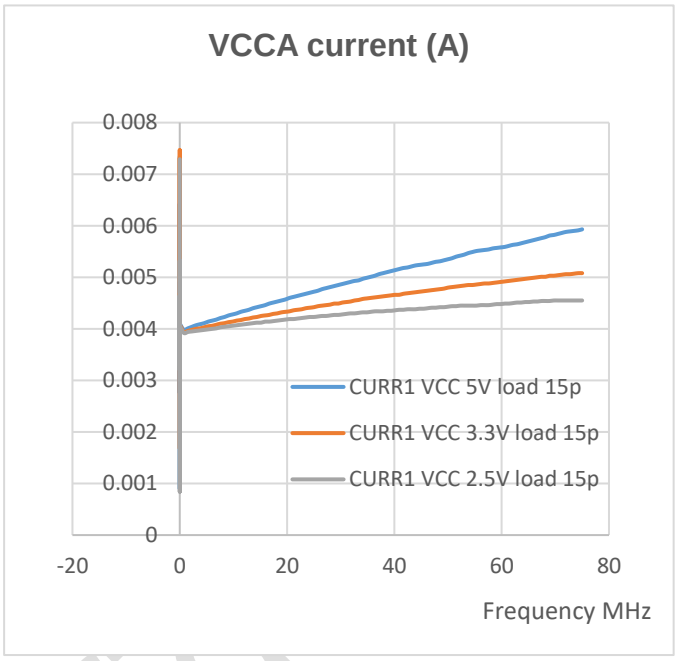


Figure 6. Supply Current vs Data Rate (With No Load)

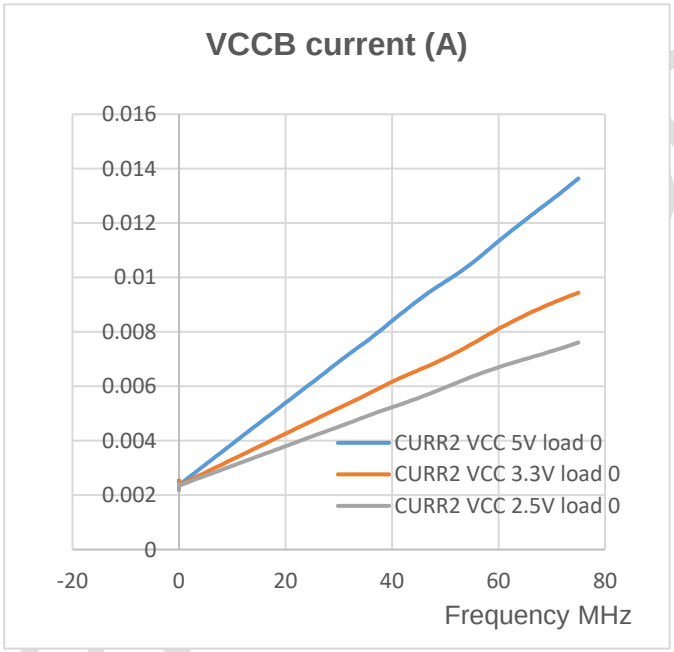


Figure 7. High-Level Output Voltage vs High-level Output Current

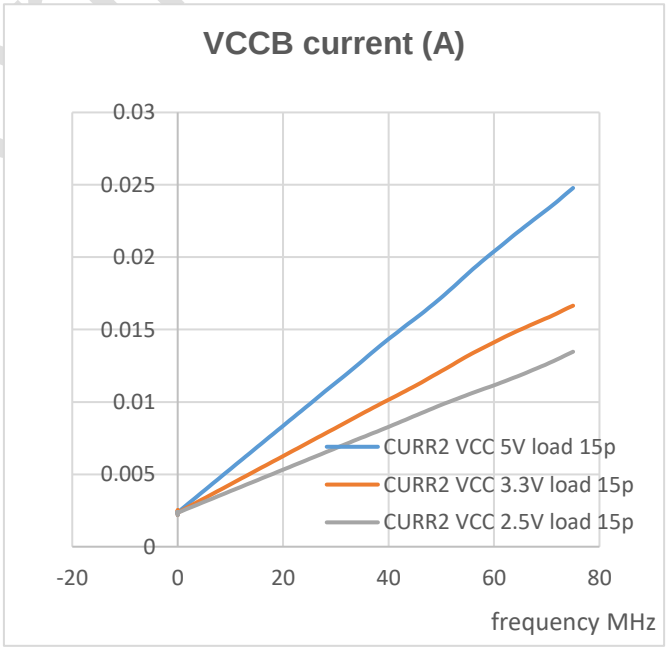


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

Test Circuits and Waveforms

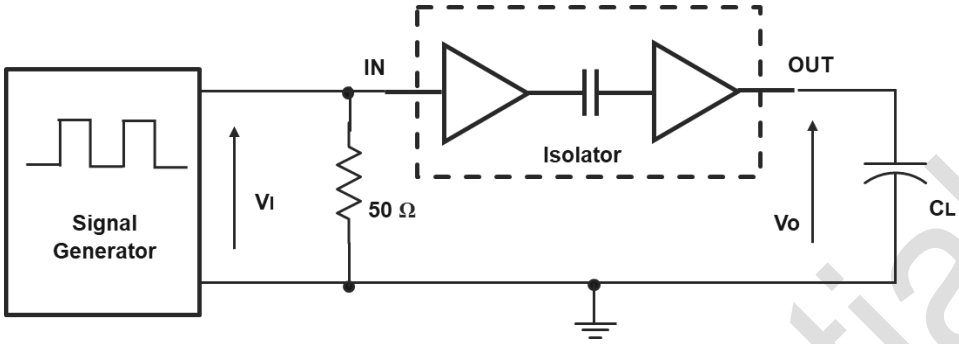


Figure 9. AC Characteristics Test Circuit

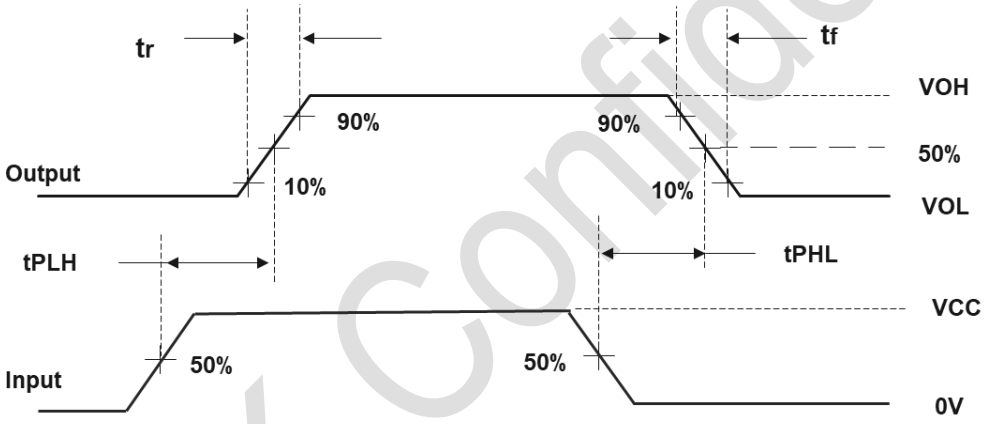


Figure 10. Timing Characteristics Voltage Waveforms

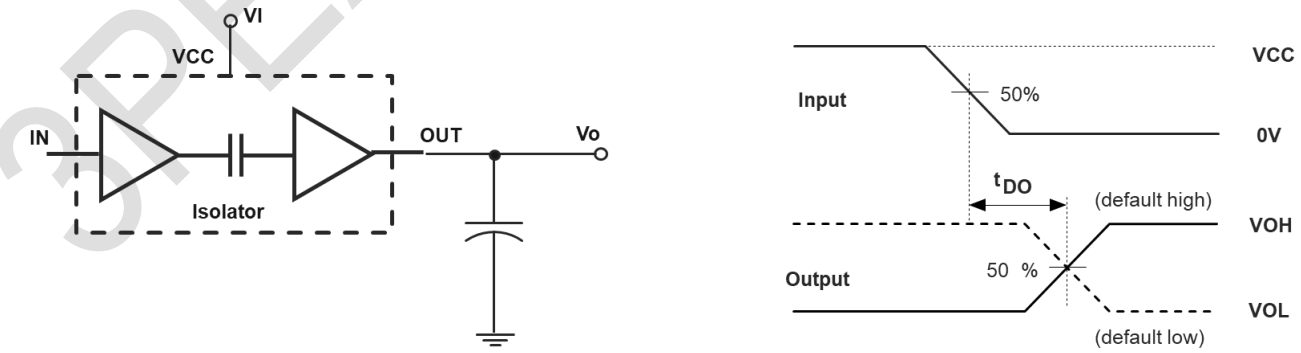


Figure 11. Default Output Delay Time Test Circuit and Voltage Waveforms

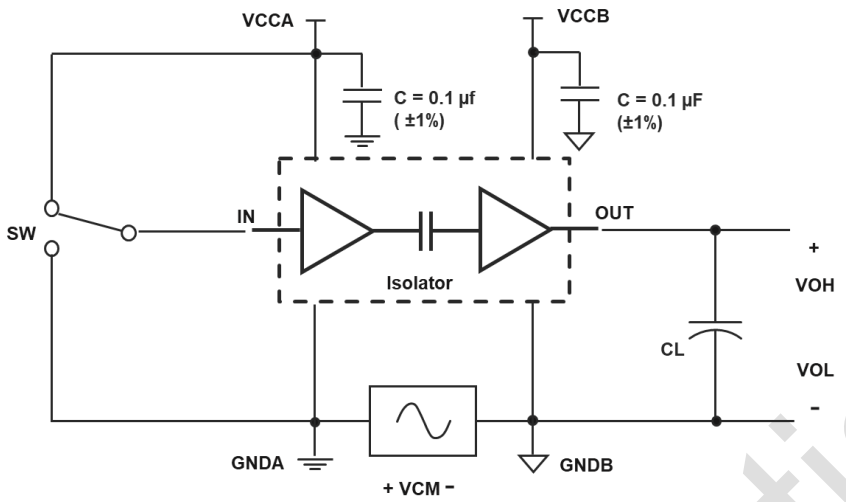


Figure 12. Common-Mode Transient Immunity Test Circuit

Theory of Operation

Overview

The TPT772x family design an ON-OFF keying (OOK) modulation circuit to transmit the digital data by the isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage, which build in a H-CMTI (High performance Common-mode transient immunity) circuit to protect the normal signal transmission and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The block diagram of a digital capacitive isolator shows a functional block diagram of a typical channel in Figure 13.

Functional Block Diagram

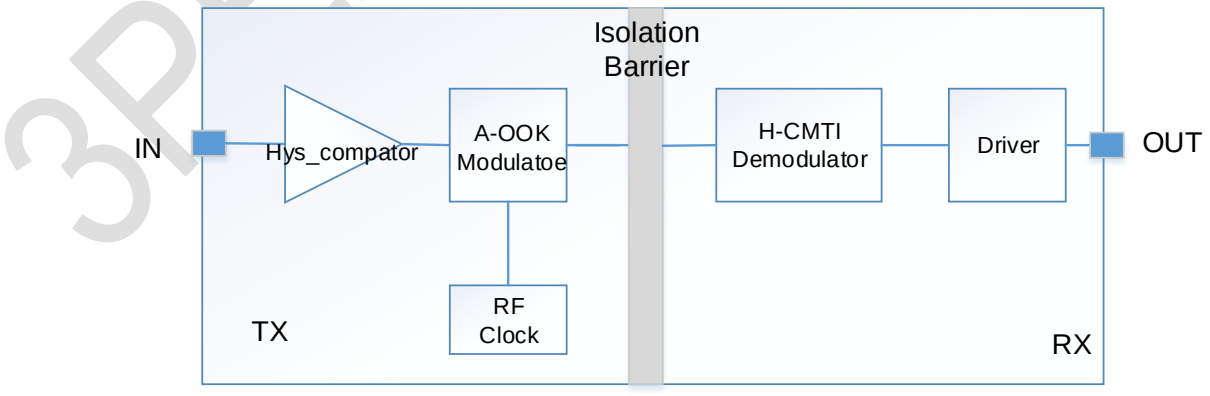


Figure 13. Conceptual Block Diagram of a Digital Capacitive Isolator

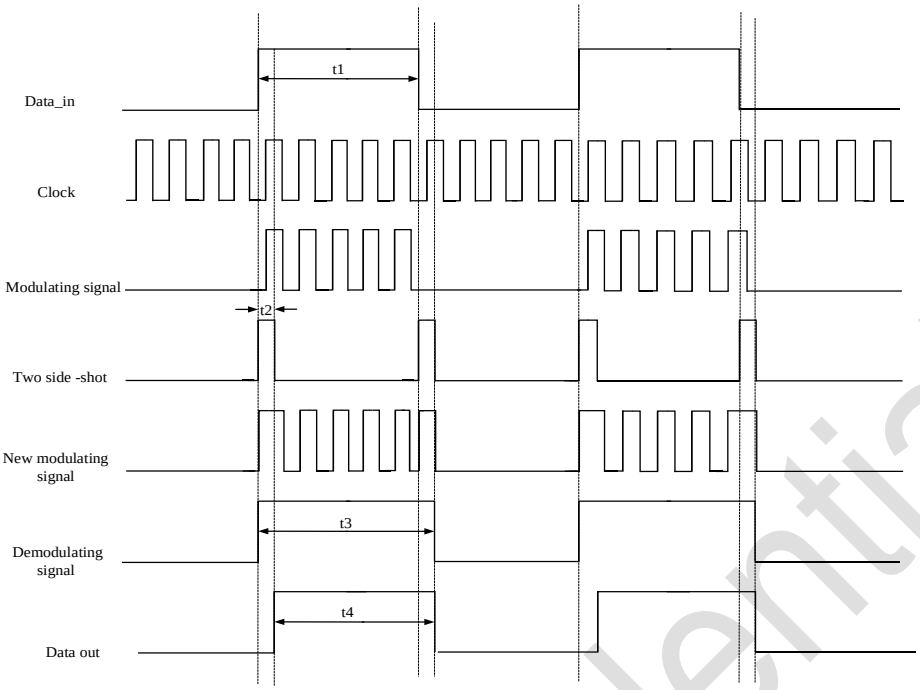


Figure 14. On-Off Keying (OOK) Based Modulation Scheme

Feature Description

The TPT772x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 14 lists the device features of the TPT772x devices.

Table 14. Device Features

Part Number	Max Data rate	Channel Direction	Default Output State	Package	Rating Isolation
TPT7720	150 Mbps	2 Forward, 0 Reverse	High	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				WSOP8	5000 V_{RMS} / 7071 V_{PK}
				SOP8	3750 V_{RMS} / 5250 V_{PK}
TPT7720F	150 Mbps	2 Forward, 0 Reverse	Low	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				WSOP8	5000 V_{RMS} / 7071 V_{PK}
				SOP8	3750 V_{RMS} / 5250 V_{PK}
TPT7721	150 Mbps	1 Forward, 1 Reverse	High	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				WSOP8	5000 V_{RMS} / 7071 V_{PK}
				SOP8	3750 V_{RMS} / 5250 V_{PK}
TPT7721F	150 Mbps	1 Forward, 1 Reverse	Low	WSOP16	5000 V_{RMS} / 8000 V_{PK}
				WSOP8	5000 V_{RMS} / 7071 V_{PK}
				SOP8	3750 V_{RMS} / 5250 V_{PK}

Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32 (new EMC standard). Although system-level performance and reliability depends on the application board design and layout, the TPT772x family integrates many chip-level design improvements for overall system robustness.

Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.

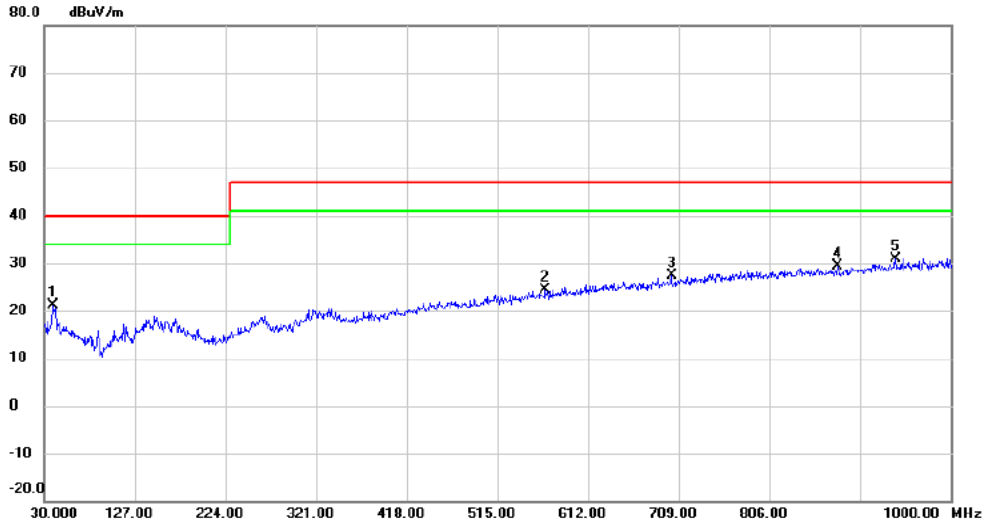


Figure15. Radiated Emission Measurement per CISPR32 Class-B -- Vertical

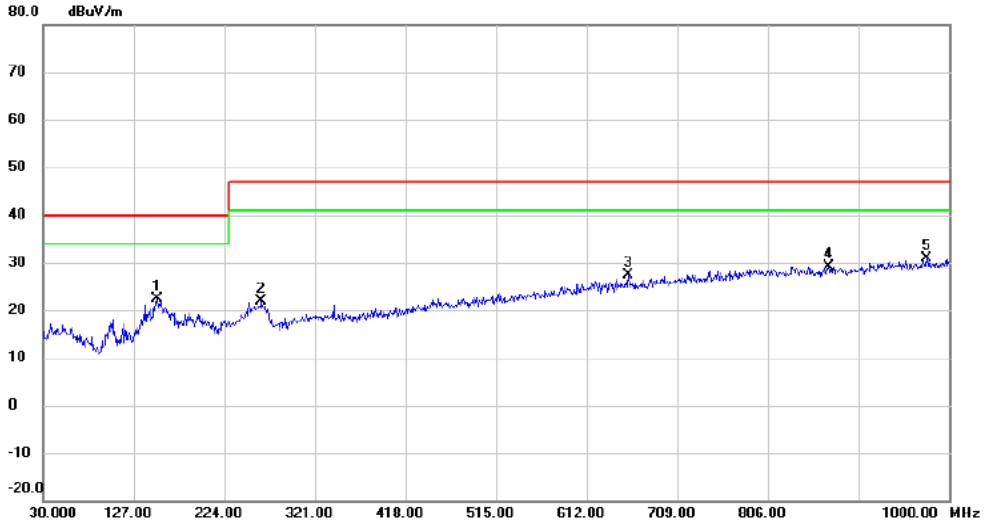


Figure16. Radiated Emission Measurement per CISPR32 Class-B -- Horizontal

Device Functional Modes

Table 15 lists the functional modes for the TPT772x devices.

Table 15. Function Table

VCC_I	VCC_O	Input (IN1, IN2)	Output (OUT1, OUT2)	Comments
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is High for TPT772x and Low for TPT772xF
PD	PU	X	Default	Default mode: When VCCI is unpowered, the default is High for TPT772x and Low for TPT772xF When VCCI transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When VCCI transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When VCCO is unpowered, a channel output is undetermined. When VCCO transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) VCC_I = Input-side VCCA; VCC_O = Output-side VCCB; PU = Powered up (VCC ≥ 2.25 V); PD = Powered down (VCC ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level

(2) The outputs are in undetermined state when 1.7 V < VCC_I, VCC_O < 2.25 V.

Application and Implementation

The following typical eye diagrams of the TPT7720 device indicate low jitter and wide open eye at the maximum data rate of 100 Mbps, and typical jitter is 736ps in lab test @5V and 25°C.

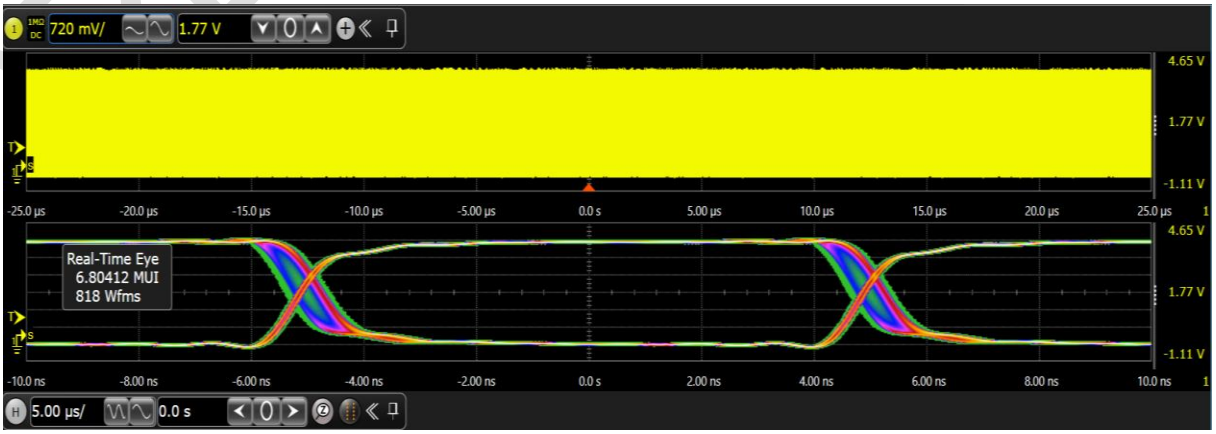
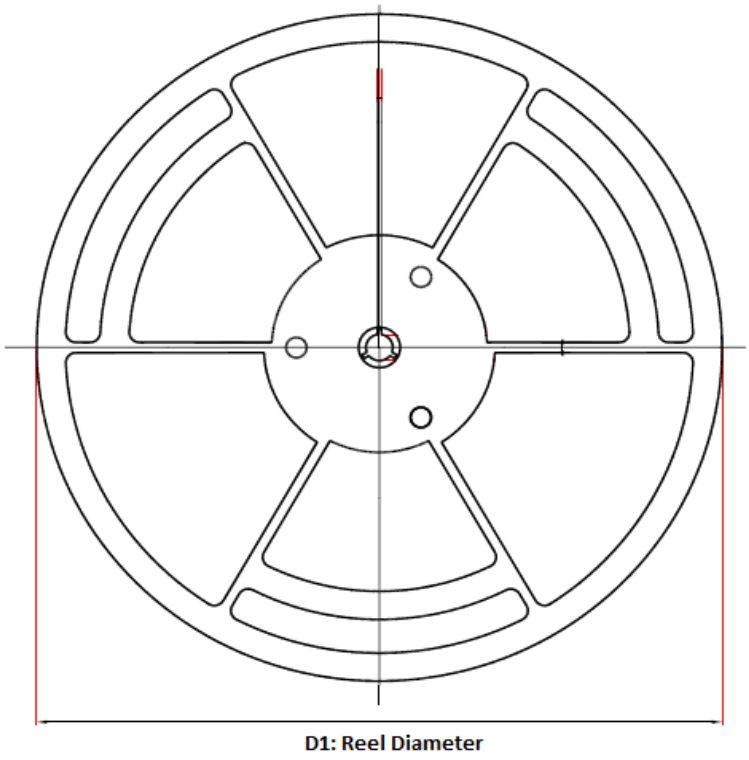
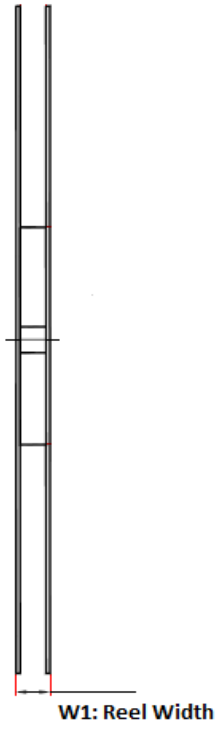
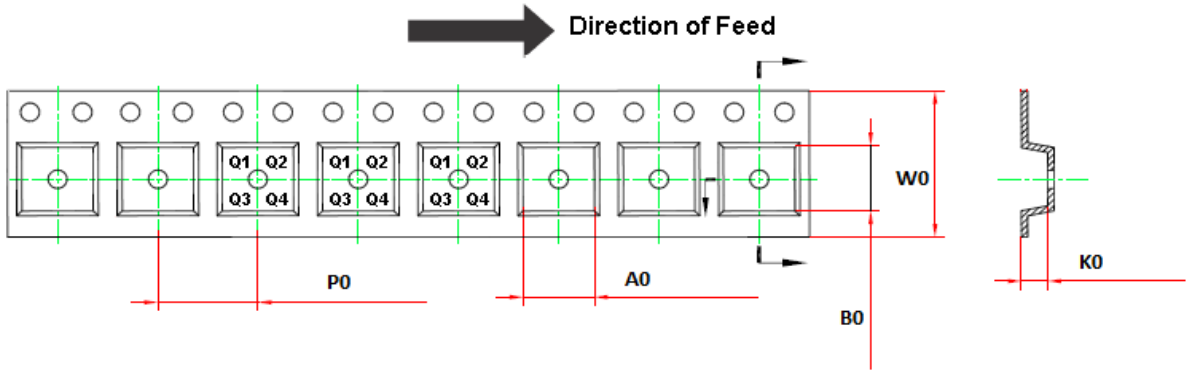


Figure 17. TPT7720 Eye Diagram at 100 Mbps PRBS, 5V Supplies and 25°C

Tape and Reel Information



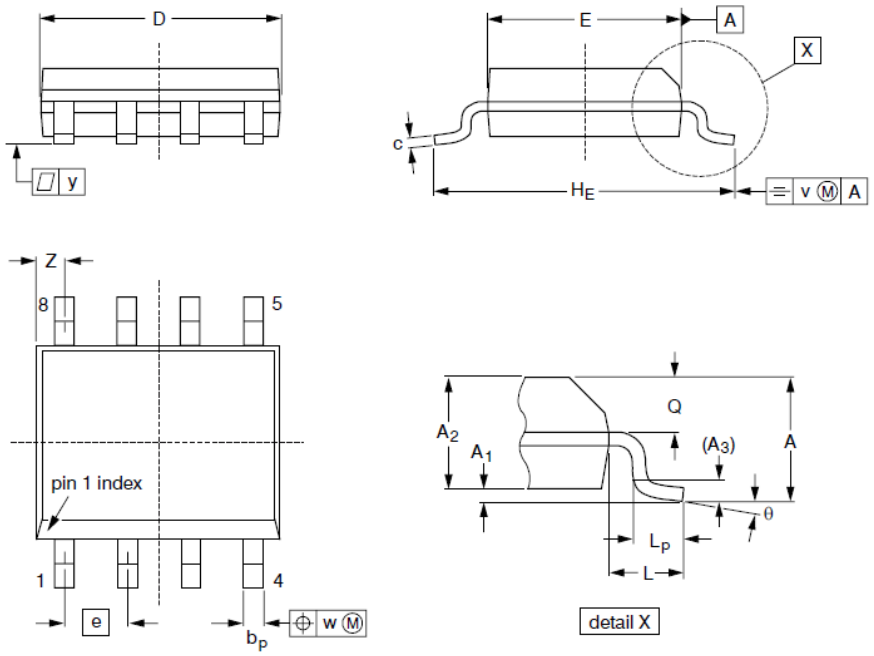




Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT7720-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPT7720F-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPT7721-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPT7721F-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SO1R (SOP8)



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	