CONTROL PORT AND RESET
OPERATION FOR BURR-BROWN
SoundPlus™ AUDIO CONVERTERS AND CODECS

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PURPOSE

This application bulletin provides operational details of the serial control port and reset functions for Burr-Brown digital audio data converters and CODECs. Specifically, this information applies to the PCM1716, PCM1717, PCM1719, PCM1720, PCM1723, PCM1727, PCM3000-series CODECs, and the PCM1800 A/D converter.

INTRODUCTION

Many of Burr-Brown's digital audio products include a three-wire serial control port for accessing special on-chip functions, such as digital attenuation, data format selection, soft mute, and output phase reversal.

For some devices, the control port is active only when Software mode is selected. The control port is inactive when these devices are operated in Hardware mode. For other devices, the control port is the only method available for changing the power-up default state. The operation of the serial control port is detailed in the next two sections. The last three sections of this document describe the proper reset of these devices when operated in Software and Hardware modes.

SERIAL CONTROL PORT OPERATION

Figure 1 shows a simplified block diagram of the serial control port. The port includes three input signals, named MC, ML, and MD. MC is the serial shift clock, used to clock data into the shift register inside the serial-to-parallel converter. MD is the serial control data, which is clocked into the serial-to-parallel converter one bit for every rising edge of the MC clock. Data is presented to the MD as a 16-bit serial word. ML is used to latch 16-bit data at the parallel output of the serial-to-parallel converter. A simplified timing diagram illustrating the control port operation is shown in Figure 2. A detailed timing diagram is presented in Figure 3.

As shown in Figure 3, in order to write 16 bits of data to the control port, the rising edge of ML must occur after the least significant bit (LSB) of MD has been clocked into the serial control port by MC. The timing parameter t_{MLH} defines the minimum time delay between MC rising edge (when data on MD is clocked into the serial-to parallel converter) and the low-to-high transition of ML, which latches the 16 bits of control data into the control port. Take a moment to study the remaining timing parameters listed in Figure 3, with special attention given to the minimum setup and hold time requirements.

Data can be written to the serial control port in either a continuous or burst (one-shot) fashion. Figure 4 shows examples for both techniques. Notice that there are two cases for ML for each example. You may use either case in your application.
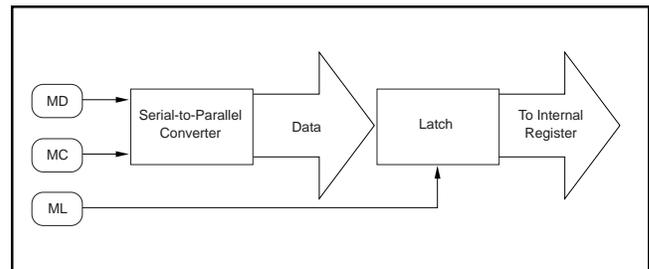

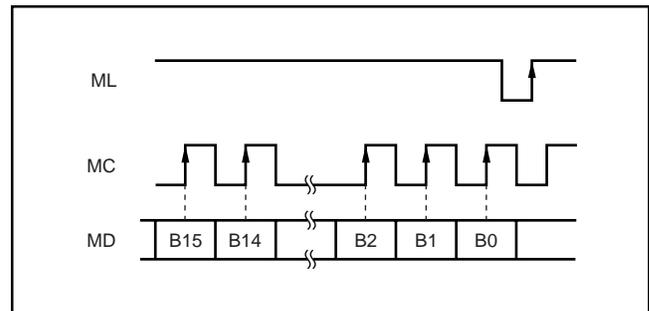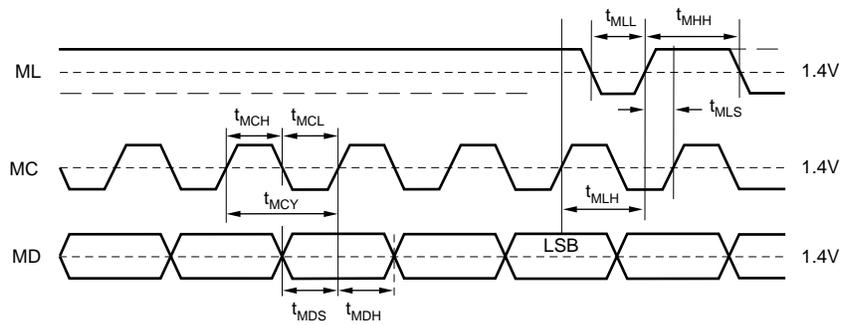FIGURE 1. Simplified Block Diagram of Serial Control Section.

FIGURE 2. Simplified Control Timing.

MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Set-up Time	t_{MDS}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
ML Low Level Time	t_{MLL}	40ns (min) + 1SYSCLK[1] (min)
ML Set-up Time	t_{MLS}	40ns (min)
ML Hold Time	t_{MLH}	40ns (min)
ML High Level Time	t_{MHH}	40ns (min) + 1SYSCLK[1] (min)

NOTE: (1) System Clock Period.

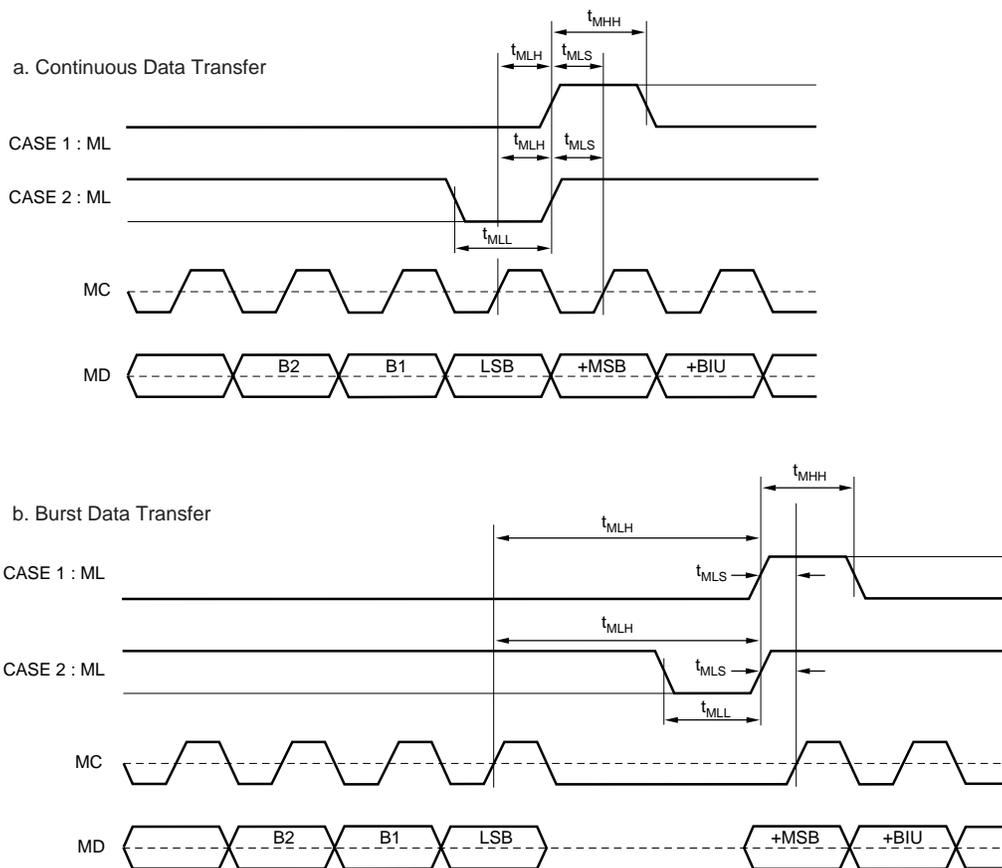FIGURE 3. Detailed Control Timing Diagram.

FIGURE 4. Continuous and Burst Transfer Examples.

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CONTROL PORT PROGRAMMING EXAMPLE

As an example of proper control port operation, the techniques used in the demonstration software included with Burr-Brown's PCM evaluation boards will be used. The software runs under Microsoft Windows 3.1, 95, or 98 and is written using Visual Basic. The software uses the parallel printer port of a PC to communicate with the control port of PCM products. The code for operating the control port is shown in Figure 5.

Data is passed to the TransmitData subroutine as a 16-bit word. The subroutine converts the 16-bit word to serial 16-bit, MSB-first data format and then outputs the data from the PC parallel port to the serial control port of the PCM device. In order to avoid noise on the ML, MC, and MD lines, ML is held HIGH during data transfer period and then goes LOW to HIGH to latch control data. Figure 6 shows the timing diagram generated using the code in Figure 5.

```
'
'    Subroutine TransmitData
'        Data: 16 bit mode register value
'
Sub TransmitData (ByVal Data As Integer)
        Dim iData As Long
        Dim Count As Integer
        Dim Dbit As Integer

        '    Transfer data from MSB to LSB

        iData = Data And &HFFFF&

        '    Repeat 16 times

        For Count = 0 to 15
            If (iData And &H8000&) = 0& Then
                Dbit = cLow
            Else
                Dbit = cHigh
            End If

            '    Data transfer at falling edge of MC
            '
            '            Usage OutputPort(ML, MC, MD)
            '
            Call OutputPort(cHigh, cLow, Dbit)
            Call OutputPort(cHigh, cHigh, Dbit)

            '    Shift 1bit to left for next transfer

            iData = (iData And &H7FFF) * &H2&

        Next Count

        '
        '    16bit data transfer finished and
        '    ML Output "H" -> "L" -> "H"
        '
        Call OutputPort(cHigh, cHigh, cHigh)
        Call OutputPort(cLow, cHigh, cHigh)
        Call OutputPort(cHigh, cHigh, cHigh)

End Sub
```

FIGURE 5. Code for Programming Example.

The timing diagram in Figure 7 shows an alternate approach, where ML is held LOW while transferring data to the port and then brought HIGH to latch the control data. Note that ML goes LOW before data transfer starts and then goes HIGH after data transfer is completed.

It is recommended that the user follow the techniques shown in Figures 6 and 7 to provide reliable control port operation.
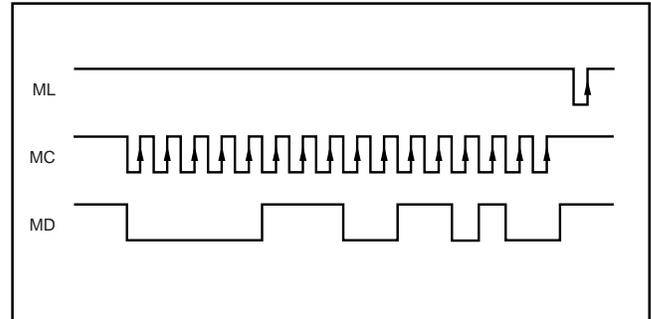
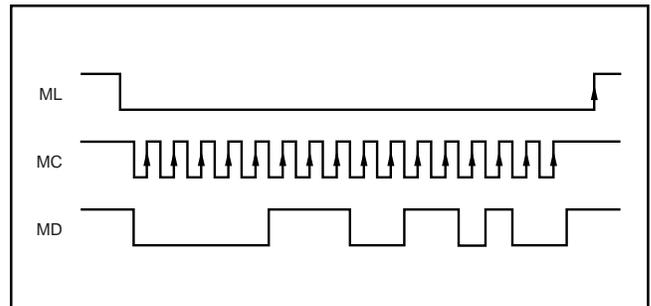FIGURE 6. Serial Control Timing Example.

FIGURE 7. Alternate Serial Control Timing Example.

RESET FOR SOFTWARE MODE

Using the serial control port to program device functions via on-chip registers is referred to in Burr-Brown PCM data sheets as Software mode. For some devices, this is the only way to set user-programmable functions. Other devices include a MODE pin which allows selection between Software and Hardware modes.

When using Software mode, the serial control section is enabled to accept data from the control port after the power-on reset or external reset initialization period has completed. Operating the MC, ML, and MD pins during the reset initialization period will not write the internal control registers. However, the serial-to-parallel converter in the control port is not initialized at reset, so it will accept data during the reset initialization period. This can cause invalid data to be written to internal control registers if ML goes HIGH without MC or MD being active after the initialization period is complete, or if the ML, MC, and MD signals are active when the device transitions from the reset initialization period to normal operation.

Figure 8 shows the Software mode timing for power-on and external reset, along with ML and MC timing related to technique #1 described below.

In order to avoid invalid data being written to the internal control registers immediately after the reset initialization period, one of two techniques is recommended.

1. Hold the ML and MC pin HIGH during the reset initialization period. This is the best way to ensure that invalid data is not clocked into the serial-to-parallel converter and latch.

2. Wait a sufficient period of time for the reset initialization period to complete, then send 16 bits of valid control data using MC and MD and provide a LOW to HIGH transition on ML to latch the valid data.

In addition to these techniques, the system designer should arrange the PCB layout to minimize noise on the ML, MC, and MD lines.

RESET FOR D/A CONVERTERS OPERATED IN HARDWARE MODE

For Hardware mode reset of PCM D/A converters, refer to the external and internal reset timing shown in Figure 8. ML and MC are ignored or redefined for Hardware mode operation.

RESET FOR PCM1800, PCM3001, PCM3003, AND PCM3006

The devices listed for this section are Hardware mode only devices. They have a special consideration for proper reset to occur. These devices require that system clock (SYSCLK) be running for a minimum of three SYSCLK periods before V_{CC} and V_{DD} exceeds 2.2V for the PCM3003 or PCM3006, and before V_{CC} and V_{DD} exceeds 4.0V for the PCM1800 and PCM3001. This is shown in Figure 9.

This requirement explicitly requires the digital section of the system, which provides the SYSCLK, to power up slightly before the A/D or CODEC section reaches the threshold voltage mentioned in the previous paragraph. This requirement must be taken into consideration when implementing the power supply design for the system application.

SUMMARY

In this document, the proper operation of the serial control port and reset conditions has been presented to aid the systems designer in the proper application of Burr-Brown's PCM digital audio products. This information, along with applications sections of the corresponding product data sheets, should be utilized to ensure optimal performance and operation of Burr-Brown products in real-world applications.
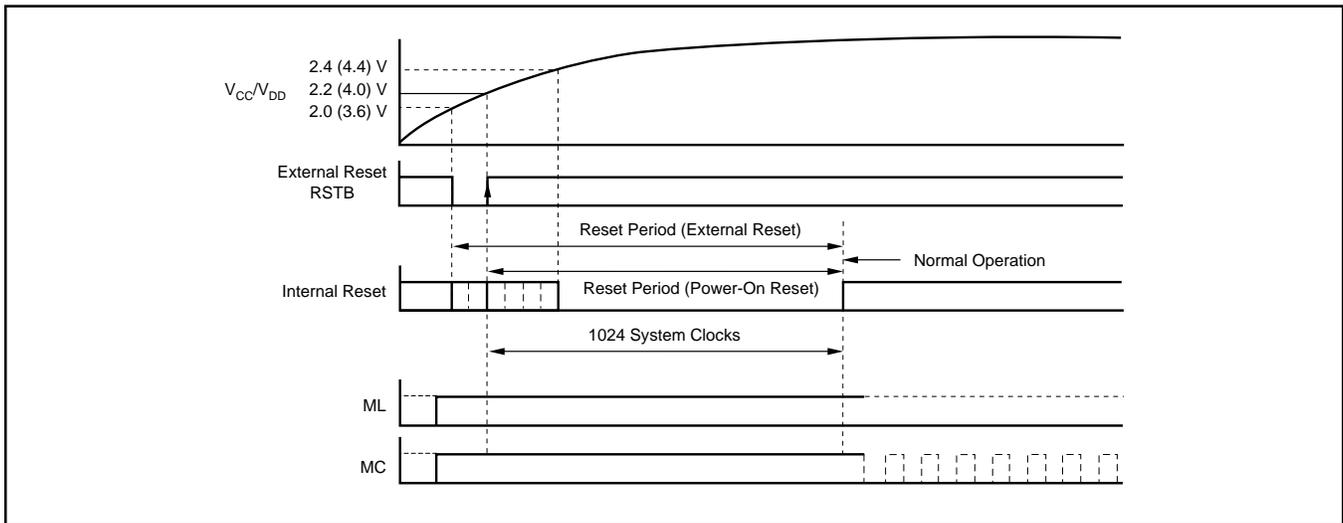

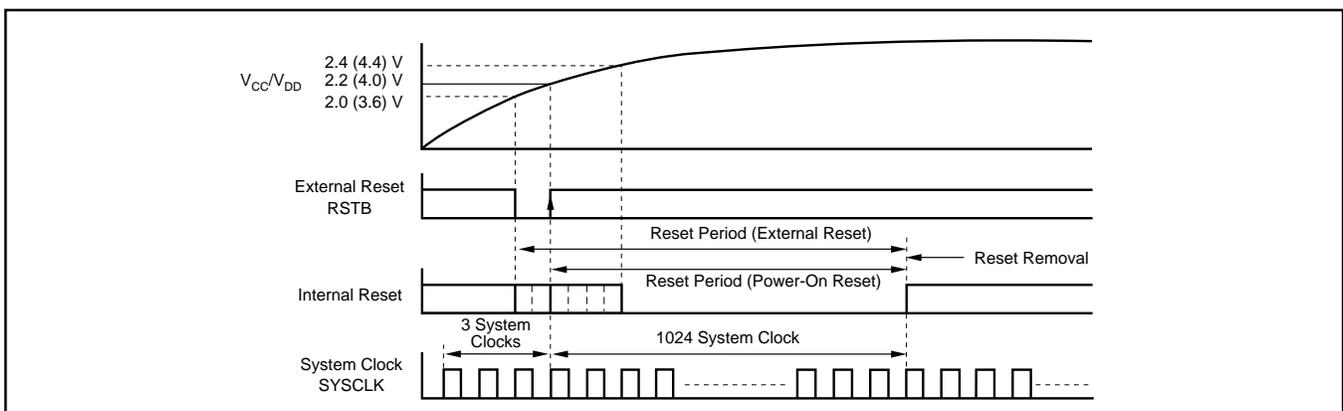FIGURE 8. Reset Timing for Software Mode.

FIGURE 9. Reset Timing for PCM1800, PCM3001, PCM3003, and PCM3006.

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