BiCMOS ADVANCED PHASE-SHIFT PWM CONTROLLER

Check for Samples: UCC2895-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Programmable Output Turn-On Delay**
- **Bidirectional Oscillator Synchronization**
- **Voltage-Mode, Peak-Current-Mode, or Average-Current-Mode Control**
- **Programmable Soft Start/Soft Stop and Chip Disable Via a Single Pin**
- **0% to 100% Duty-Cycle Control**
- **7-MHz Error Amplifier**
- **Operation to 1 MHz**
- **Typical 5-mA Operating Current at 500 kHz**
- **Very Low 150-µA Current During Undervoltage Lockout (UVLO)**

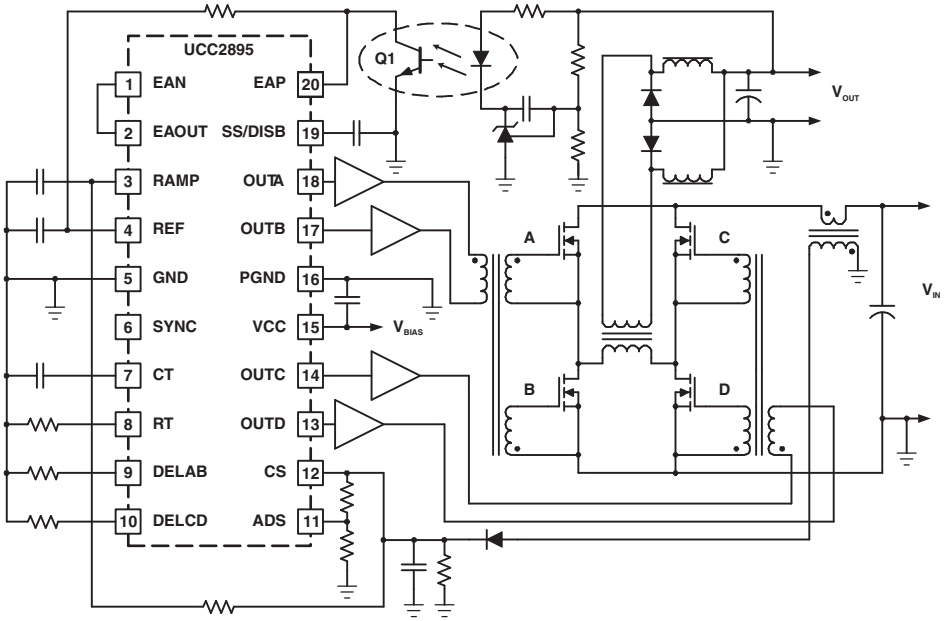
APPLICATIONS

- **Phase-Shifted Full-Bridge Converters**
- **Off-Line, Telecom, Datacom, and Servers**
- **Distributed Power Architecture**
- **High-Density Power Modules**

DESCRIPTION

The UCC2895-Q1 is a phase-shift pulse-width modulation (PWM) controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant-frequency PWM in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The device can be used either as a voltage-mode or current-mode controller.

Although the UCC2895-Q1 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Because it is built using the BCDMOS process, it operates with dramatically less supply current than its bipolar counterparts. The UCC2895-Q1 can operate with a maximum clock frequency of 1 MHz.

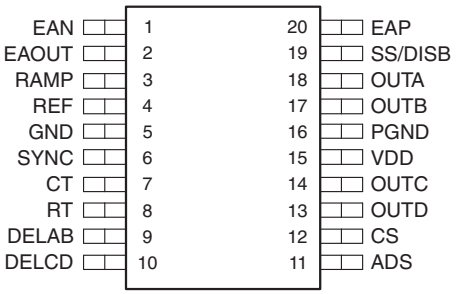


ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – DW	Reel of 2000	UCC2895QDWRQ1	UCC2895Q

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DW PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)

T_A = –40°C to 125°C, all voltage values are with respect to the network ground terminal (unless otherwise noted)

			VALUE
V_{DD}	Supply voltage	I_{DD} < 10 mA	17 V
I_{DD}	Supply current		30 mA
I_{REF}	Reference current		15 mA
I_O	Output current		100 mA
	Analog input voltage range	EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB	–0.3 V to REF + 0.3 V
	Drive output voltage range	OUTA, OUTB, OUTC, OUTD	–0.3 V to VDD + 0.3 V
P_D	Power dissipation	T_A = 25°C	650 mW
T_{stg}	Storage temperature range		–65°C to 150°C
T_J	Junction temperature range		–55°C to 150°C
ESD	Electrostatic discharge protection	Human-body model (HBM)	800 V
		Machine model (MM)	200 V
		Charged-device model (CDM)	2000 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		10		16.5	V
C_{VDD}	Supply voltage bypass capacitor(2)			10 × C_{REF}		µF
C_{REF}	Reference bypass capacitor(3)		0.1		4.7	µF
C_T	Timing capacitor	For 500-kHz switching frequency		220		pF
R_T	Timing resistor	For 500-kHz switching frequency		82		kΩ

(1) It is recommended that there be a single point grounded between GND and PGND directly under the device. There should be a separate ground plane associated with the GND pin and all components associated with pins 1 through 12 plus 19 and 20 should be located over this ground plane. Any connections associated with these pins to ground should be connected to this ground plane.
(2) The V_{DD} capacitor should be a low-ESR, -ESL ceramic capacitor located directly across the VDD and PGND pins. A larger bulk capacitor should be located as physically close as possible to the V_{DD} pins.
(3) The V_{REF} capacitor should be a low-ESR, -ESL ceramic capacitor located directly across the REF and GND pins. If a larger capacitor is desired for V_{REF}, then it should be located near the V_{REF} capacitor and connected to the V_{REF} pin with a resistor of 51 Ω or greater. The bulk capacitor on VDD must be a factor of 10 geater than the total V_{REF} capacitance.

RECOMMENDED OPERATING CONDITIONS(1) (continued)

		MIN	NOM	MAX	UNIT
R_{DEL_AB} R_{DEL_CD}	Delay resistor	2.5		40	kΩ
T_J	Operating junction temperature(4)	–55		125	°C

(4) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF, no load on the outputs, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage Lockout (UVLO)						
$UVLO_{(on)}$	Start-up voltage threshold		10.2	11	11.8	V
$UVLO_{(off)}$	Minimum operating voltage after start-up		8.2	9	9.8	V
$UVLO_{(hys)}$	Hysteresis		1	2	3	V
Supply						
I_{START}	Start-up current	V_{DD} = 8 V		150	250	µA
I_{DD}	Operating current			5	6	mA
V_{DD_CLAMP}	VDD clamp voltage	I_{DD} = 10 mA	16.5	17.5	18.5	V
Voltage Reference						
V_{REF}	Output voltage	T_J = 25°C	4.94	5	5.06	V
		10 V < V_{DD} < V_{DD_CLAMP}, 0 mA < I_{REF} < 5 mA, T_J = –40°C to 125°C	4.85	5	5.15	
I_{SC}	Short-circuit current	REF = 0 V, T_J = 25°C	10	20		mA
Error Amplifier						
	Common-mode input voltage		–0.1		3.6	V
V_{IO}	Offset voltage		–7		7	mV
I_{BIAS}	Input bias current (EAP, EAN)		–1		1	µA
V_{OH_EAOUT}	High-level output voltage	EAP – EAN = 500 mV, I_{EAOUT} = –0.5 mA	4	4.5	5	V
V_{OL_EAOUT}	Low-level output voltage	EAP – EAN = –500 mV, I_{EAOUT} = 0.5 mA	0	0.2	0.4	V
I_{SOURCE}	Error amplifier output source current	EAP – EAN = 500 mV, EAOUT = 2.5 V	1	1.5		mA
I_{SINK}	Error amplifier output sink current	EAP – EAN = –500 mV, EAOUT = 2.5 V	2.5	4.5		mA
A_{VOL}	Open-loop dc gain		75	85		dB
GBW	Unity gain bandwidth(1)		5	7		MHz
	Slew rate(1)	1 V < EAN < 0 V, EAP = 500 mV, 0.5 V < EAOUT < 3 V	1.5	2.2		V/µs
	No-load comparator turn-off threshold		0.45	0.5	0.55	V
	No-load comparator turn-on threshold		0.55	0.6	0.69	V
	No-load comparator hysteresis		0.035	0.1	0.165	V
Oscillator						
f_{OSC}	Frequency	T_J = 25°C	473	500	527	kHz
	Frequency total variation(1)	Over line and temperature		2.5%	5%	
V_{IH_SYNC}	High-level input voltage, SYNC		2.05	2.1	2.4	V
V_{OH_SYNC}	High-level input voltage, SYNC	I_{SYNC} = –400 µA, V_{CT} = 2.6 V	4.1	4.5	5	V
V_{OL_SYNC}	Low-level output voltage, SYNC	I_{SYNC} = 100 µA, V_{CT} = 2.6 V	0	0.5	1	V
	SYNC output pulse width	$LOAD_{SYNC}$ = 3.9 kΩ and 30 pF in parallel		85	135	ns
V_{RT}	Timing resistor voltage		2.9	3	3.1	V
$V_{CT(peak)}$	Timing capacitor peak voltage		2.25	2.35	2.55	V
$V_{CT(valley)}$	Timing capacitor valley voltage		0	0.2	0.4	V

(1) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF, no load on the outputs, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense						
$I_{CS(bias)}$	Current sense bias current	0 V < CS < 2.5 V, 0 V ADS < 2.5 V	–4.5		20	µA
	Peak current threshold		1.9	2	2.1	V
	Overcurrent threshold		2.4	2.5	2.6	V
	Current sense to output delay	0 V ≤ CS ≤ 2.3 V, DELAB = DELCD = REF		75	110	ns

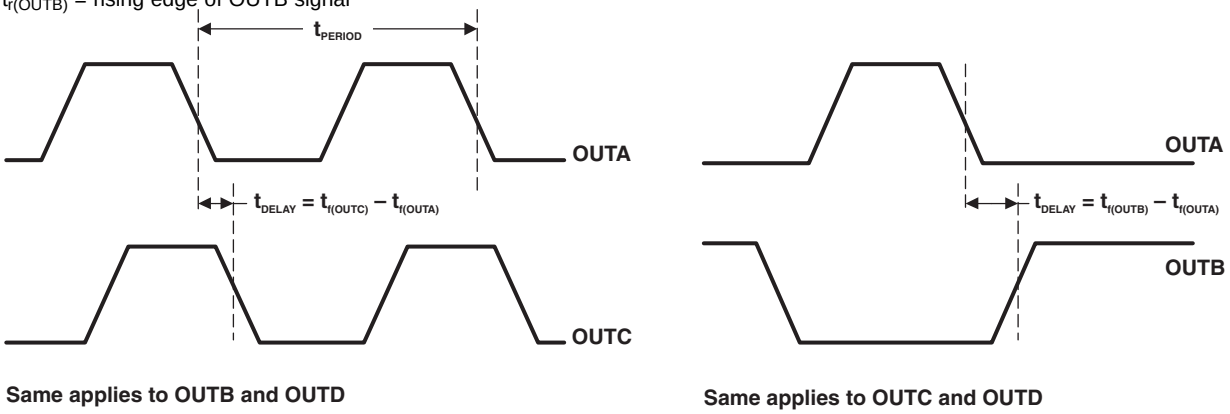
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF, no load on the outputs, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start/Shutdown						
I_{SOURCE}	Soft-start source current	SS/DISB = 3 V, CS = 1.9 V	–40	–35	–30	µA
I_{SINK}	Soft-start sink current	SS/DISB = 3 V, CS = 2.6 V	325	350	375	µA
	Soft-start/disable comparator threshold		0.44	0.5	0.56	V
Adaptive Delay Set (ADS)						
	DELAB/DELCD output voltage	ADS = CS = 0 V	0.45	0.5	0.55	V
		ADS = 0 V, CS = 2 V	1.9	2	2.1	
t_{DELAY}	Output delay(2) (3)	ADS = CS = 0 V	450	560	620	ns
	ADS bias current	0 V < ADS < 2.5 V, 0 V < CS < 2.5 V	–20		20	µA
Output						
V_{OH}	High-level output voltage (all outputs)	I_{OUT} = –10 mA, VDD to output		250	420	mV
V_{OL}	Low-level output voltage (all outputs)	I_{OUT} = 10 mA		150	270	mV
t_R	Rise time(2)	C_{LOAD} = 100 pF		20	35	ns
t_F	Fall time(2)	C_{LOAD} = 100 pF		20	35	ns

(2) Specified by design

(3) Output delay is measured between OUTA and OUTB or between OUTC and OUTD. Output delay is defined as shown in the following figure, where:
$t_{f(OUTA)}$ = falling edge of OUTA signal
$t_{r(OUTB)}$ = rising edge of OUTB signal



ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF, no load on the outputs, $T_A = T_J$ = –40°C to 125°C (unless otherwise noted)

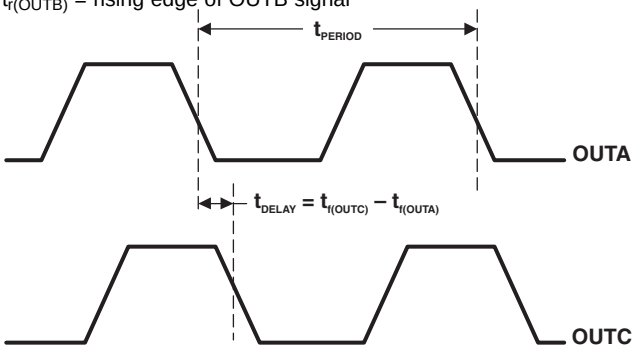
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM Comparator						
	EAOUT to RAMP input offset voltage	RAMP = 0 V, DELAB = DELCD = REF	0.7	0.85	1.05	V
	Minimum phase shift(4) (OUTA to OUTC, OUTB to OUTD)	RAMP = 0 V, EAOUT = 650 mV	0	0.85%	1.5%	
t_{DELAY}	Delay(5) (RAMP to OUTC, RAMP to OUTD)	0 V < RAMP < 2.5 V, EAOUT = 1.2 V, DELAB = DELCD = REF		70	120	ns
$I_{R(bias)}$	RAMP bias current	RAMP < 5 V, CT = 2.2 V	–5		5	µA
$I_{R(sink)}$	RAMP sink current	RAMP = 5 V, CT = 2.6 V	11	19		mA

(4) Minimum phase shift is defined as:

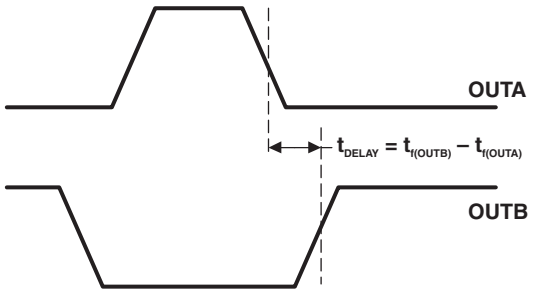
$$\Phi = 180 \times \frac{t_{f\,(OUTC)} - t_{f\,(OUTA)}}{t_{PERIOD}} \quad \text{or} \quad \Phi = 180 \times \frac{t_{f\,(OUTC)} - t_{f\,(OUTB)}}{t_{PERIOD}}$$

where:
$t_{f(OUTA)}$ = falling edge of OUTA signal
$t_{f(OUTB)}$ = falling edge of OUTB signal
$t_{f(OUTC)}$ = falling edge of OUTC signal
$t_{f(OUTD)}$ = falling edge of OUTD signal
t_{PERIOD} = period of OUTA or OUTB signal

(5) Output delay is measured between OUTA and OUTB or between OUTC and OUTD. Output delay is defined as shown in the following figure, where:
$t_{f(OUTA)}$ = falling edge of OUTA signal
$t_{r(OUTB)}$ = rising edge of OUTB signal



Same applies to OUTB and OUTD

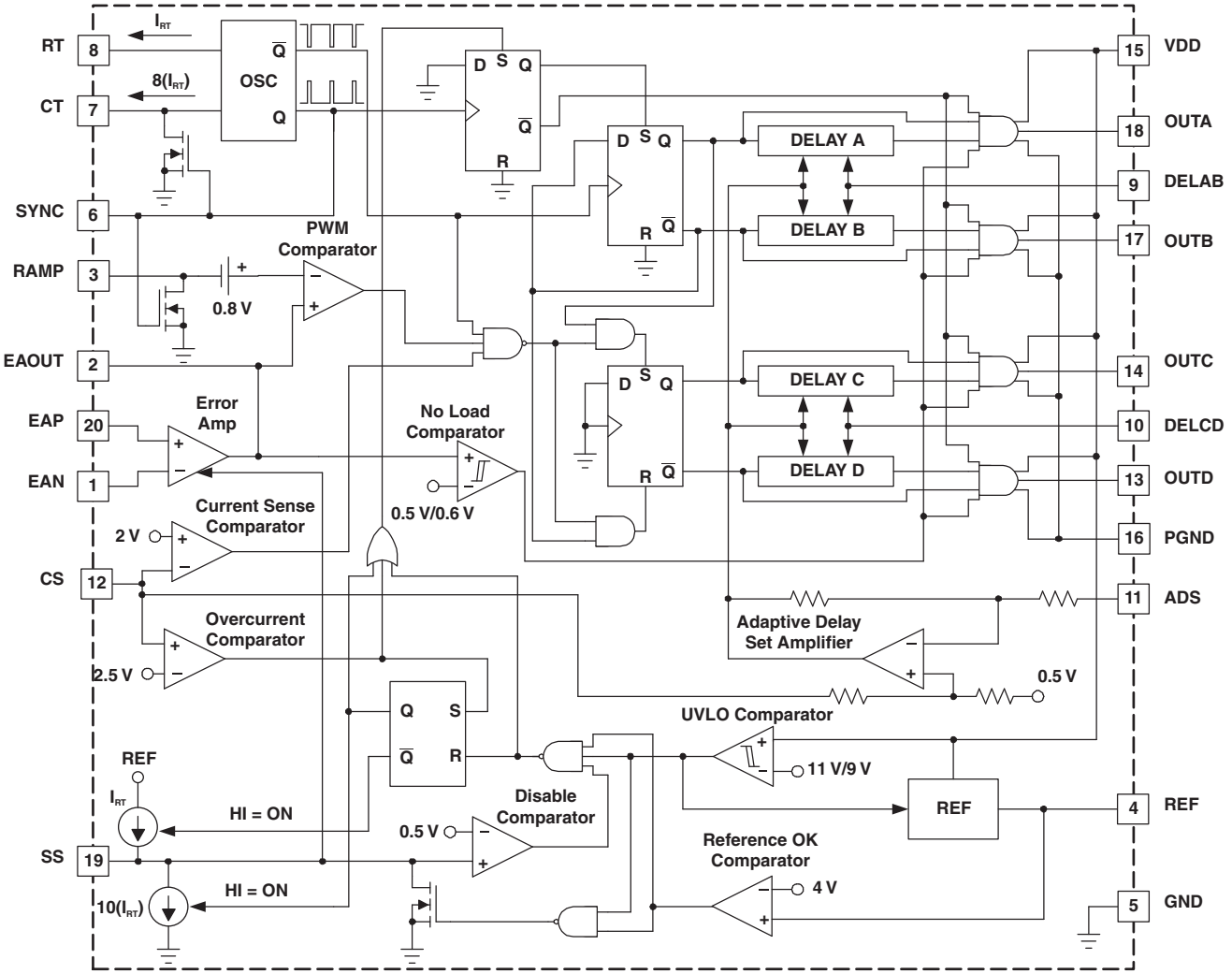


Same applies to OUTC and OUTD

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADS	11	I	Adaptive delay set. Sets the ratio between the maximum and minimum programmed output delay dead time.
CS	12	I	Current-sense input for cycle-by-cycle current limiting and for overcurrent comparator
CT	7	I	Oscillator timing capacitor for programming the switching frequency. The oscillator charges CT via a programmed current.
DELAB	9	I	Delay programming between complementary outputs. DELAB programs the dead time between switching of output A and output B.
DELCD	10	I	Delay programming between complementary outputs. DELCD programs the dead time between switching of output C and output D.
EAOUT	2	I/O	Error amplifier output
EAP	20	I	Noninverting input to the error amplifier. Keep below 3.6 V for proper operation.
EAN	1	I	Inverting input to the error amplifier. Keep below 3.6 V for proper operation.
GND	5	–	Ground for all circuits except the output stages
OUTA	18	O	The four outputs are 100-mA CMOS drivers and are optimized to drive FET driver circuits such as the UCC27424 or gate-drive transformers.
OUTB	17	O	
OUTC	14	O	
OUTD	13	O	
PGND	16	–	Output-stage power ground
RAMP	3	I	Inverting input of the PWM comparator
REF	4	O	5-V ± 1.2% 5-mA voltage reference. For best performance, bypass with a 0.1-µF low-ESR low-ESL capacitor to ground. Do not use more than 1 µF of total capacitance on this pin.
RT	8	I	Oscillator timing resistor for programming the switching frequency
SS/DISB	19	I	Soft start/disable. This pin combines two independent functions.
SYNC	6	I/O	Oscillator synchronization. This pin is bidirectional.
VDD	15	I	Power-supply input. VDD must be bypassed with a minimum of a 1-µF low-ESR low-ESL capacitor to ground.

FUNCTIONAL BLOCK DIAGRAM



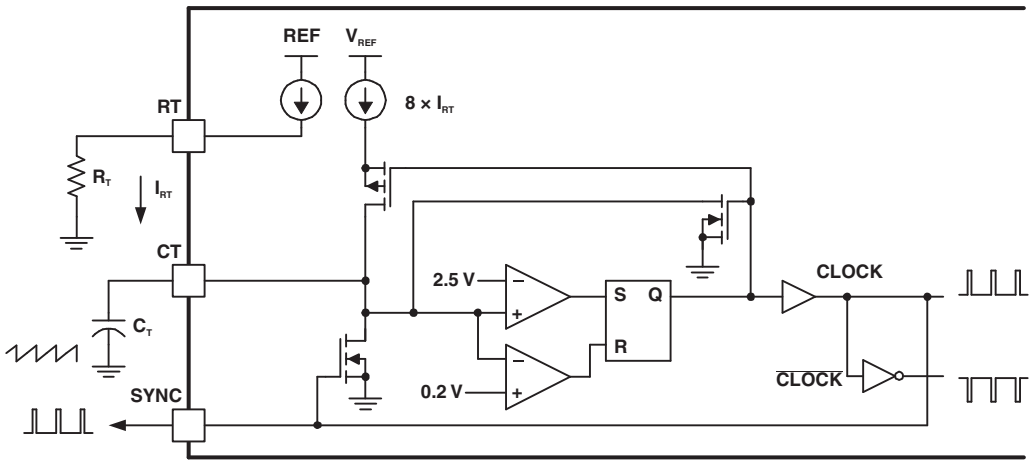


Figure 1. Oscillator Block Diagram

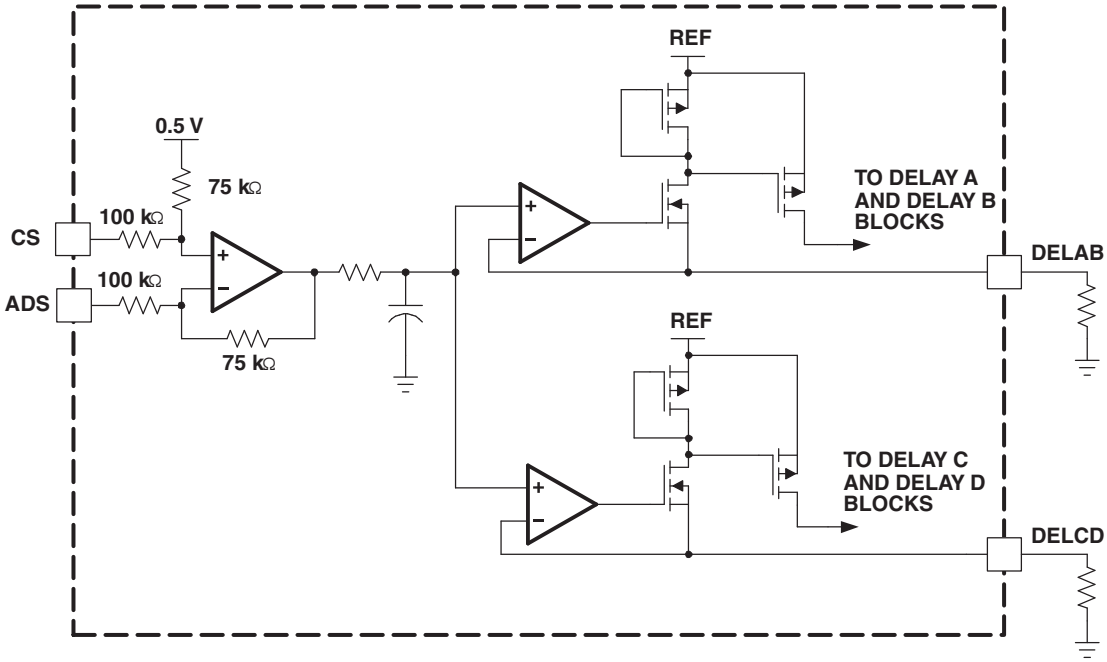


Figure 2. Adaptive Delay Setting Block Diagram

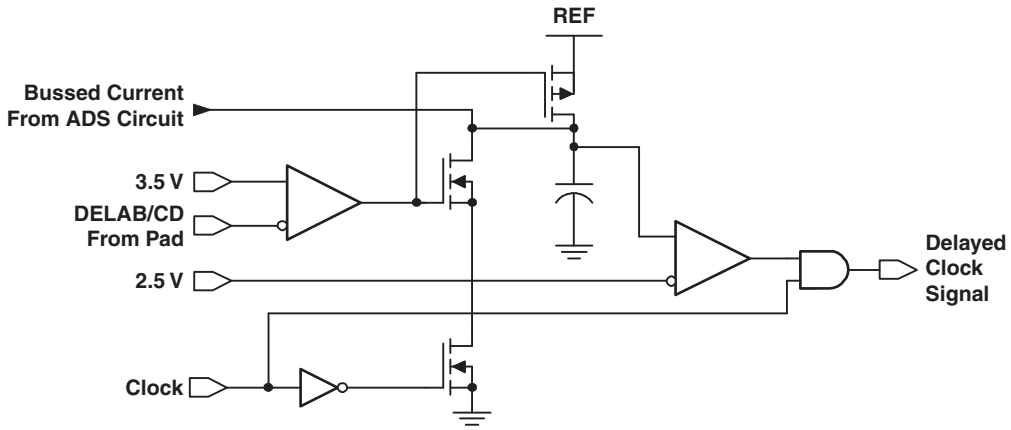


Figure 3. Delay Block Diagram (One Delay Block Per Outlet)

DETAILED PIN DESCRIPTIONS

Adaptive Delay Set (ADS)

This function sets the ratio between the maximum and minimum programmed output-delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2 V (the peak-current threshold); ADS changes the output voltage on the delay pins DELAB and DELCD by Equation 1:

$$V_{DEL} = [0.75 \times (V_{CS} - V_{ADS})] + 0.5\ V \quad (1)$$ (1)

where V_{CS} and V_{ADS} are in volts. ADS must be limited to between 0 V and 2.5 V and must be less than or equal to CS. DELAB and DELCD are clamped to a minimum of 0.5 V.

Current Sense (CS)

CS is the inverting input of the current-sense comparator and the noninverting input of the overcurrent comparator and the ADS amplifier. The current-sense signal is used for cycle-by-cycle current limiting in peak-current mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called soft stop, with full soft start.

Oscillator Timing Capacitor (CT)

The oscillator charges CT via a programmed current. The waveform on CT is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by Equation 2:

$$t_{OSC} = [(5 \times R_T \times C_T)/48] + 120\ ns \quad (2)$$ (2)

where C_T is in farads, R_T is in Ω, and t_{OSC} is in seconds. C_T can range from 100 pF to 880 pF.

NOTE

A large C_T and a small R_T combination results in extended fall times on the CT waveform. The increased fall time increases the SYNC pulse duration, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter (see Figure 1).

Delay Programming Between Complementary Outputs (DELAB, DELCD)

DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC2895N allows the user to select the delay, during which the resonant switching of the external power stages takes place. Separate delays are provided for the two half bridges to accommodate differences in resonant-capacitor charging currents. The delay in each stage is set according to Equation 3:

$$t_{DELAY} = [(25 \times 10^{-12} \times R_{DEL})/V_{DEL}] + 25\ ns \quad (3)$$ (3)

where V_{DEL} is in volts, R_{DEL} is in ohms, and t_{DELAY} is in seconds. DELAB and DELCD can source approximately 1 mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay is defeated by tying DELAB and/or DELCD to REF. For optimum performance, keep stray capacitance on these pins at less than 10 pF.

Error Amplifier (EAOUT, EAP, EAN)

EAOUT is connected internally to the noninverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft-start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500 mV, and allows the outputs to turn on again when EAOUT rises above 600 mV.

EAP is the noninverting input and the EAN is the inverting input to the error amplifier.

Output MOSFET Drivers (OUTA, OUTB, OUTC, OUTD)

The four outputs are 100-mA CMOS drivers and are optimized to drive MOSFET driver circuits. OUTA and OUTB are fully complementary, assuming no programming delay. They operate near 50% duty cycle and one-half the oscillator frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD drive the other half-bridge circuit and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB.

NOTE

Changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

Power Ground (PGND)

To keep output switching noise from critical analog circuits, the UCC2895-Q1 has two different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, because PGND carries high current, board traces must be low-impedance.

Inverting Input of the PWM Comparator (RAMP)

This pin receives either the CT waveform in voltage control and average-current-mode control or the current signal (plus slope compensation) in peak-current-mode control.

Voltage Reference (REF)

The 5 V ± 1.2% reference supplies power to internal circuitry, and can also supply up to 5 mA to external loads. The reference is shut down during undervoltage lockout (UVLO) but is operational during all other disable modes. For best performance, bypass with a 0.1-µF low-ESR low-ESL capacitor to GND. Do not use more than 1 µF of total capacitance on this pin to ensure the stability of the internal reference.

Oscillator Timing Resistor (RT)

The oscillator operates by charging an external timing capacitor (C_T) with a fixed current programmed by R_T. R_T current is calculated by Equation 4:

$$I_{RT}(A) = 3\ V / R_T\ (\Omega) \quad (4)$$

R_T can range from 40 kΩ to 120 kΩ. Soft-start charging and discharging currents are also programmed by I_{RT} (see Figure 1).

Analog Ground (GND)

This pin is the ground for all internal circuits except the output stages.

Soft Start/Disable (SS/DISB)

This pin combines two independent functions.

Disable Mode: A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, or if VDD drops below the UVLO threshold. In the case of REF being pulled below 4 V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

If an overcurrent fault is sensed (CS = 2.5 V), a soft stop is initiated. In this mode, SS/DISB sinks a constant current of 10 × I_{RT}. The soft stop continues until SS/DISB falls below 0.5 V. When any of these faults is detected, all outputs are forced to ground immediately.

NOTE

If SS/DISB is forced below 0.5 V, the pin starts to source current equal to I_{RT}. The only time the device switches into low I_{DD} current mode is when the device is in UVLO.

Soft-Start Mode: After a fault or disable condition has passed, VDD is above the start threshold, or SS/DISB falls below 0.5 V during a soft stop, SS/DISB switches to a soft-start mode. The pin then sources current equal to I_{RT}. A user-selected resistor-and-capacitor combination on SS/DISB determines the soft-start time constant.

NOTE

SS/DISB actively clamps the EAOUT pin voltage to approximately the SS/DISB pin voltage during both soft-start, soft-stop, and disable conditions.

Oscillator Synchronization (SYNC)

This pin is bidirectional (see Figure 1). When used as an output, SYNC can be used as a clock, which is the same as the internal clock of the device. When used as an input, SYNC overrides the internal oscillator of the device and acts as its clock signal. This bidirectional feature allows synchronization of multiple power supplies. Also, the SYNC signal internally discharges the C_T capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level-sensitive, with an input-low threshold of 1.9 V and an input-high threshold of 2.1 V. A resistor as small as 3.9 kΩ may be tied between SYNC and GND to reduce the SYNC pulse duration.

Chip Supply (VDD)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1-µF low-ESR low-ESL capacitor to ground.

APPLICATION INFORMATION

Programming DELAB, DELCD, and ADS

The UCC2895N allows the user to set the delay between switch commands within each leg of the full-bridge power circuit according to Equation 5:

$$t_{DELAY} = [(25 \times 10^{-12} \times R_{DEL})/V_{DEL}] + 25 \text{ ns} \quad (5)$$

From Equation 5, V_{DEL} is determined in conjunction with the desire to use (or not use) the ADS feature from Equation 6:

$$V_{DEL} = [0.75 \times (V_{CS} - V_{ADS})] + 0.5 \text{ V} \quad (6)$$

Figure 4 illustrates the resistors needed to program the delay periods and the ADS function.

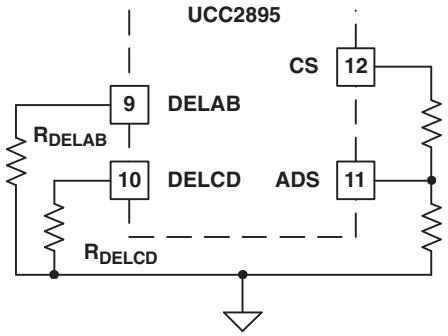


Figure 4. Programming Adaptive Delay Set

The ADS feature allows the user to vary the delay times between switch commands within each of the two legs of the converter. The delay-time modulation is implemented by connecting ADS (pin 11) to CS, GND, or a resistive divider from CS through ADS to GND to set V_{ADS} as shown in Figure 1. From Equation 6 for V_{DEL}, if ADS is tied to GND then V_{DEL} rises in direct proportion to V_{CS}, causing a decrease in t_{DELAY} as the load increases. In this condition, the maximum value of V_{DEL} is 2 V.

If ADS is connected to a resistive divider between CS and GND, the term ($V_{CS} - V_{ADS}$) becomes smaller, reducing the level of V_{DEL}. This decreases the amount of delay modulation. In the limit of ADS tied to CS, V_{DEL} = 0.5 V, and no delay modulation occurs. Figure 5 shows the delay time versus load for varying adaptive-delay-set feature voltages (V_{ADS}).

In the case of maximum delay modulation (ADS = GND), when the circuit goes from light load to heavy load, the variation of V_{DEL} is from 0.5 V to 2 V. This causes the delay times to vary by a 4:1 ratio as the load is changed.

The ability to program an adaptive delay is a desirable feature, because the optimum delay time is a function of the current flowing in the primary winding of the transformer and can change by a factor of 10:1 or more as circuit loading changes. Reference [5] describes the many interrelated factors for choosing the optimum delay times for the most-efficient power conversion, and illustrates an external circuit to enable adaptive delay set using the UC3879. Implementing this adaptive feature is simplified in the UCC2895-Q1 controller, giving the user the ability to tailor the delay times to suit a particular application with a minimum of external parts.

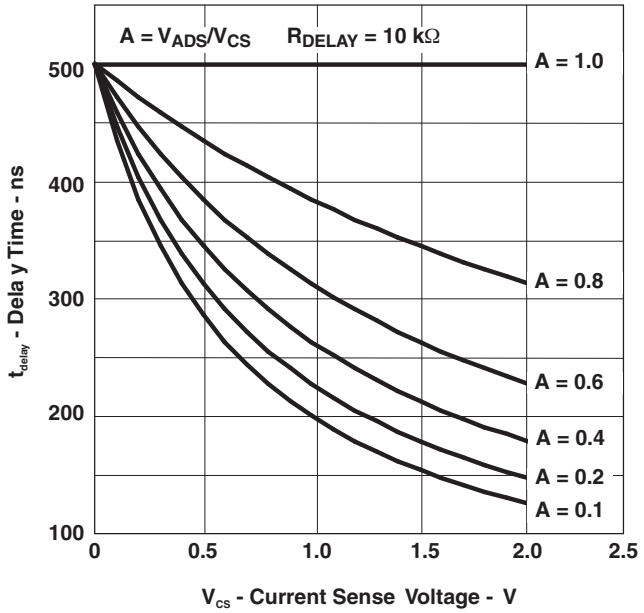


Figure 5. Delay Time Under Varying ADS Voltages

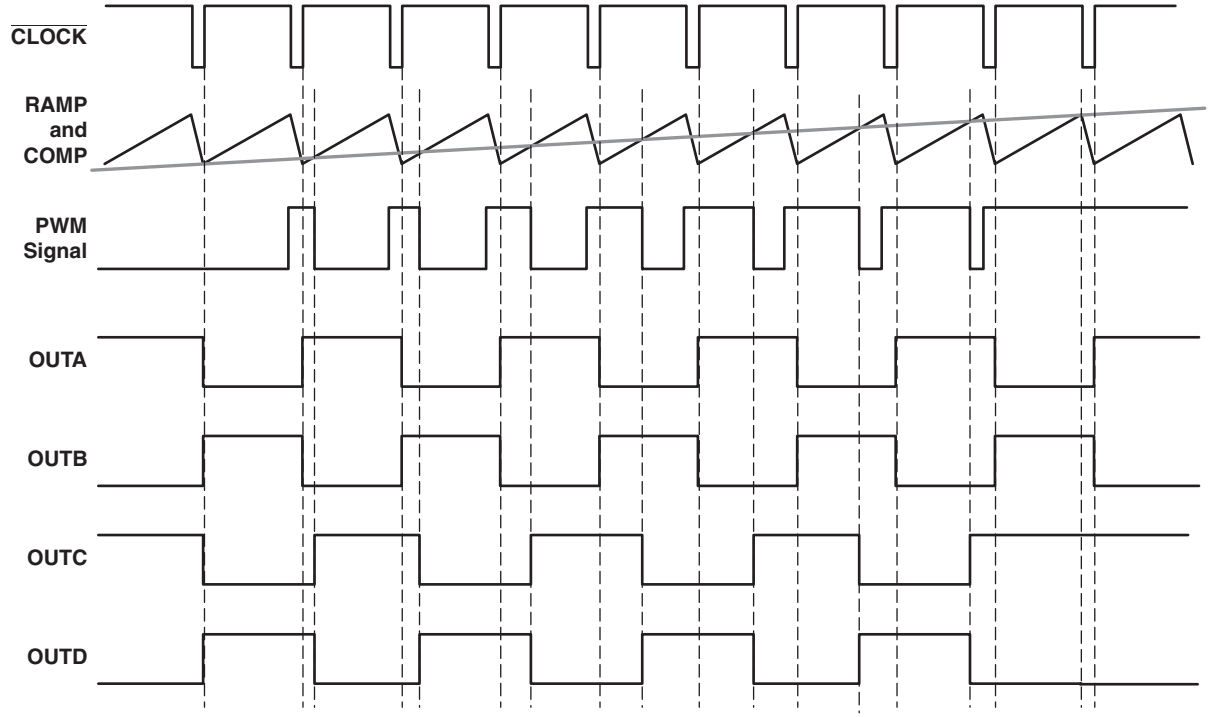


Figure 6. Timing Diagram (No Output Delay Shown, COMP to RAMP Offset Not Included)

TYPICAL CHARACTERISTICS

OUTPUT DELAY vs DELAY RESISTANCE

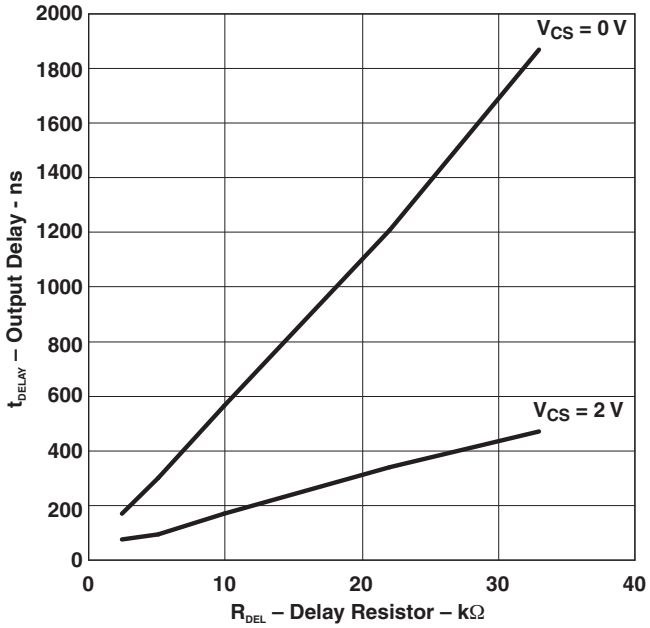


Figure 7.

OSCILLATOR FREQUENCY vs TIMING CAPACITANCE

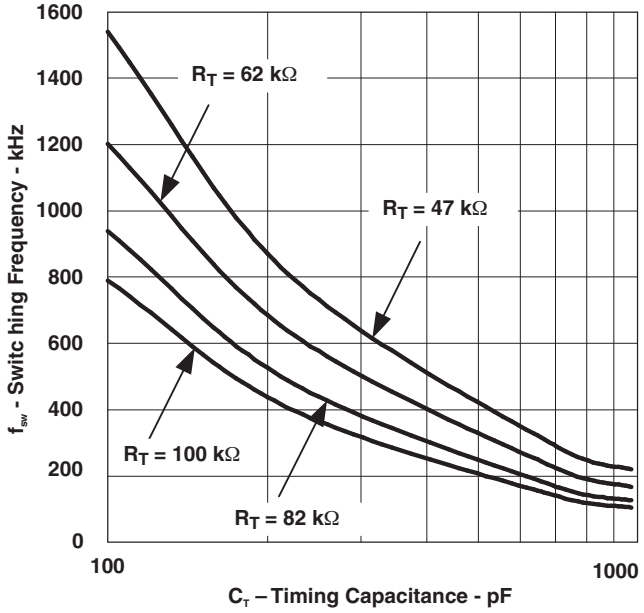


Figure 8.

EAOUT TO RAMP OFFSET vs TEMPERATURE

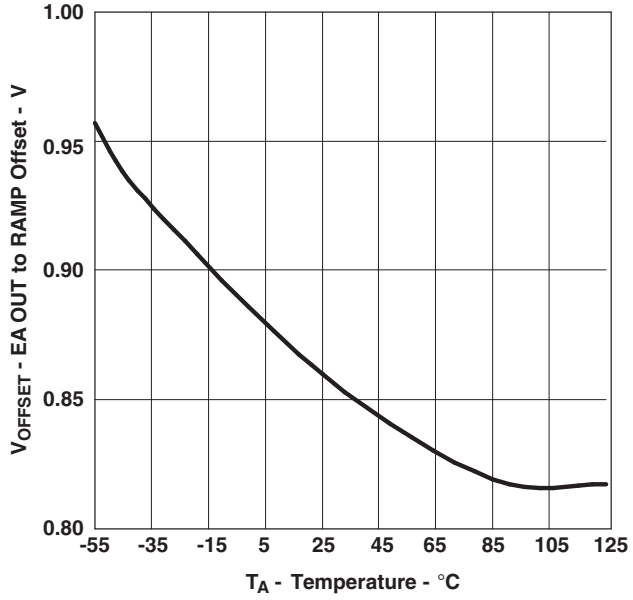


Figure 9.

AMPLIFIER GAIN AND PHASE MARGIN vs FREQUENCY

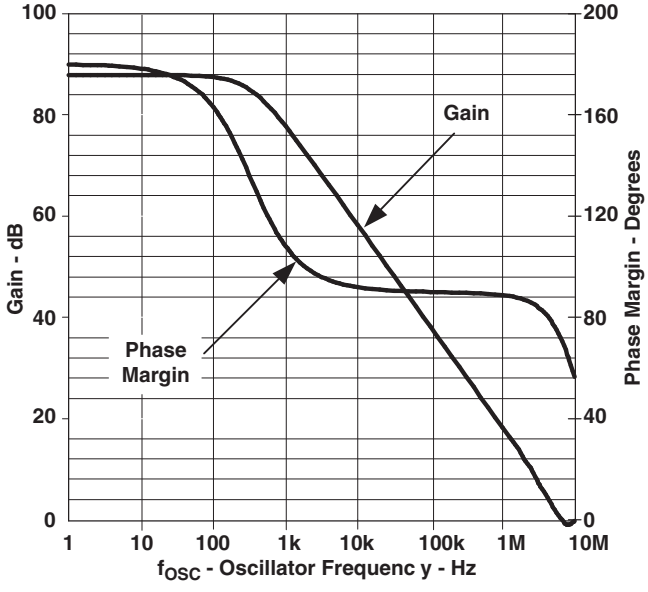


Figure 10.

TYPICAL CHARACTERISTICS (continued)

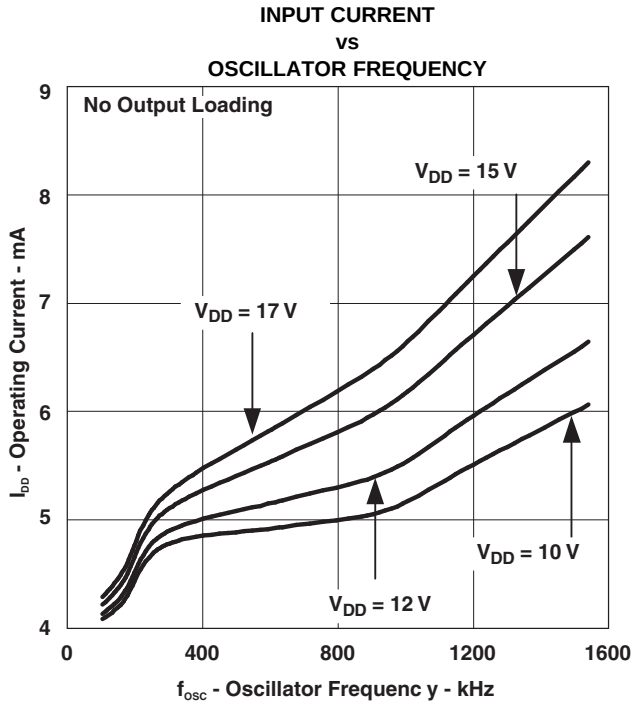


Figure 11.

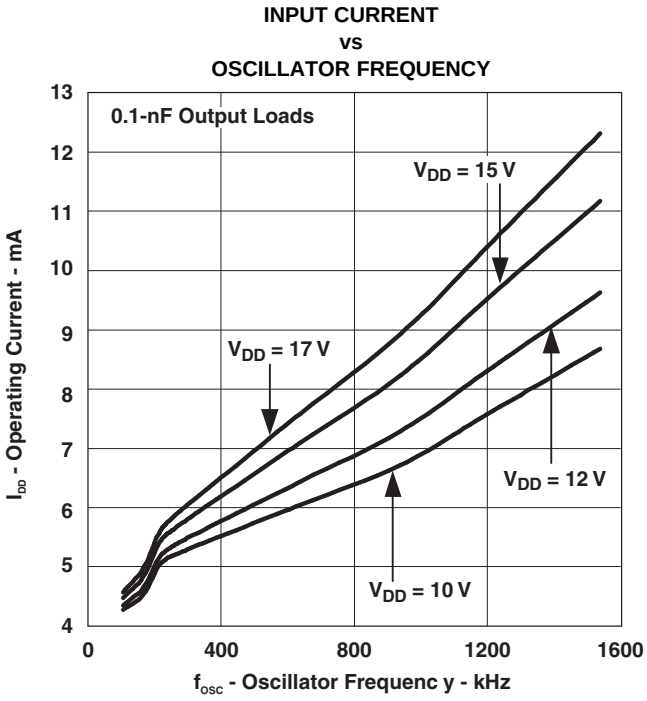


Figure 12.

REFERENCES

1. M. Dennis, *A Comparison Between the BiCMOS UCC2895 Phase Shift Controller and the UC3875* (SLUA246)
2. L. Balogh, *The Current-Doubler Rectifier: An Alternative Rectification Technique For Push-Pull and Bridge Converters* (SLUA121)
3. W. Andreycak, *Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller* (SLUA107)
4. L. Balogh, *The New UC3879 Phase-Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters* (SLUA122)
5. L. Balogh, *Design Review: 100 W, 400 kHz, dc-to-dc Converter with Current Doubler Synchronous Rectification Achieves 92% Efficiency*, Unitrode Power Supply Design Seminar Manual, SEM-1100, 1996, Topic 2.
6. UC3875 Phase Shift Resonant Controller data sheet (SLUS229)
7. UC3879 Phase Shift Resonant Controller data sheet (SLUS230)
8. *Configuring the UCC2895 for Direct Control Driven Synchronous Rectification* (SLUU109)
9. S. Mappus, *UCC2895 OUTC/OUTD Asymetric Duty Cycle Operation* (SLUA275)
10. S. Mappus, *Current Doubler Rectifier Offers Ripple Current Cancellation* (SLUA323)
11. S. Mappus, *Control Driven Synchronous Rectifiers In Phase Shifted Full Bridge Converters* (SLUA287)

REVISION HISTORY

Changes from Revision B (July 2012) to Revision C **Page**

- Changed T_J from –40ºC to –55ºC 2
- Changed T_J from –40ºC to –55ºC 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC2895QDWRQ1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC2895Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF UCC2895-Q1 :

- Catalog: UCC2895

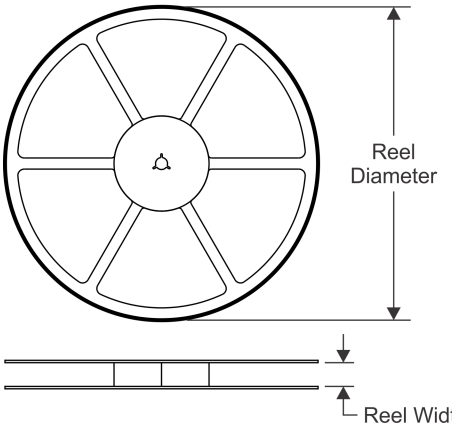
- Enhanced Product: UCC2895-EP

NOTE: Qualified Version Definitions:

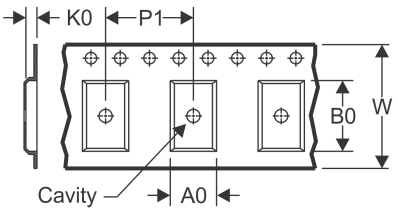
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

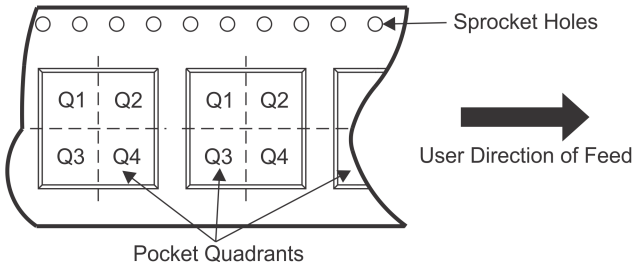


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

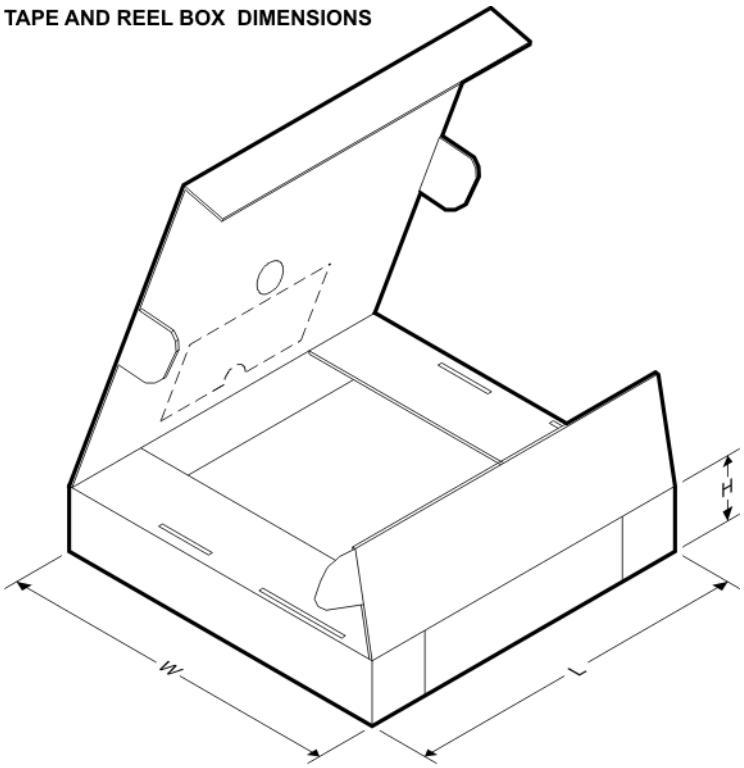
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

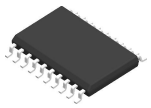
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2895QDWRQ1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2895QDWRQ1	SOIC	DW	20	2000	367.0	367.0	45.0

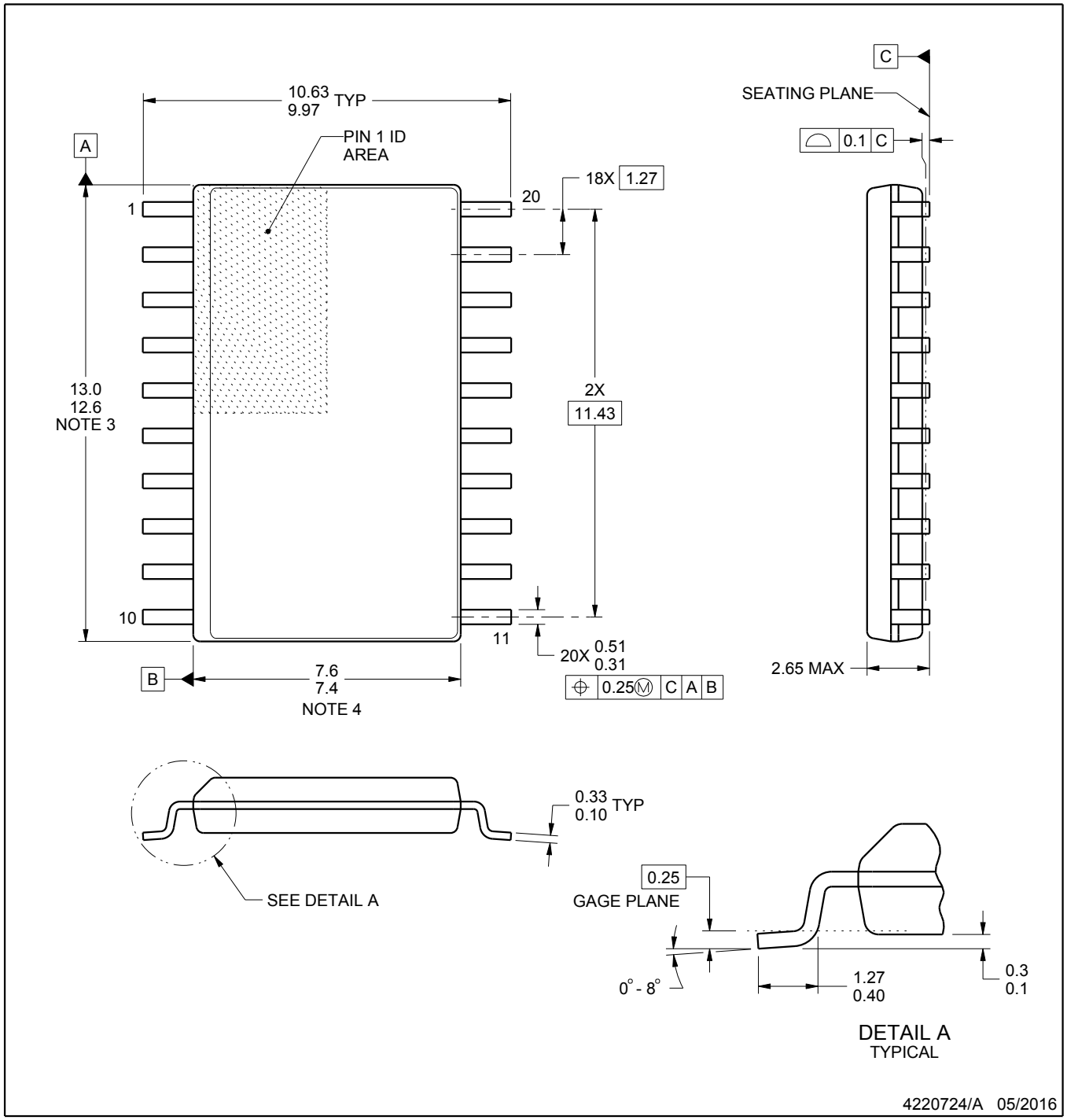


PACKAGE OUTLINE

DW0020A

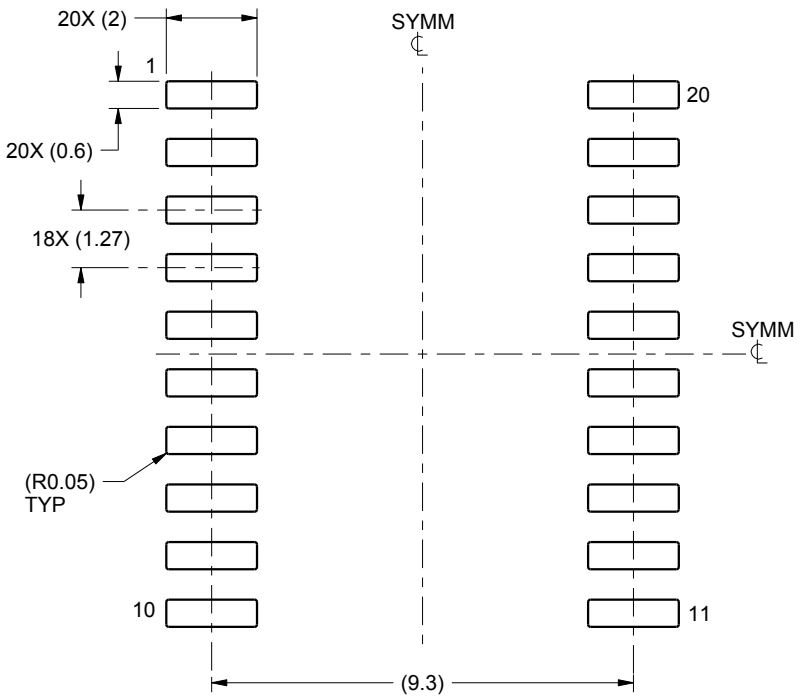
SOIC - 2.65 mm max height

SOIC

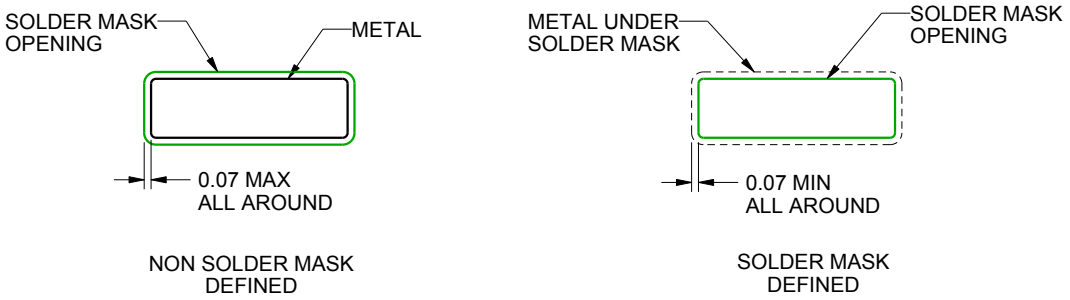


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

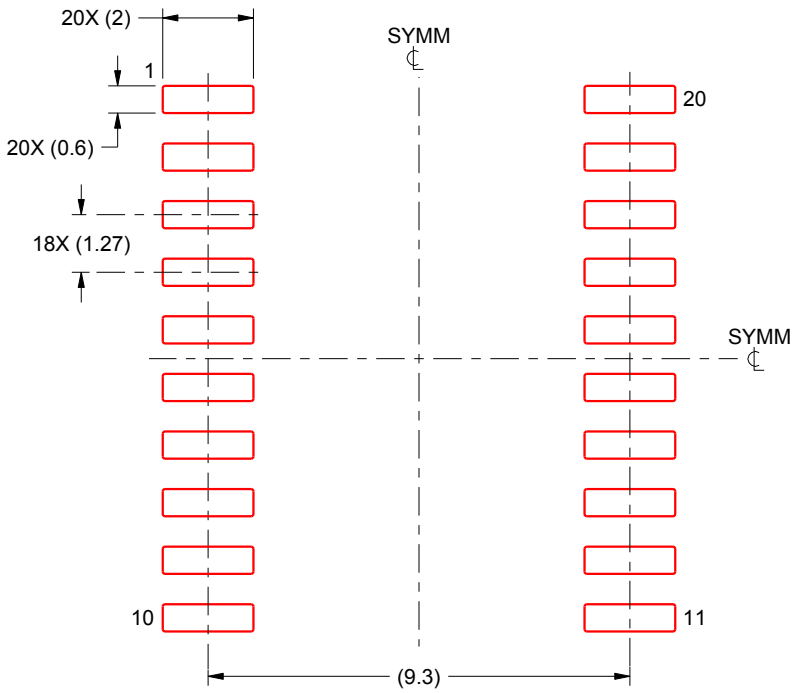


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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