LMK04610 Evaluation Module

User's Guide

Literature Number: SNAU201A
January 2017–Revised February 2017

Contents

Overview

Overview

The LMK04610EVM features LMK04610 ultra-low noise and low-power JESD204B compliant Dual Loop Jitter Cleaner. With a power consumption of only typical 880 mW with 10 outputs running, LMK04610 supports typical 65 fs jitter (12 kHz to 20 MHz) using a low noise VCXO module. Integrated LDOs provide high PSRR that enables the use of DC-DC converters.

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock and SYSREF generation. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module.

Features

- Dual Loop Architecture with typical 65 fs rms from 10 kHz to 20 MHz at 122.88-MHz output frequency
- 880 mW typical power consumption for 10 outputs at 122.88 MHz
- JEDEC JESD204B Support
- Jumper configurable supplies with onboard LDOs and DC-DC converters
- GUI platform for full access to device registers

Quick Start Guide

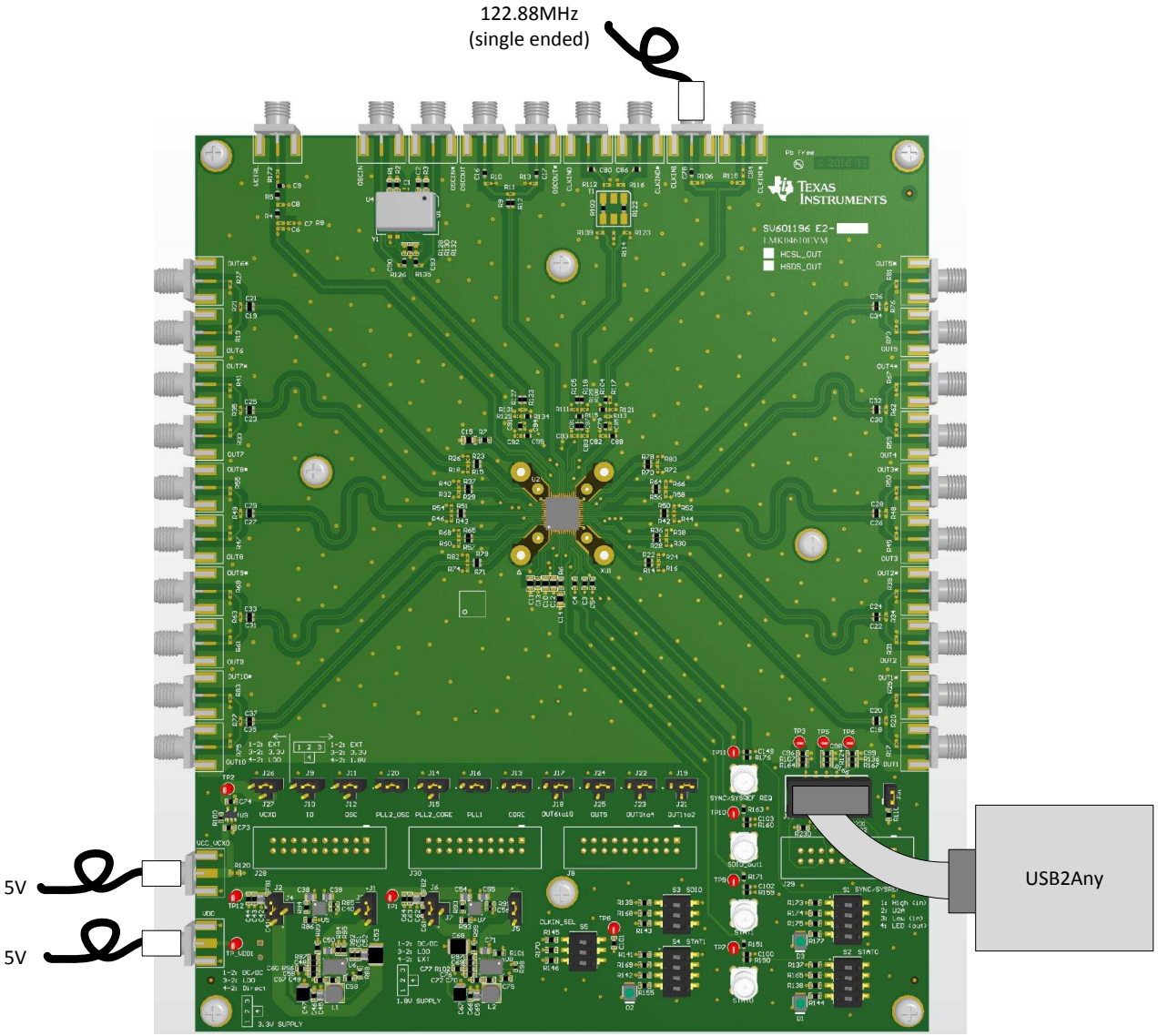


Figure 1-1. LMK04610 EVM Quick Start Connection

1.1 Quick Start Description

The LMK04610 EVM allows full verification of the device functionality and performance specification. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1-1.

1. Place Dip switches S1 to S5 into default position as shown in Figure 4-6
2. Connect a supply voltage of 5 V to the VCC and VCC_VCXO SMA.
3. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use 122.88 MHz for default.
4. Connect the SPI header to a computer using USB2ANY.
5. Program the device with TICS Pro.
   (a) Start TICS Pro
   (b) Select LMK04610 from *Select device → Clock Generator/Jitter Cleaner (Dual Loop) → LMK0461x* Menu.
   (c) Select from *USB Communications → Interface* Menu USB2ANY.
   (d) Select default mode from the *Default Configuration* Menu. For the quick start, use *Dual Loop: PLL1 BW= 40Hz REF: CLKin1 (single-ended)*
   (e) Ctrl-L must be pressed at least once to load all registers. Alternatively click menu *Keyboard Controls → Load Device*.
   (f) Click *Device Start* button in the *Generic* page or use the *Device: DEV_STARTUP* button from the Tool bar.
6. Measurements may be made at an active CLKout port through its SMA connector.

1.2 Device Start-Up Sequence

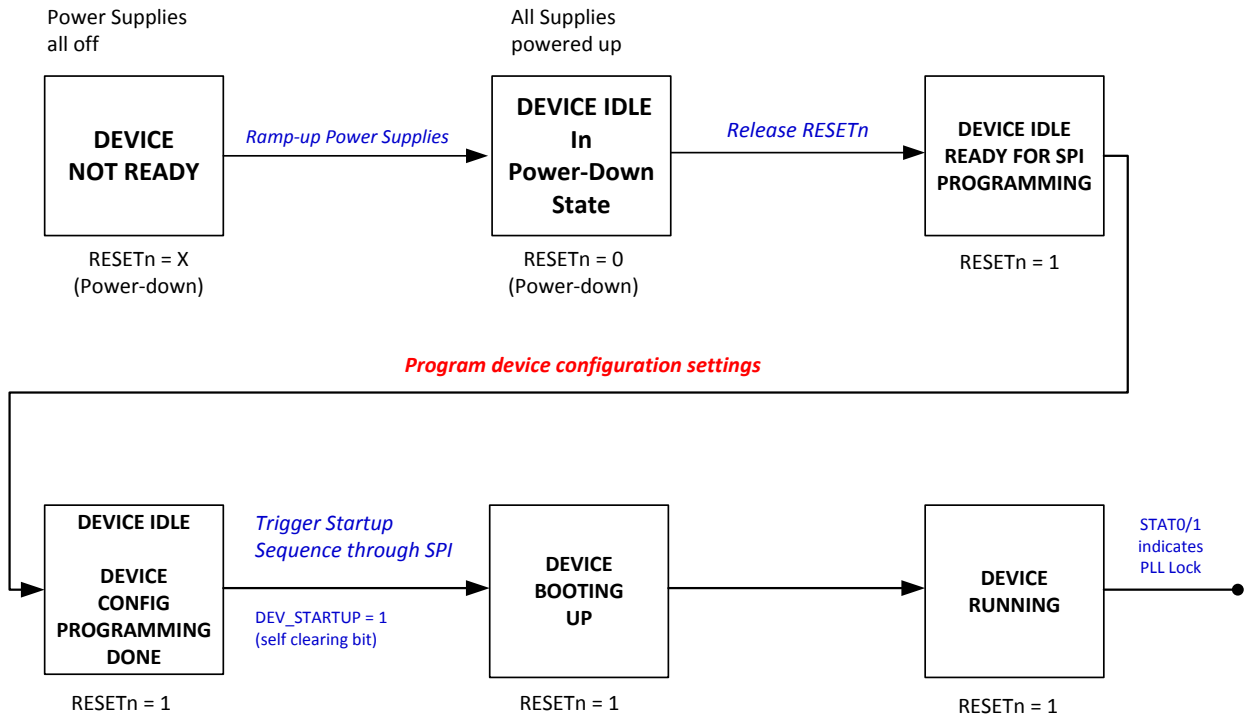


Figure 1-2. Device Start-Up Sequence

Installing the EVM Control Software

1. Install latest TICS Pro software from web: http://www.ti.com/tool/ticspro-sw
2. Start TICS Pro.
3. Select *Device → Clock Generator/Jitter Cleaner (Dual Loop) → LMK0461x → LMK04610*

Using the EVM Control Software

3.1 Keyboard Shortcuts

CTRL + L => write all registers

3.2 TICS Pro Overview

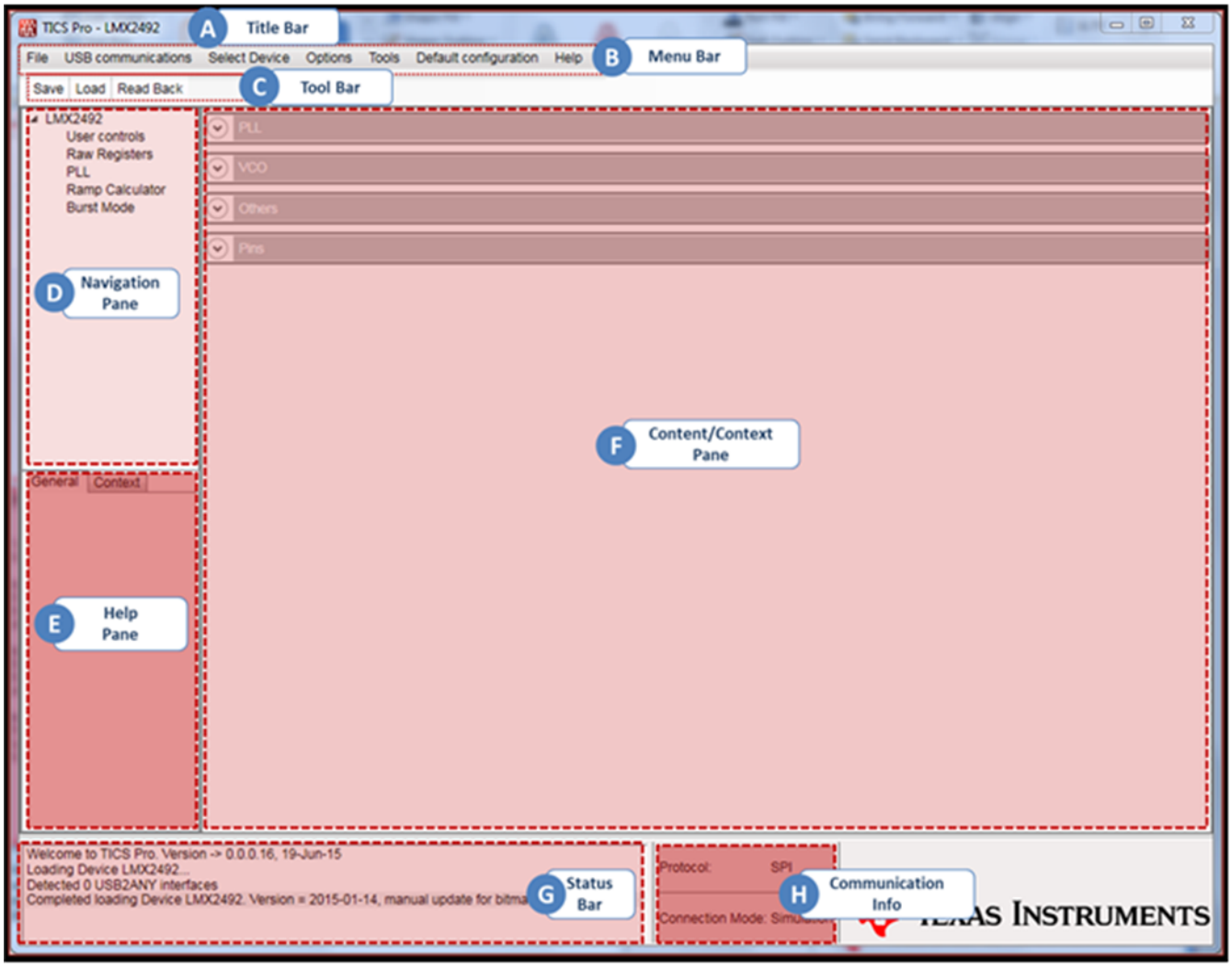


Figure 3-1. TICS Pro Overview

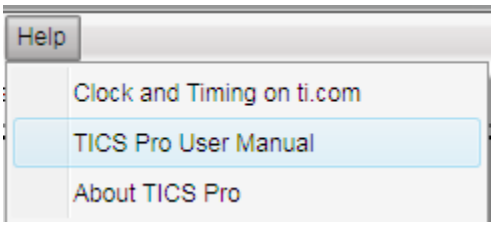


Figure 3-2. TICS Pro User Manual

Further information at *Help → TICS Pro User Manual*

3.3 TICS Pro with LMK04610 GUI Loaded

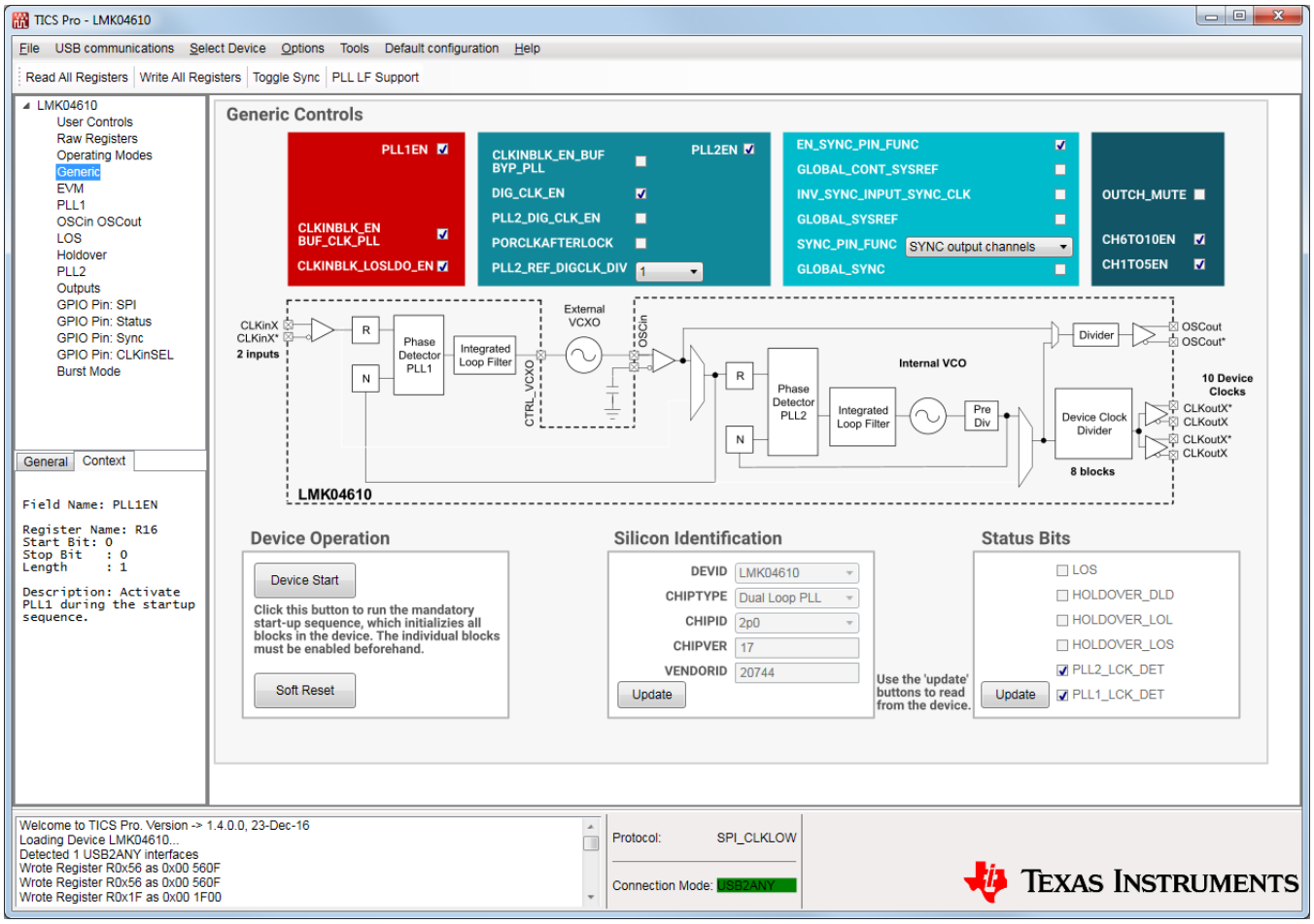


Figure 3-3. TICS Pro With LMK04610 GUI Loaded

3.4 GUI: Generic Control

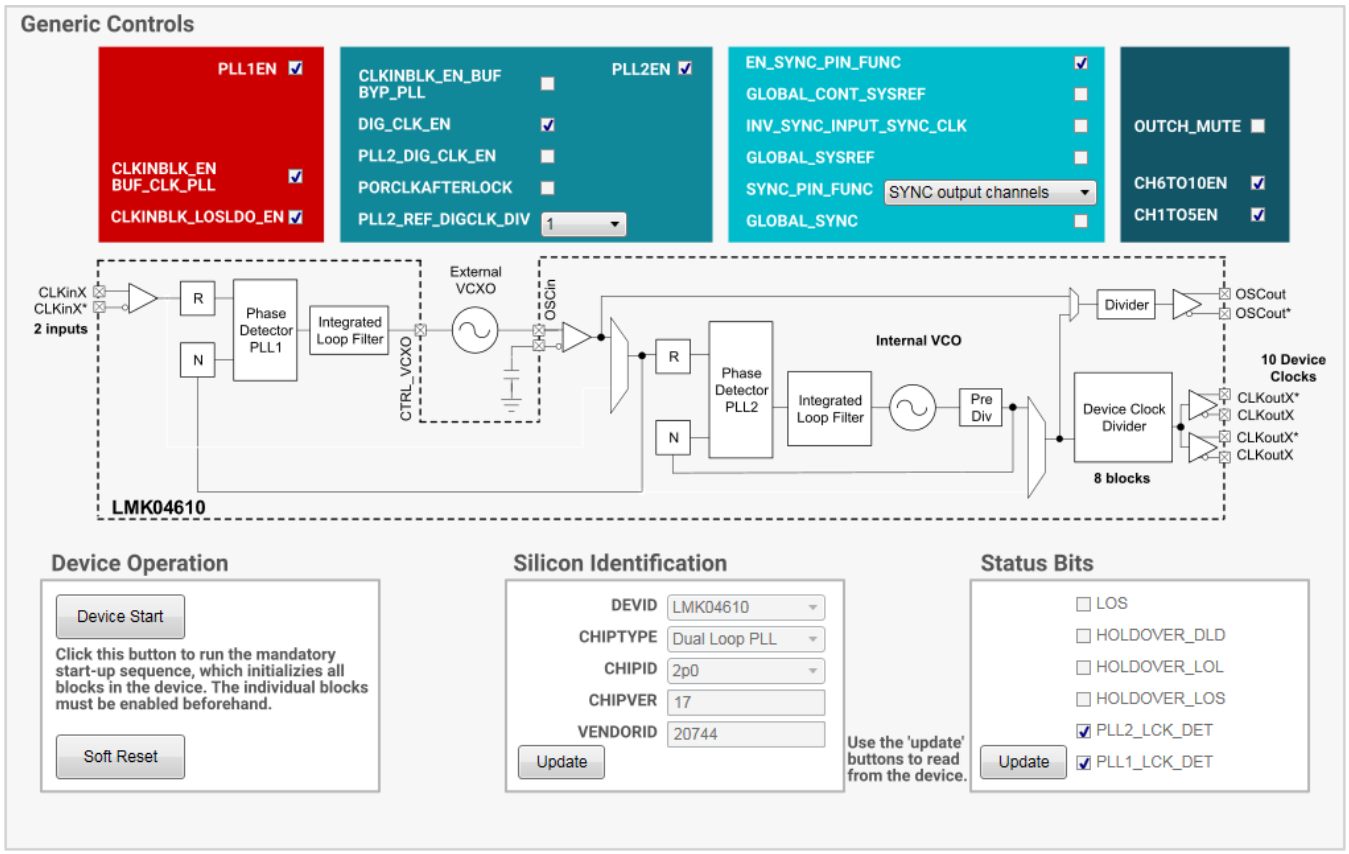


Figure 3-4. GUI: Generic Control

3.5 GUI: Operating Modes

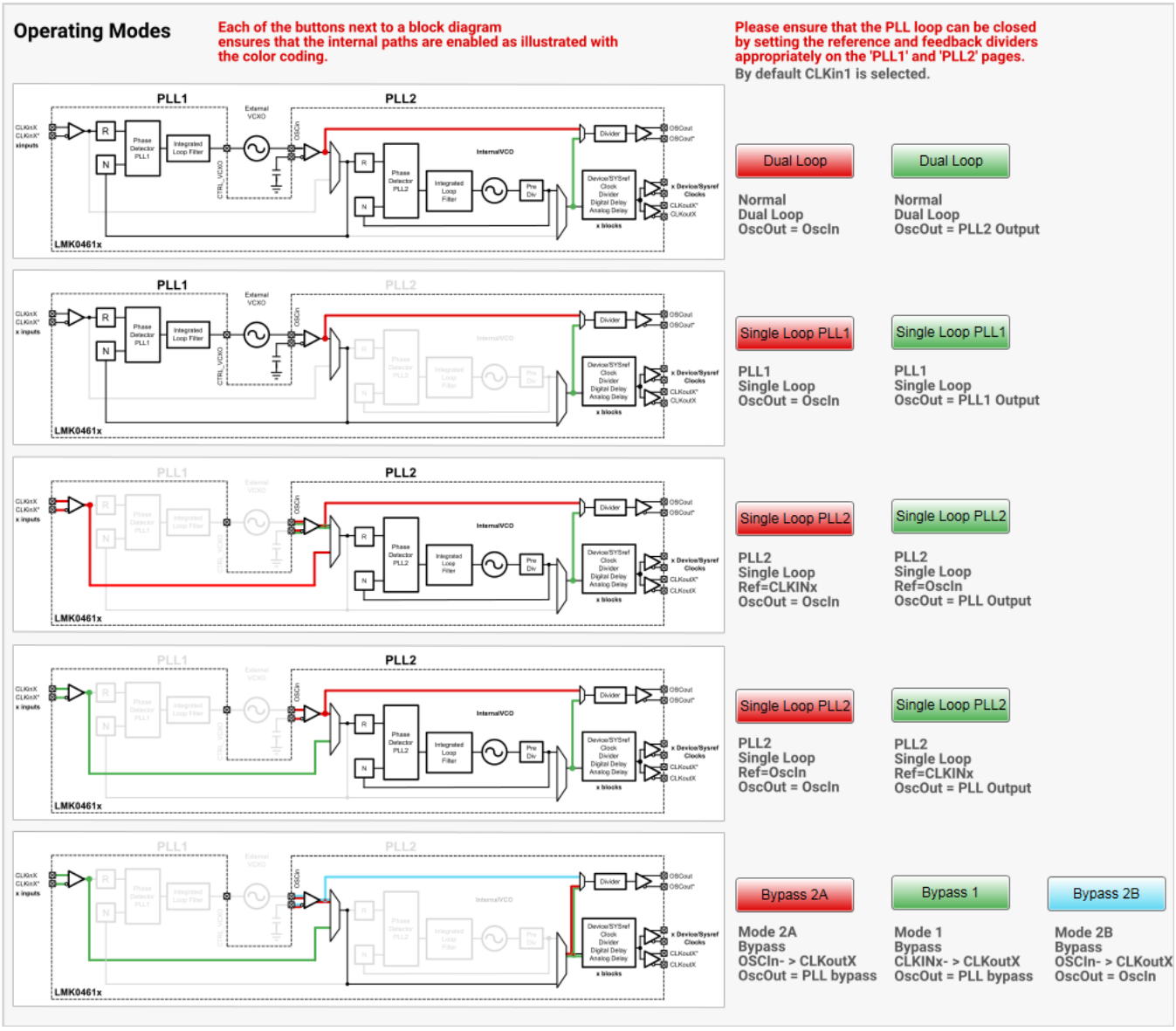


Figure 3-5. GUI: Operating Modes

3.6 GUI: OSCin and OSCout

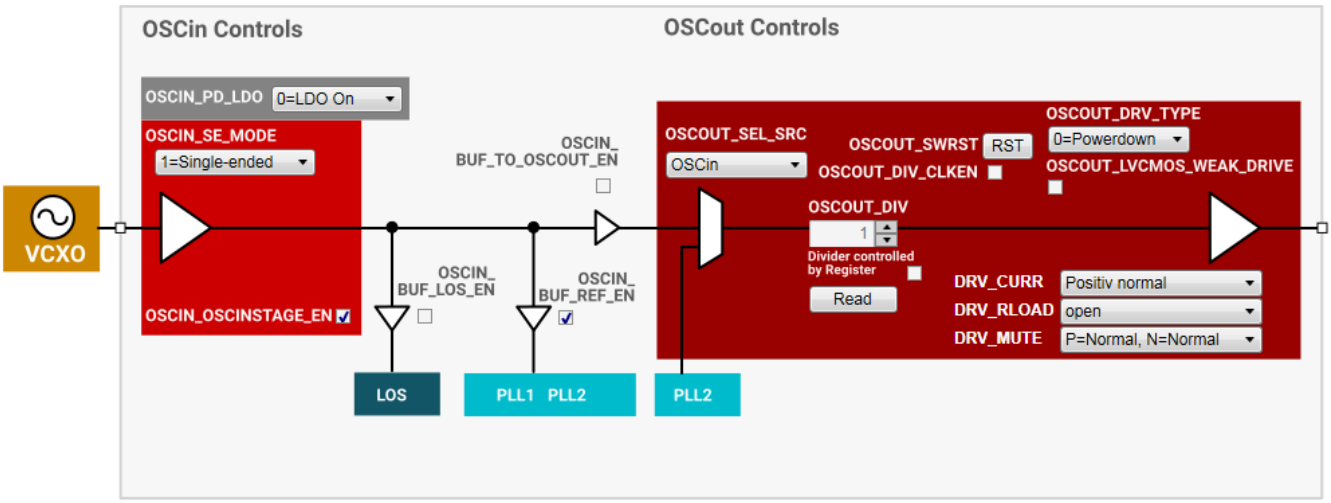
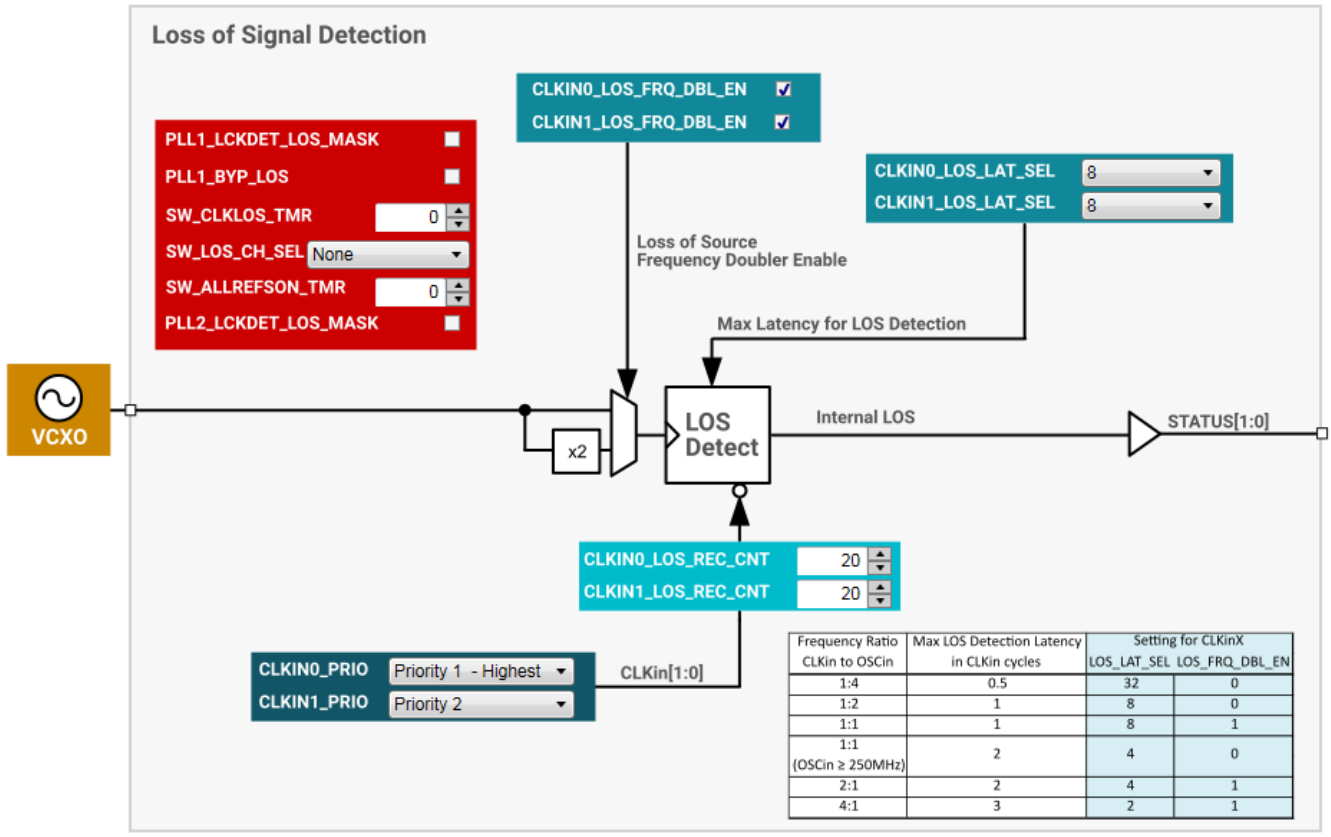


Figure 3-6. GUI: OSCin and OSCout

3.7 GUI: LOS Control



Frequency Ratio CLKin to OSCin	Max LOS Detection Latency in CLKin cycles	Setting for CLKinX LOS_LAT_SEL	LOS_FRQ_DBL_EN
1:4	0.5	32	0
1:2	1	8	0
1:1	1	8	1
1:1 (OSCin ≥ 250MHz)	2	4	0
2:1	2	4	1
4:1	3	2	1

Figure 3-7. GUI: LOS Control

3.8 GUI: Holdover Control

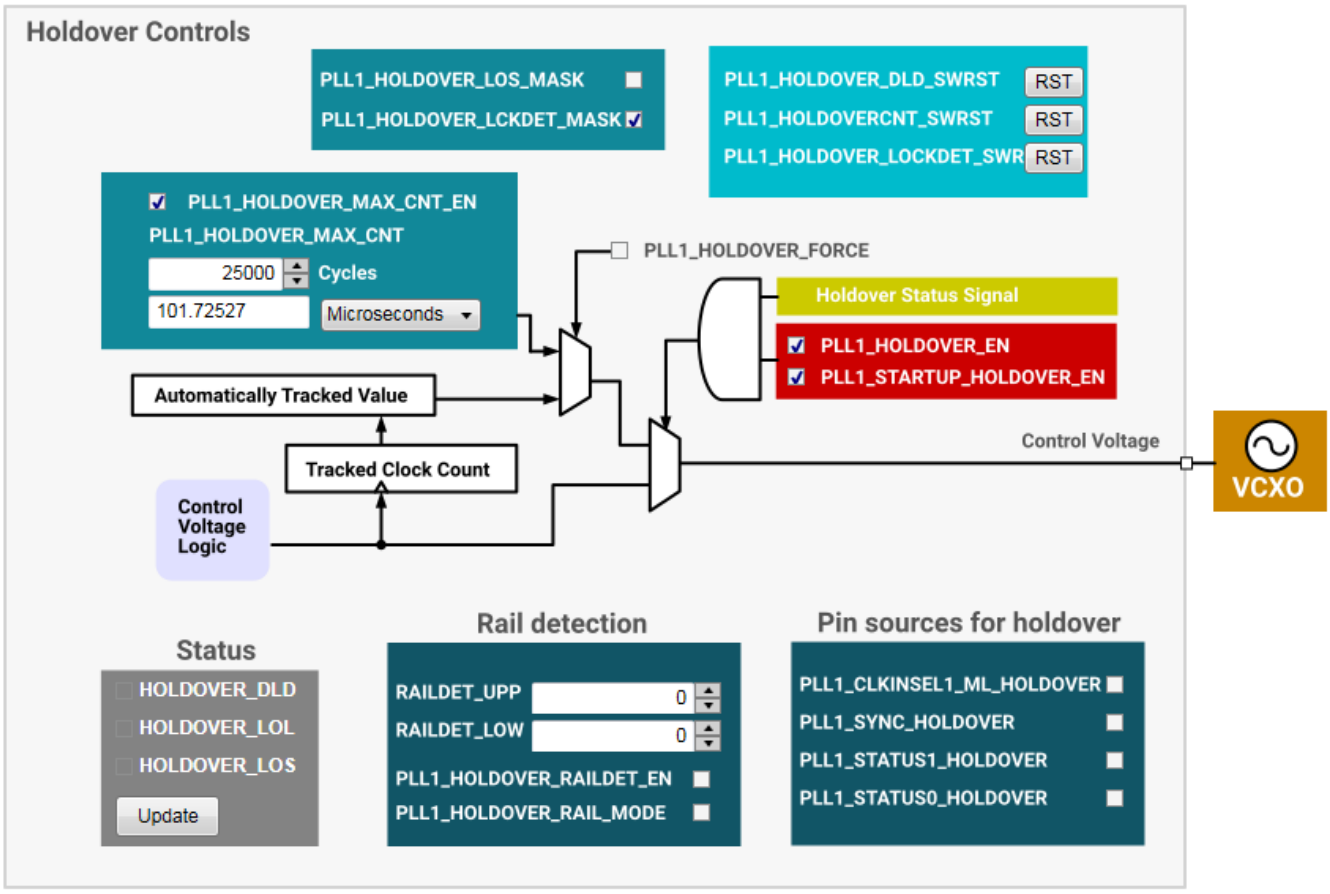
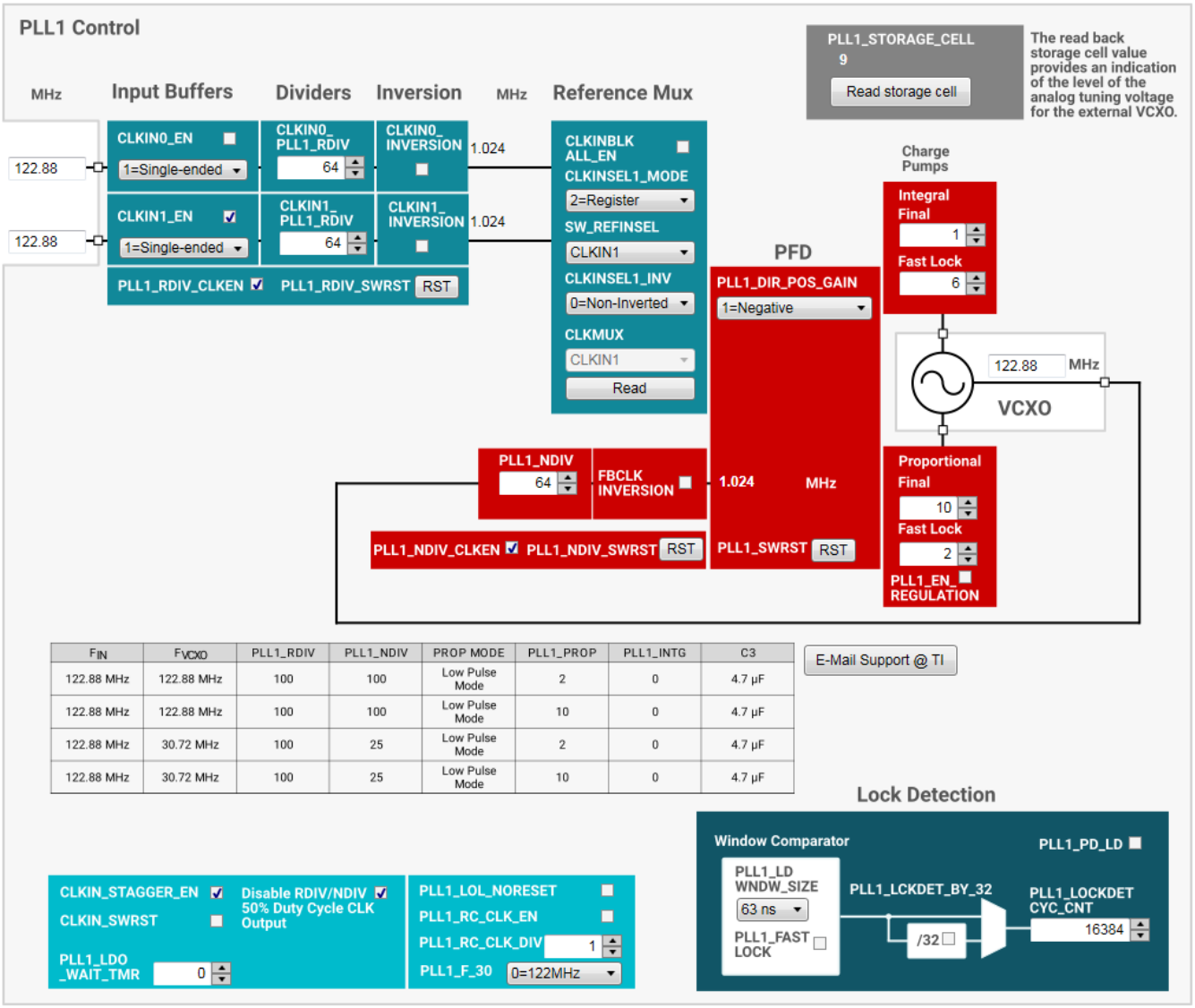


Figure 3-8. GUI: Holdover Control

3.9 GUI: Inputs and PLL1



FIN	FVCXO	PLL1_RDIV	PLL1_NDIV	PROP MODE	PLL1_PROP	PLL1_INTG	C3
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	2	0	4.7 µF
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	10	0	4.7 µF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	2	0	4.7 µF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	10	0	4.7 µF

Figure 3-9. GUI: Inputs and PLL1

3.10 GUI: PLL2

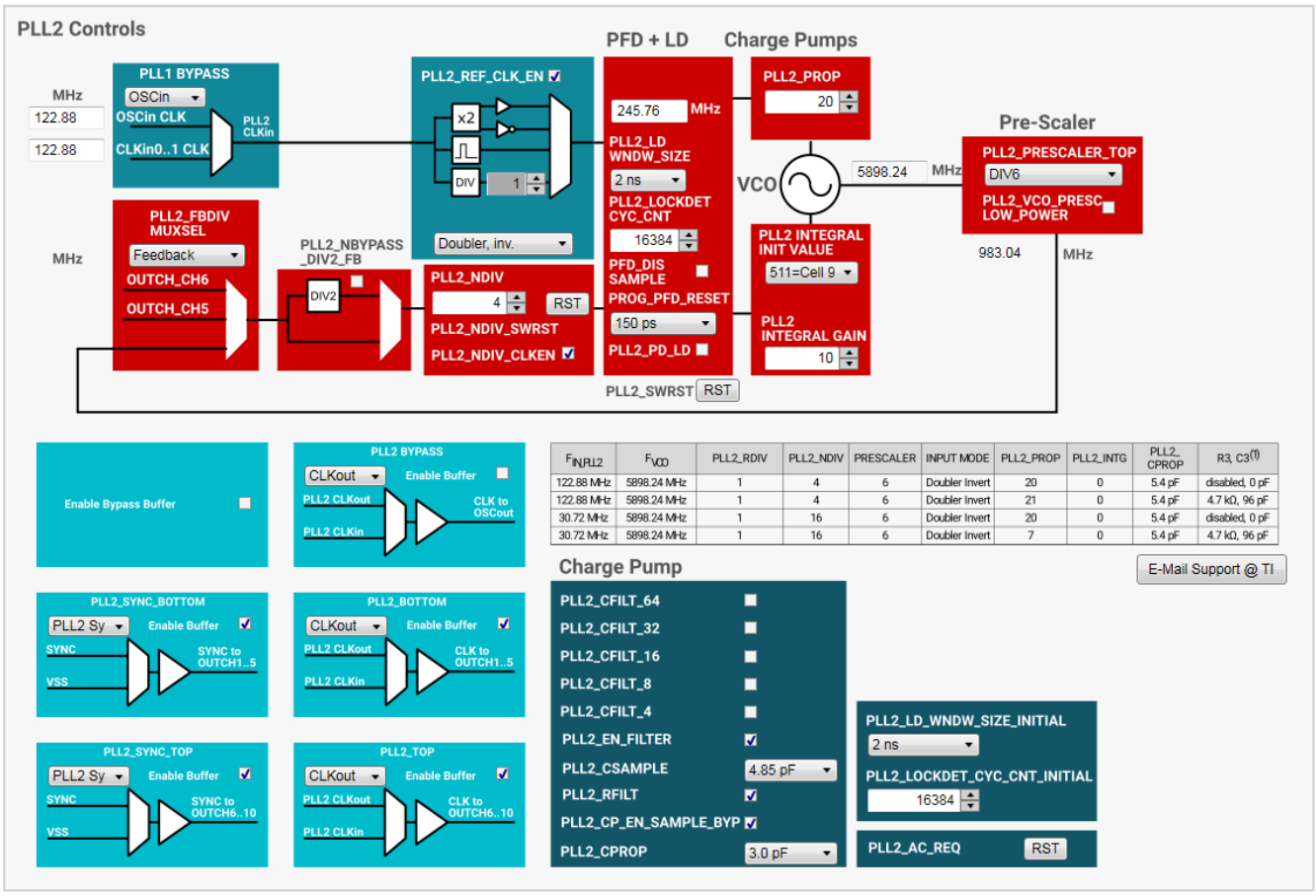


Figure 3-10. GUI: PLL2

3.11 GUI: Outputs

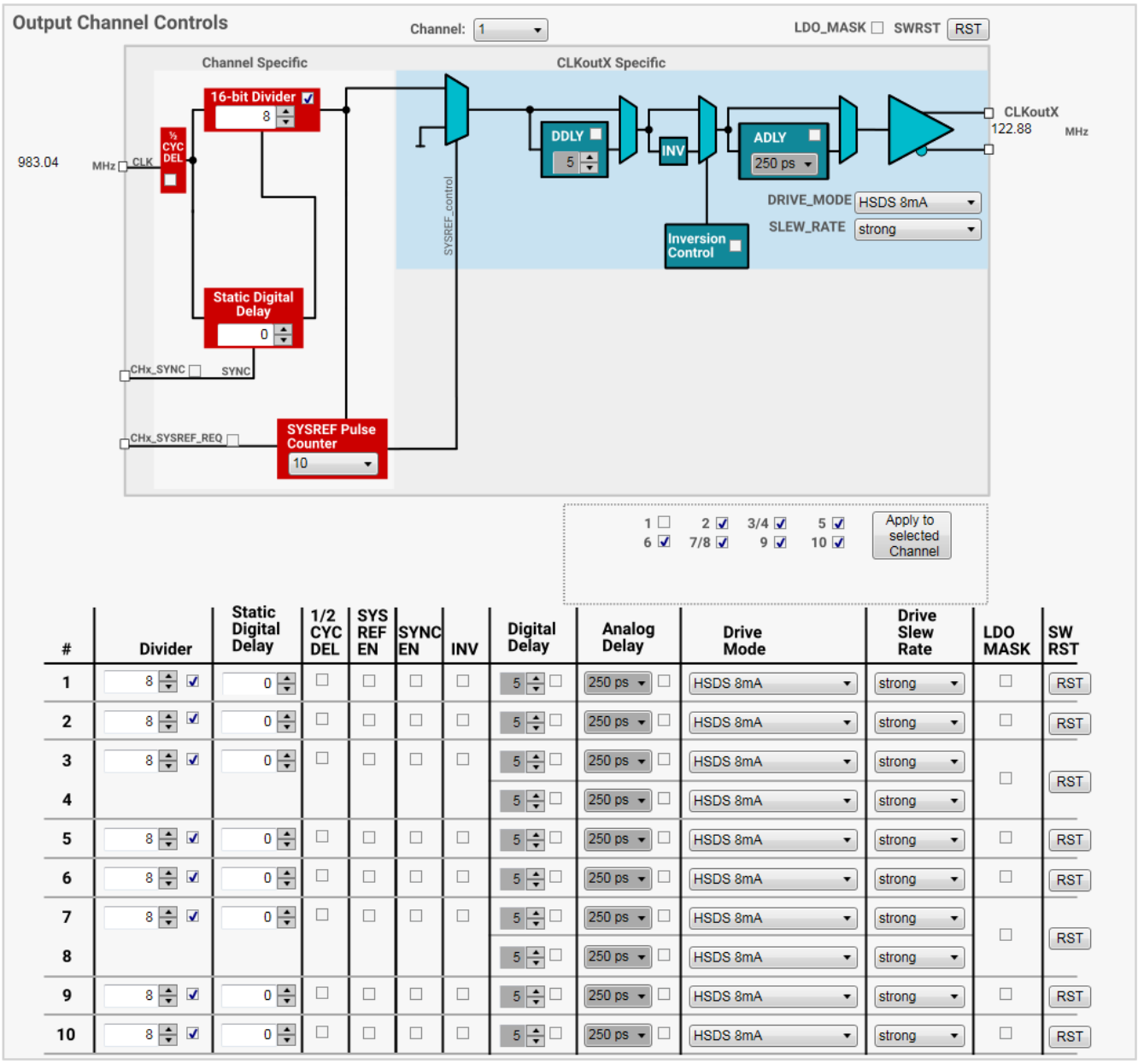


Figure 3-11. GUI: Outputs

3.12 GUI: EVM

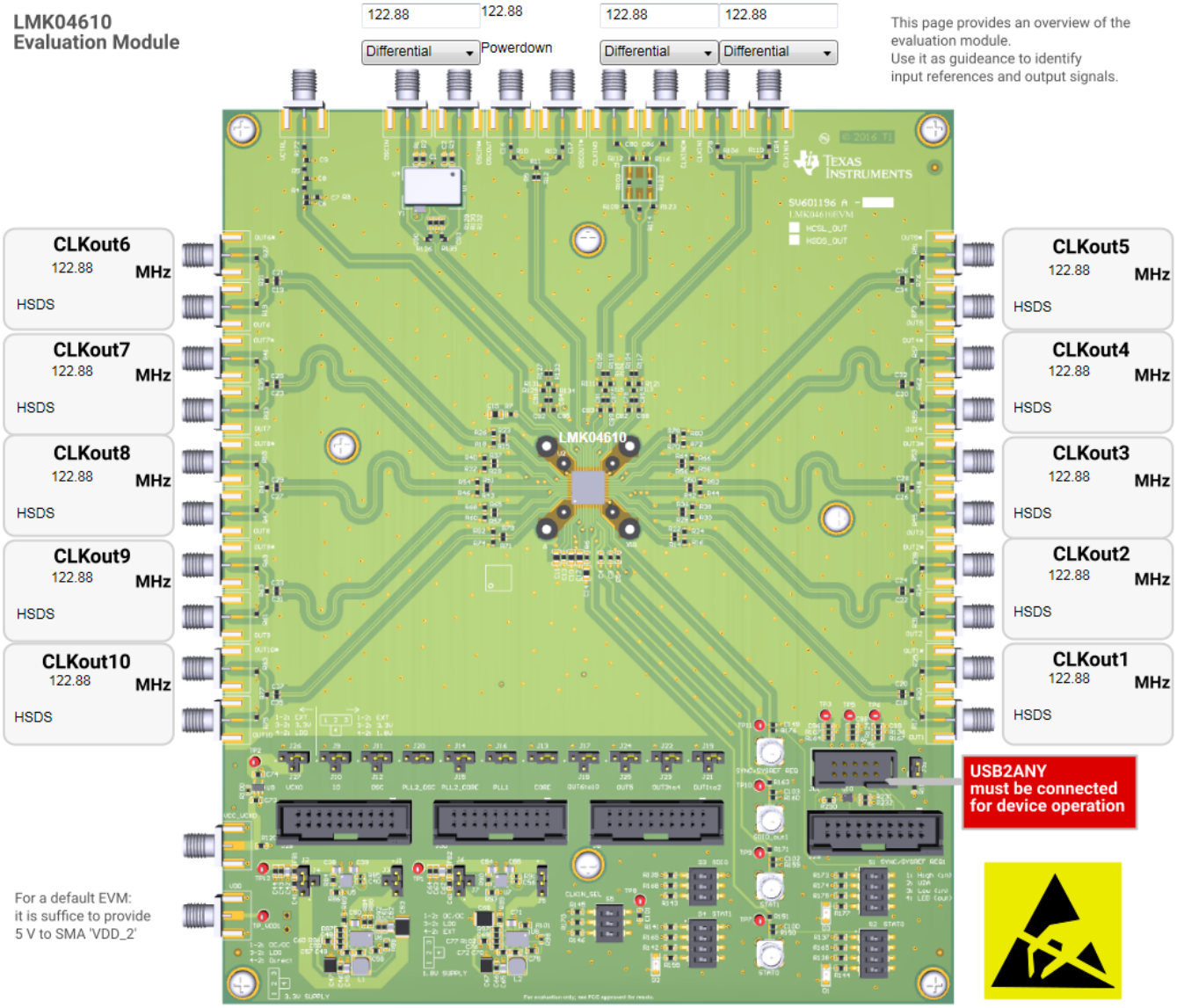


Figure 3-12. GUI: EVM Overview

Configuring the Board

The LMK04610 is a programmable clock jitter cleaner with many options. The EVM was designed with maximum flexibility so engineers can configure the EVM for operation at its desired mode.

Figure 4-1 shows the connection concept of the LMK04610EVM.

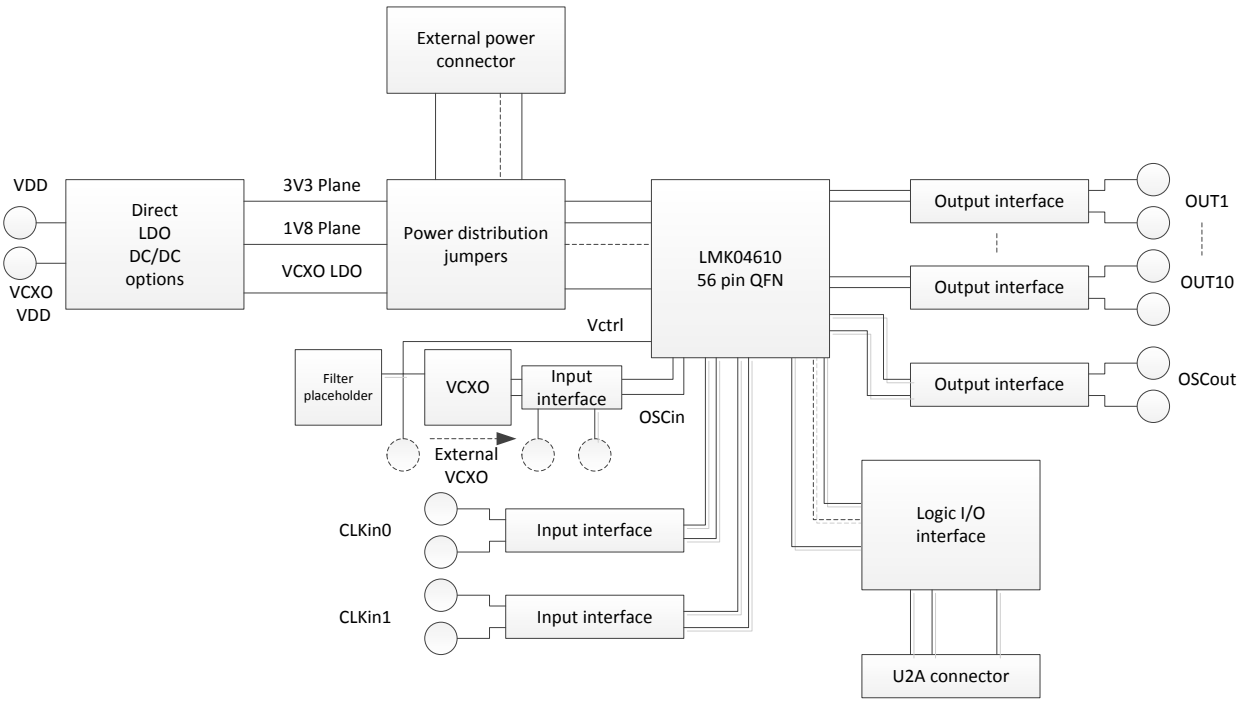


Figure 4-1. EVM Connection Concept

4.1 Configuring the Power Supply

Figure 4-2 shows the default jumper setting to supply 3.3 V and 1.8 V to the device.

The VDD SMA or VDD_2 terminal block (on the back side of the EVM) is connected to J1 and J5 to provide the external supply voltage for the 3.3-V and 1.8-V supply plane. Connect 5-V external power supply if LDO or DCDC converter is used.

The VDD_VCXO SMA is directly connected to the VCXO LDO.

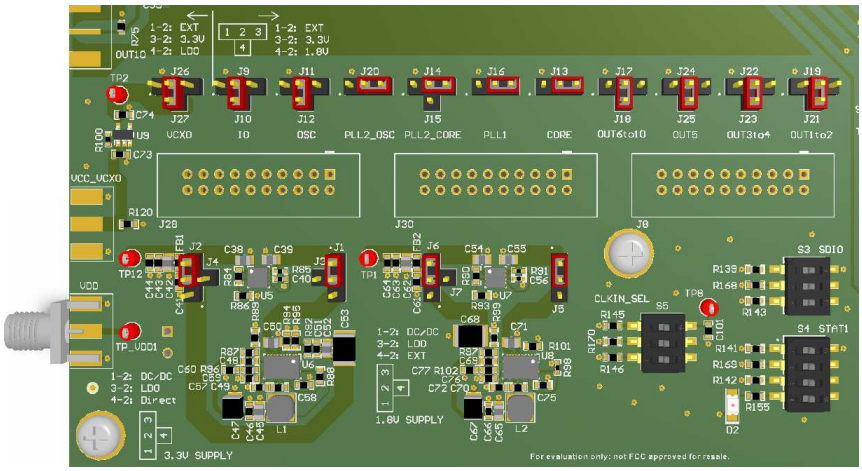


Figure 4-2. Default Power Supply Connection

4.1.1 Supply Plane Source Selection

Jumper J1 and J2 selects the Power connection for the 3.3-V plane from either the LDO, a DC-DC switcher, or direct from VDD SMA Connector. A 5-V supply needs to be connected to VDD SMA Connector.

Table 4-1. 3.3-V Supply Plane Connections

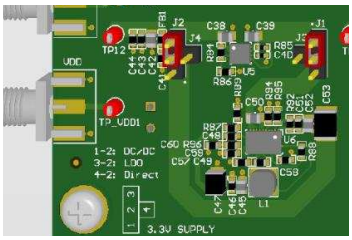
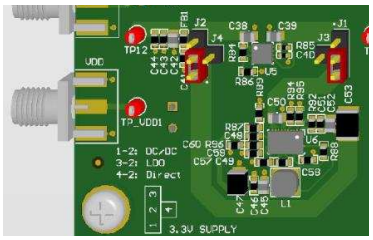
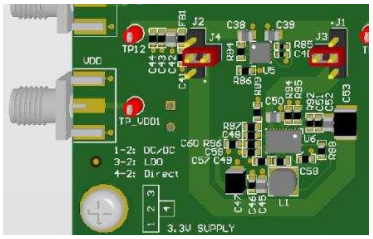
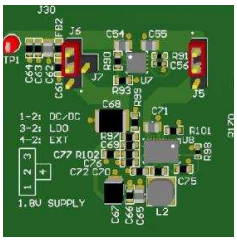
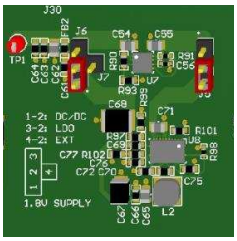
3.3-V LDO (TPS7A8101)	J1: 1-2 J2: 2-3	
3.3-V DC-DC (TPS54120)	J1: 2-3 J2: 1-2	

Table 4-1. 3.3-V Supply Plane Connections (continued)

Direct from VDD SMA **NOTE: Apply 3.3 V only**	J1: 2-4 J2: 2-4	

Jumper J6 and J5 selects the Power connection for the 1.8-V plane from either a LDO or a DC-DC switcher.

Table 4-2. 1.8-V Supply Plane Connections

1.8-V LDO (TPS7A8101)	J5: 1-2 J6: 2-3	
1.8-V DC-DC (TPS54120)	J5: 2-3 J6: 1-2	

4.1.2 Power Distribution

The power distribution jumpers (J9, J11, J13, J14, J16, J17, J19, J20, J22, and J24) are connected to the 3.3-V and 1.8-V supply planes and individual external connections.

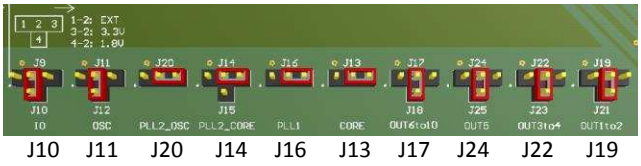


Figure 4-3. Power Distribution Jumpers

J13 (VDD_CORE), J16 (VDD_PLL1), and J20 (VDD_PLL2_OSC) selects between 3.3-V supply plane and external supply connection as shown in Figure 4-4.

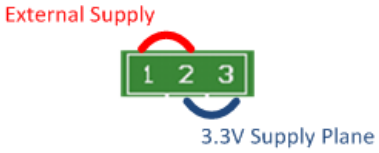


Figure 4-4. J13, J16, J20 Connection Description

J9 (VDD_IO), J11 (VDD_OSC), J14 (VDD_PLL2_CORE), J17 (VDD_OUT6to10), J19 (VDD_OUT1to2), J22 (VDD_OUT3to4), and J24 (VDD_OUT5) selects between 3.3-V supply plane, 1.8-V supply plane and external supply connection as shown in Figure 4-5.

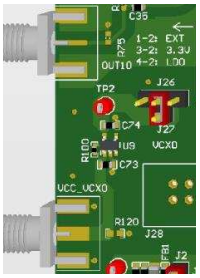
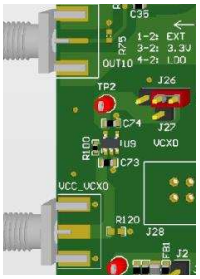
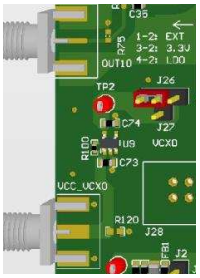
Figure 4-5. J9, J11, J14, J17, J19, J22, J24 Connection Description

NOTE: External supply connection is available on Jumpers J8, J28, and J30.

4.1.3 VCXO Supply Connection

The VCXO has its own LDO (LM5907MFX-3.3). A 5-V supply needs to be connected to VCC_VCXO SMA. Jumper J26 selects between this LDO, the LMK04610 3.3-V supply plane and external supply connection as shown inTable 4-3.

Table 4-3. VCXO Supply Connections

3.3-V LDO (LM5907MFX-3.3)	J26: 2-4	
3.3-V supply plane (TPS7A8101 or TPS54120)	J26: 2-3	
External supply connection on Jumper J28 **NOTE: Apply 3.3 V only**	J26: 1-2	

4.2 Dip Switch Configuration

Default configuration of Dip Switches is shown in Table 4-4 or Figure 4-6.

Table 4-4. Default Dip Switch Configuration

SWITCH POSITION	S1 SYNC/SYSREF REQ	S2 STAT0	S3 SDIO	S4 STAT1	S5 CLKin_SEL
1 – High	OFF	OFF	OFF	OFF	OFF
2 – U2A	**ON**	**ON**	**ON**	**ON**	**ON**
3 – Low	OFF	OFF	OFF	OFF	OFF
4 – LED	**ON**	**ON**	n/a	**ON**	n/a

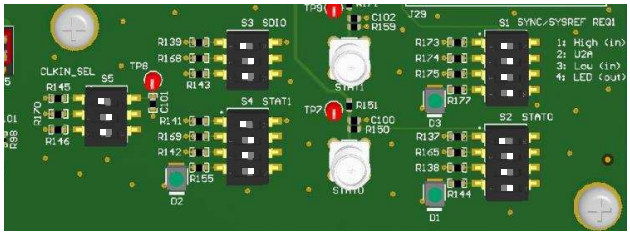


Figure 4-6. Default Dip Switch Setting

LMK04610 EVM Board Schematics

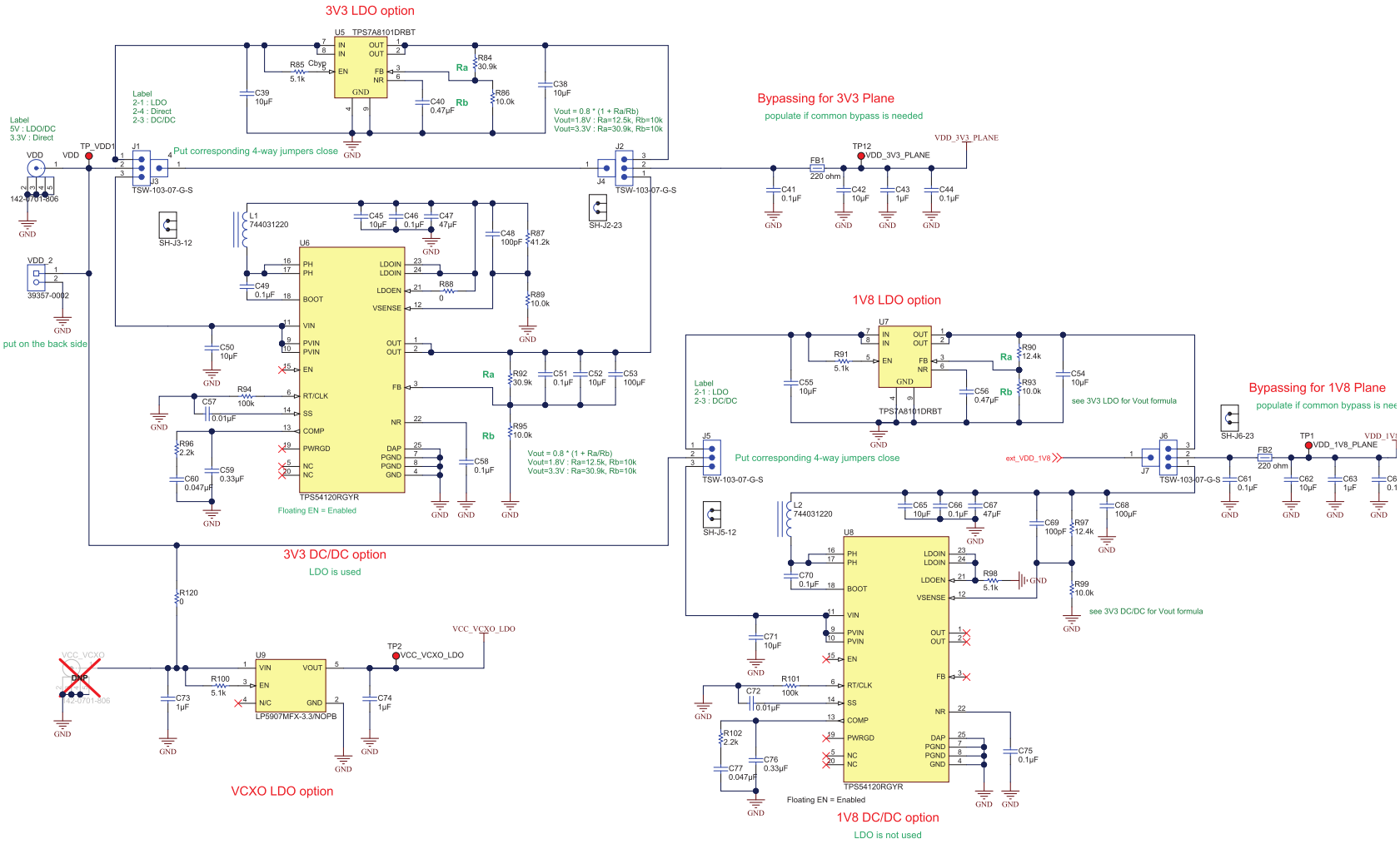


Figure 5-1. Power Supply Connection

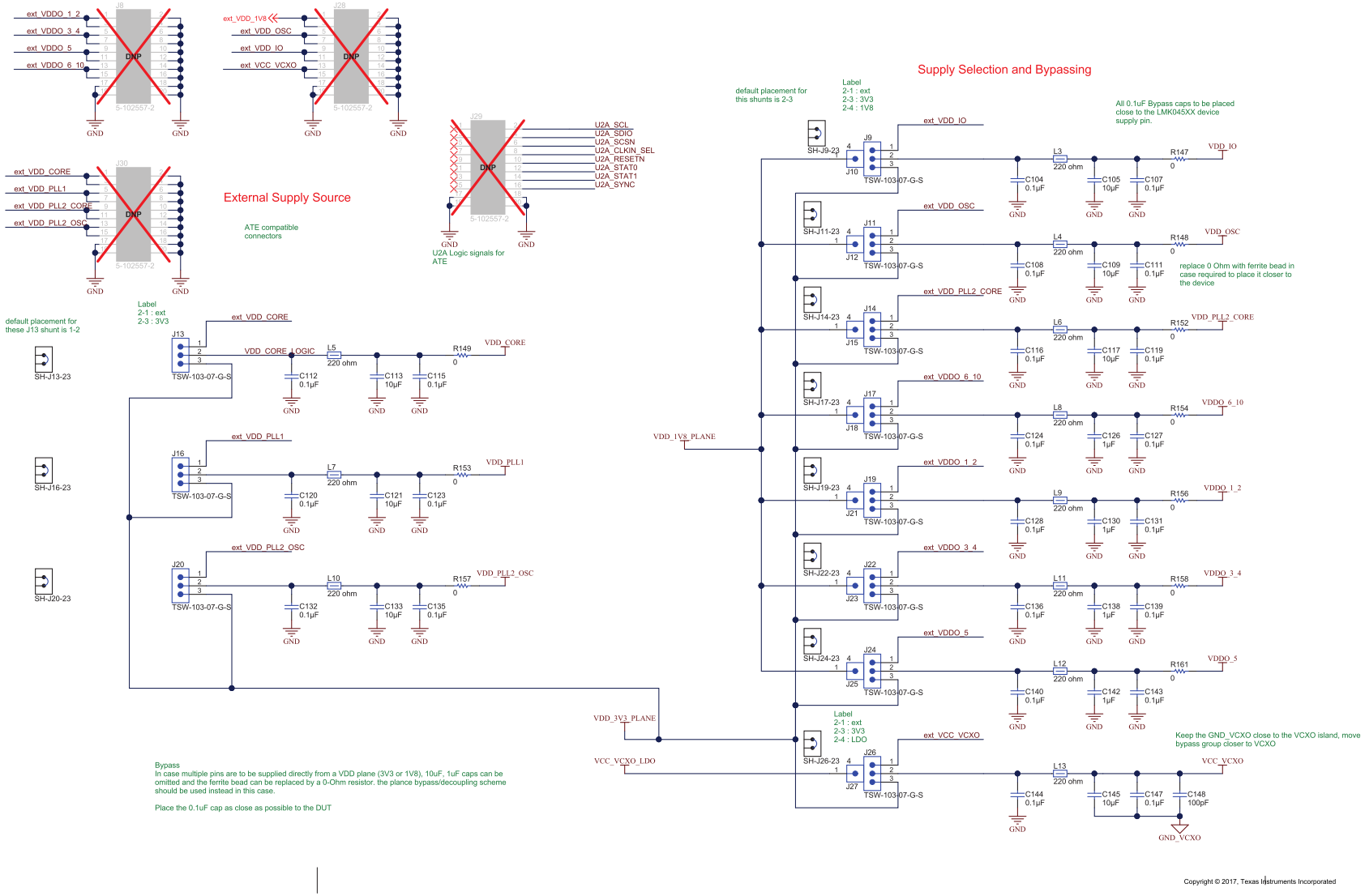


Figure 5-2. Power Distribution

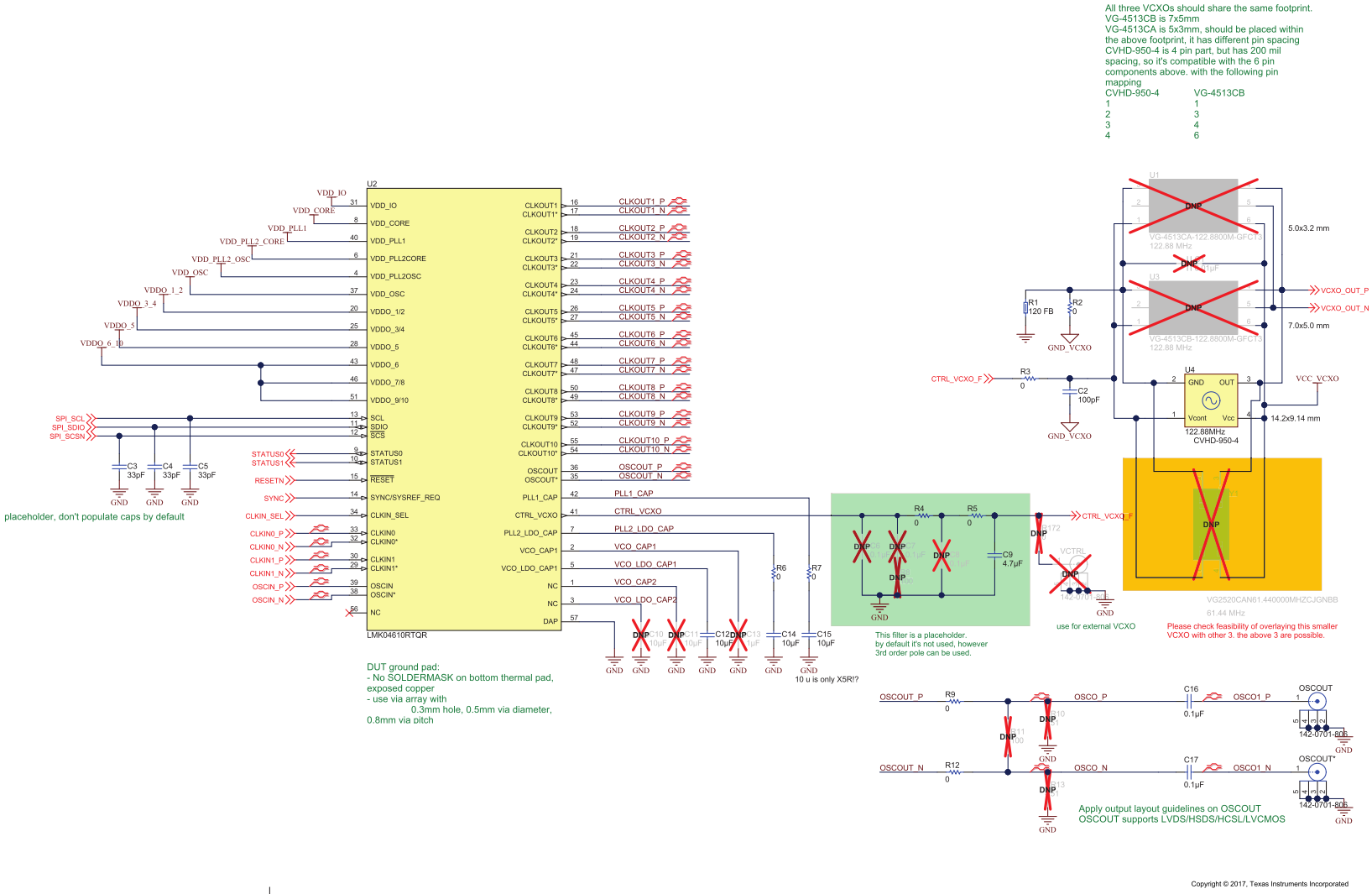


Figure 5-3. LMK04610 Main

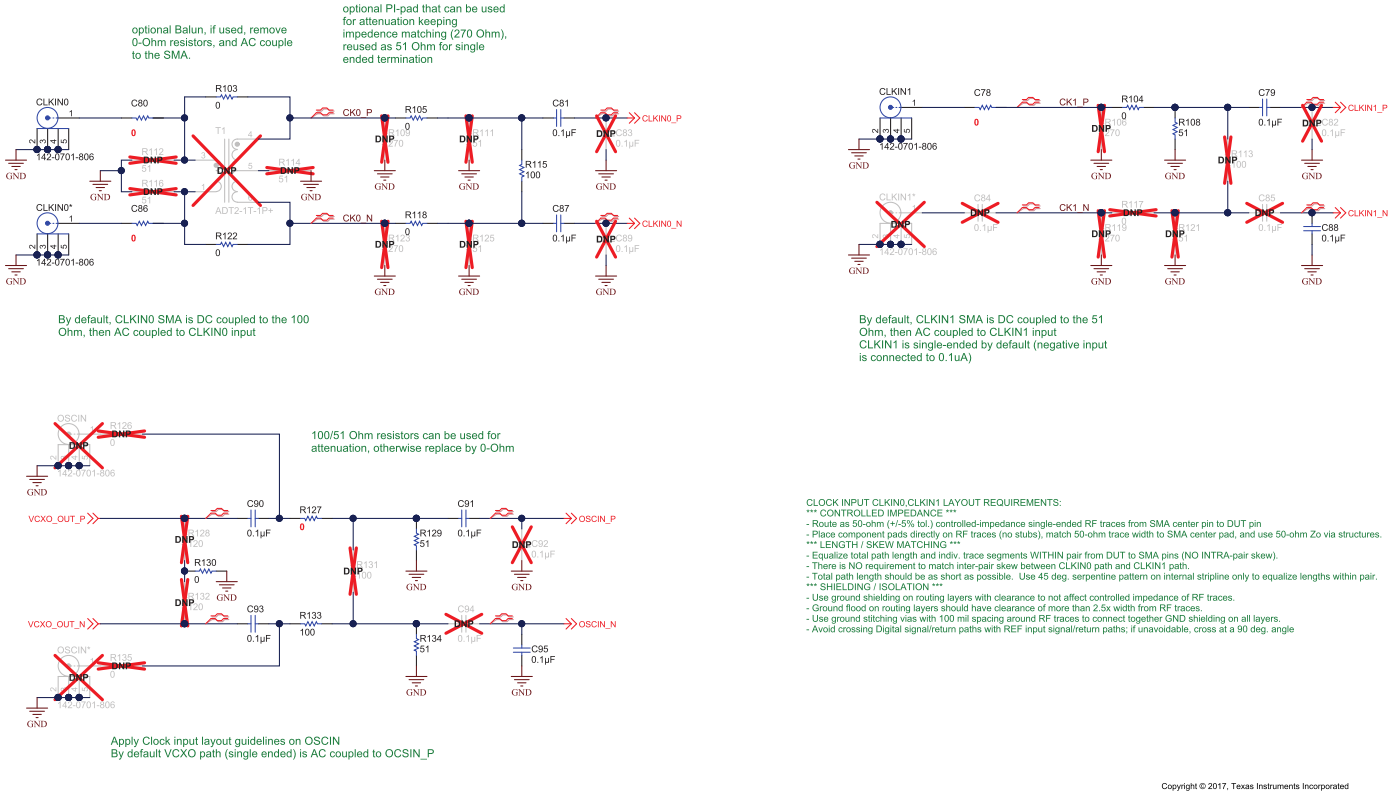


Figure 5-4. Inputs

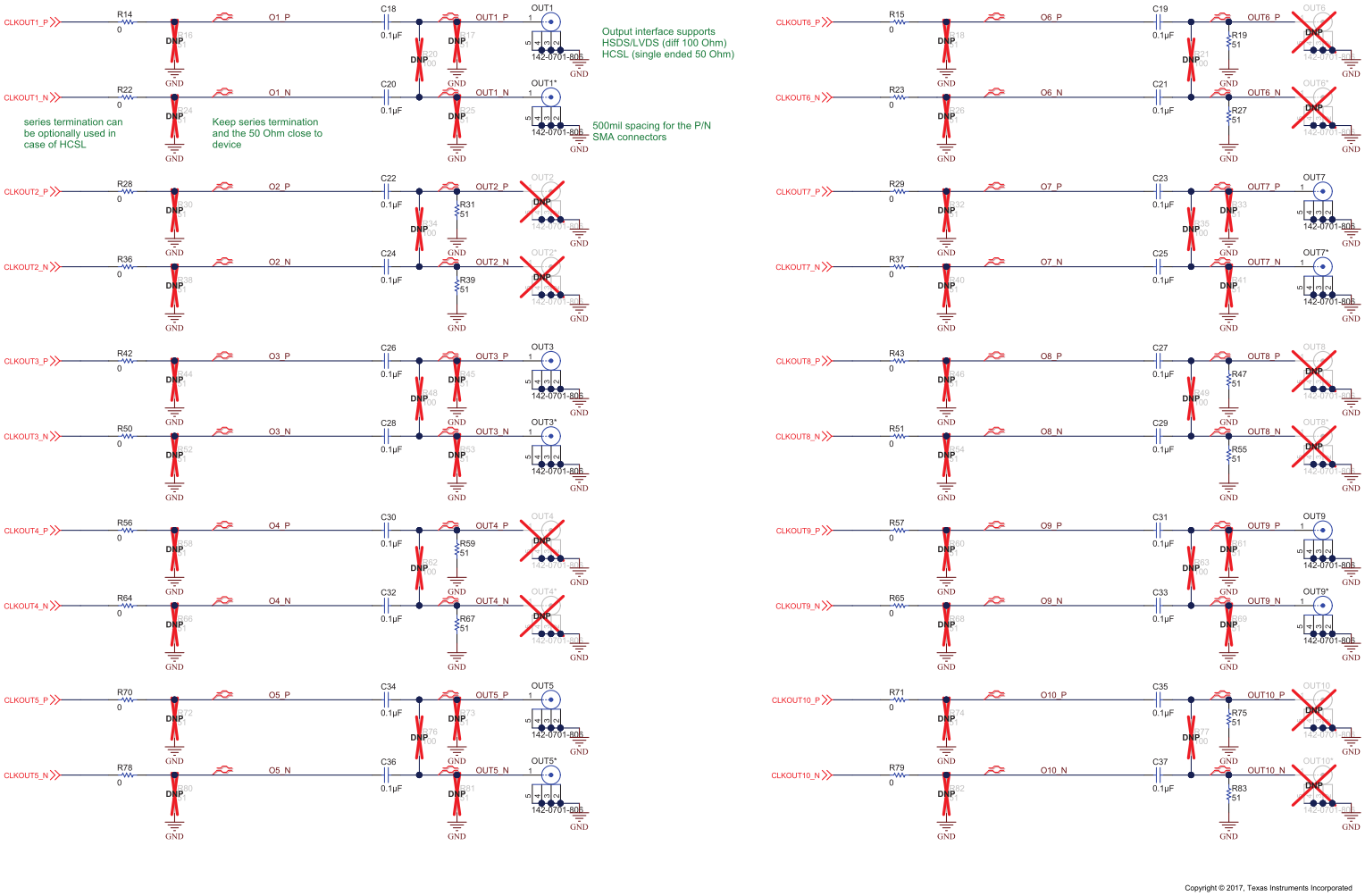


Figure 5-5. Outputs

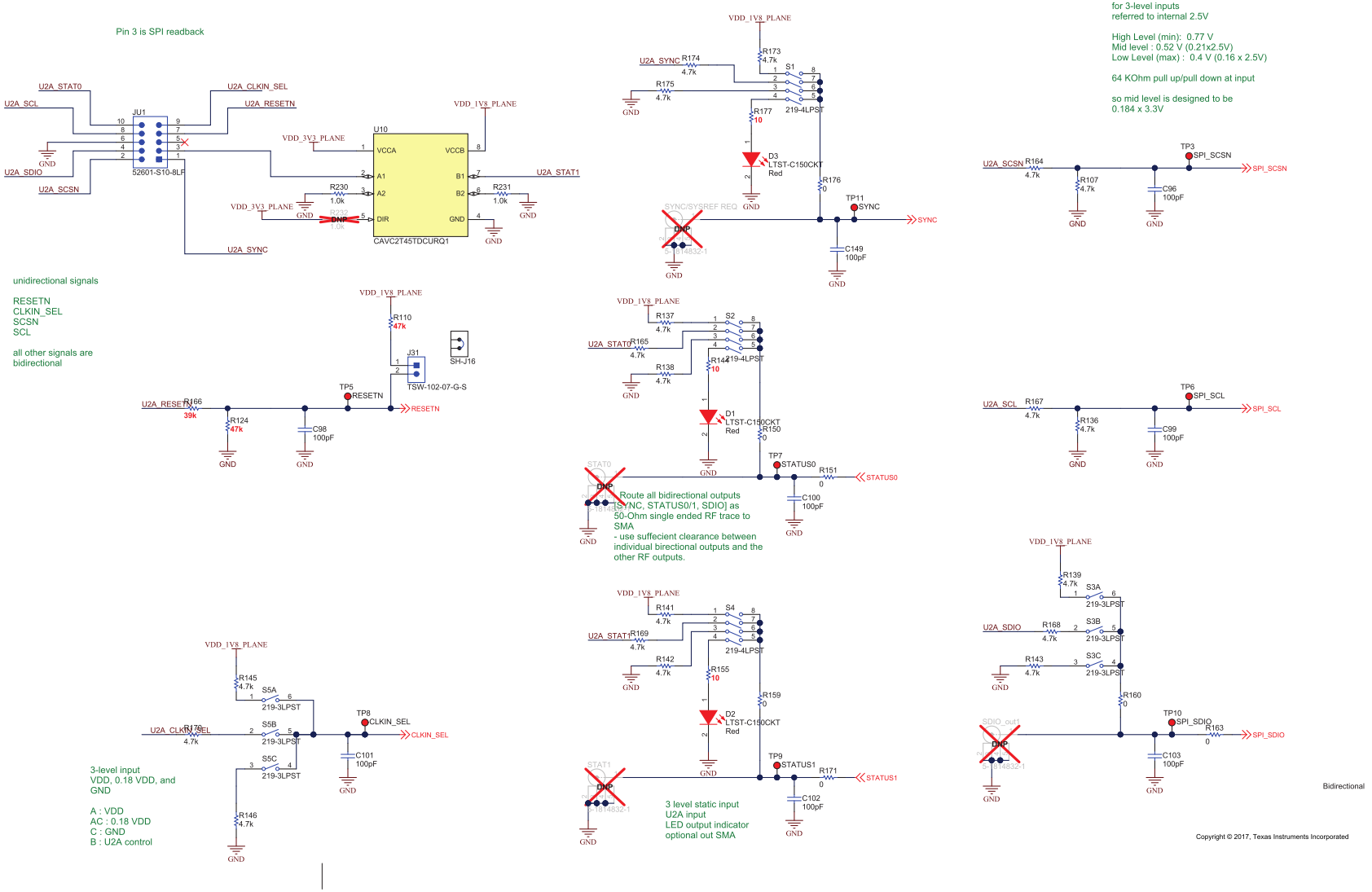


Figure 5-6. Logic/GPIO

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2017) to A Revision	Page
• Updated the text in the *Overview* section	3
• Changed typical rms value from: 60 fs to: 65 fs	3
• Changed typical power consumption value from: 0.9 W to: 880 mW	3

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