# TSA50N20M
200V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.
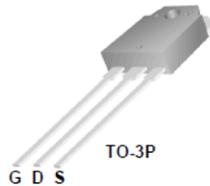
Features

- 50A,200V,Max.$R_{DS(on)}$=0.046Ω @ V_{GS} =10V
- Low gate charge
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

TO-3P

G D S
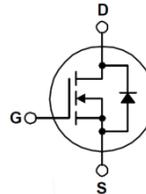
Absolute Maximum Ratings T_J=25℃ unless otherwise specified

Absolute Maximum Ratings T_C = 25⁰C, unless otherwise noted

Parameter		Symbol	Value	Unit
Drain-Source Voltage	(note1)	V_{DSS}	200	V
Continuous Drain Current		I_D	50	A
Pulsed Drain Current	(note2)	I_{DM}	200	
Gate-Source Voltage		V_{GSS}	±20	V
Single Pulse Avalanche Energy	(note2)	E_{AS}	1700	mJ
Power Dissipation		P_D	300	W
Derating Factor above 25°C			2.4	W/⁰C
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~+150	⁰C

Thermal Resistance Characteristics

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	0.42	⁰C/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	40	

Electrical Characteristics T_J=25℃ unless otherwise specified

Specifications T_J = 25℃, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	200	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	--	4	V
Drain-Source On-Resistance (Note4)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 25A	--	0.041	0.046	Ω
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	4010	--	pF
Output Capacitance	C_{oss}		--	437	--	
Reverse Transfer Capacitance	C_{rss}		--	280	--	
Total Gate Charge	Q_g	V_{DD} = 160V, I_D = 50A, V_{GS} 0 to 10V	--	244	--	nC
Gate-Source Charge	Q_{gs}		--	16	--	
Gate-Drain Charge	Q_{gd}		--	144	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 100V, I_D = 50A, VGS =10V.RG = 25Ω	--	53	--	ns
Turn-on Rise Time	t_r		--	65	--	
Turn-off Delay Time	$t_{d(off)}$		--	429	--	
Turn-off Fall Time	t_f		--	230	--	
Drain-Source Body Diode Characteristics						
Continuous Source Current	I_{SD}	Integral PN-diode in MOSFET	--	--	50	A
Pulsed Source Current	I_{SM}		--	--	200	
Body Forward Voltage	V_{SD}	I_S = 20A, V_{GS} = 0V	--	--	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0V, I_F = 10A, di$_F$/dt =100A /μs	--	261	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.04	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L = 10mH, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 ℃

3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Characteristics $T_J = 25^oC$, unless otherwise noted

Figure 1. Output Characteristics ($T_J = 25^oC$)

Drain Current (20 A/div.) vs. Drain to Source Voltage

120 A ... 0 A, 0 V ... 5 V/div. ... 30 V

VGS = 10 V
VGS = 5.5 V
VGS = 5 V
VGS = 4.5 V
VGS = 3 V VGS = 4 V
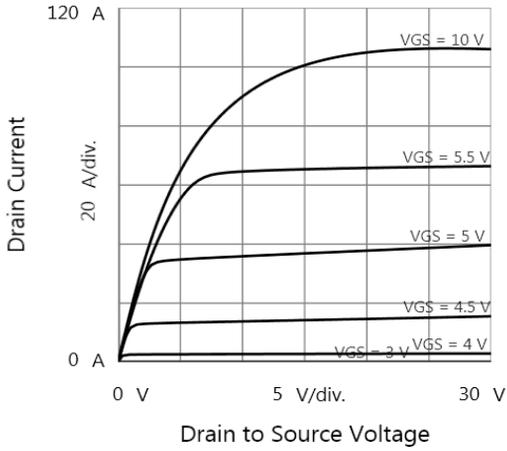
Figure 2. Transfer Characteristics

Drain Current (10 A/div.) vs. Gate to Source Voltage

80 A ... 0 A, 0 V ... 1 V/div. ... 8 V
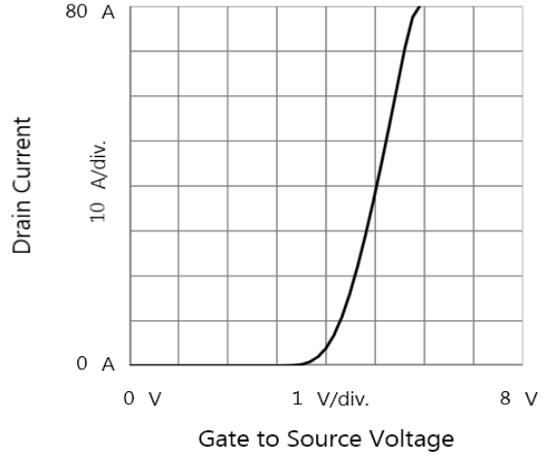
Figure 3. Drain to Source Resistance vs. Drain Current

Drain to Source Resistance (5 m ohm/div.) vs. Drain Current

65 m ohm ... 30 m ohm, 5 A ... 5 A/div. ... 40 A

VGS = 8 V
VGS = 10 V
VGS = 12 V
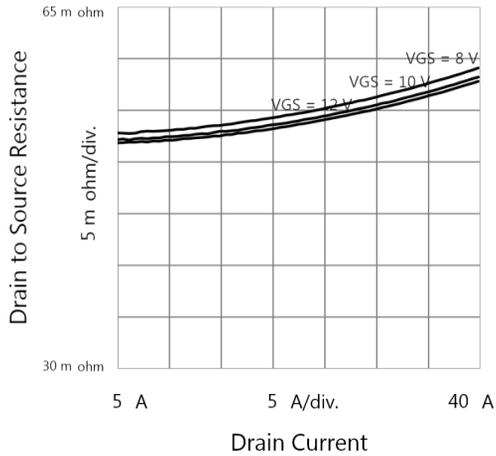
Figure 4. Drain to Source Resistance vs. Gate to Source Voltage

Drain to Source Resistance (5 m ohm/div.) vs. Gate to Source Voltage

65 m ohm ... 30 m ohm, 5 V ... 1 V/div. ... 15 V

ID = 20 A
ID = 10 A
ID = 5 A
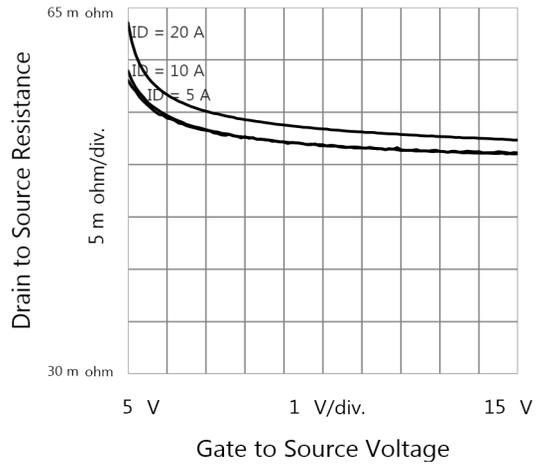
Figure 5. Drain to Source Voltage vs. Gate to Source Voltage

Drain to Source Voltage (1 V/div.) vs. Gate to Source Voltage

10 V ... 0 V, 2 V ... 2 V/div. ... 15 V

ID = 5 A
ID = 20 A
ID = 10 A
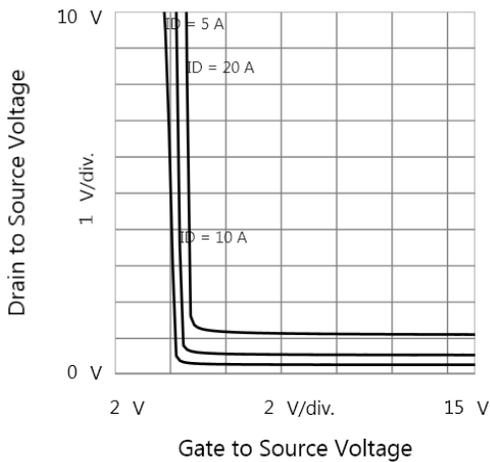
Figure 6. Body Diode Forward Characteristics

Source Current (5 A/div.) vs. Source to Drain Voltage

40 A ... 0 A, 0 V ... 200 m V/div. ... 2 V
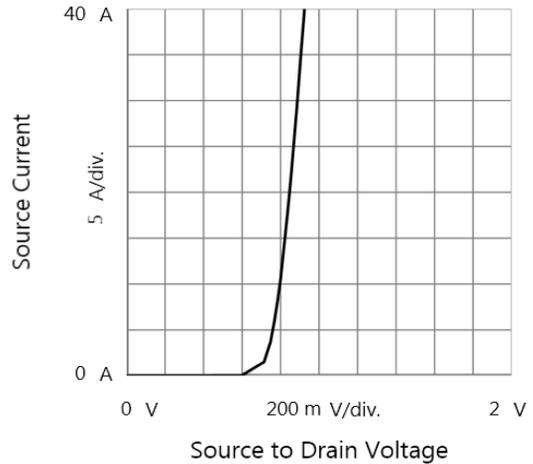
Typical Characteristics $T_J = 25°C$, unless otherwise noted

Figure 7. Capacitance

Capacitance

decade/div.

100 n F

Ciss

Coss

Crss

10 p F

0 V   10 V/div.   100 V

Drain to Source Voltage

Figure 8. Gate Charge

Gate to Source Voltage

1 V/div.

10 V

0 V

0 C   20 n C/div.   120 n C
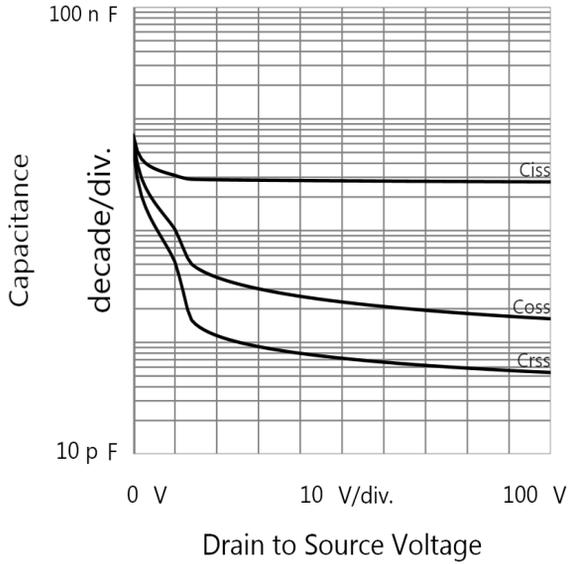
Gate Charge
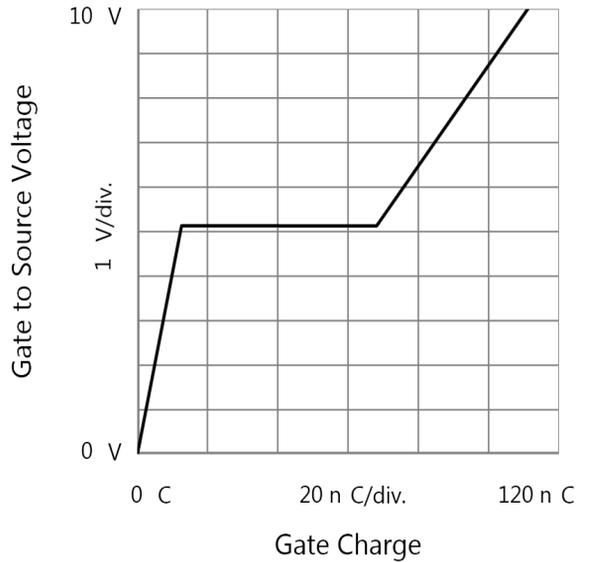
Figure 9. Transient Thermal Impedance

Z_{thJC}, Thermal Impedance (K/W)

D= 0.5
D= 0.2
D= 0.1
D= 0.05
D= 0.02
D= 0.01
Single Pulse

10^{-6} 10^{-5} 10^{-4} 10^{-3} 10^{-2} 10^{-1} 10^{0} 10^{1}

T_p, Pulse Width (s)
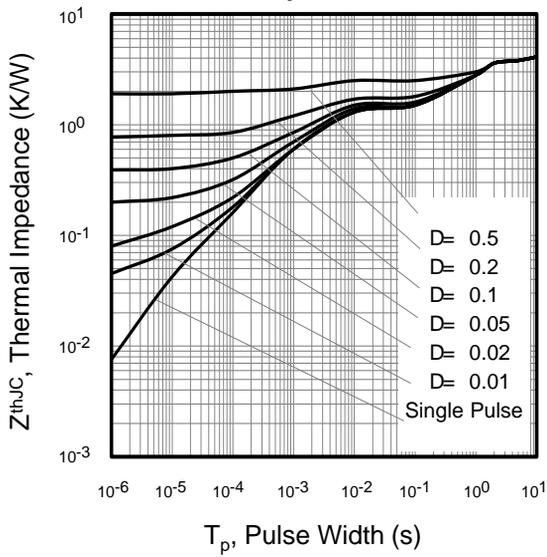
Figure 10. Transient Thermal Impedance

Z_{thJC}, Thermal Impedance (K/W)

D= 0.5
D= 0.2
D= 0.1
D= 0.05
D= 0.02
D= 0.01
Single Pulse

10^{-7} 10^{-6} 10^{-5} 10^{-4} 10^{-3} 10^{-2} 10^{-1}

T_p, Pulse Width (s)

Typical Characteristics $T_J = 25^0C$, unless otherwise noted

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

Duty Factor

NOTES:
DUTY FACTOR: D=t1/t2
PEAK TJ=P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$+TC

$Z_{\theta JC}$, Thermal Impedance (Normalized)

t_p, Rectangular Pulse Duration (s)
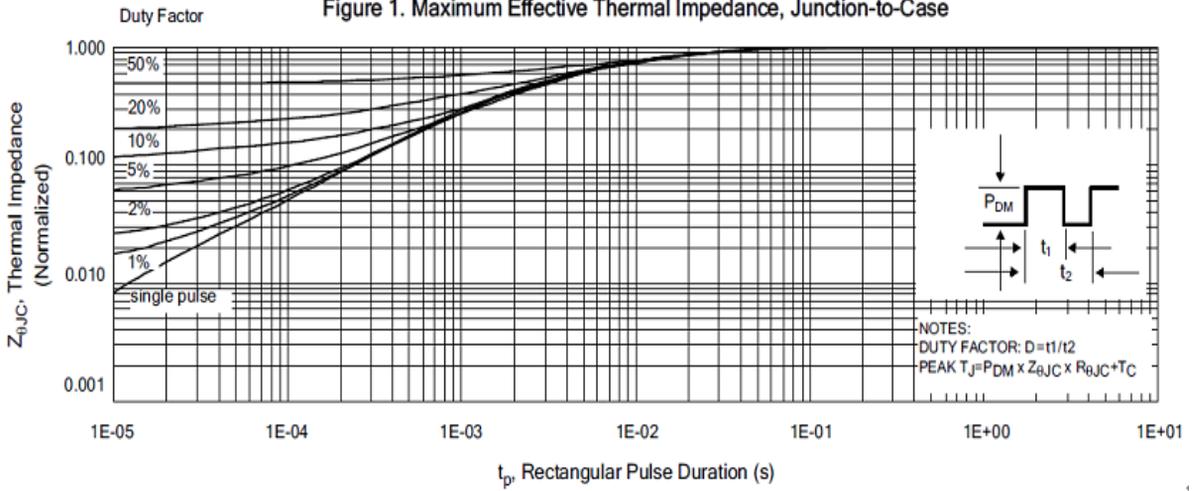
Figure 2. Maximum Power Dissipation vs Case Temperature

P_D, Power Dissipation (W)

T_C, Case Temperature ($^{\circ}$C)
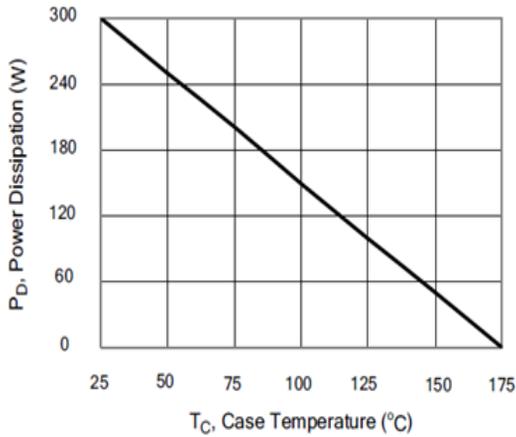
Figure 3. Maximum Continuous Drain Current vs Case Temperature

I_D, Drain Current (A)

T_C, Case Temperature ($^{\circ}$C)
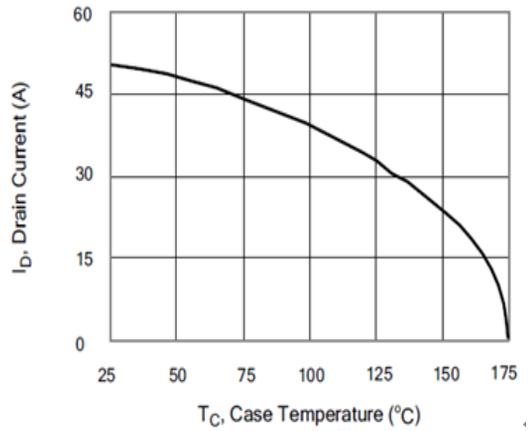
Figure 4. Typical Output Characteristics

PULSE DURATION = 250 µS
DUTY FACTOR = 0.5% MAX
T_C = 25°C

V_{GS} = 15V
V_{GS} = 8.0V
V_{GS} = 6.0V
V_{GS} = 5.0V
V_{GS} = 4.5V

I_D, Drain Current (A)

V_{DS}, Drain-to-Source Voltage (V)
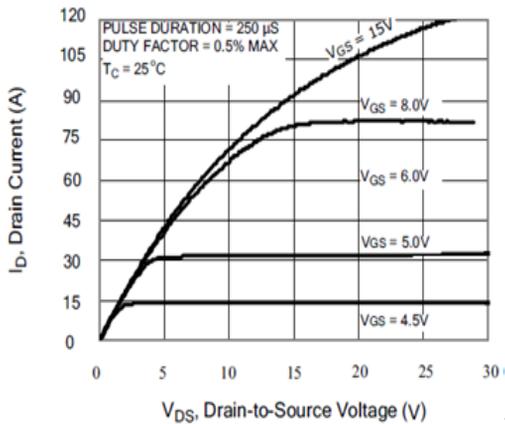
Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

PULSE DURATION = 2 µS
DUTY FACTOR = 0.5% MAX
T_C = 25°C

I_D = 100A
I_D = 50A
I_D = 28A
I_D = 14A

RDS(ON), Drain-to-Source ON Resistance (mΩ)

V_{GS}, Gate-to-Source Voltage (V)
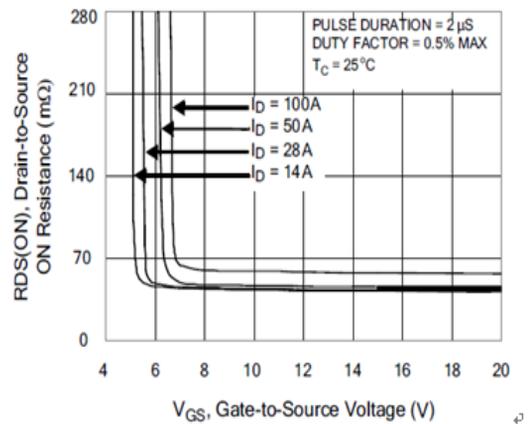
Typical Characteristics $T_J = 25^oC$, unless

Figure 6. Maximum Peak Current Capability

TRANSCONDUCTANCE MAY LIMIT CURRENT IN THIS REGION

FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25}\left[\sqrt{\frac{150 - T_C}{125}}\right]$$

$V_{GS} = 10V$

t_p, Pulse Width (s)

I_{DM}, Peak Current (A)
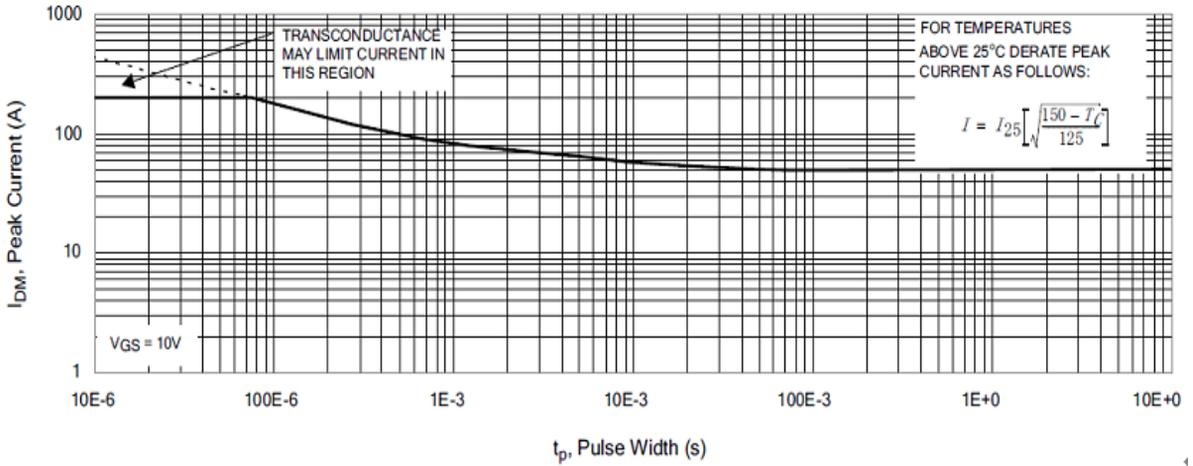
Figure 7. Typical Transfer Characteristics

PULSE DURATION = 250 µs
DUTY CYCLE = 0.5% MAX
$V_{DS} = 10V$

+150 °C
+25 °C
-55 °C

I_D, Drain-to-Source Current (A)

V_{GS}, Gate-to-Source Voltage (V)
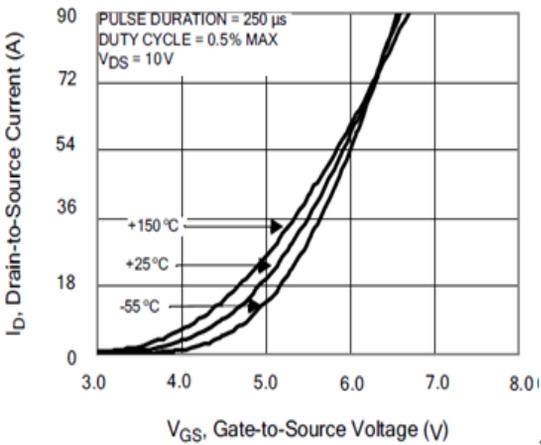
Figure 8. Unclamped Inductive Switching Capability

If R = 0: $t_{AV} = (L \times I_{AS})/(1.3BV_{DSS} - V_{DD})$
If R ≠ 0: $t_{AV} = (L/R) \ln[I_{AS} \times R)/(1.3BV_{DSS} - V_{DD}) + 1]$
R equals total Series resistance of Drain circuit

STARTING $T_J = 25°C$
STARTING $T_J = 150°C$

I_{AS}, Avalanche Current (A)

t_{AV}, Time in Avalanche (s)
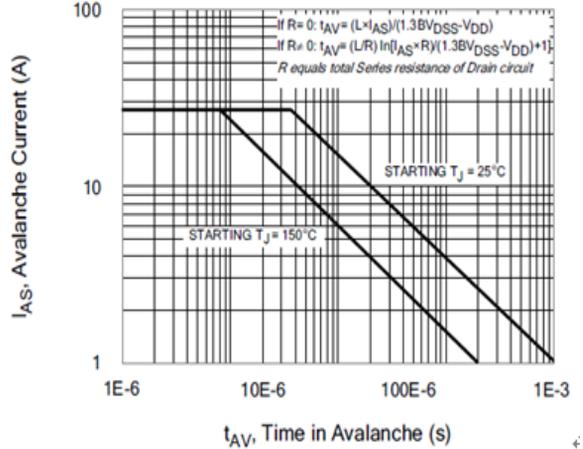
Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

PULSE DURATION = 2 µs
DUTY CYCLE = 0.5% MAX
$T_C = 25°C$

$V_{GS} = 20V$
$V_{GS} = 10V$

$R_{DS(ON)}$, Drain-to-Source ON Resistance (mΩ)

I_D, Drain Current (A)
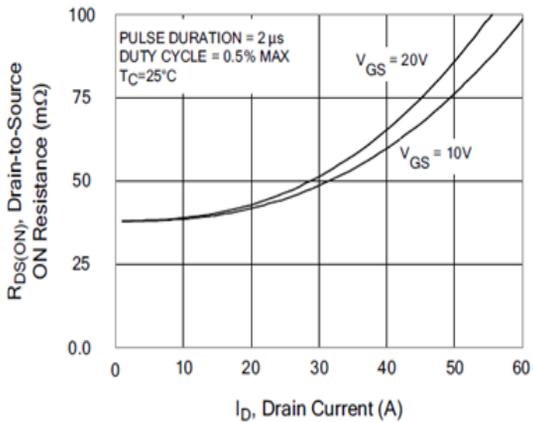
Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

PULSE DURATION = 250 µs
DUTY CYCLE = 0.5% MAX
$V_{GS} = 10V$, $I_D = 28A$

$R_{DS(ON)}$, Drain-to-Source Resistance (Normalized)

T_J, Junction Temperature (°C)
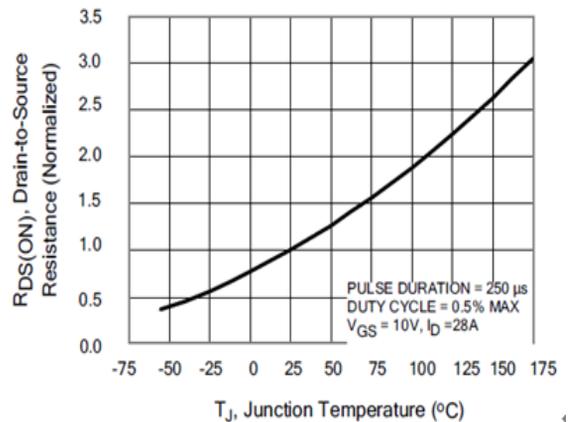
Figure 11. Typical Breakdown Voltage vs Junction Temperature

Figure showing BV_{DSS}, Drain-to-Source Breakdown Voltage (Normalized) vs T_J, Junction Temperature (°C). $V_{GS} = 0V$, $I_D = 250\,\mu A$
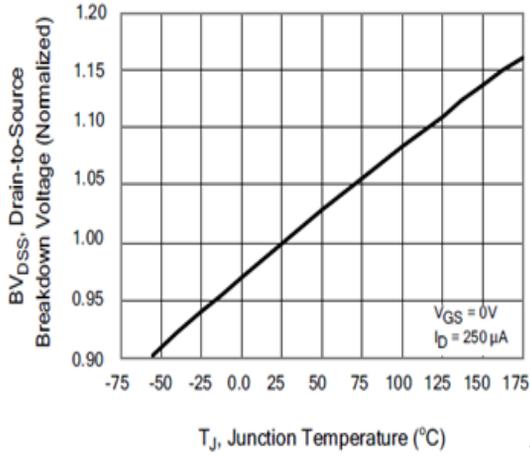
Figure 12. Typical Threshold Voltage vs Junction Temperature

Figure showing $V_{GS(TH)}$, Threshold Voltage (Normalized) vs T_J, Junction Temperature (°C). $V_{GS} = V_{DS}$, $I_D = 250\,\mu A$
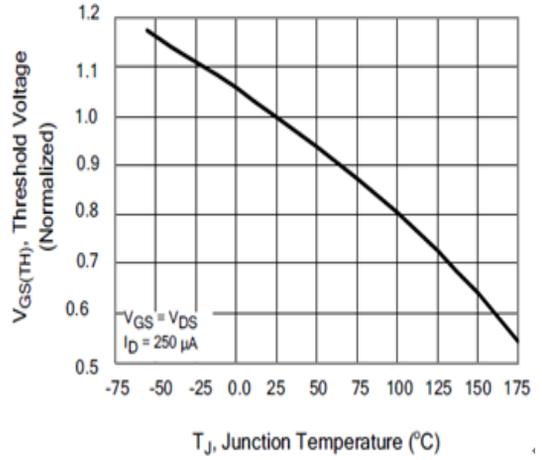
Figure 13. Maximum Forward Bias Safe Operating Area

Figure showing I_D, Drain Current (A) vs V_{DS}, Drain-to-Source Voltage (V). OPERATION IN THIS AREA MAY BE LIMITED BY $R_{DS(ON)}$. T_J = MAX RATED, T_C = 25°C, Single Pulse. Curves labeled 100µs, 1.0ms, 10ms, DC
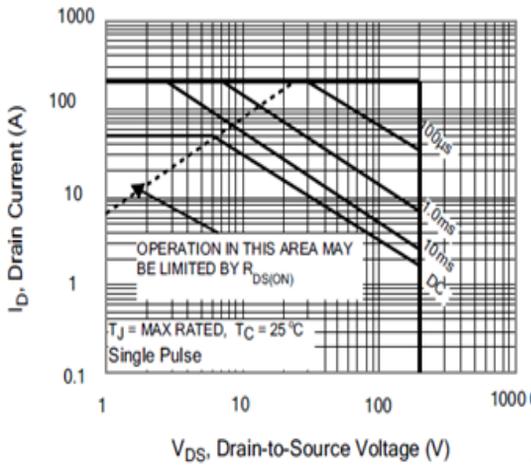
Figure 14. Capacitance vs Vds

Figure showing Capacitance, pF vs Vds, Drain to Source Voltage, Volts
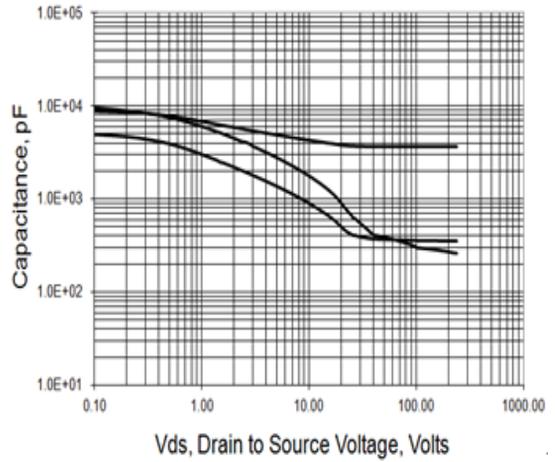
Figure 15. Typical Gate Charge

Figure showing Vgs, gate to source voltage (V) vs Qg, Total gate charge (nC)
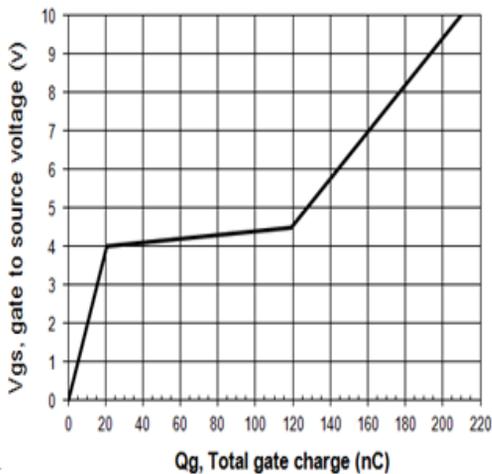
Figure 16. Typical Body Diode Transfer Characteristics

Figure showing I_{SD}, Reverse Drain Current (A) vs V_{SD}, Source-to-Drain Voltage (V). Curves: +150°C, +25°C, -55°C. $V_{GS} = 0V$
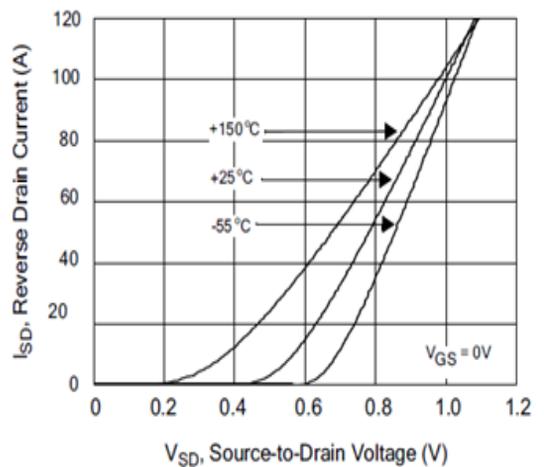
## Figure A：Gate Charge Test Circuit and
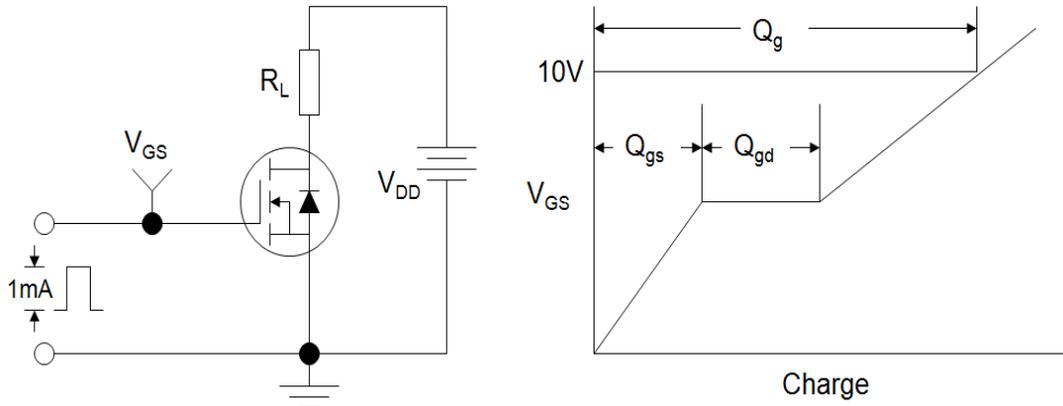
## Figure B：Resistive Switching Test Circuit and Waveform
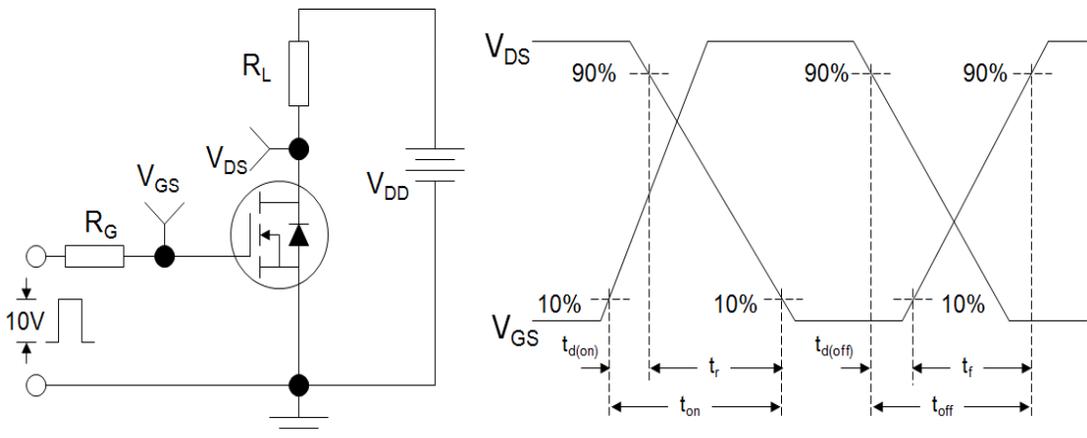
Figure C：Unclamped Inductive Switching Test Circuit and Waveform
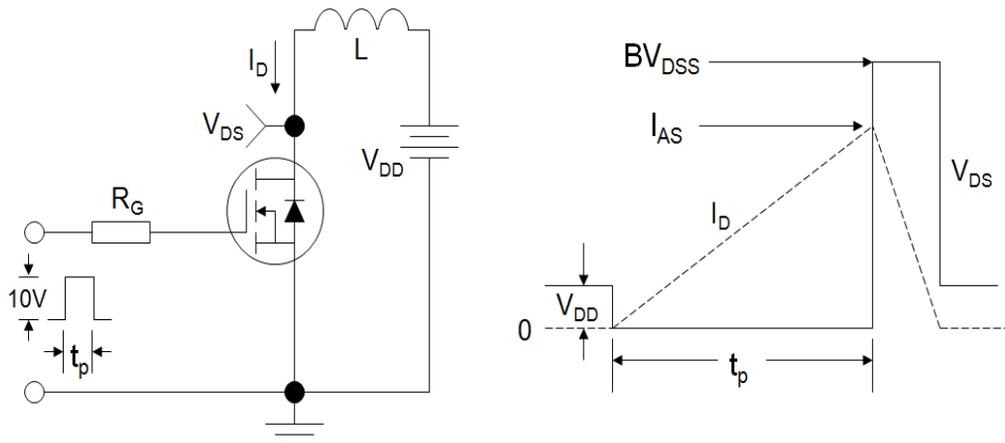
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