NXB0106-Q100

Dual supply translating transceiver; auto direction sensing; 3-state

Rev. 2.1 — 31 July 2024 Product data sheet

1. General description

The NXB0106-Q100 is an 6-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 6-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V).

Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2500 V for A port
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 15000 V for B port
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- DHVQFN package with Side-Wettable Flanks enabling Automated Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXB0106PW-Q100	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NXB0106BQ-Q100	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

nexperia

4. Functional diagram

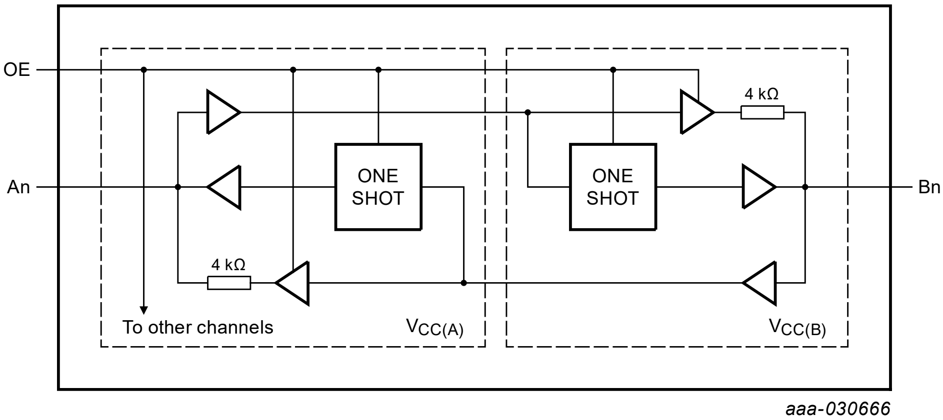
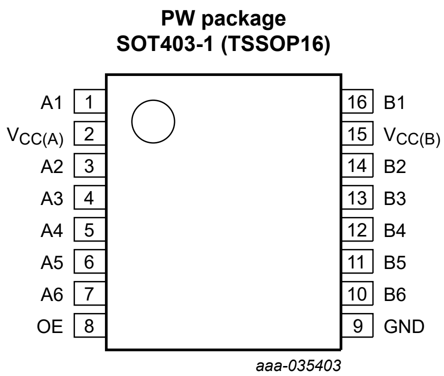
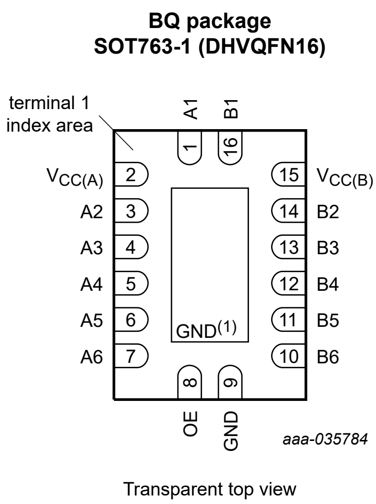


Fig. 1. Functional diagram (for one channel)

5. Pinning information

5.1. Pinning





(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6	1, 3, 4, 5, 6, 7	data input or output (referenced to $V_{CC(A)}$)
$V_{CC(A)}$	2	supply voltage A
OE	8	output enable input (active HIGH; referenced to $V_{CC(A)}$)
GND	9	ground (0 V)
B1, B2, B3, B4, B5, B6	16, 14, 13, 12, 11, 10	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	15	supply voltage B

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	L	Z	Z
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	H	input or output	output or input
GND[1]	GND[1]	X	Z	Z

[1] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
V_I	input voltage		[1]	-0.5	+6.5	V
V_O	output voltage	Active mode	[1] [2] [3]	-0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	500	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Power-down or 3-state mode; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V			
		A port	0	3.6	V
		B port	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

9. Static characteristics

Table 6. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = -20 µA	-	1.1	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = 20 µA	-	0.09	-	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	-	±1	µA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V to V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V [1]	-	-	±1	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	-	±1	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	-	±1	µA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	5	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	5	-	pF
		B port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	8	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 7. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
V_{OH}	HIGH-level output voltage	A or B port; I_O = -20 μA [2]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V	V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V	V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 20 μA [2]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V	-	0.4	-	0.4	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	0.4	-	0.4	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	±2	-	±5	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V [2]	-	±2	-	±10	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	±2	-	±10	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	-	±2	-	±10	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A [1]					
		$I_{CC(A)}$					
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	4.3	-	15	μA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	4.3	-	20	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	1.7	-	15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	-1.7	-	-15	μA
		$I_{CC(B)}$					
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	4.3	-	20	μA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	11.1	-	65	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	-1.7	-	-15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	1.7	-	15	μA
		$I_{CC(A)}$ + $I_{CC(B)}$					
		$V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	12.8	-	70	μA

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.

10. Dynamic characteristics

Table 9. Typical dynamic characteristics for temperature 25 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
$V_{CC(A)}$ = 1.2 V; T_{amb} = 25 °C							
t_{pd}	propagation delay	A to B	6.9	5.6	5.1	4.9	ns
		B to A	7.1	5.8	5.0	5.1	ns
t_{en}	enable time	OE to A, B	500	500	500	500	ns
t_{dis}	disable time	OE to A; no external load [2]	14.5	14.5	14.5	14.5	ns
		OE to B; no external load [2]	12.2	10.1	9.3	8.7	ns
		OE to A; see Fig. 3	87	87	87	87	ns
		OE to B; see Fig. 3	98	71	101	68	ns
t_t	transition time	A port	4.2	4.2	4.2	4.2	ns
		B port	2.7	2.0	1.7	1.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	1.4	0.7	0.6	0.5	ns
t_W	pulse width	data inputs	13	13	13	13	ns
f_{data}	data rate		60	60	60	60	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{pd}	propagation delay	A to B	1.4	11.4	1.2	8.0	1.1	6.7	0.8	6.2	ns
		B to A	0.9	10.8	0.7	8.3	0.4	7.8	0.3	7.2	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	3.4	18.0	3.4	18.0	3.4	18.0	3.4	18.0	ns
		OE to B; no external load [2]	3.4	19.5	3.4	15.0	2.8	13.0	1.6	11.5	ns
		OE to A; see Fig. 3	-	100	-	100	-	100	-	100	ns
		OE to B; see Fig. 3	-	150	-	105	-	150	-	105	ns
t_t	transition time	A port	0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
		B port	1.0	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	2.6	-	1.9	-	1.6	-	1.3	ns
t_W	pulse width	data inputs	20	-	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	-	50	Mbps

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{pd}	propagation delay	A to B		1.6	10.8	1.4	7.9	1.3	6.2	1.2	5.3	ns
		B to A		1.5	9.2	1.3	7.2	0.8	6.3	0.5	5.8	ns
t_{en}	enable time	OE to A, B		-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load	[2]	2.7	13.0	2.7	13.0	2.7	13.0	2.7	13.0	ns
		OE to B; no external load	[2]	3.7	18.0	2.8	13.0	2.3	11.5	1.4	9.5	ns
		OE to A; see Fig. 3		-	120	-	120	-	120	-	120	ns
		OE to B; see Fig. 3		-	150	-	105	-	150	-	105	ns
t_t	transition time	A port		0.7	5.1	0.7	5.0	1.0	5.0	0.7	5.0	ns
		B port		1.0	7.3	0.7	5.0	0.7	3.9	0.6	3.8	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	0.8	-	0.7	-	0.6	-	0.6	ns
t_W	pulse width	data inputs		19	-	17	-	17	-	17	-	ns
f_{data}	data rate			-	52	-	60	-	60	-	60	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{pd}	propagation delay	A to B		-	-	1.1	7.5	1.0	5.2	0.9	4.2	ns
		B to A		-	-	1.0	5.6	0.6	5.0	0.3	4.2	ns
t_{en}	enable time	OE to A, B		-	-	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load	[2]	-	-	2.3	8.0	2.3	8.0	2.3	8.0	ns
		OE to B; no external load	[2]	-	-	1.8	11.5	2.5	9.5	1.1	8.0	ns
		OE to A; see Fig. 3		-	-	-	85	-	85	-	85	ns
		OE to B; see Fig. 3		-	-	-	105	-	150	-	100	ns
t_t	transition time	A port		-	-	0.8	3.6	0.6	3.6	0.5	3.5	ns
		B port		-	-	0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	0.4	-	0.3	-	0.3	ns
t_W	pulse width	data inputs		-	-	13	-	10	-	10	-	ns
f_{data}	data rate			-	-	-	80	-	100	-	100	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{pd}	propagation delay	A to B	-	-	-	-	0.9	4.8	0.8	3.9	ns
		B to A	-	-	-	-	0.5	4.3	0.2	3.7	ns
t_{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	-	1.9	6.5	1.8	6.5	ns
		OE to B; no external load [2]	-	-	-	-	0.9	8.5	1.6	7.0	ns
		OE to A; see Fig. 3	-	-	-	-	-	125	-	125	ns
		OE to B; see Fig. 3	-	-	-	-	-	150	-	100	ns
t_t	transition time	A port	-	-	-	-	0.5	3.0	0.5	3.0	ns
		B port	-	-	-	-	0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	-	-	0.4	-	0.3	ns
t_W	pulse width	data inputs	-	-	-	-	9.0	-	9.0	-	ns
f_{data}	data rate		-	-	-	-	-	110	-	110	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C [1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4; for waveforms see Fig. 2 and Fig. 3.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{pd}	propagation delay	A to B	1.4	11.9	1.2	9.0	1.1	7.3	0.8	6.5	ns
		B to A	0.9	10.9	0.7	8.8	0.4	7.9	0.3	7.7	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	3.4	19.0	3.4	19.0	3.4	19.0	3.4	19.0	ns
		OE to B; no external load [2]	3.4	22.0	3.4	16.0	2.8	14.0	1.6	12.5	ns
		OE to A; see Fig. 3	-	105	-	105	-	105	-	105	ns
		OE to B; see Fig. 3	-	155	-	110	-	155	-	105	ns
t_t	transition time	A port	0.8	8.1	0.8	7.9	0.8	7.9	0.8	7.9	ns
		B port	1.0	9.1	0.7	6.1	0.7	5.8	0.6	5.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	2.6	-	1.9	-	1.6	-	1.3	ns
t_W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f_{data}	data rate		-	40	-	40	-	40	-	40	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{pd}	propagation delay	A to B	1.6	11.1	1.4	8.1	1.3	6.5	1.2	5.5	ns
		B to A	1.5	9.6	1.2	7.8	0.8	6.6	0.5	6.3	ns
t_{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	2.7	14.0	2.7	14.0	2.7	14.0	2.7	14.0	ns
		OE to B; no external load [2]	3.7	20.5	2.8	14.5	2.3	12.5	1.4	10.5	ns
		OE to A; see Fig. 3	-	125	-	125	-	125	-	125	ns
		OE to B; see Fig. 3	-	150	-	105	-	150	-	105	ns
t_t	transition time	A port	0.8	6.4	0.7	6.3	1.0	6.3	0.7	6.3	ns
		B port	1.0	9.1	0.7	6.3	0.7	4.9	0.6	4.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.7	-	0.6	-	0.6	ns
t_W	pulse width	data inputs	22	-	18	-	18	-	18	-	ns
f_{data}	data rate		-	45	-	55	-	55	-	55	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{pd}	propagation delay	A to B	-	-	1.1	7.6	1.0	5.8	0.9	4.4	ns
		B to A	-	-	1.0	7.1	0.6	5.1	0.3	4.8	ns
t_{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	2.3	9.0	2.3	9.0	2.3	9.0	ns
		OE to B; no external load [2]	-	-	1.8	13.0	2.6	10.5	1.1	8.5	ns
		OE to A; see Fig. 3	-	-	-	85	-	85	-	85	ns
		OE to B; see Fig. 3	-	-	-	105	-	150	-	100	ns
t_t	transition time	A port	-	-	0.8	4.5	0.6	4.5	0.5	4.4	ns
		B port	-	-	0.6	6.1	0.7	4.9	0.6	4.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.4	-	0.3	-	0.3	ns
t_W	pulse width	data inputs	-	-	13	-	13	-	13	-	ns
f_{data}	data rate		-	-	-	75	-	80	-	80	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{pd}	propagation delay	A to B	-	-	-	-	0.9	5.3	0.8	4.2	ns
		B to A	-	-	-	-	0.5	4.4	0.2	4.0	ns
t_{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load [2]	-	-	-	-	1.9	7.0	1.8	7.0	ns
		OE to B; no external load [2]	-	-	-	-	0.9	9.5	1.6	7.5	ns
		OE to A; see Fig. 3	-	-	-	-	-	125	-	125	ns
		OE to B; see Fig. 3	-	-	-	-	-	150	-	100	ns
t_t	transition time	A port	-	-	-	-	0.5	3.8	0.5	3.8	ns
		B port	-	-	-	-	0.7	4.9	0.6	4.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	-	-	0.4	-	0.3	ns
t_W	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

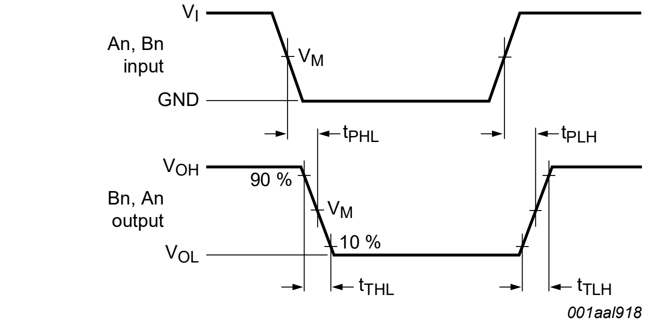
Table 12. Typical power dissipation capacitance [1] [2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			$V_{CC(B)}$							
			1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V	
T_{amb} = 25 °C										
C_{PD}	power dissipation capacitance	outputs enabled; OE = $V_{CC(A)}$								
		A port: (direction A to B)	7.0	6.5	7.2	7.6	7.6	7.0	8.0	pF
		A port: (direction B to A)	9.6	10.0	9.8	10.1	10.5	10.3	10.8	pF
		B port: (direction A to B)	23.3	28.7	23.1	23.1	23.7	25.9	25.9	pF
		B port: (direction B to A)	17.8	25.5	17.1	16.8	17.4	21.0	20.5	pF
		outputs disabled; OE = GND								
		A port: (direction A to B)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	pF
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction A to B)	0.01	0.02	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction B to A)	0.2	0.3	0.2	0.2	0.3	0.3	0.3	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = load capacitance in pF; V_{CC} = supply voltage in V;
N = number of inputs switching; $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.
[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

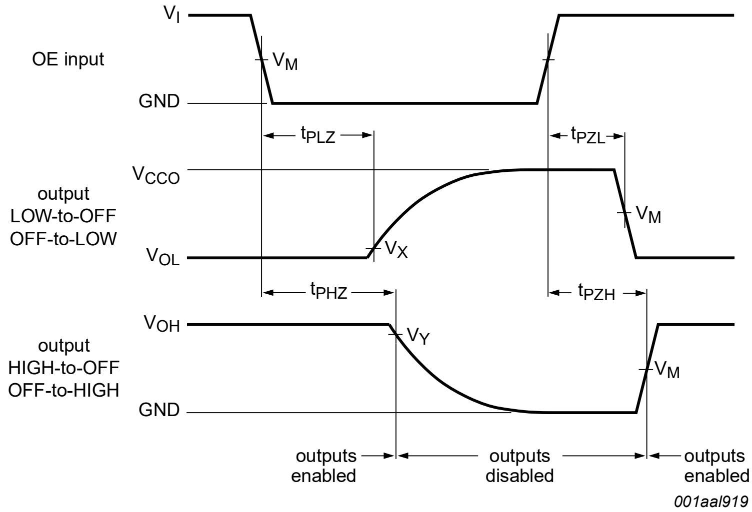
10.1. Waveforms and test circuit



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 2. The data input (An, Bn) to data output (Bn, An) propagation delay times



Measurement points are given in Table 13.

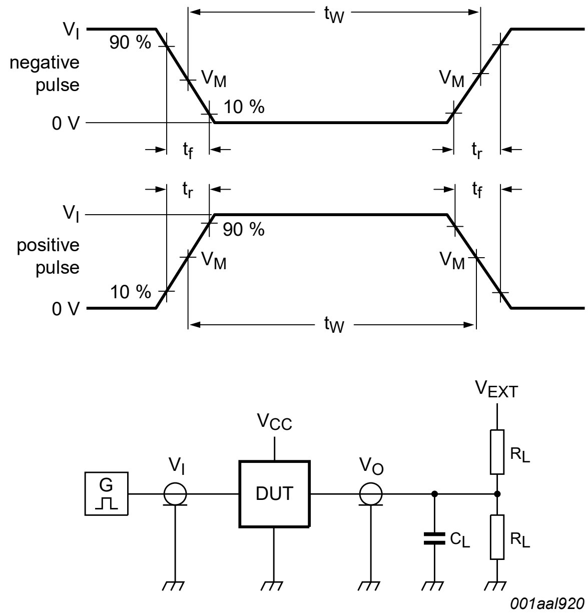
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. 3-state enable and disable times

Table 13. Measurement points [1]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.5 V ± 0.1 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 14.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

V_{EXT} = External voltage for measuring switching times.

Fig. 4. Test circuit for measuring switching times

Table 14. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCO} is the supply voltage associated with the output.

11. Application information

11.1. Applications

Voltage level-translation applications. The NXB0106-Q100 can be used to interface between devices or systems operating at different supply voltages. See Fig. 5 for a typical operating circuit using the NXB0106-Q100.

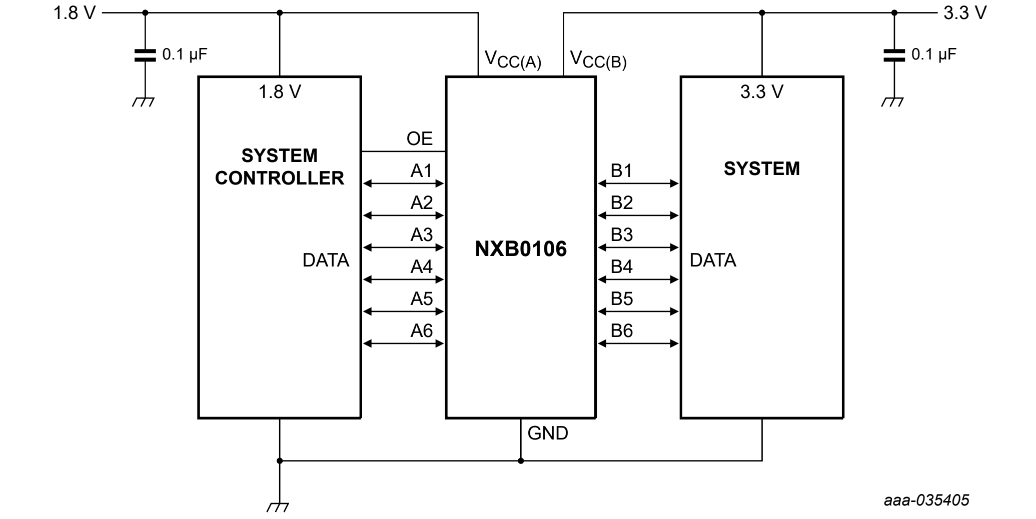


Fig. 5. Typical operating circuit

11.2. Architecture

The architecture of the NXB0106-Q100 is shown in Fig. 6. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the NXB0106-Q100 can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V and 40 Ω at V_{CCO} = 3.3 V to 5.0 V.

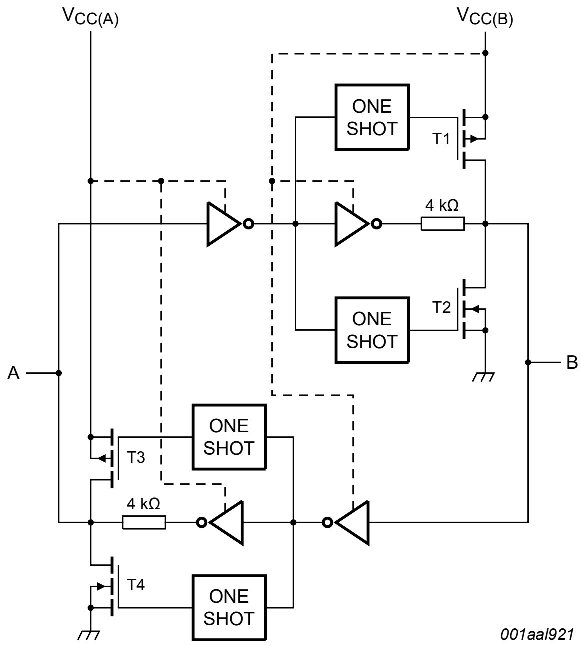
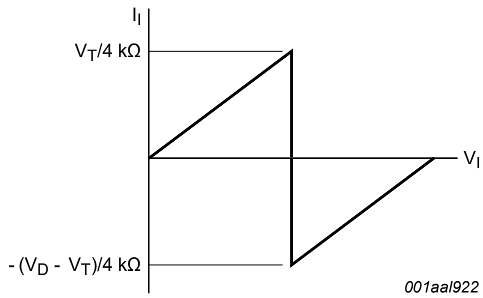


Fig. 6. Architecture of NXB0106-Q100 I/O cell (one channel)

11.3. Input driver requirements

For correct operation, the device driving the data I/Os of the NXB0106-Q100 must have a minimum drive capability of ±2 mA. See Fig. 7 for a plot of typical input current versus input voltage.



V_T: input threshold voltage of the NXB0106-Q100 (typically V_{CCI} / 2).
V_D: supply voltage of the external driver.

Fig. 7. Typical input current versus input voltage graph

11.4. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NXB0106-Q100 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

11.5. Enable and disable

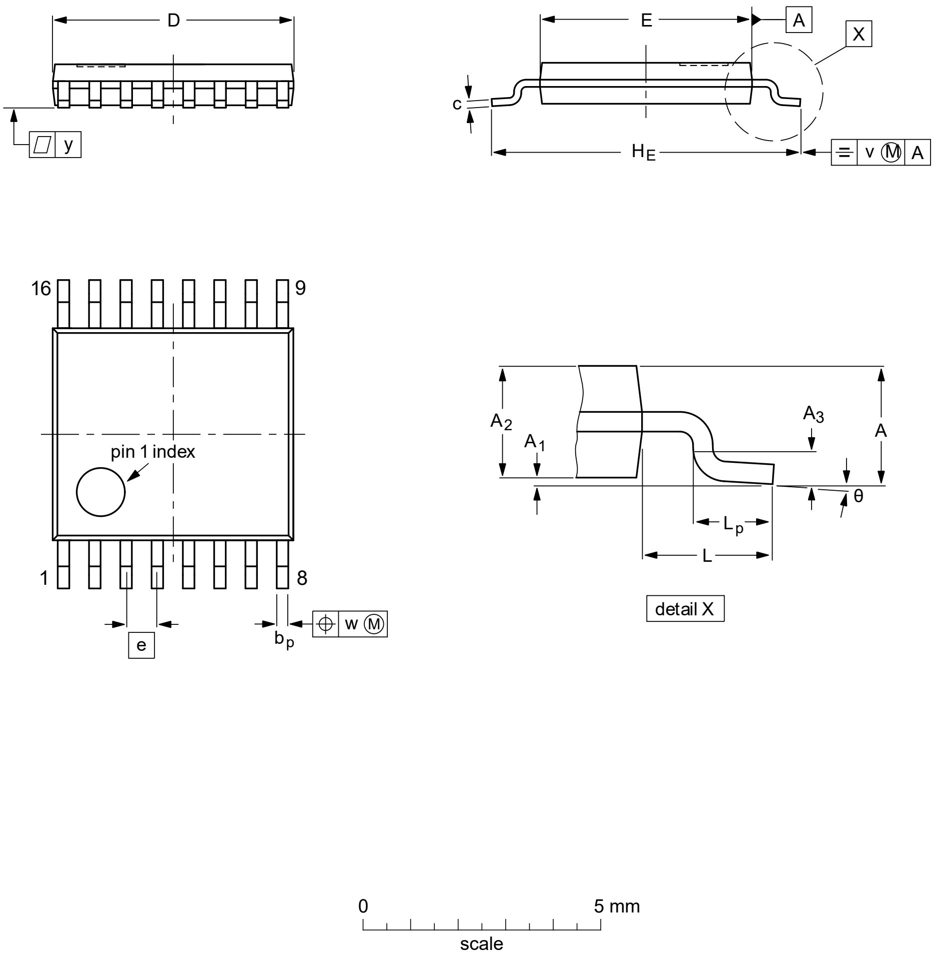
An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

11.6. Pull-up or pull-down resistors on I/O lines

As mentioned previously the NXB0106-Q100 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 kΩ. For this reason the NXB0106-Q100 is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the NXS0106-Q100 level translator is recommended.

12. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

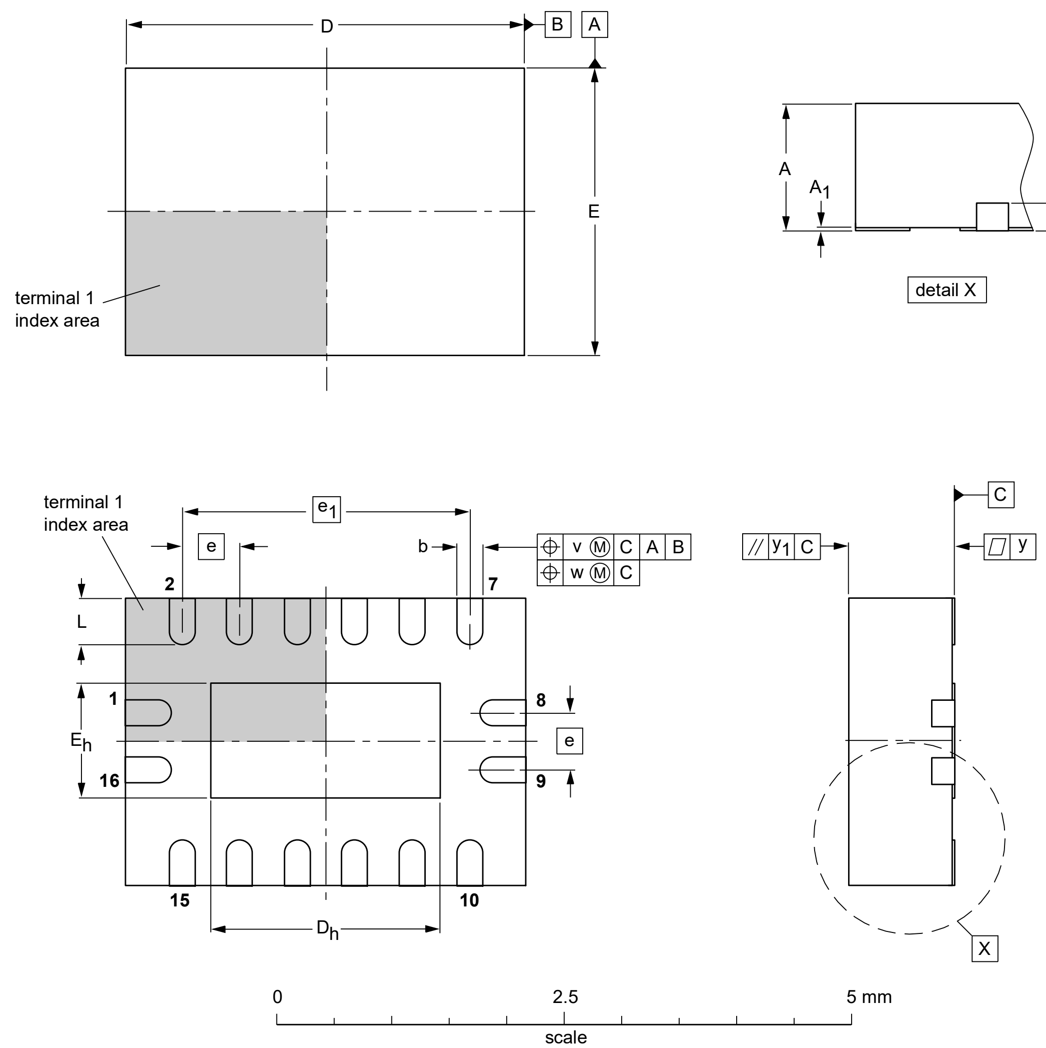
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 9. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 15. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	Electro Static Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXB0106_Q100 v.2.1	20240731	Product data sheet	-	NXB0106_Q100 v.2
NXB0106_Q100 v.2	20240404	Product data sheet	-	NXB0106_Q100 v.1
Modifications:	• Fig. 8: Aligned TSSOP package outline drawing to JEDEC MO-153.			
NXB0106_Q100 v.1	20230802	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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