| Title | *Reference Design Report for a 12 W Power Supply Using TinySwitch<sup>TM</sup>-4 TNY288PG* |
|---|---|
| **Specification** | 85 VAC – 265 VAC Input, 12 V, 1 A Output |
| **Application** | TinySwitch-4 Reference Design |
| **Author** | Applications Engineering Department |
| **Document Number** | RDR-839 |
| **Date** | July 29, 2020 |
| **Revision** | 1.2 |

## Summary and Features

- EcoSmart$^{TM}$ – meets all existing and proposed energy efficiency standards including ErP.
  - No-load consumption <30 mW; more than 300 mW available in stand-by with 500 mW input
  - > 84% average active-mode efficiency – DOE6 and EC CoC (v5)
- The board can fit P/G or the cost-effective D package
- BP/M capacitor value selects power MOSFET current limit for greater design flexibility
- Accurate detection output overvoltage protection (OVP) using primary bias winding sensed shutdown feature
- Accurately toleranced $I^2f$ parameter (-10%, +12%) reduces system cost
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitor costs
- Integrated TinySwitch-4 safety / reliability features
  - Accurate (±5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short-circuit and open loop fault conditions
  - P and G package with >3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >12 dBµV margin
- Meets IEC61000-4-5 Class 3 AC line surge

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

## Table of Contents

**Important Note:** Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

# 1    Introduction

This engineering report describes an isolated flyback converter designed to provide a nominal output voltage of 12 V at 1 A load from a wide input voltage range of 85 VAC to 265 VAC. This adapter utilizes the TNY288P from the TinySwitch-4 family of ICs, with provision for D and K packages placed on the top layer.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.



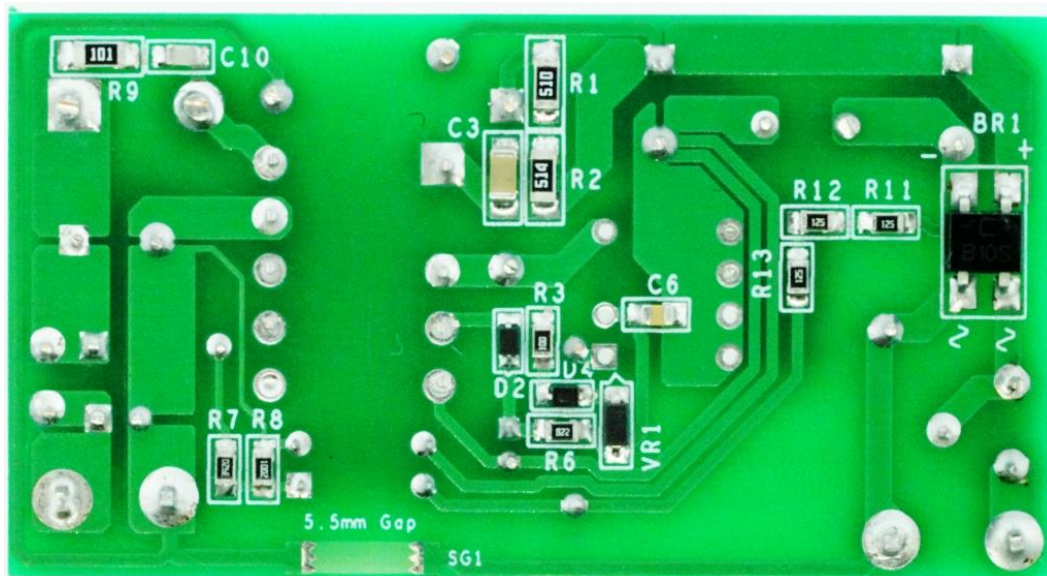**Figure 1 –** Populated Circuit Board, Top View.



**Figure 2 –** Populated Circuit Board, Bottom View.

## 2   **Power Supply Specification**

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

| Description | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Input** Voltage Frequency No-load Input Power (230 VAC) No-load Input Power (230 VAC) | $V_{IN}$ $f_{LINE}$ | 85 47 | 50/60 | 265 64 0.15 0.030 | VAC Hz W W | 2 Wire – no P.E. With Bias Winding Support.w/o UVLO Resistor or Bias Winding. |
| **Output** Output Voltage Output Ripple Voltage Output Current | $V_{OUT}$ $V_{RIPPLE}$ $I_{OUT}$ | 11 | 12 | 13 100 1 | V mV A | $\pm$ 8% 20 MHz Bandwidth. |
| **Total Output Power** Continuous Output Power Overvoltage Shutdown | $P_{OUT}$ $V_{OV}$ | 14 | | 12 16 | W V | With Bias Sense. |
| **Efficiency** Full Load Required average efficiency at 25, 50, 75 and 100 % of $P_{OUT}$ | $\eta$ $\eta_{DOE}$ | 84 83 | | | % % | Measured at $P_{OUT}$ 25 $^{\circ}$C Per DOE EISA2007 (Level VI) with TNY278 & Standard Current Limit |
| **Environmental** Conducted EMI | | Meets CISPR22B / EN55022B | | | | |
| Safety | | Designed to meet IEC950, UL1950 Class II | | | | |
| Surge (Differential) | | | | 1 | kV | 1.2/50 $\mu$s surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 $\Omega$ Common Mode: 12 $\Omega$ |
| Surge (Common mode) | | | | 2 | kV | |
| Ring Wave | | | | 3 | kV | |
| Electrical Fast Transient | | | | 4 | kV | |
| ESD | | | | ±15 ±8 | kV kV | Air Discharge. Contact Discharge. |
| Ambient Temperature | $T_{AMB}$ | 0 | | 50 | $^{\circ}$C | Free Convection, Sea Level. |

# 3　Schematic
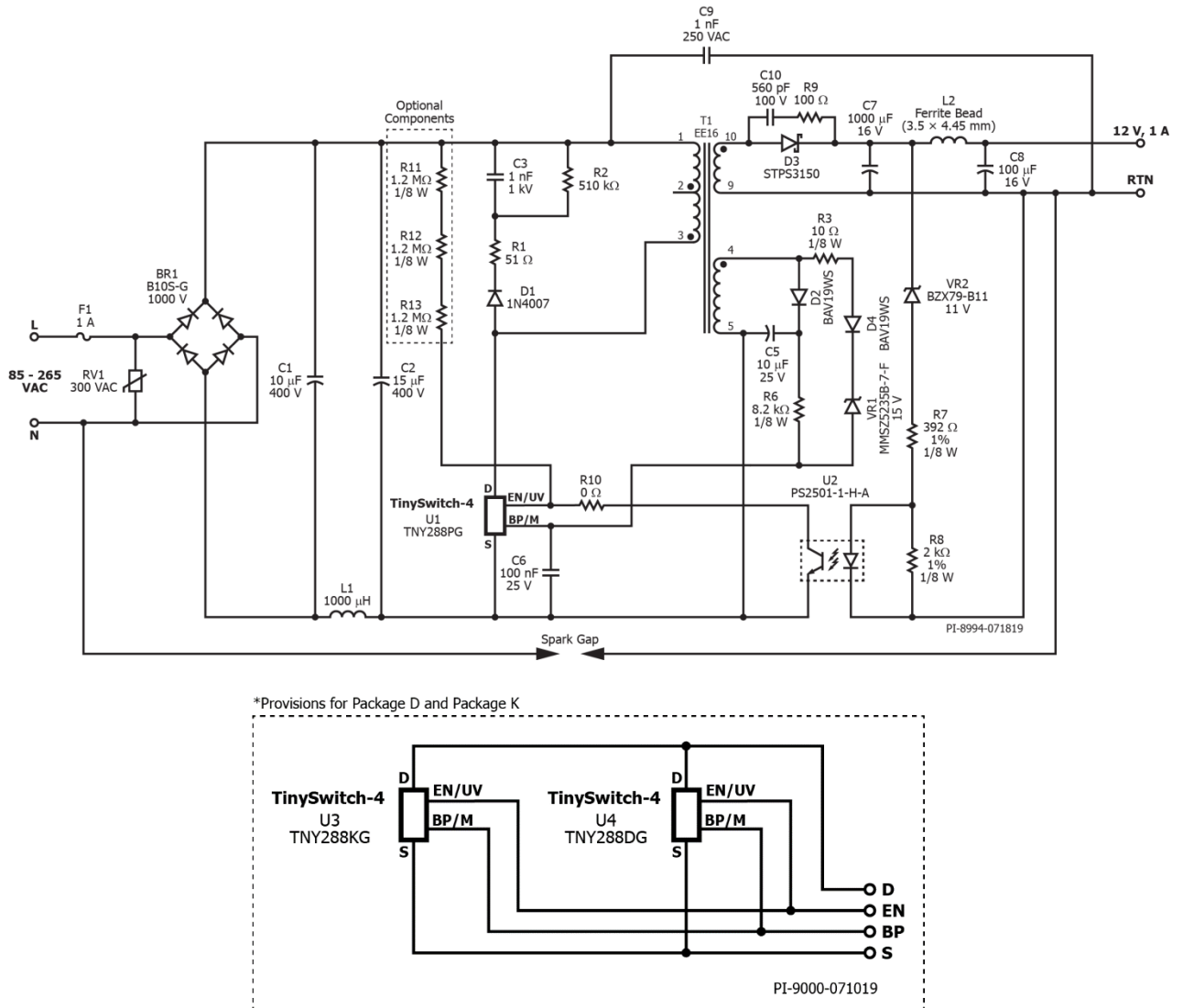


**Figure 3 –** Schematic.

# 4    Circuit Description

This circuit is configured as a flyback topology power supply utilizing the TNY288PG. Secondary-side constant voltage (CV) regulation is accomplished through optocoupler feedback with a Zener reference.

## 4.1    *Input Rectifier and Filter*

The AC input voltage is rectified by input bridge BR1. The rectified DC is then filtered by the bulk storage capacitors C1 and C2. Inductor L1, C1 and C2 form an input pi filter, which attenuates differential mode conducted EMI.

## 4.2    *TNY288PG Operation*

The TNY288PG device U1 integrates the power switching device, oscillator, control, startup, and protection functions.

The rectified and filtered input voltage is applied to the primary winding of T1. One side of the power transformer (T1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN (D) pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, delivering energy from bulk capacitor to transformer. When that current reaches the limit threshold, the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy is delivered to the output capacitor during off time.

When the power MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consists of D1, C3, R2 and R1. Resistor R2 and R1 not only damp the high frequency leakage ring that occurs when the power MOSFET turns off, but also limit the reverse current through D1 when the power MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of $\leq 2$ $\mu$s.) to be used for D1. The slow diode also improves conducted EMI and efficiency.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to its ENABLE/UNDERVOLTAGE (EN/UV) pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 $\mu$A, the next switching cycle begins, and is terminated when the current through the power MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN/UV pin threshold current is modulated between 115 $\mu$A and 60 $\mu$A based on the state during the previous cycle. An internal state machine sets the current limit to one of 4 levels appropriate for the operating conditions, ensuring that the switching frequency remains above the audible range until the transformer flux density is low enough to prevent audible noise. This practically eliminates audible noise when standard dip varnishing of the transformer is used.

### 4.3    *Output Rectification and Filtering*

Output rectification is provided by D3. Low ESR capacitor C7 achieves minimum output voltage ripple and noise in a small can size for the rated ripple current specification. A post filter (ferrite bead L2 and C8) attenuates noise and ripple further to meet the specification.

### 4.4    *Feedback and Output Voltage Regulation*

The supply's output voltage regulation set point is set by the voltage that develops across Zener diode VR2, R7 and the LED in optocoupler U2. The value of R8 was calculated to bias VR2 to about 0.5 mA when it goes into reverse avalanche conduction. This ensures that it is operating close to its rated knee current. Resistor R7 limits the maximum current during load transients. The values of R7 and R8 can both be varied slightly to fine-tune the output regulation set point. When the output voltage rises above the set point, the LED in U2 becomes forward biased. On the primary-side, the photo-transistor of U2 turns on and draws current out of the EN/UV pin of U1. Just before the start of each switching cycle, the controller checks the EN/UV pin current. If the current flowing out of the EN/UV pin is greater than 115 $\mu$A, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point.  For greater output voltage regulation accuracy, a reference IC such as a TL431 can be used in place of VR2.

### 4.5    *Output Overvoltage Shutdown*

PI's proprietary primary overvoltage detection eliminates the use additional opto-coupler and enables to low voltage rated output. It is accomplished by sensing the switching bias winding voltage during power MOSFET off time. When the power MOSFET is off, the reflected voltage on the bias winding is proportional to the output voltage by a factor determined by the bias and output turns ratio. When this voltage exceeds the sum of VR1, forward voltage of D4, and the BYPASS (BP) pin voltage, an overvoltage condition occurs and current begins to flow into the BYPASS pin. When this current exceeds 5 mA the internal shutdown circuit in U1 is activated. Reset is accomplished by removing input power and allowing the BYPASS pin voltage to drop below 2 V. Resistor R3 can be used to fine tune the overvoltage limit.

### 4.6    *Undervoltage Lockout*

Undervoltage (UV) lockout detection is accomplished by sensing the rectified dc voltage thru resistors R11, R12 and R13. When installed, power MOSFET switching is disabled at start-up until the current into the EN/UV pin exceeds 25 $\mu$A. This allows the designer to set the input voltage at which MOSFET switching will be enabled by choosing the sum of R11 – R13. For example, a value of 3.6 M$\Omega$ requires an input voltage of 65 VAC (92 VDC across C2) before the current into the EN/UV pin exceeds 25 $\mu$A. The UV detect function also prevents the output of the power supply from glitching (trying to restart) after output regulation is lost (during shutdown), by disabling power MOSFET switching until the input voltage rises above the undervoltage lockout threshold.

## 4.7   *EMI Design Aspects*

In addition to the simple input $\pi$ filter (C1, L1 and C2) for differential mode EMI, this design makes use of shielding techniques in the transformer to reduce common mode EMI displacement currents. Resistor R2 and capacitor C3 are added to act as damping network to reduce high frequency transformer ringing. These techniques combined with the frequency jitter of TNY288PG gives excellent conducted and radiated EMI performance.

## 4.8   *ESD Design Aspects*

Component placement and board layout play a crucial role in order to pass ESD compliance requirements. The following design considerations were applied in this reference board:

- Place C6 as close as possible and directly to BP and SOURCE pins.

- Separate the ground trace of U2 from the ground trace of C5. The two ground traces can be merged at the bulk capacitor C2 ground pin. This minimizes coupling of ESD.

- Route Y capacitor C9 traces directly to bulk capacitor C2 positive pin, and the other end to directly to RTN terminal

- Route the spark gap between RTN terminal and Neutral terminal

## 5    PCB Layout
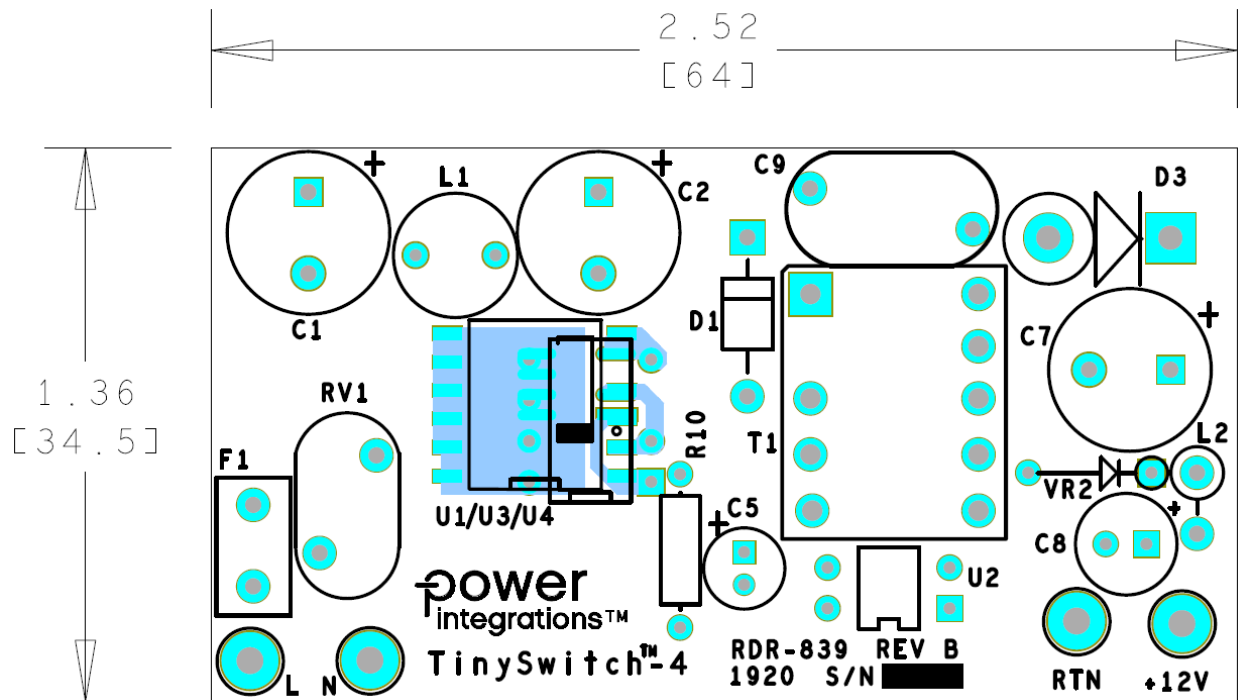


**Figure 4 –** Populated Circuit Board, Top View.
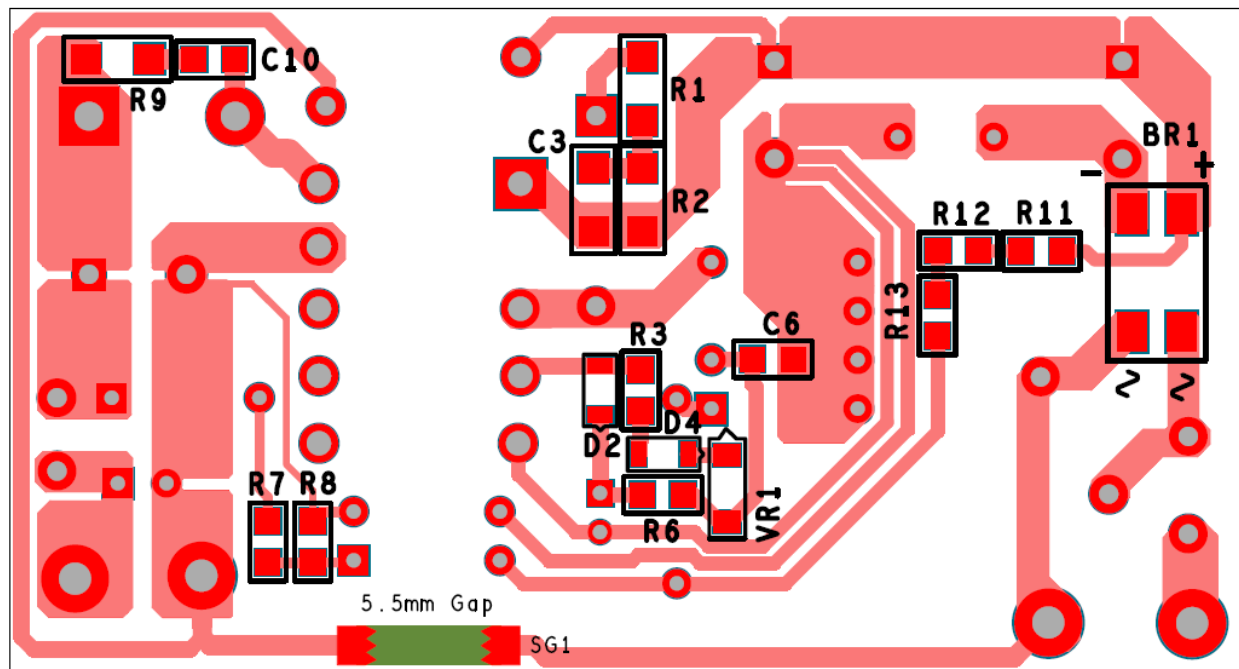


**Figure 5 –** Populated Circuit Board, Bottom View.

## 6    Bill of Materials

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|------|-----|---------|-------------|-----------------|-----|
| 1 | 1 | BR1 | 1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC | B10S-G | Comchip |
| 2 | 1 | C1 | 10 $\mu$F,±20%, 400 V, Electrolytic, (10 x 14.5) | UVC2G100MPD | Nichicon |
| 3 | 1 | C2 | 15 $\mu$F, 400 V, Electrolytic, (10 x 16) | UVC2G150MPD | Nichicon |
| 4 | 1 | C3 | 1 nF, 1000 V, Ceramic, X7R, 1206 | CC1206KKX7RCBB102 | Yageo |
| 5 | 1 | C5 | 10 $\mu$F, 25 V, Electrolytic, Gen. Purpose, (5 x 12) | ECA-1EM100 | Panasonic |
| 6 | 1 | C6 | 100 nF, 25 V, Ceramic, X7R, 0805 | 08053C104KAT2A | AVX |
| 7 | 1 | C7 | 1000 $\mu$F, 16 V, Electrolytic, Very Low ESR, 23 m$\Omega$, (10 x 20) | EKZE160ELL102MJ20S | Nippon Chemi-Con |
| 8 | 1 | C8 | 100 $\mu$F, 16 V, Electrolytic, Low ESR, 250 m$\Omega$, (6.3 x 11.5) | ELXZ160ELL101MFB5D | Nippon Chemi-Con |
| 9 | 1 | C9 | 1 nF, Ceramic, Y1 | 440LD10-R | Vishay |
| 10 | 1 | C10 | 560 pF, ±5%, 100 V, Gederal Purpose, Ceramic Capacitor, C0G, NP0, 0805 | CC0805JRNPO0BN561 | Yageo |
| 11 | 1 | D1 | 1000 V, 1 A, Rectifier, DO-41 | 1N4007-E3/54 | Vishay |
| 12 | 2 | D2 D4 | 100 V, 0.2 A, Fast Switching, 50 ns, SOD-323 | BAV19WS-7-F | Diodes, Inc. |
| 13 | 1 | D3 | 150 V, 3 A, Schottky, DO-201AD | STPS3150RL | ST |
| 14 | 1 | F1 | 1 A, 250 V, Slow, Long Time Lag, RST 1 | RST 1 | Belfuse |
| 15 | 1 | L1 | 1000 $\mu$H, 0.3 A | RLB0914-102KL | Bourns |
| 16 | 1 | L2 | 3.5 mm x 4.45 mm, 56 $\Omega$ at 100 MHz, #22 AWG hole, Ferrite Bead | 2761001112 | Fair-Rite |
| 17 | 1 | R1 | RES, 51 $\Omega$, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ510V | Panasonic |
| 18 | 1 | R2 | RES, 510 k$\Omega$, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ514V | Panasonic |
| 19 | 1 | R3 | RES, 10 $\Omega$, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ100V | Panasonic |
| 20 | 1 | R6 | RES, 8.2 k$\Omega$, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ822V | Panasonic |
| 21 | 1 | R7 | RES, 392 $\Omega$, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF3920V | Panasonic |
| 22 | 1 | R8 | RES, 2.00 k$\Omega$, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF2001V | Panasonic |
| 23 | 1 | R9 | RES, 100 $\Omega$, 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ101V | Panasonic |
| 24 | 1 | R10 | RES, 0 $\Omega$, 5%, 1/4 W, Carbon Film | ZOR-25-B-52-0R | Yageo |
| 25 | 3 | R11 R12 R13 | RES, 1.2 M$\Omega$, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ125V | Panasonic |
| 26 | 1 | RV1 | 300 VAC, 25 J, 7 mm, RADIAL | V300LA4P | Littlefuse |
| 27 | 1 | T1 | Bobbin, EE16 Vertical, 10 pins Transformer | YW-527-00B PNY-83912 | Yih-Hwa Premier Magnetics |
| 28 | 1 | U1 | TinySwitch-4, TNY288PG, DIP-8C | TNY288PG | Power Integrations |
| 29 | 1 | U2 | Optocoupler, 80 V, CTR 80-160%, 4-DIP | PS2501-1-H-A | CEL |
| 30 | 1 | VR1 | DIODE ZENER 6.8 V 500 mW SOD123 | MMSZ5235B-7-F | Diodes, Inc. |
| 31 | 1 | VR2 | 11 V, 500 mW, 2%, DO-35 | BZX79-B11,133 | NXP Semi |
| 32 | 1 | +12V | Test Point, RED, THRU-HOLE MOUNT | 5010 | Keystone |
| 33 | 2 | N RTN | Test Point, BLK, THRU-HOLE MOUNT | 5011 | Keystone |
| 34 | 1 | L | Test Point, WHT, THRU-HOLE MOUNT | 5012 | Keystone |

## 7    Transformer Specification

### 7.1    Electrical Diagram
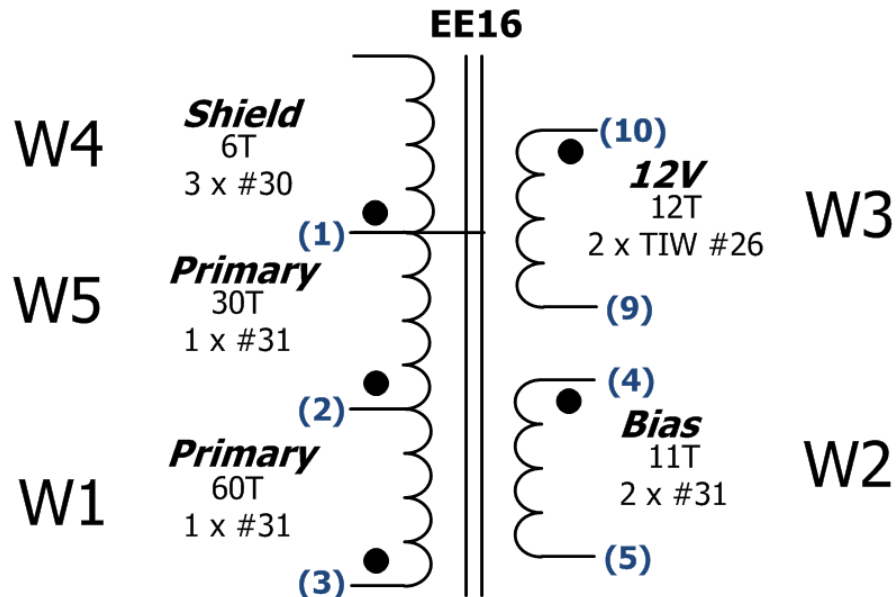


**Figure 6 –** Transformer Electrical Diagram.

### 7.2    Electrical Specifications

| Parameter | Condition | Spec. |
|---|---|---|
| Nominal Primary Inductance | Measured at 1 $V_{PK\text{-}PK}$, 100 kHz switching frequency, between pin 1 and pin 3 with all other windings open. | 860 $\mu$H |
| Tolerance | Tolerance of Primary Inductance. | ±10% |
| Leakage Inductance | Measured across primary winding with all other windings shorted. | <20 $\mu$H |

### 7.3    Material List

| Item | Description |
|---|---|
| **[1]** | Core: EE16 PC44. |
| **[2]** | Bobbin: EE16, Vertical, 10 Pins. PI#: 25-00970-00. |
| **[3]** | Magnet Wire: #31 AWG. |
| **[4]** | Magnet Wire: #30 AWG. |
| **[5]** | Tripe Insulated Wire: #26. |
| **[6]** | Polyester Tape: 9 mm. |
| **[7]** | Polyester Tape: 5 mm. |
| **[8]** | Varnish: Dolph BC 359 or equivalent. |

### 7.4    *Transformer Build Diagram*
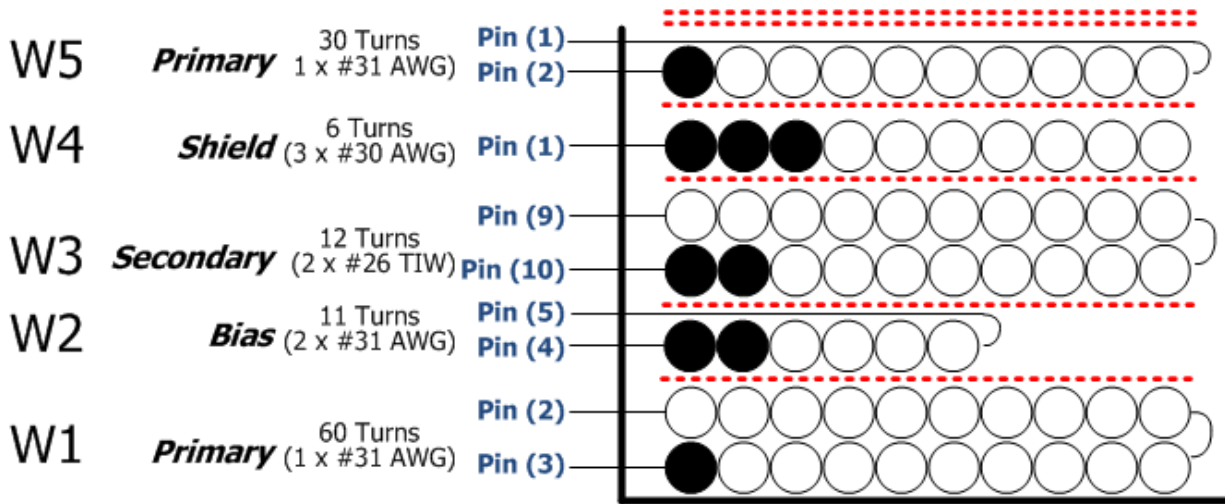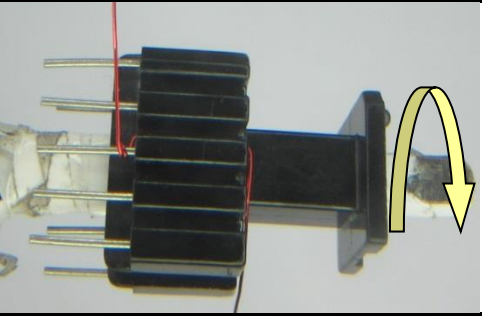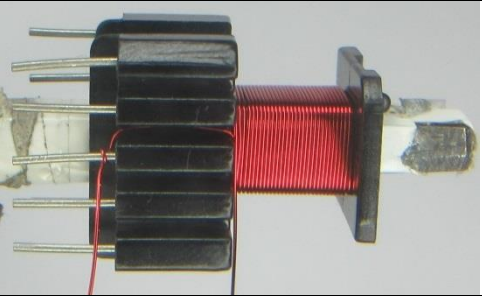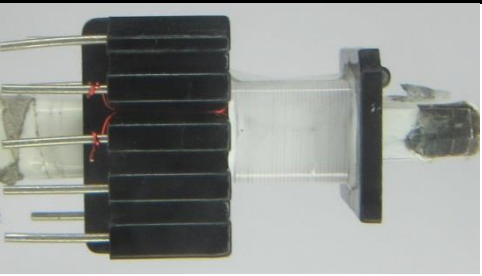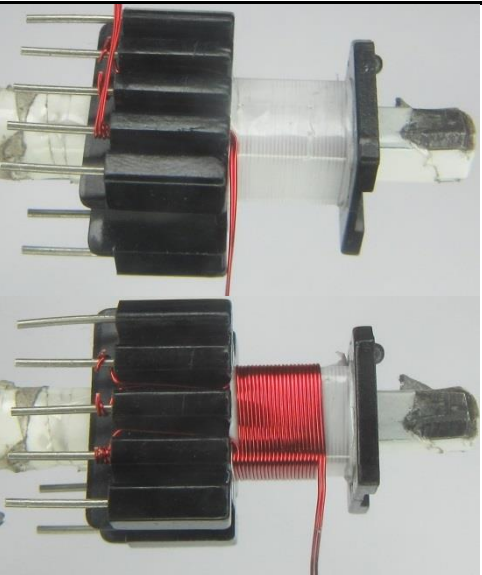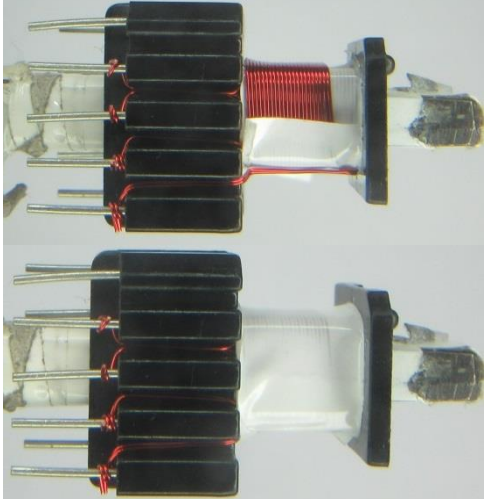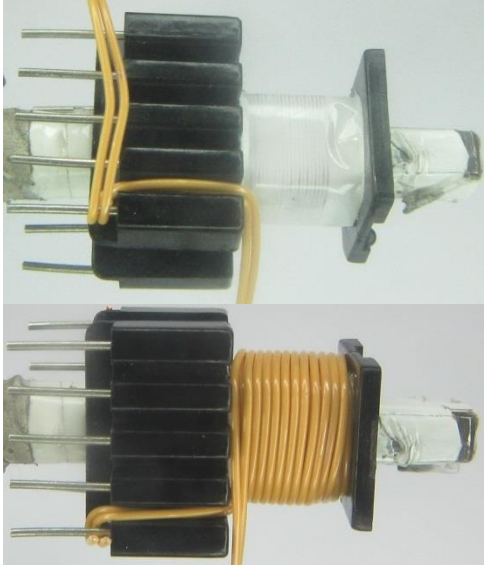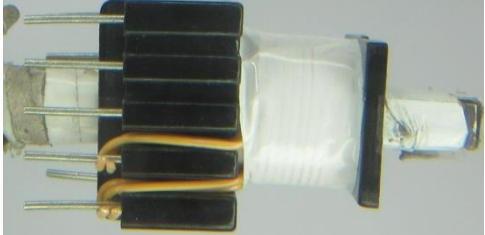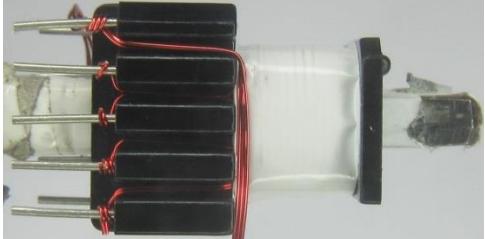


**Figure 7 –** Transformer Build Diagram.
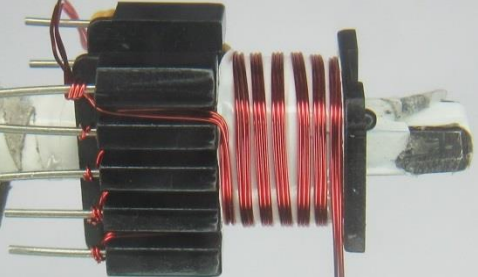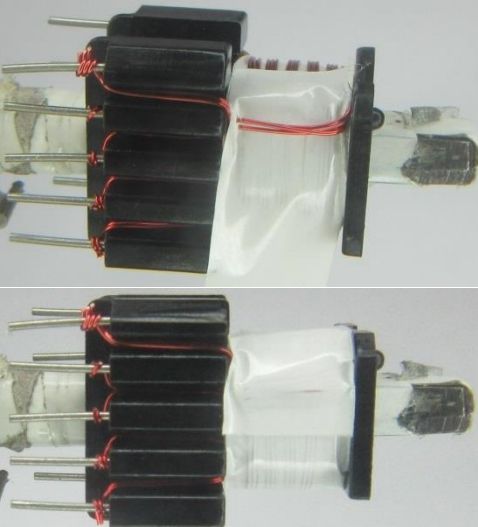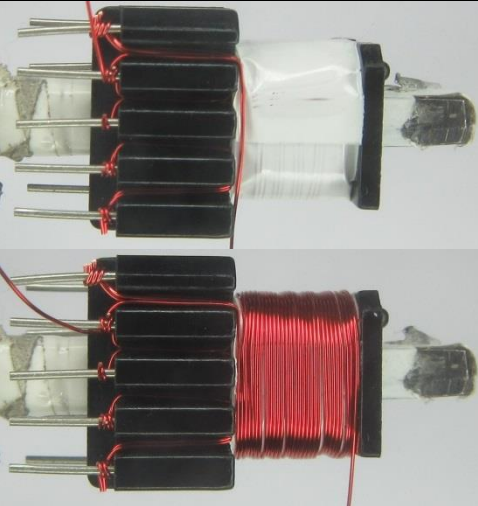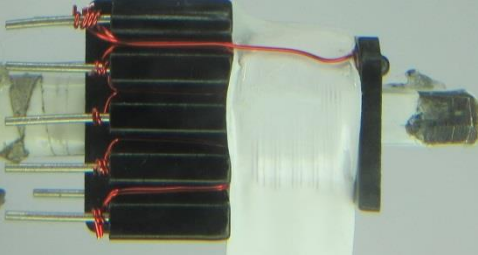
### 7.5    *Transformer Instructions*

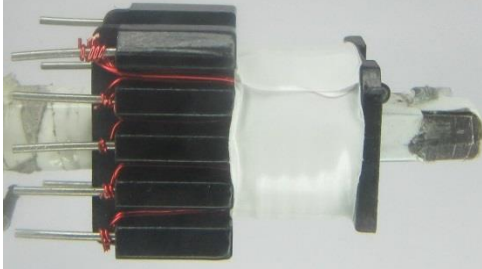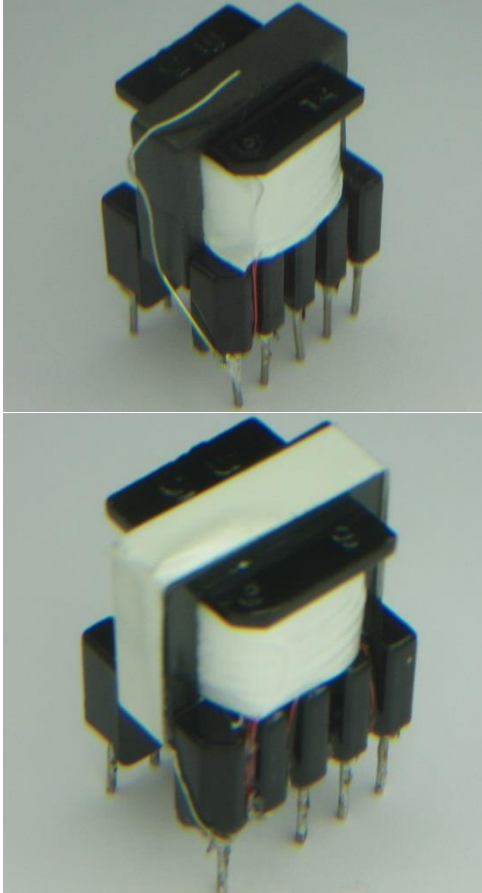| Winding Preparation | Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise as shown. |
|---|---|
| W1 1st Primary | Start at pin 3. Wind 60 turns of wire Item [3] in two layers. After the last turn, bring the wire back across the windings into pin 2. |
| Insulation | Place one layer of tape Item [6] for insulation. |
| W2 Bias | Start at pin 4. Wind 11 turns of two strands of wire Item [3] in one layer. Wind all turns on tightly on one side. Bring the back into pin 5. |
| Insulation | Place one layer of tape Item [6] for insulaton. |
| W3 Secondary | Start at pin 10. Wind 12 turns of two strands of wire Item [5] in two layers. Finish at pin 9. |
| Insulation | Place one layer of tape Item [6] for insulation. |
| W4 Shield | Start at pin 1. Wind 6 turns of three strands of wire Item [4] in one layer. Spread the turns evenly across the bobbin. The end of the last turn is no-connect (NC). |
| Insulation | Place one layer of tape Item [6] for insulation |
| W5 2nd Primary | Start at pin 2. Wind 30 turns of wire Item [3] in one layer. After the last turn, bring the wire back across the windings into pin 1. |
| Insulation | Place one layer of tape Item [6] for insulation |
| Assembly | Grind core halves for specified primary inductance. Place a floating wire along the core, and solder one end to pin 1. Wrap core halves and floating wire with tape Item [7]. Remove pin 2. Varnish with Item [8]. |

## 7.6    *Transformer Winding Illustrations*

| | | |
|---|---|---|
| **Winding Preparation** | | Place the bobbin Item [2] with the pins facing the winder. Winding direction is counter-clockwise as shown. |
| **W1 1st Primary** | | Start at pin 3. Wind 60 turns of wire Item [3] in two layers. End at pin 2. |
| **Insulation** | | Place one layer of tape Item [6] for insulation. |
| **W2 Bias** | | Start at pin 4. Wind 11 turns of two strands of wire Item [3] in one layer. Wind all turns on tightly on one side. Bring the back into pin 5. |

| | | |
|---|---|---|
| **Insulation** |  | Place one layer of tape Item [6] for insulation. |
| **W3 Secondary** |  | Start at pin 10. Wind 12 turns of two strands of wire Item [5] in two layers. Finish at pin 9. |
| **Insulation** |  | Place one layer of tape Item [6] for insulation. |
| **W4 Shield** |  | Start at pin 1. Wind 6 turns of three strands of wire Item [4] in one layer. Spread the turns evenly across the bobbin. The end of the last turn is no connect (NC). |

| | | |
|---|---|---|
| | | |
| **Insulation** | | Place one layer of tape Item [6] for insulation |
| **W5 2<sup>nd</sup> Primary** | | Start at pin 2. Wind 30 turns of wire Item [3] in one layer. After the last turn, bring the wire back across the windings into pin 1. |
| **Insulation** | | Place two layers of tape Item [6] for insulation |

| | | | |
|---|---|---|---|
| |  | | |
| **Assembly** |  | Grind core halves for specified primary inductance.<br><br>Place a floating wire along the core, and solder one end to pin 1.<br><br>Wrap core halves and floating wire with tape Item [7].<br><br>Remove pin 2. Varnish with Item [8]. | |

## 9    Transformer Design Spreadsheet

| ACDC_TinySwitch-4_110618; Rev.1.2; Copyright Power Integrations 2018 | INPUT | INFO | OUTPUT | UNIT | ACDC_TinySwitch-4_110618_Rev1-2.xls; TinySwitch-4 Continuous/Discontinuous Flyback Transformer Design Spreadsheet |
|---|---|---|---|---|---|
| **ENTER APPLICATION VARIABLES** | | | | | |
| VACMIN | 85 | | 85 | Volts | Minimum AC Input Voltage |
| VACMAX | 265 | | 265 | Volts | Maximum AC Input Voltage |
| fL | 50 | | 50 | Hertz | AC Mains Frequency |
| VO | 12.00 | | 12.00 | Volts | Output Voltage (at continuous power) |
| IO | 1.00 | | 1.00 | Amps | Power Supply Output Current (corresponding to peak power) |
| Power | | | 12.00 | Watts | Continuous Output Power |
| n | 0.84 | | 0.84 | | Efficiency Estimate at output terminals. Under 0.7 if no better data available |
| Z | 0.50 | | 0.50 | | Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available |
| tC | | | 3.00 | mSeconds | Bridge Rectifier Conduction Time Estimate |
| CIN | 25.00 | | 25.00 | uFarads | Input Capacitance |
| **ENTER TinySwitch-4 VARIABLES** | | | | | |
| TinySwitch-4 | TNY288D | | TNY288D | | User-defined TinySwitch-4 |
| Chose Configuration | STD | | Standard Current Limit | | Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications) |
| ILIMITMIN | | | 0.512 | Amps | Minimum Current Limit |
| ILIMITTYP | | | 0.55 | Amps | Typical Current Limit |
| ILIMITMAX | | | 0.588 | Amps | Maximum Current Limit |
| fSmin | | | 124000 | Hertz | Minimum Device Switching Frequency |
| I^2fmin | | | 35.937 | A^2kHz | I^2f (product of current limit squared and frequency is trimmed for tighter tolerance) |
| VOR | 95.6 | | 95.6 | Volts | Reflected Output Voltage (VOR < 135 V Recommended) |
| VDS | | | 10.0 | Volts | TinySwitch-4 on-state Drain to Source Voltage |
| VD | | | 0.70 | Volts | Output Winding Diode Forward Voltage Drop |
| KP | | | 0.75 | | Ripple to Peak Current Ratio (KP < 6) |
| KP_TRANSIENT | | | 0.44 | | Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25 |
| **ENTER BIAS WINDING VARIABLES** | | | | | |
| VB | 11.65 | | 11.65 | Volts | Bias Winding Voltage |
| VDB | | | 0.70 | Volts | Bias Winding Diode Forward Voltage Drop |
| NB | | | 11 | | Bias Winding Number of Turns |
| VZOV | | | 17.65 | Volts | Over Voltage Protection zener diode voltage. |
| **UVLO VARIABLES** | | | | | |
| V_UV_TARGET | | | 88.34 | Volts | Target DC under-voltage threshold, above which the power supply with start |
| V_UV_ACTUAL | | | 84.70 | Volts | Typical DC start-up voltage based on standard value of RUV_ACTUAL |
| RUV_IDEAL | | | 3.45 | Mohms | Calculated value for UV Lockout resistor |
| RUV_ACTUAL | | | 3.30 | Mohms | Closest standard value of resistor to RUV_IDEAL |
| **ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES** | | | | | |
| Core Type | EE16 | | EE16 | | Enter Transformer Core |
| Core | | EE16 | | P/N: | PC40EE16-Z |
| Custom core | | | | P/N: | EE16_BOBBIN |
| AE | | | 0.19 | cm^2 | Core Effective Cross Sectional Area |
| LE | | | 3.50 | cm | Core Effective Path Length |
| AL | | | 1140 | nH/T^2 | Ungapped Core Effective Inductance |
| BW | | | 8.6 | mm | Bobbin Physical Winding Width |
| M | | | 0.00 | mm | Safety Margin Width (Half the Primary to |

| | | | | Secondary Creepage Distance) |
|---|---|---|---|---|
| L | 3 | 3 | | Number of Primary Layers |
| NS | 12 | 12 | | Number of Secondary Turns |
| **DC INPUT VOLTAGE PARAMETERS** | | | | |
| VMIN | | 80.3 | Volts | Minimum DC Input Voltage |
| VMAX | | 374.8 | Volts | Maximum DC Input Voltage |
| **CURRENT WAVEFORM SHAPE PARAMETERS** | | | | |
| DMAX | | 0.58 | | Duty Ratio at full load, minimum primary inductance and minimum input voltage |
| IAVG | | 0.20 | Amps | Average Primary Current |
| IP | | 0.51 | Amps | Minimum Peak Primary Current |
| IR | | 0.39 | Amps | Primary Ripple Current |
| IRMS | | 0.29 | Amps | Primary RMS Current |
| **TRANSFORMER PRIMARY DESIGN  PARAMETERS** | | | | |
| LP | | 861 | uHenries | Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 774 uH |
| LP_TOLERANCE | 10 | 10 | % | Primary inductance tolerance |
| NP | | 90 | | Primary Winding Number of Turns |
| ALG | | 105 | nH/T^2 | Gapped Core Effective Inductance |
| BM | | 2918 | Gauss | Maximum Operating Flux Density, BM<3100 is recommended |
| BAC | | 1099 | Gauss | AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) |
| ur | | 1654 | | Relative Permeability of Ungapped Core |
| LG | | 0.21 | mm | Gap Length (Lg > 0.1 mm) |
| BWE | | 25.8 | mm | Effective Bobbin Width |
| OD | | 0.286 | mm | Maximum Primary Wire Diameter including insulation |
| INS | | 0.05 | mm | Estimated Total Insulation Thickness (= 2 * film thickness) |
| DIA | | 0.23 | mm | Bare conductor diameter |
| AWG | | 31 | AWG | Primary Wire Gauge (Rounded to next smaller standard AWG value) |
| CM | | 81 | Cmils | Bare conductor effective area in circular mils |
| CMA | | 274 | Cmils/Amp | Primary Winding Current Capacity (200 < CMA < 500) |
| **TRANSFORMER SECONDARY DESIGN PARAMETERS** | | | | |
| Lumped parameters | | | | |
| ISP | | 3.85 | Amps | Peak Secondary Current |
| ISRMS | | 1.90 | Amps | Secondary RMS Current |
| IRIPPLE | | 1.62 | Amps | Output Capacitor RMS Ripple Current |
| CMS | | 381 | Cmils | Secondary Bare Conductor minimum circular mils |
| AWGS | | 24 | AWG | Secondary Wire Gauge (Rounded up to next larger standard AWG value) |
| **VOLTAGE STRESS PARAMETERS** | | | | |
| VDRAIN | | 596 | Volts | Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance) |
| PIVS | | 62 | Volts | Output Rectifier Maximum Peak Inverse Voltage |
| **TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)** | | | | |
| **1st output** | | | | |
| VO1 | 12.00 | 12.00 | Volts | Main Output Voltage (if unused, defaults to single output design) |
| IO1 | 1.00 | 1.00 | Amps | Output DC Current |
| PO1 | | 12 | Watts | Output Power |
| VD1 | | 0.70 | Volts | Output Diode Forward Voltage Drop |
| NS1 | | 12.00 | | Output Winding Number of Turns |
| ISRMS1 | | 1.903 | Amps | Output Winding RMS Current |
| IRIPPLE1 | | 1.62 | Amps | Output Capacitor RMS Ripple Current |
| PIVS1 | | 62 | Volts | Output Rectifier Maximum Peak Inverse Voltage |
| Recommended Diodes | | 1N5820, SB320 | | Recommended Diodes for this output |

| | | | | | |
|---|---|---|---|---|---|
| CMS1 | | | 381 | Cmils | Output Winding Bare Conductor minimum circular mils |
| AWGS1 | | | 24 | AWG | Wire Gauge (Rounded up to next larger standard AWG value) |
| DIAS1 | | | 0.51 | mm | Minimum Bare Conductor Diameter |
| ODS1 | | | 0.72 | mm | Maximum Outside Diameter for Triple Insulated Wire |

## 10    **Performance Data**

### 10.1  *Efficiency*

10.1.1 Active Mode Measurement Data

| Measured Performance | | | Standards | | |
|:---:|:---:|:---:|:---:|:---:|:---:|
| | | $V_{IN}$ **(VAC)** | **DOE6** | **EC CoC (v5)** | |
| | | 115 \| 230 | | 2014 Tier 1 | 2016 Tier 2 |
| | | Efficiency (%) | | | |
| **Load (%)** | **10** | 77.88 \| 75.27 | | 70 | 73 |
| | **25** | 83.68 \| 82.67 | | | |
| | **50** | 84.87 \| 84.46 | | | |
| | **75** | 85.14 \| 84.77 | | | |
| | **100** | 84.61 \| 85.02 | | | |
| | **Ave** | **84.57** \| **84.23** | 83 | 80 | 83 |
| **No-Load Input Power (mW)** | | **36 (27)** \| **60 (28)** | 100 | 150 | 75 |
| | **Compliant** | | Y | Y | Y |

[†] Numbers in parenthesis represent no-load input power without UV sensing.

## 10.1.2    Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.
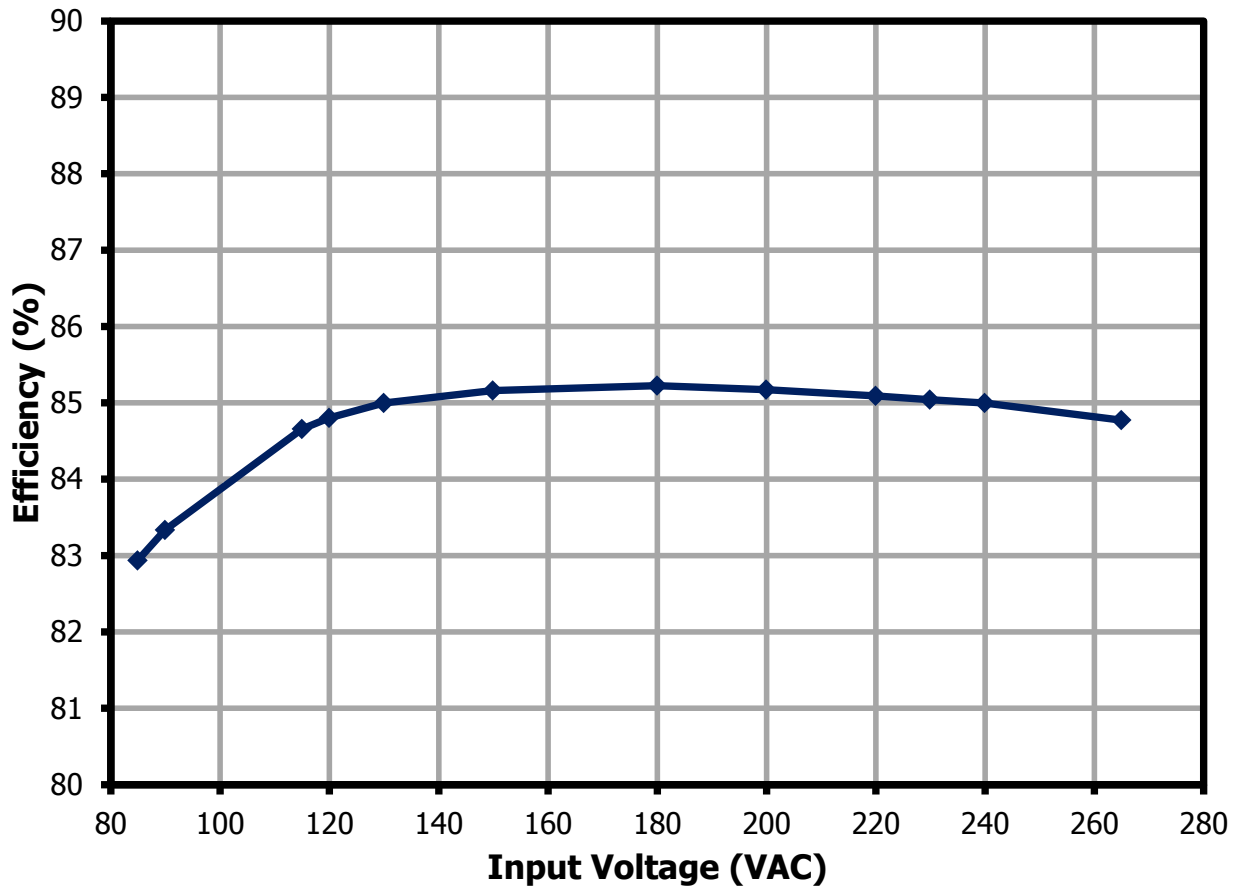
**Figure 8 –** Full Load Efficiency vs. Line.

### 10.1.3 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.
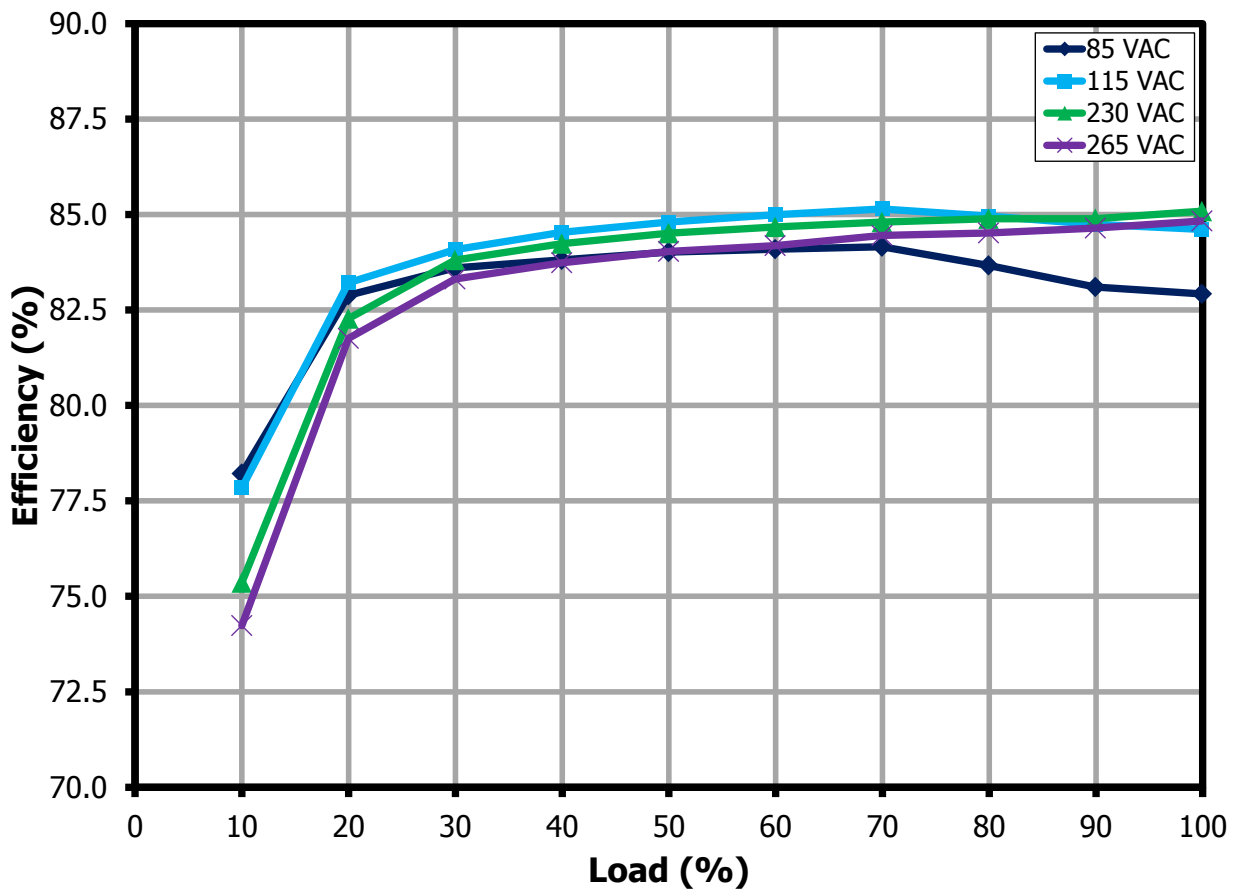


**Figure 9 –** Efficiency vs. Percentage Load.

## 10.2 *Available Standby Output Power*
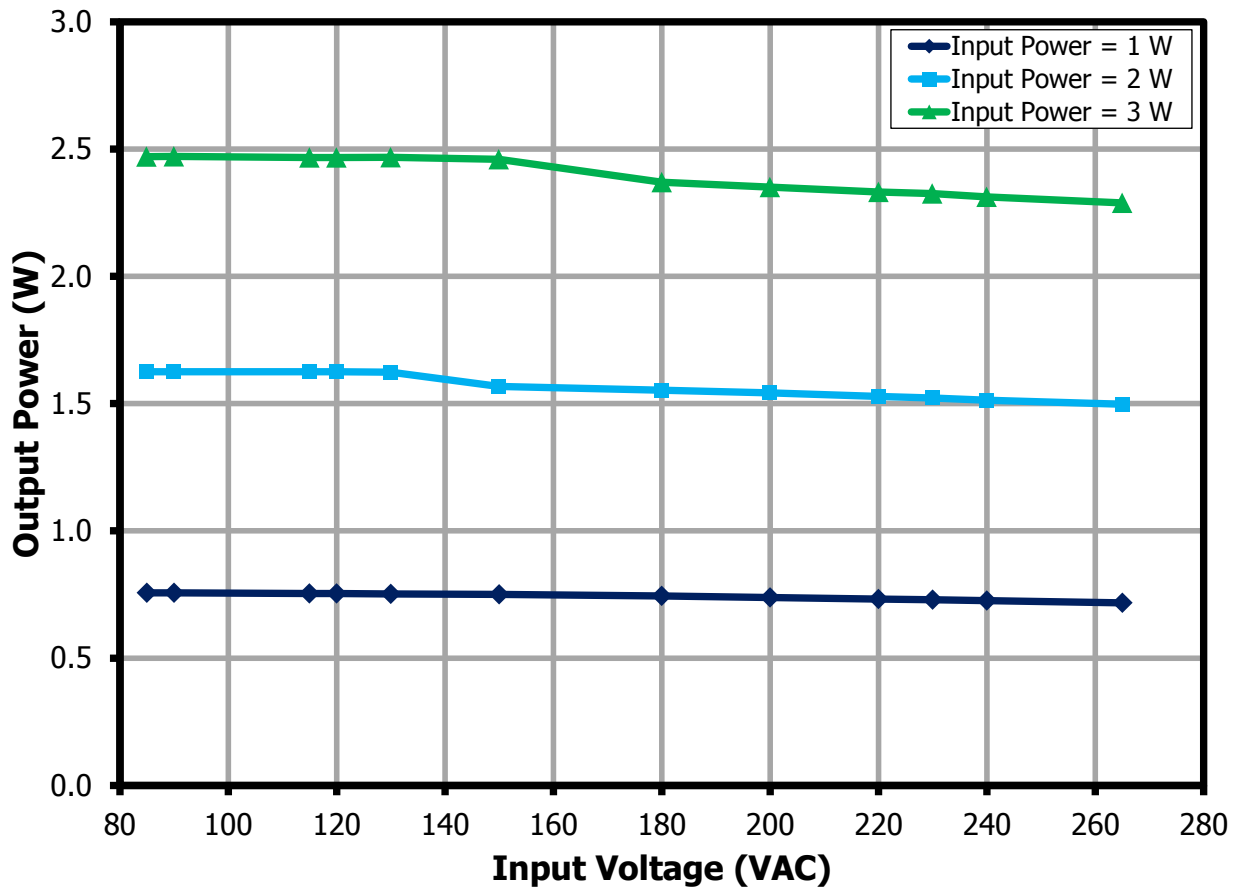


**Figure 10 –** Available Standby Output Power for 1 W, 2 W and 3 W Input Power.
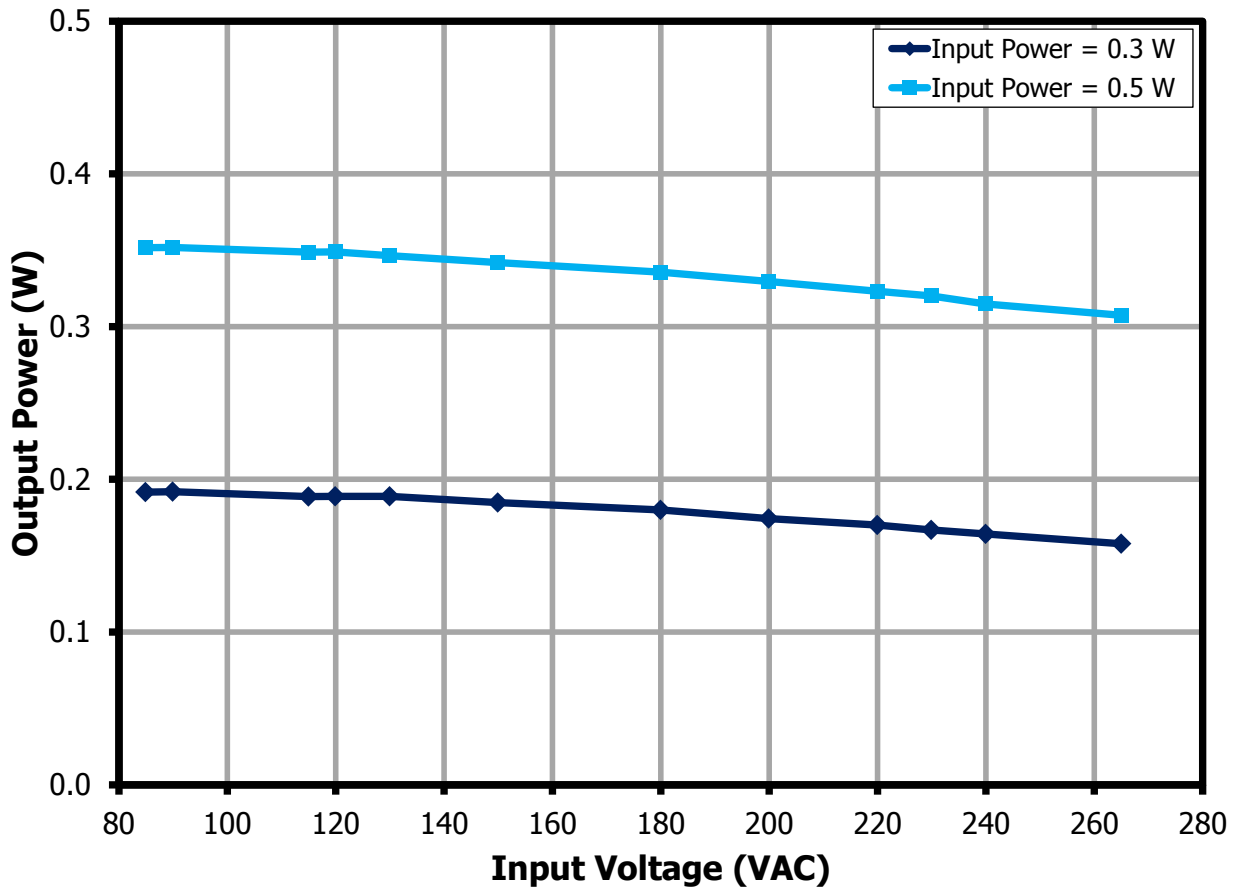
**Figure 11 –** Available Standby Output Power for 0.3 W and 0.5 W Input Power.

## 10.3  *No-Load Input Power*

Test Condition: Soak for 15 minutes each line and 1 minute integration time.
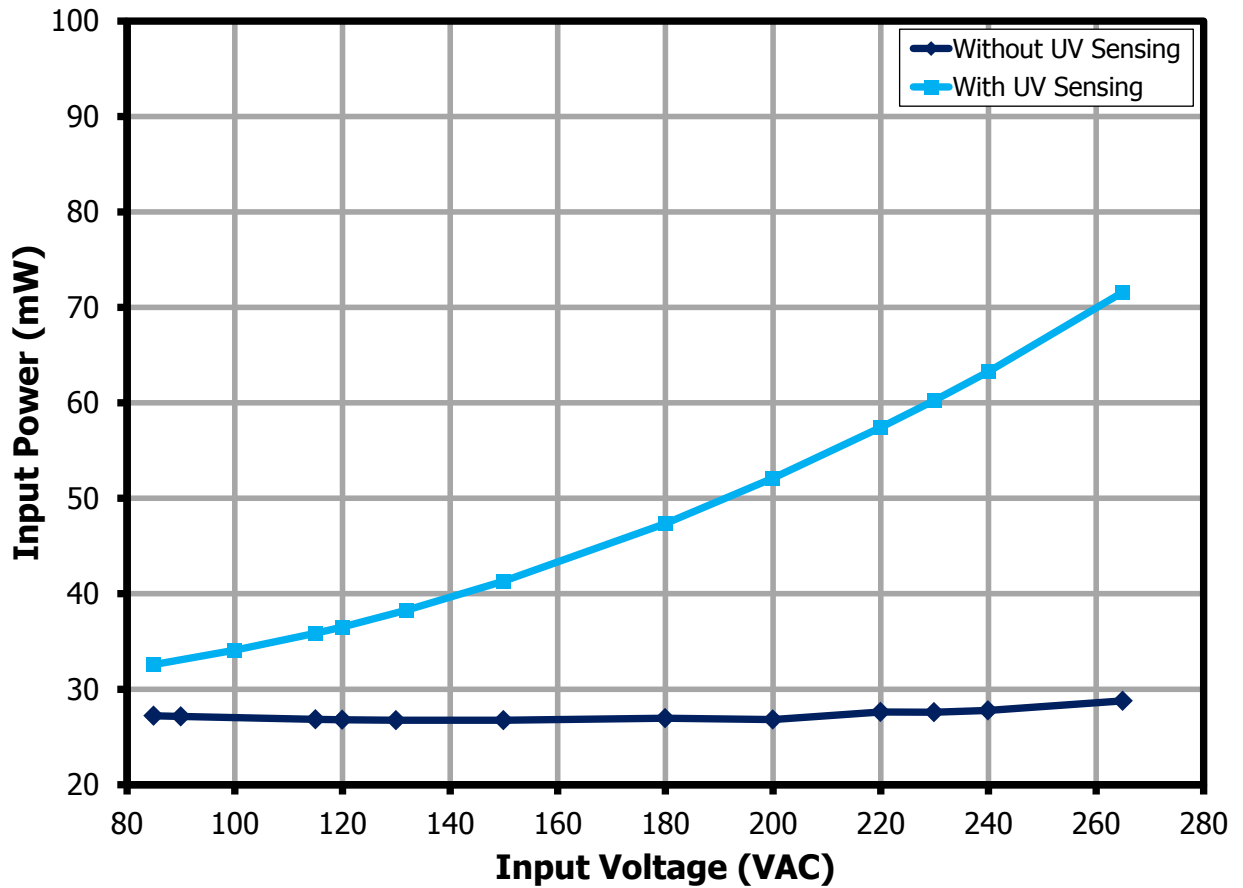


**Figure 12 –** No-Load Input Power vs. Line at Room Temperature.

## 10.4  *Line Regulation*

Test Condition: Soak for 15 minutes for each line.
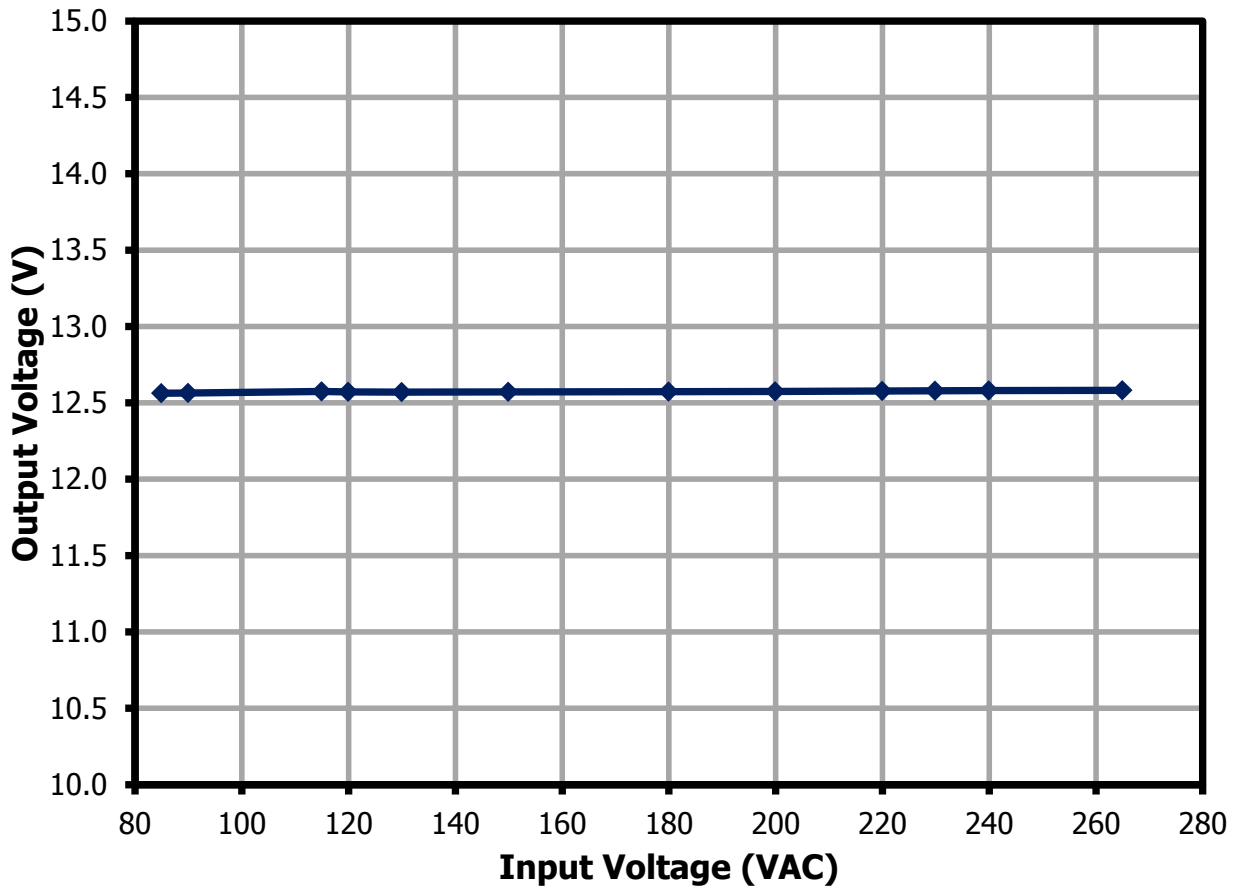


**Figure 13 –** Output Voltage vs. Line Voltage.

## 10.5    *Load Regulation*

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.
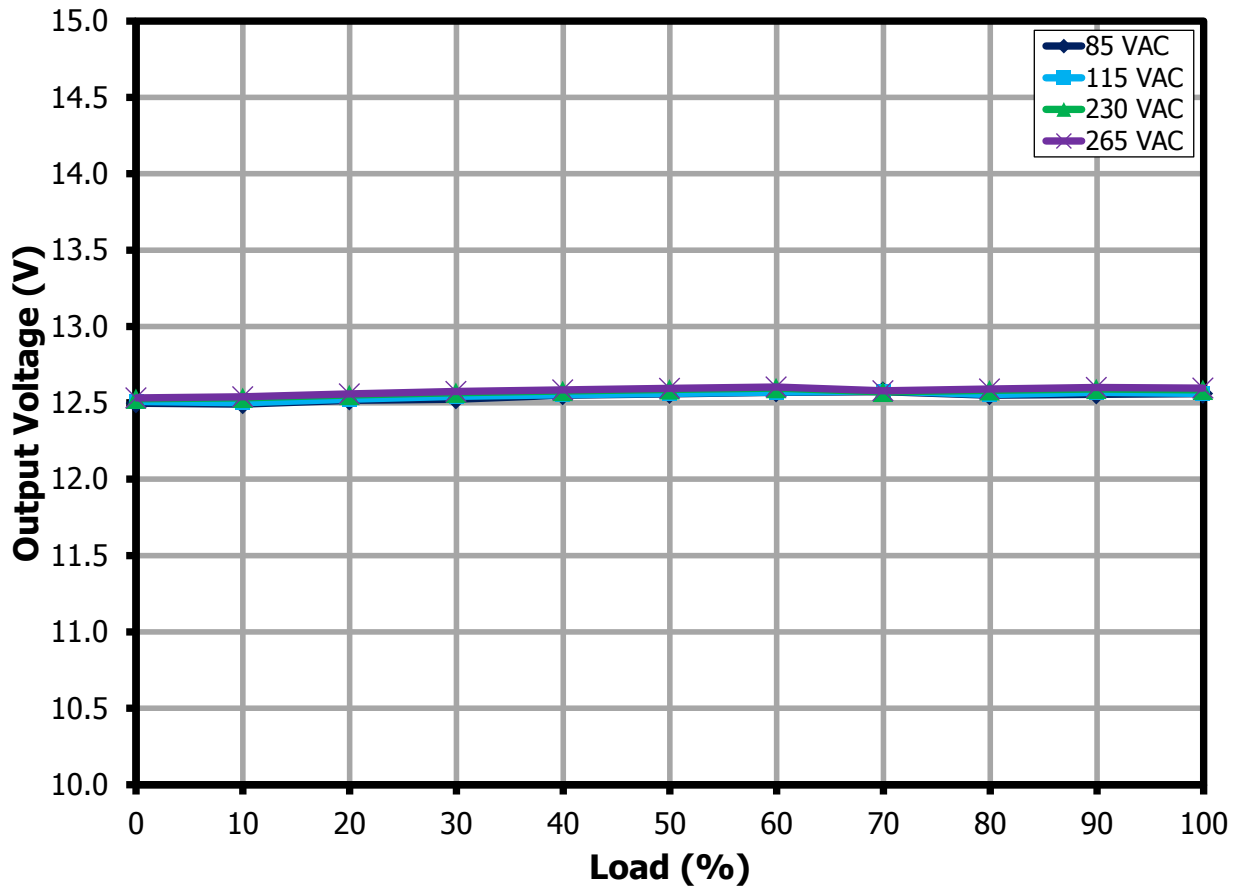


**Figure 14 –** Output Voltage vs. Percent Load.

## 11 **Waveforms**

### 11.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 1 kHz, Duty cycle = 50 %

### 11.1.1 0% - 100% Load Change
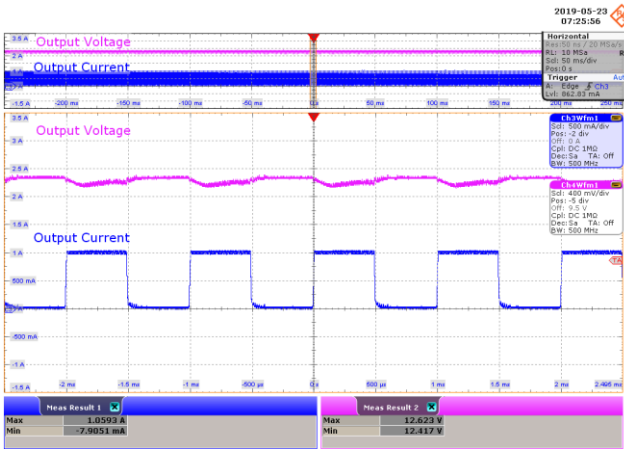


**Figure 15 –** 85 VAC 60 Hz.
CH3: $I_{OUT}$, 500 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
$V_{MAX}$: 12.623 V, $V_{MIN}$: 12.417 V.
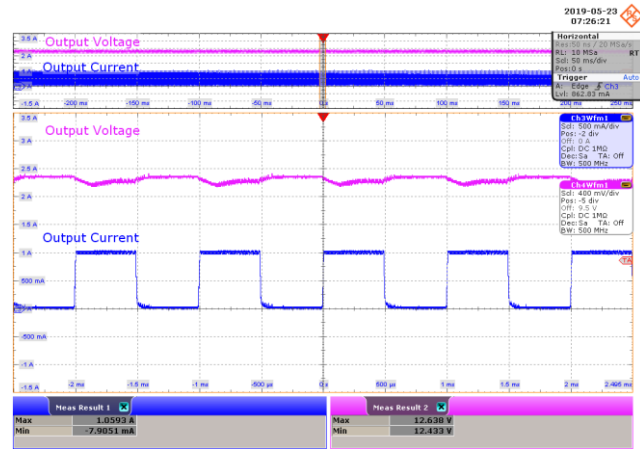


**Figure 16 –** 115 VAC 60 Hz.
CH3: $I_{OUT}$, 500 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
$V_{MAX}$: 12.638 V, $V_{MIN}$: 12.433 V.
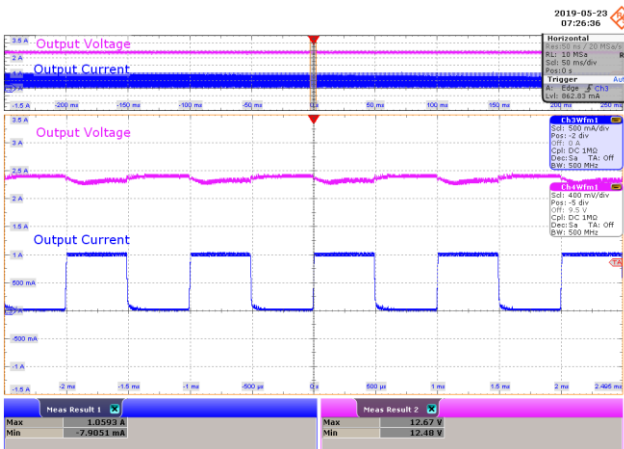


**Figure 17 –** 230 VAC 50 Hz.
CH3: $I_{OUT}$, 500 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
$V_{MAX}$: 12.67 V, $V_{MIN}$: 12.48 V.
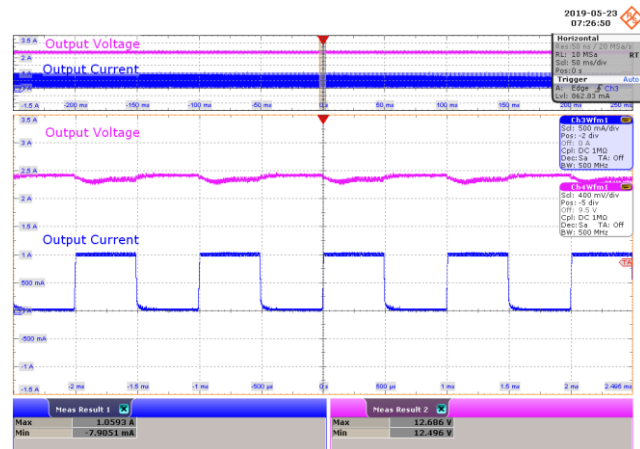


**Figure 18 –** 265 VAC 50 Hz.
CH3: $I_{OUT}$, 500 mA / div., 50 ms / div.
CH4: $V_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
$V_{MAX}$: 12.686 V, $V_{MIN}$: 12.496 V.

## 11.1.2    50% - 100% Load Change
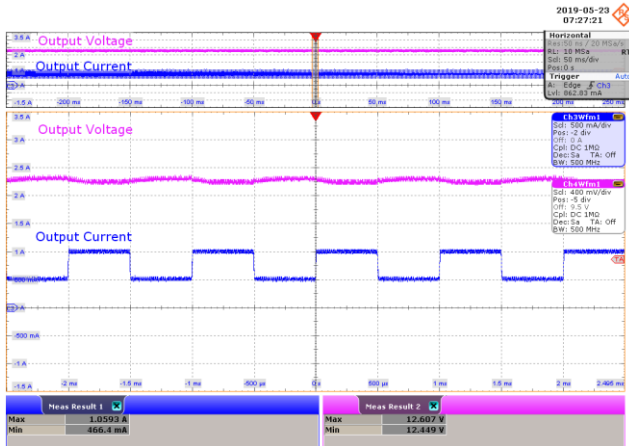


**Figure 19 –** 85 VAC 60 Hz.
CH3: I$_{OUT,}$ 500 mA / div., 50 ms / div.
CH4: V$_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
V$_{MAX}$: 12.607 V, V$_{MIN}$: 12.449 V.
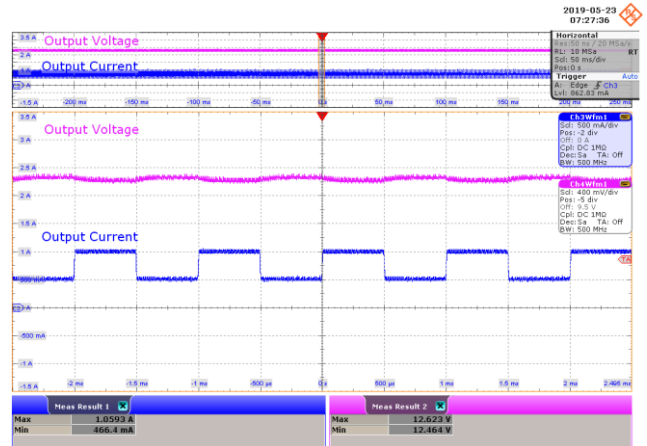
**Figure 20 –** 115 VAC 60 Hz.
CH3: I$_{OUT,}$ 500 mA / div., 50 ms / div.
CH4: V$_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
V$_{MAX}$: 12.623 V, V$_{MIN}$: 12.464 V.
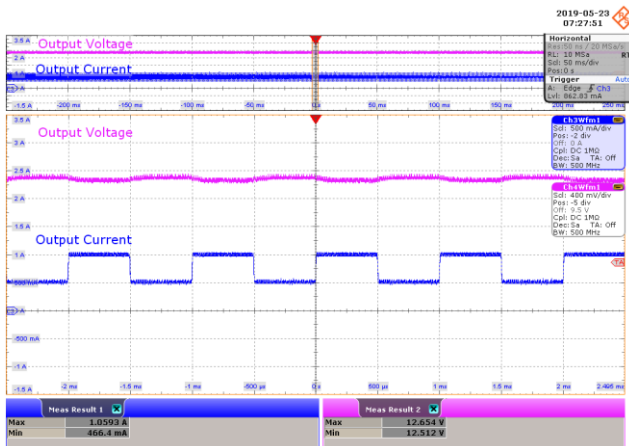


**Figure 21 –** 230 VAC 50 Hz.
CH3: I$_{OUT,}$ 500 mA / div., 50 ms / div.
CH4: V$_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
V$_{MAX}$: 12.654 V, V$_{MIN}$: 12.512 V.
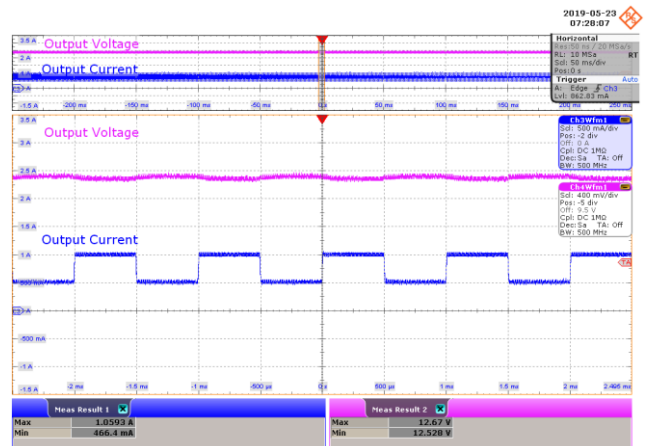
**Figure 22 –** 265 VAC 50 Hz.
CH3: I$_{OUT,}$ 500 mA / div., 50 ms / div.
CH4: V$_{OUT}$, 400 mV / div., 50 ms / div.
Zoom = 500 µs / div.
V$_{MAX}$: 12.67 V, V$_{MIN}$: 12.528 V.

## 11.2   *Output Voltage at Start-up*

### 11.2.1   CC Mode

#### 11.2.1.1   100% Load
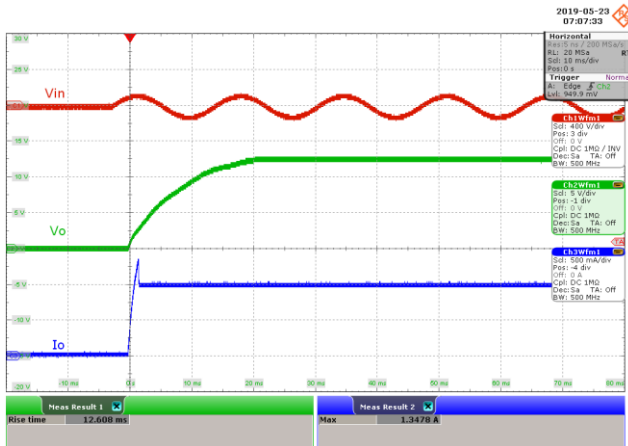


**Figure 23 –** 85 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
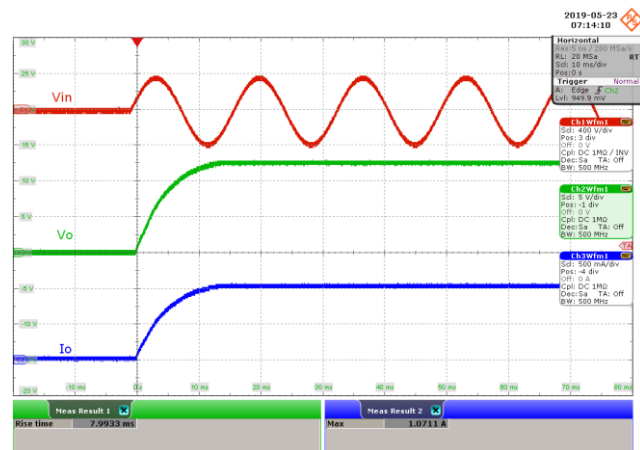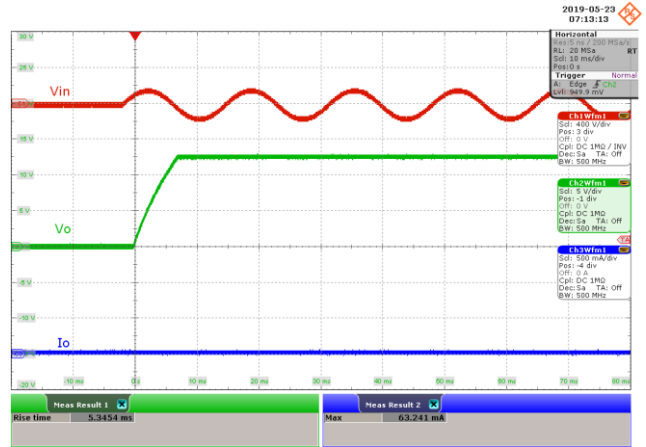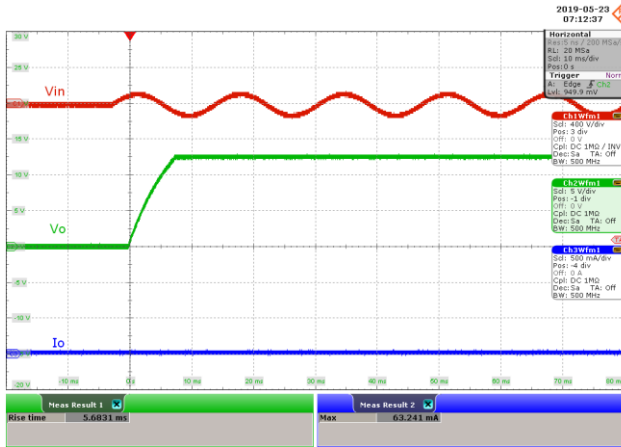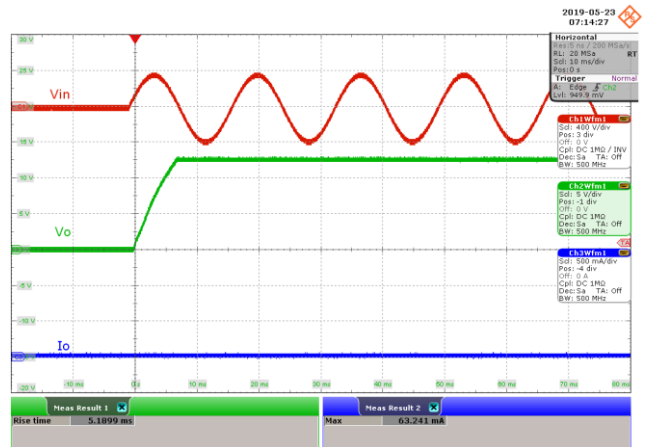CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 12.608 ms.
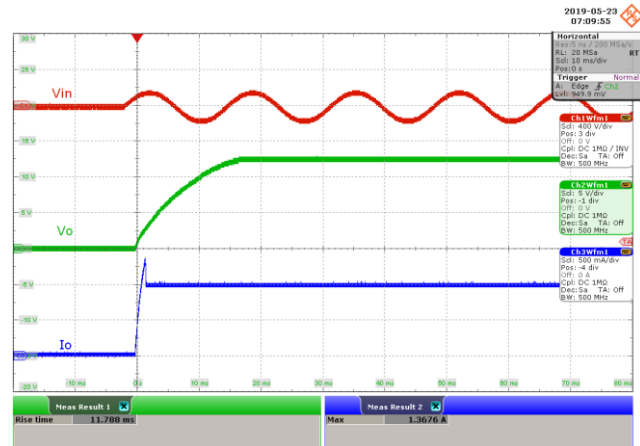


**Figure 24 –** 115 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
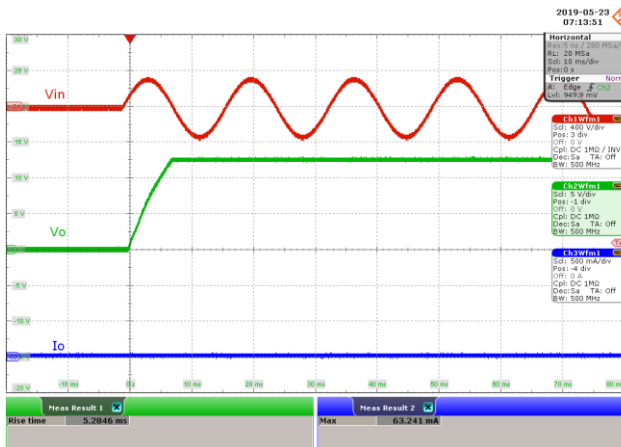Rise Time = 11.788 ms.
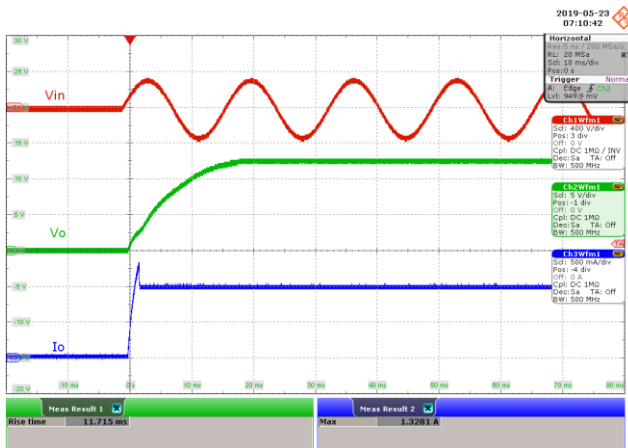


**Figure 25 –** 230 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 11.715 ms.
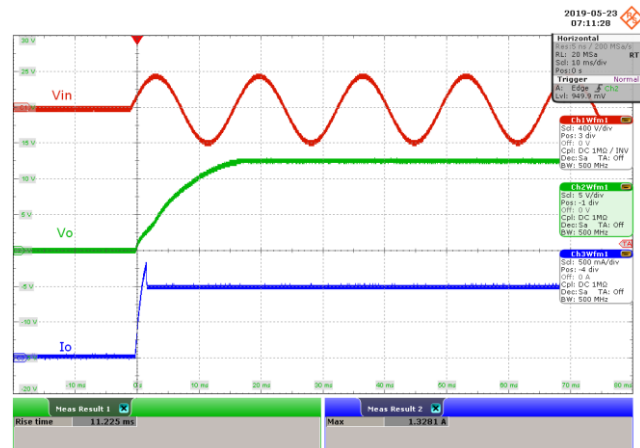


**Figure 26 –** 265 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 11.225 ms.

## 11.2.1.2   0% Load
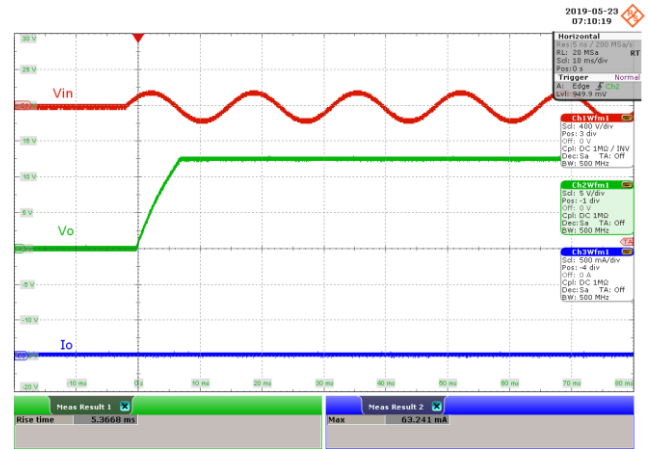


**Figure 27 –** 85 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.6977 ms.



**Figure 28 –** 115 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.3668 ms.
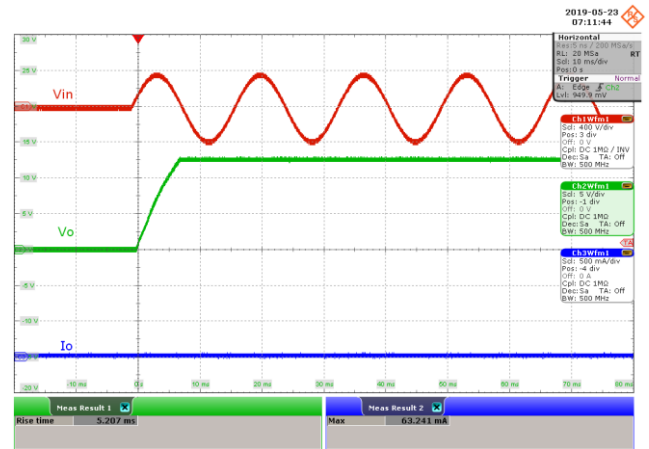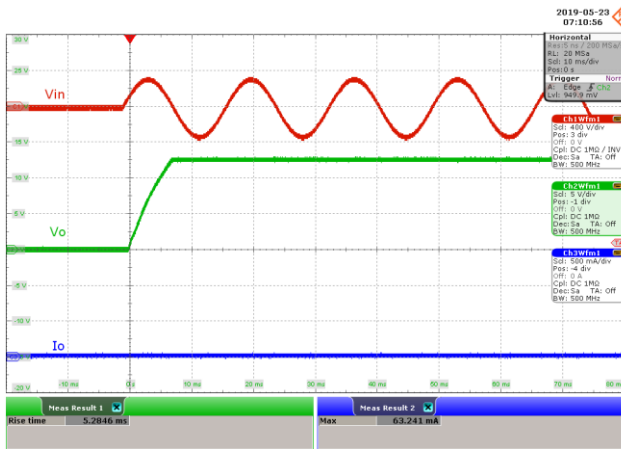


**Figure 29 –** 230 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.2846 ms.



**Figure 30 –** 265 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.207 ms.

**Power Integrations**
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## 11.2.2    CR Mode

### 11.2.2.1    100% Load
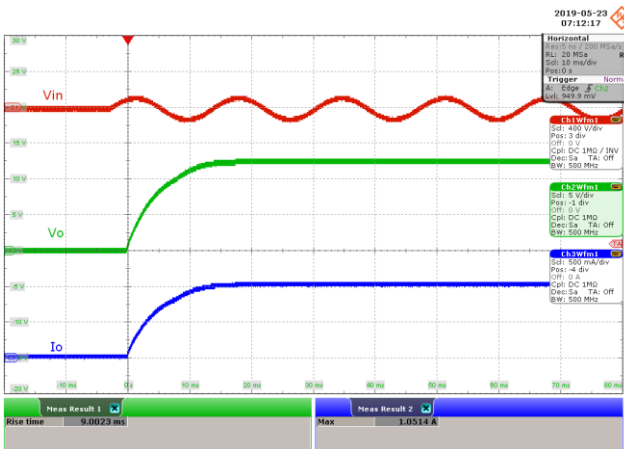


**Figure 31 –** 85 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 9.0023 ms.
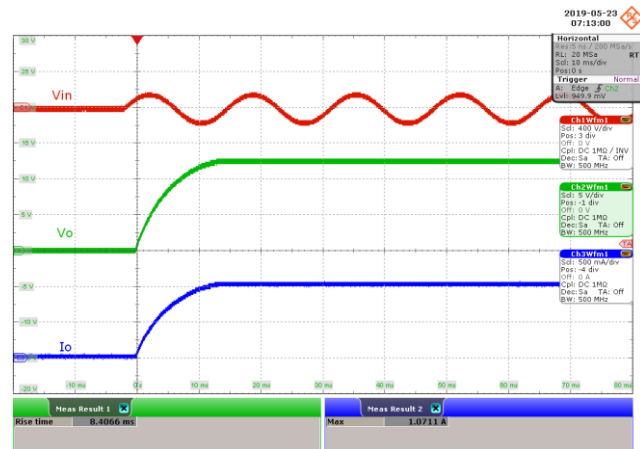


**Figure 32 –** 115 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 8.4066 ms.
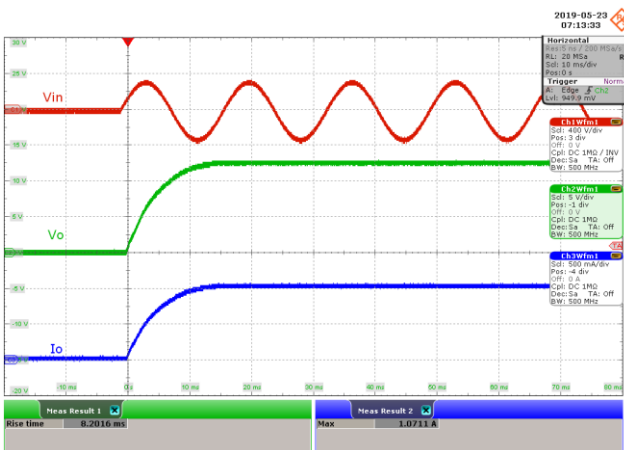


**Figure 33 –** 230 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 8.2016 ms.



**Figure 34 –** 265 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 7.9933 ms.

## 11.2.2.2    0% Load



**Figure 35 –** 85 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.6831 ms.



**Figure 36 –** 115 VAC 60 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.3454 ms.



**Figure 37 –** 230 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.2846 ms.



**Figure 38 –** 265 VAC 50 Hz.
CH1: $V_{IN}$, 400 V / div., 10 ms / div.
CH2: $V_{OUT}$, 5 V / div., 10 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 10 ms / div.
Rise Time = 5.1899 ms.

## 11.3   *Switching Waveforms*

### 11.3.1     Primary MOSFET Drain-Source Voltage and Current at Normal Operation

#### 11.3.1.1   100% Load
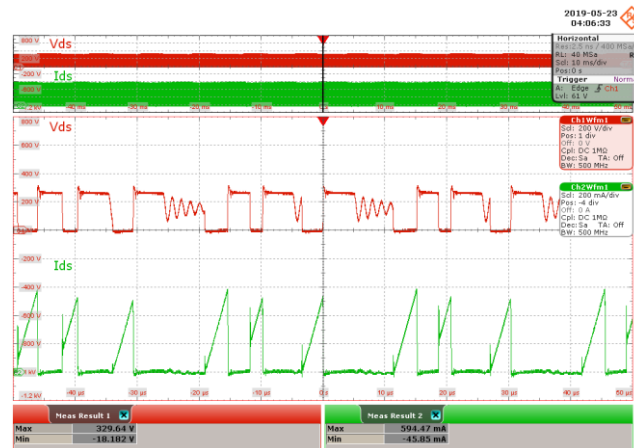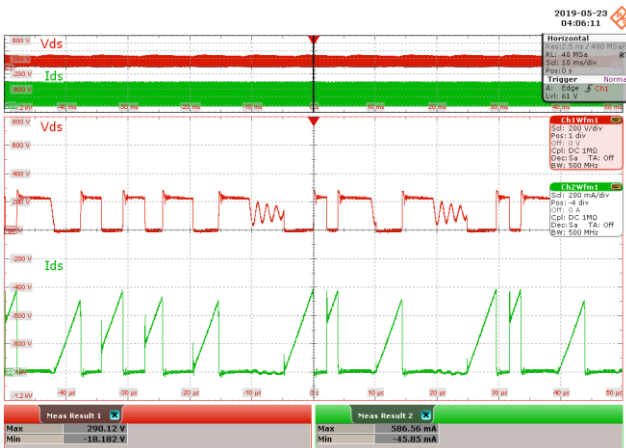


**Figure 39 —** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 290.12 V, $I_{DS(MAX)}$ = 586.56 mA.



**Figure 40 —** 115 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 329.64 V, $I_{DS(MAX)}$ = 594.47 mA.



**Figure 41 —** 230 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 487.75 V, $I_{DS(MAX)}$ = 547.04 mA.



**Figure 42 —** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 μs / div.
$V_{DS(MAX)}$ = 543.08 V, $I_{DS(MAX)}$ = 539.13 mA.

## 11.3.1.2    0% Load
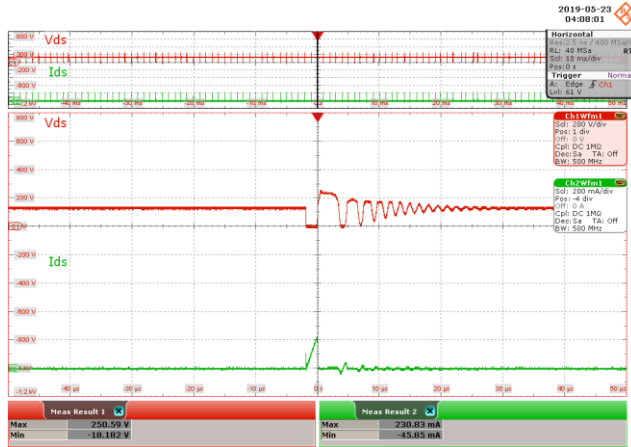


**Figure 43 —** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 $\mu$s / div.
$V_{DS(MAX)}$ = 250.59 V, $I_{DS(MAX)}$ = 230.83 mA.
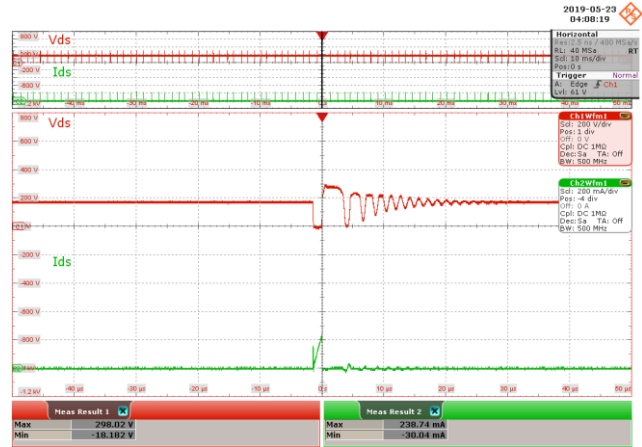


**Figure 44 —** 115 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 $\mu$s / div.
$V_{DS(MAX)}$ = 298.02 V, $I_{DS(MAX)}$ = 238.74 mA.
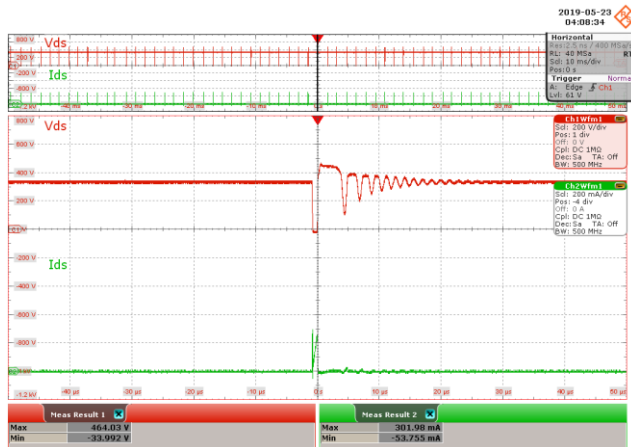


**Figure 45 —** 230 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 $\mu$s / div.
$V_{DS(MAX)}$ = 464.03 V, $I_{DS(MAX)}$ = 301.98 mA.
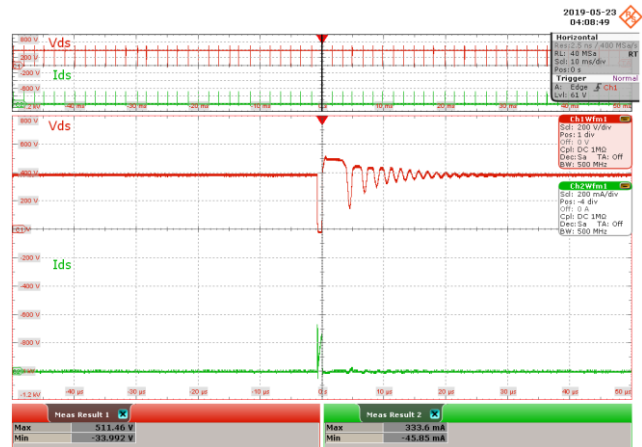


**Figure 46 —** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 10 ms / div.
CH2: $I_{DS}$, 200 mA / div., 10 ms / div.
Zoom: 10 $\mu$s / div.
$V_{DS(MAX)}$ = 511.46 V, $I_{DS(MAX)}$ = 333.6 mA.

## 11.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

### 11.3.2.1 100% Load
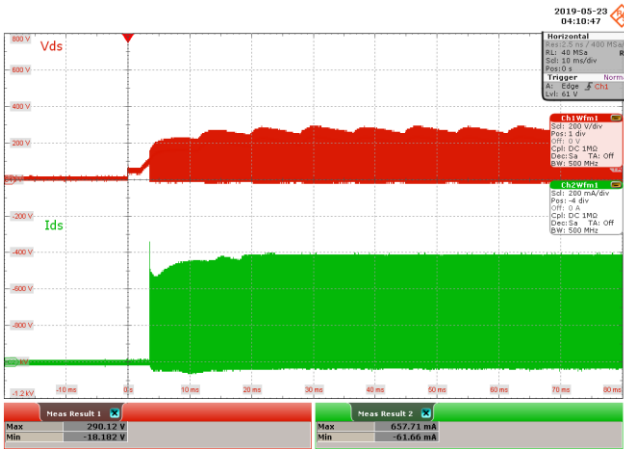


**Figure 47 –** 85 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 ms / div.
CH2: $I_{DS,}$ 200 mA / div., 10 ms / div.
$V_{DS(MAX)}$ = 290.12 V, $I_{DS(MAX)}$ = 657.71 mA.



**Figure 48 –** 115 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 ms / div.
CH2: $I_{DS,}$ 200 mA / div., 10 ms / div.
$V_{DS(MAX)}$ = 329.64 V, $I_{DS(MAX)}$ = 673.52 mA.



**Figure 49 –** 230 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 ms / div.
CH2: $I_{DS,}$ 200 mA / div., 10 ms / div.
$V_{DS(MAX)}$ = 495.65 V, $I_{DS(MAX)}$ = 744.66 mA.
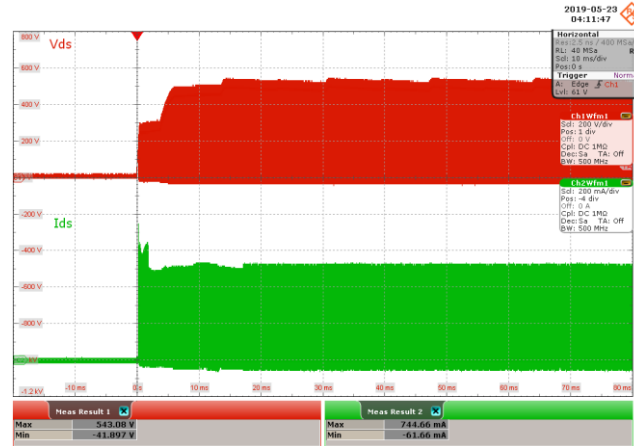


**Figure 50 –** 265 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 ms / div.
CH2: $I_{DS,}$ 200 mA / div., 10 ms / div.
$V_{DS(MAX)}$ = 543.08 V, $I_{DS(MAX)}$ = 744.66 mA.

## 11.3.2.2    0% Load



**Figure 51 —** 85 VAC 60 Hz.
CH1: V$_{DS}$, 200 V / div., 10 ms / div.
CH2: I$_{DS}$, 200 mA / div., 10 ms / div.
V$_{DS(MAX)}$ = 274.31 V, I$_{DS(MAX)}$ = 720.95 mA.



**Figure 52 —** 115 VAC 60 Hz.
CH1: V$_{DS}$, 200 V / div., 10 ms / div.
CH2: I$_{DS}$, 200 mA / div., 10 ms / div.
V$_{DS(MAX)}$ = 305.93 V, I$_{DS(MAX)}$ = 728.85 mA.
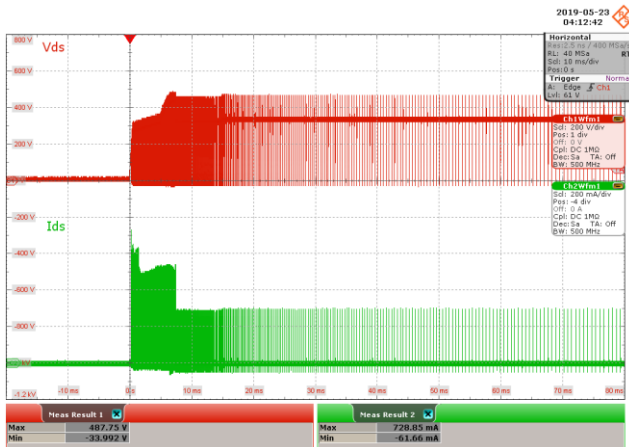


**Figure 53 —** 230 VAC 50 Hz.
CH1: V$_{DS}$, 200 V / div., 10 ms / div.
CH2: I$_{DS}$, 200 mA / div., 10 ms / div.
V$_{DS(MAX)}$ = 487.75 V, I$_{DS(MAX)}$ = 728.85 mA.
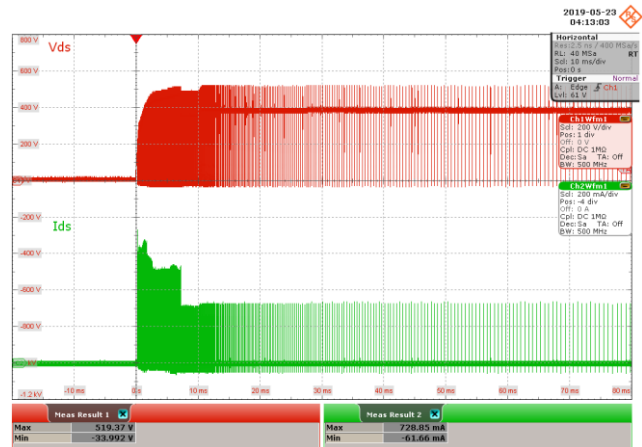


**Figure 54 —** 265 VAC 50 Hz.
CH1: V$_{DS}$, 200 V / div., 10 ms / div.
CH2: I$_{DS}$, 200 mA / div., 10 ms / div.
V$_{DS,MAX}$ = 519.37 V, I$_{DS(MAX)}$ = 728.85 mA.

### 11.3.3    Output Diode Voltage and Current at Normal Operation

### 11.3.3.1    100% Load
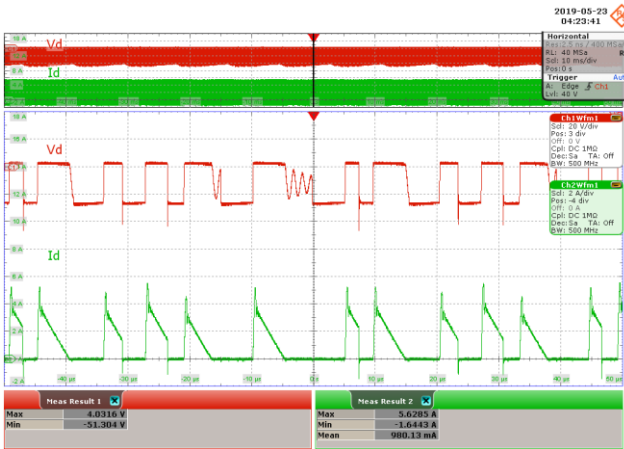


**Figure 55 –** 85 VAC 60 Hz.
CH1: $V_D$, 20 V / div., 10 ms / div.
CH2: $I_D$, 2 A / div., 10 ms / div.
Zoom: 10 μs / div.
PIV = 51.304 V, $I_{D(MAX)}$ = 5.6285 A.
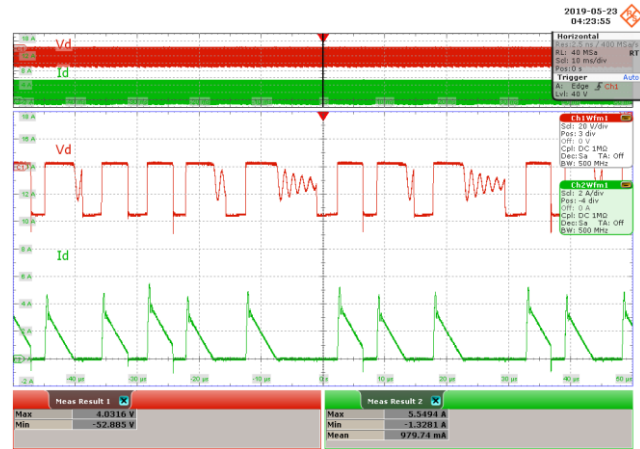


**Figure 56 –** 115 VAC 60 Hz.
CH1: $V_D$, 20 V / div., 10 ms / div.
CH2: $I_D$, 2 A / div., 10 ms / div.
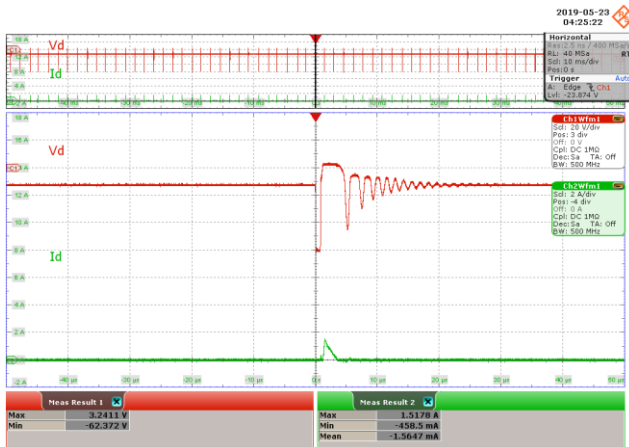Zoom: 10 μs / div.
PIV = 52.885 V, $I_{D(MAX)}$ = 5.5494 A.
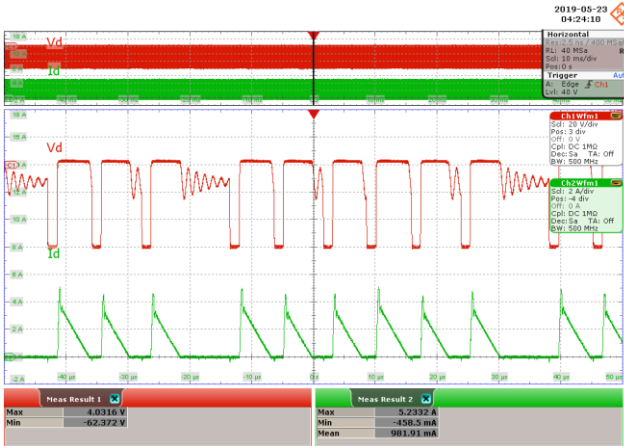


**Figure 57 –** 230 VAC 50 Hz.
CH1: $V_D$, 20 V / div., 10 ms / div.
CH2: $I_D$, 2 A / div., 10 ms / div.
Zoom: 10 μs / div.
PIV = 62.372 V, $I_{D(MAX)}$ = 5.2332 A.
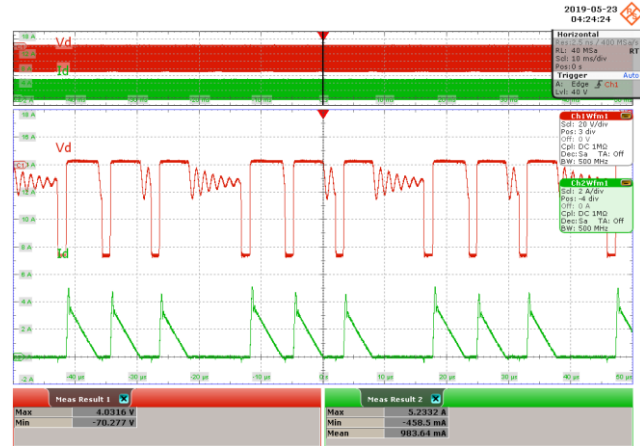


**Figure 58 –** 265 VAC 50 Hz.
CH1: $V_D$, 20 V / div., 10 ms / div.
CH2: $I_D$, 2 A / div., 10 ms / div.
Zoom: 10 μs / div.
PIV = 70.277 V, $I_{D(MAX)}$ = 5.2332 A.

## 11.3.3.2    0% Load
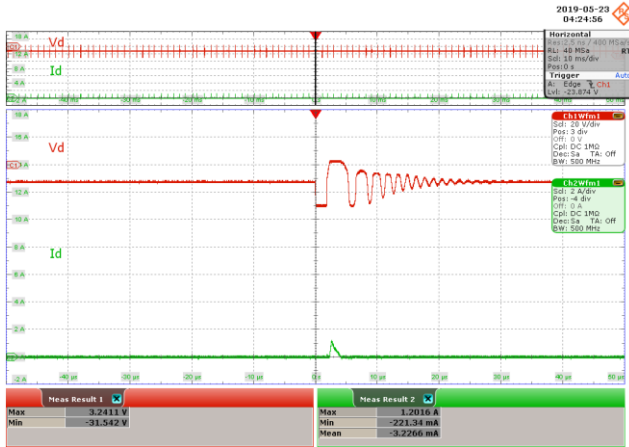


**Figure 59 –** 85 VAC 60 Hz.
CH1: V$_D$, 20 V / div., 10 ms / div.
CH2: I$_D$, 2 A / div., 10 ms / div.
Zoom: 10 µs / div.
PIV = 31.542 V, I$_{D(MAX)}$ = 1.2016 A.
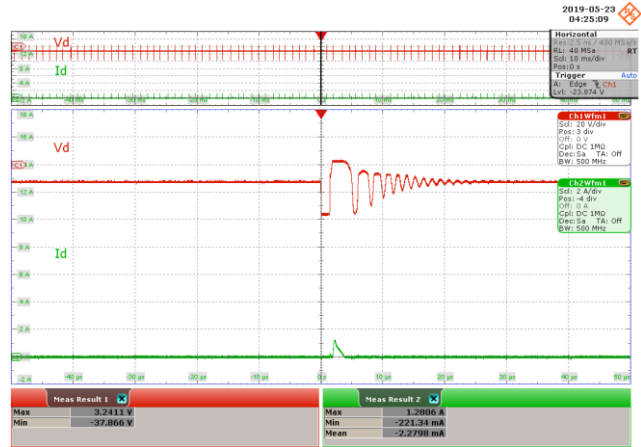
**Figure 60 –** 115 VAC 60 Hz.
CH1: V$_D$, 20 V / div., 10 ms / div.
CH2: I$_D$, 2 A / div., 10 ms / div.
Zoom: 10 µs / div.
PIV = 37.866 V, I$_{D(MAX)}$ = 1.2806 A.



**Figure 61 –** 230 VAC 50 Hz.
CH1: V$_D$, 20 V / div., 10 ms / div.
CH2: I$_D$, 2 A / div., 10 ms / div.
Zoom: 10 µs / div.
PIV = 62.372 V, I$_{D(MAX)}$ = 1.5178 A.
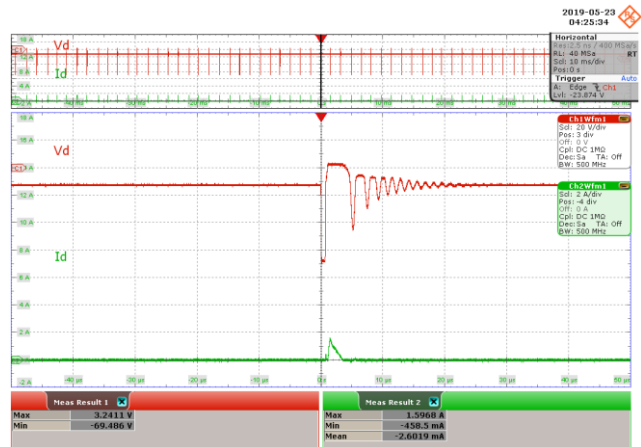
**Figure 62 –** 265 VAC 50 Hz.
CH1: V$_D$, 20 V / div., 10 ms / div.
CH2: I$_D$, 2 A / div., 10 ms / div.
Zoom: 10 µs / div.
PIV = 69.486 V, I$_{D(MAX)}$ = 1.5968 A.

## 11.3.4    Output Diode Voltage and Current at Start-up Operation
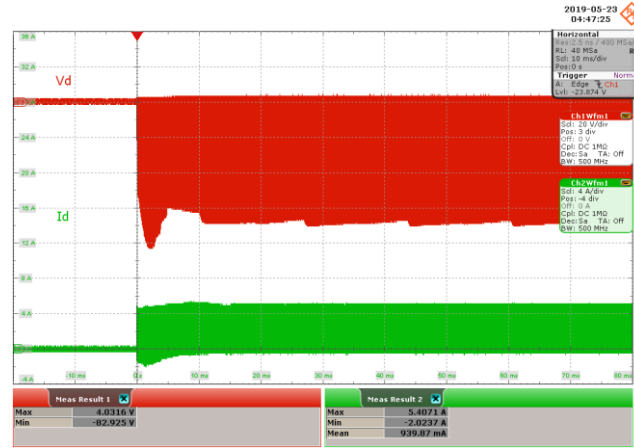
### 11.3.4.1    100% Load
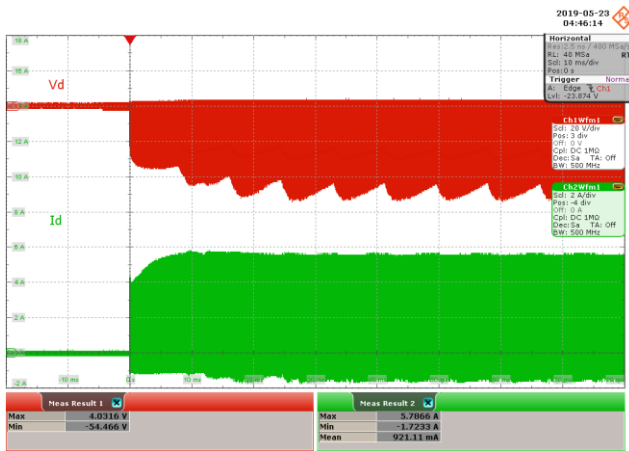


**Figure 63 –** 85 VAC 60 Hz.
    CH1: $V_D$, 20 V / div., 10 ms / div.
    CH2: $I_D$, 2 A / div., 10 ms / div.
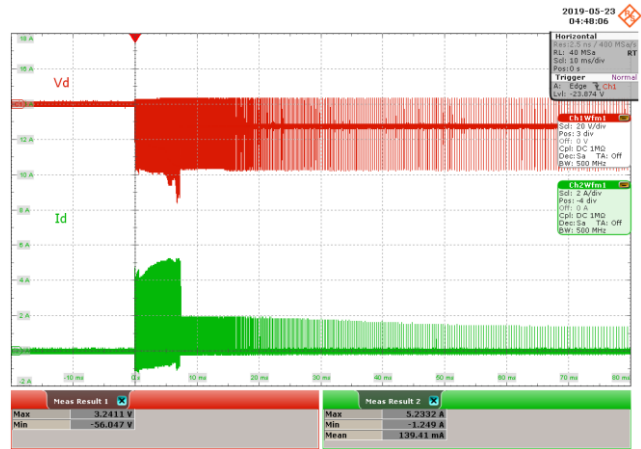    PIV = 54.466 V, $I_{D(MAX)}$ = 5.7866 A.
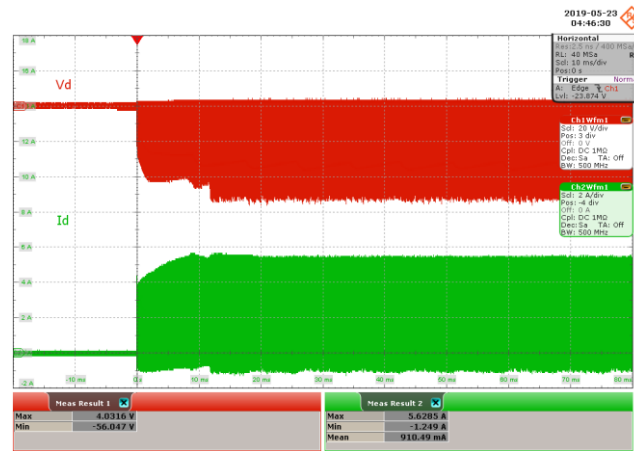


**Figure 64 –** 115 VAC 60 Hz.
    CH1: $V_D$, 20 V / div., 10 ms / div.
    CH2: $I_D$, 2 A / div., 10 ms / div.
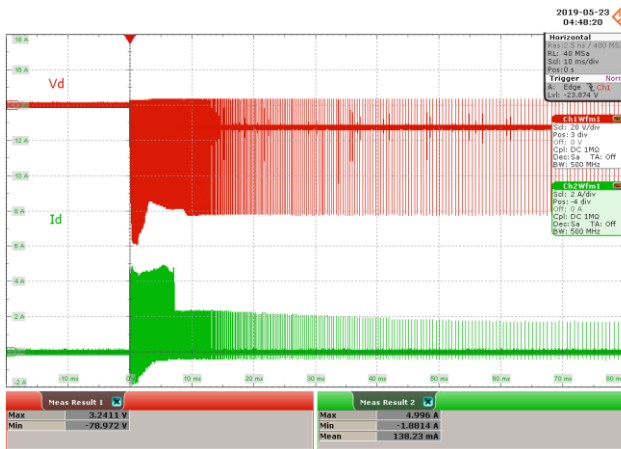    PIV = 56.047 V, $I_{D(MAX)}$ = 5.6285 A.
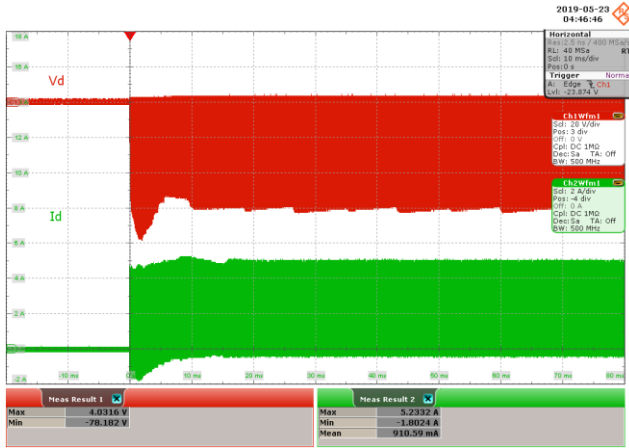


**Figure 65 –** 230 VAC 50 Hz.
    CH1: $V_D$, 20 V / div., 10 ms / div.
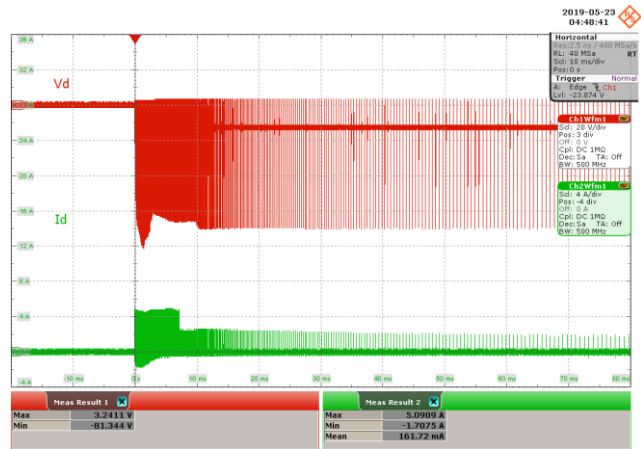    CH2: $I_D$, 2 A / div., 10 ms / div.
    PIV = 78.182 V, $I_{D(MAX)}$ = 5.2332 A.



**Figure 66 –** 265 VAC 50 Hz.
    CH1: $V_D$, 20 V / div., 10 ms / div.
    CH2: $I_D$, 4 A / div., 10 ms / div.
    PIV = 82.925 V, $I_{D(MAX)}$ = 5.4071 A.

## 11.3.4.2    0% Load



**Figure 67 –** 85 VAC 60 Hz.
   CH1: $V_D$, 20 V / div., 10 ms / div.
   CH2: $I_D$, 2 A / div., 10 ms / div.
   PIV = 41.818 V, $I_{D(MAX)}$ = 5.3913 A.



**Figure 68 –** 115 VAC 60 Hz.
   CH1: $V_D$, 20 V / div., 10 ms / div.
   CH2: $I_D$, 2 A / div., 10 ms / div.
   PIV = 56.047 V, $I_{D(MAX)}$ = 5.2332 A.



**Figure 69 –** 230 VAC 50 Hz.
   CH1: $V_D$, 20 V / div., 10 ms / div.
   CH2: $I_D$, 2 A / div., 10 ms / div.
   PIV = 78.972 V, $I_{D(MAX)}$ = 4.996 A.



**Figure 70 –** 265 VAC 50 Hz.
   CH1: $V_D$, 20 V / div., 10 ms / div.
   CH2: $I_D$, 4 A / div., 10 ms / div.
   PIV = 81.344 V, $I_{D(MAX)}$ = 5.0909 A.

## 11.4    *Brown-In and Brown-Out*
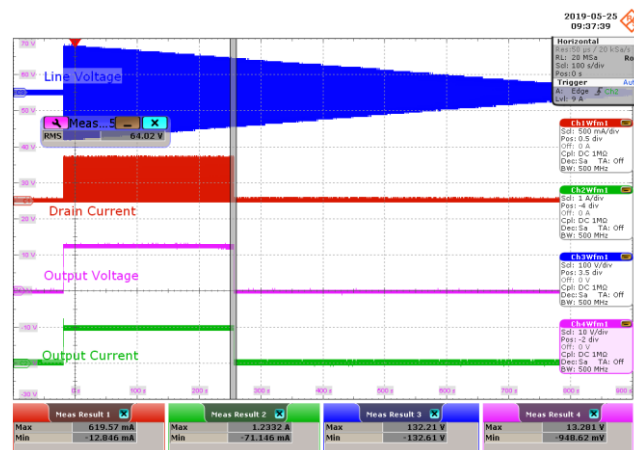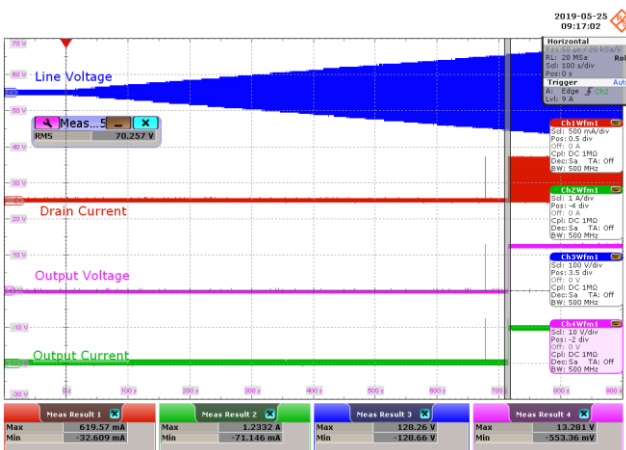
### 11.4.1    Without UV Sensing
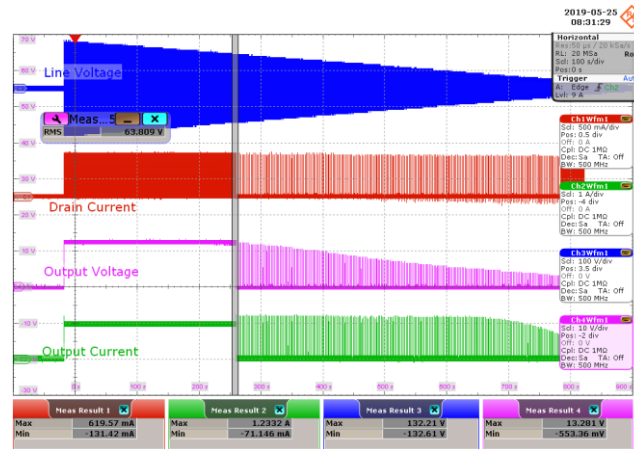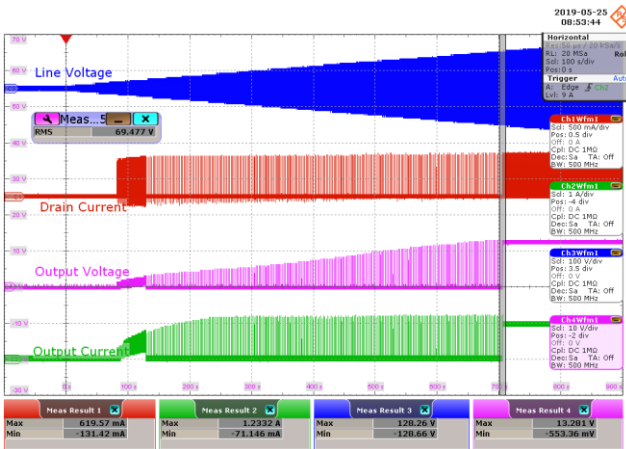


**Figure 71 –** Brown-In, Full Load.
CH1: $I_{DS}$, 500 mA / div., 100 s / div.
CH2: $I_{OUT}$, 1 A / div., 100 s / div.
CH3: $V_{IN}$, 100 V / div., 100 s / div.
CH4: $V_{OUT}$, 10 V / div., 100 s / div.

**Figure 72 –** Brown-Out, Full Load.
CH1: $I_{DS}$, 500 mA / div., 100 s / div.
CH2: $I_{OUT}$, 1 A / div., 100 s / div.
CH3: $V_{IN}$, 100 V / div., 100 s / div.
CH4: $V_{OUT}$, 10 V / div., 100 s / div.

### 11.4.2    With UV sensing



**Figure 73 –** Brown-In, Full Load.
CH1: $I_{DS}$, 500 mA / div., 100 s / div.
CH2: $I_{OUT}$, 1 A / div., 100 s / div.
CH3: $V_{IN}$, 100 V / div., 100 s / div.
CH4: $V_{OUT}$, 10 V / div., 100 s / div.

**Figure 74 –** Brown-In, Full Load.
CH1: $I_{DS}$, 500 mA / div., 100 s / div.
CH2: $I_{OUT}$, 1 A / div., 100 s / div.
CH3: $V_{IN}$, 100 V / div., 100 s / div.
CH4: $V_{OUT}$, 10 V / div., 100 s / div.

## 11.5   *Fault Conditions*

### 11.5.1    Output Overvoltage
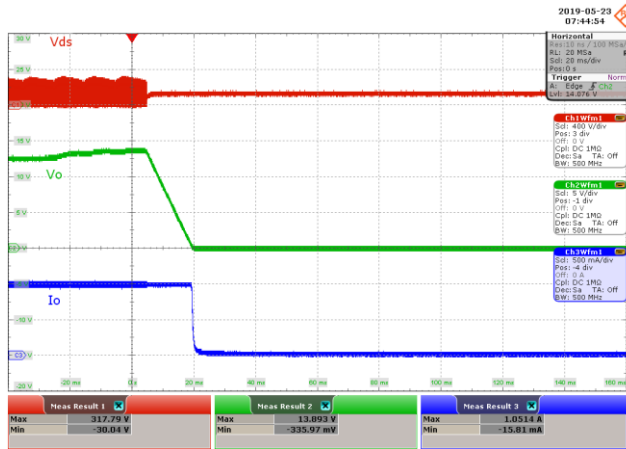
#### 11.5.1.1    100% Load, 25 ºC



**Figure 75** – 85 VAC 60 Hz.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
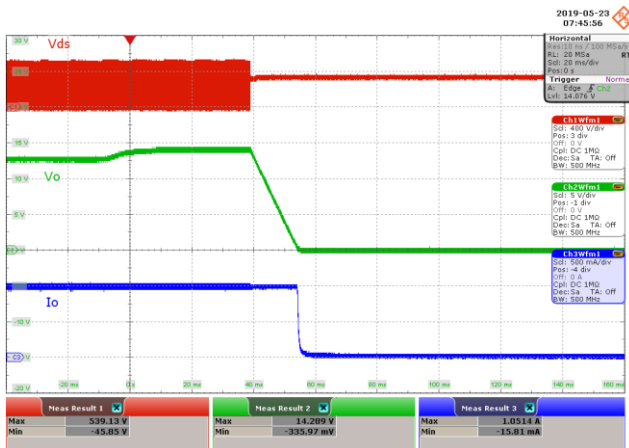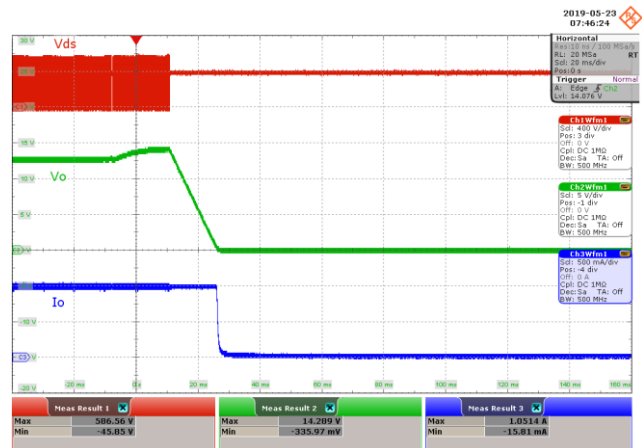CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 13.893 V.



**Figure 76** – 115 VAC 60 Hz.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.289 V.



**Figure 77** – 230 VAC 50 Hz.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.289 V.



**Figure 78** – 265 VAC 50 Hz.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
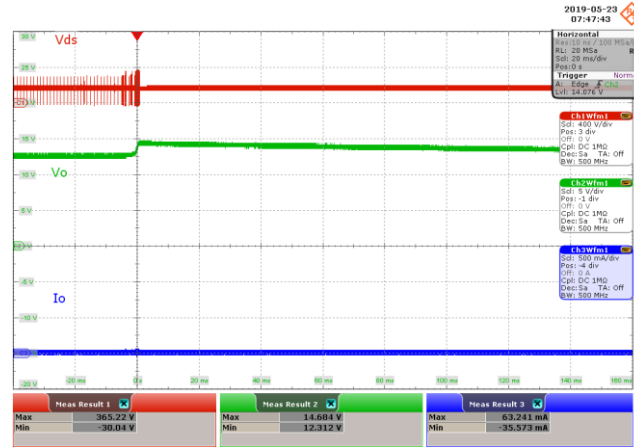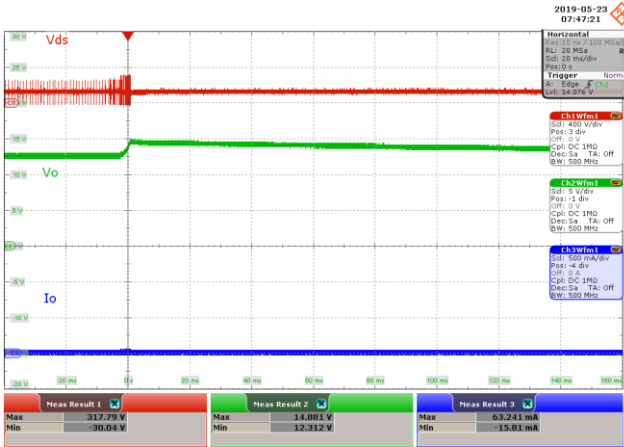$V_{OUT(MAX)}$ = 14.289 V.

## 11.5.1.2    0% Load, 25 ºC



**Figure 79 –** 85 VAC 60 Hz.
CH1: V$_{DS}$, 400 V / div., 20 ms / div.
CH2: V$_{OUT}$, 5 V / div., 20 ms / div.
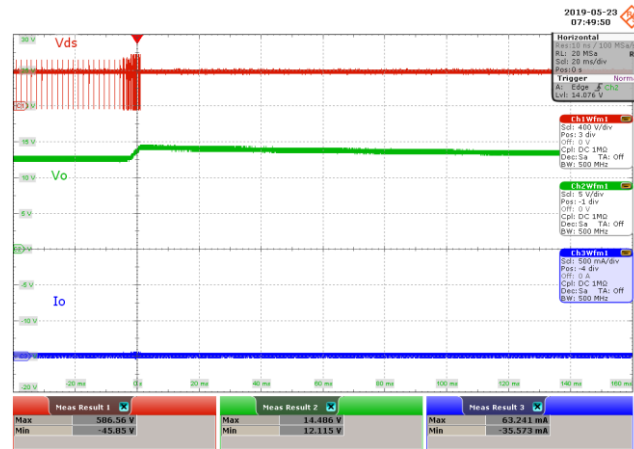CH3: I$_{OUT}$, 500 mA / div., 20 ms / div.
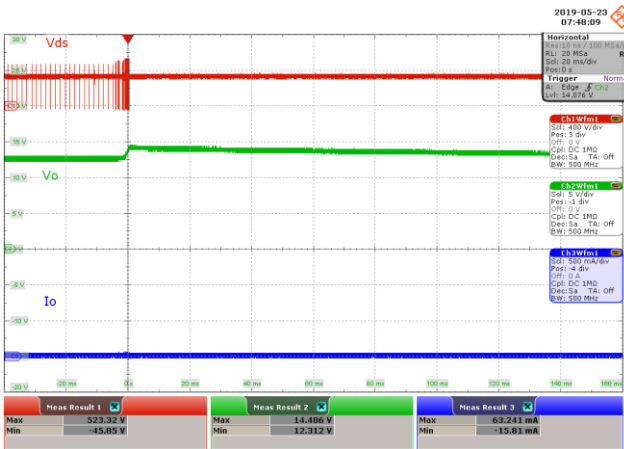V$_{OUT(MAX)}$ = 14.881 V.



**Figure 80 –** 115 VAC 60 Hz.
CH1: V$_{DS}$, 400 V / div., 20 ms / div.
CH2: V$_{OUT}$, 5 V / div., 20 ms / div.
CH3: I$_{OUT}$, 500 mA / div., 20 ms / div.
V$_{OUT(MAX)}$ = 14.684 V.



**Figure 81 –** 230 VAC 50 Hz.
CH1: V$_{DS}$, 400 V / div., 20 ms / div.
CH2: V$_{OUT}$, 5 V / div., 20 ms / div.
CH3: I$_{OUT}$, 500 mA / div., 20 ms / div.
V$_{OUT(MAX)}$ = 14.486 V.



**Figure 82 –** 265 VAC 50 Hz.
CH1: V$_{DS}$, 400 V / div., 20 ms / div.
CH2: V$_{OUT}$, 5 V / div., 20 ms / div.
CH3: I$_{OUT}$, 500 mA / div., 20 ms / div.
V$_{OUT(MAX)}$ = 14.486 V.
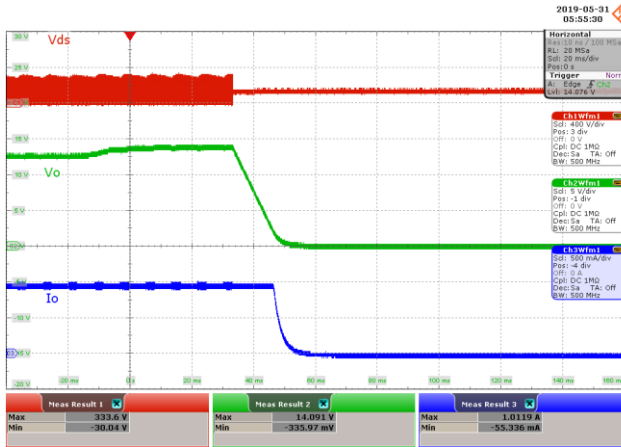
## 11.5.1.3    OVP at 50 °C



**Figure 83 –** 85 VAC 60 Hz, Full Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
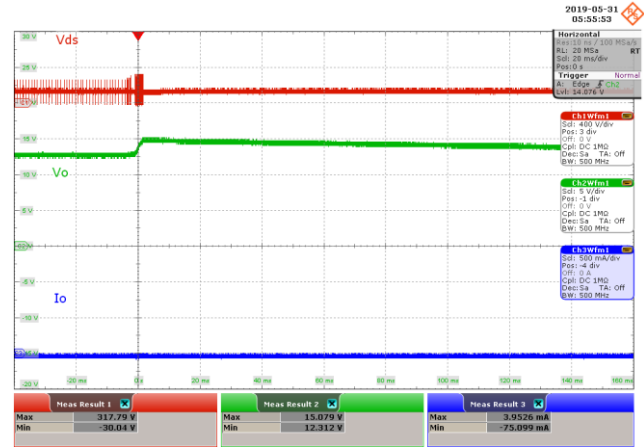CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.091 V.



**Figure 84 –** 85 VAC 60 Hz, No-Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
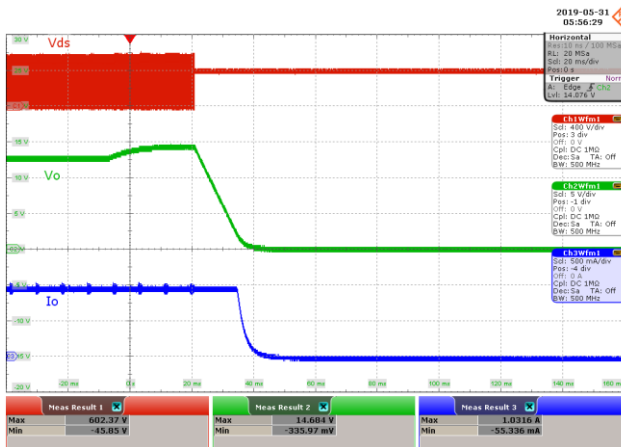$V_{OUT(MAX)}$ = 15.079 V.



**Figure 85 –** 265 VAC 50 Hz, Full Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
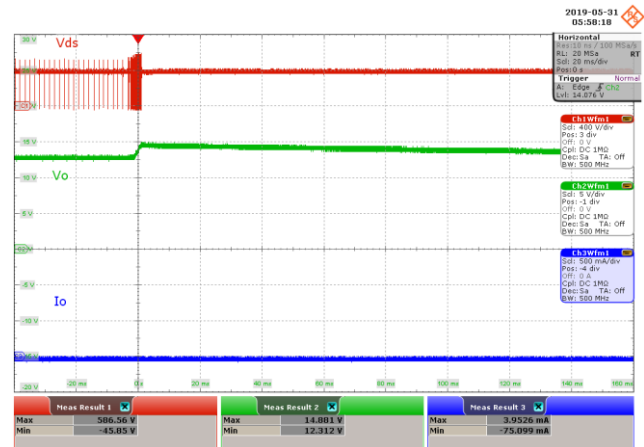CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.684 V.



**Figure 86 –** 265 VAC 50 Hz, No-Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.881 V.

**Power Integrations**
Tel: +1 408 414 9200   Fax: +1 408 414 9201
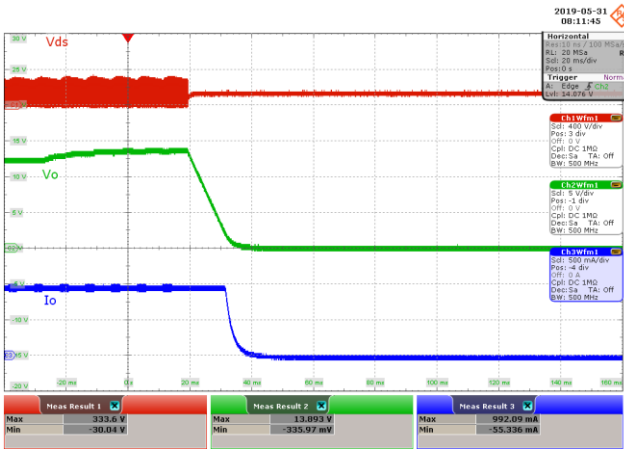www.power.com

## 11.5.1.4   OVP at 0 °C



**Figure 87 –** 85 VAC 60 Hz, Full Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
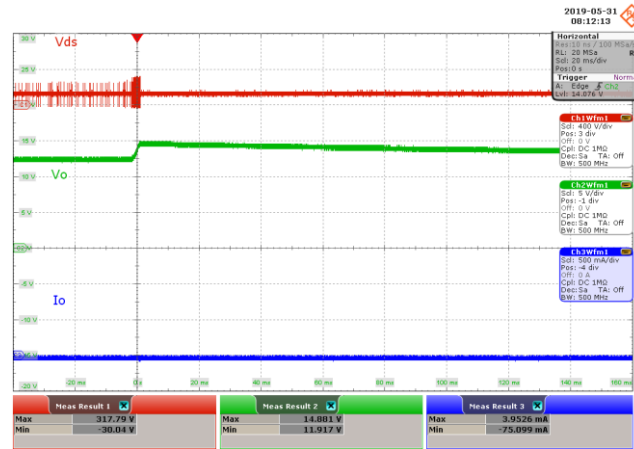CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 13.893 V.



**Figure 88 –** 85 VAC 60 Hz, No-Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
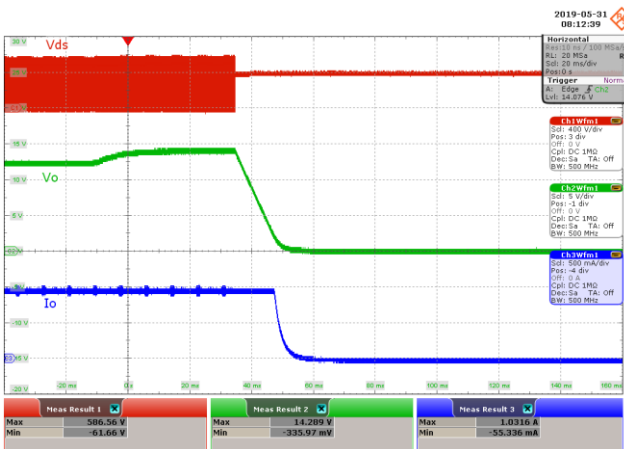$V_{OUT(MAX)}$ = 14.881 V.



**Figure 89 –** 265 VAC 50 Hz, Full Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
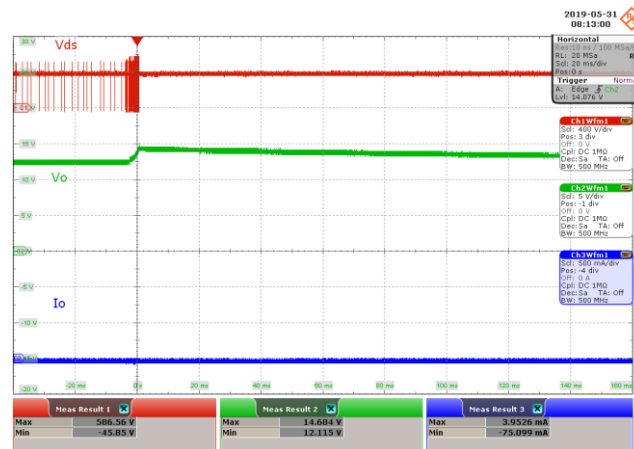$V_{OUT(MAX)}$ = 14.289 V.



**Figure 90 –** 265 VAC 50 Hz, No-Load.
CH1: $V_{DS}$, 400 V / div., 20 ms / div.
CH2: $V_{OUT}$, 5 V / div., 20 ms / div.
CH3: $I_{OUT}$, 500 mA / div., 20 ms / div.
$V_{OUT(MAX)}$ = 14.684 V.

## 11.5.2    Output Short Circuit

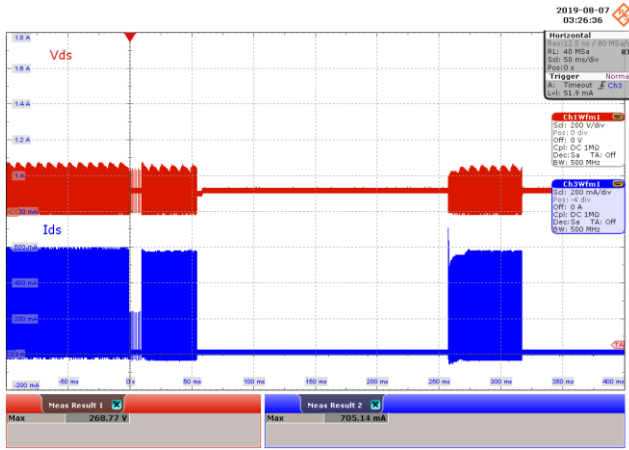Test Condition: Short circuit applied at normal operation



**Figure 91 –** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 50 ms / div.
CH3: $I_{DS}$, 200 mA / div., 50 ms / div.
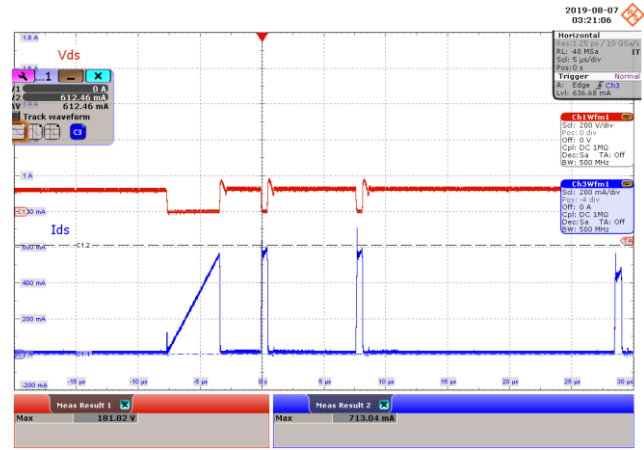$V_{DS,MAX}$ = 268.77 V.
$I_{DS,MAX}$ = 705.14 mA.



**Figure 92 –** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 5 µs / div.
CH3: $I_{DS}$, 200 mA / div., 5 µs / div.
$I_{LIM,MAX}$ = 612.46 mA



**Figure 93 –** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 50 ms / div.
CH3: $I_{DS}$, 200 mA / div., 50 ms / div.
$V_{DS,MAX}$ = 521.74 V.
$I_{DS,MAX}$ = 1.0055 A.



**Figure 94 –** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 5 µs / div.
CH3: $I_{DS}$, 200 mA / div., 5 µs / div.
$I_{LIM,MAX}$ = 802.77 mA

### 11.5.3 Output Overload

Test Condition: Output current step from 1A to 1.3A



**Figure 95 –** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 50 ms / div.
CH3: $I_{DS}$, 200 mA / div., 50 ms / div.
$V_{DS,MAX}$ = 276.68 V.
$I_{DS,MAX}$ = 689.33 mA.



**Figure 96 –** 85 VAC 60 Hz.
CH1: $V_{DS}$, 200 V / div., 5 µs / div.
CH3: $I_{DS}$, 200 mA / div., 5 µs / div.
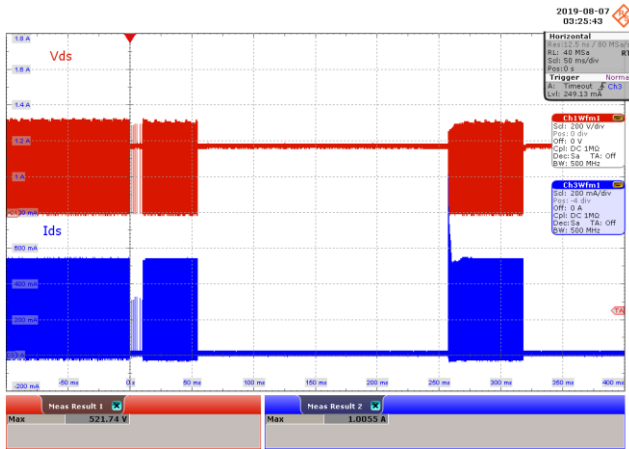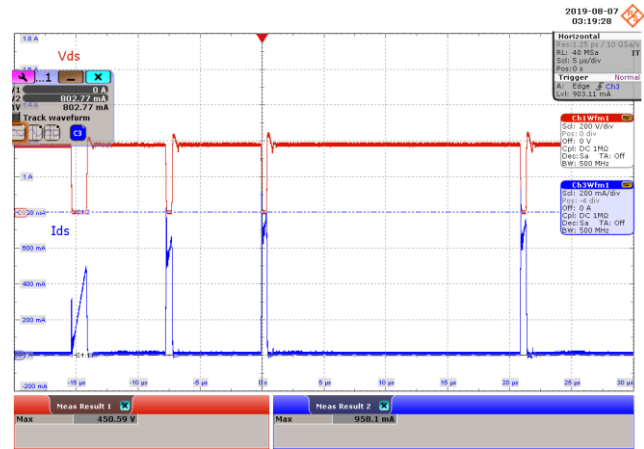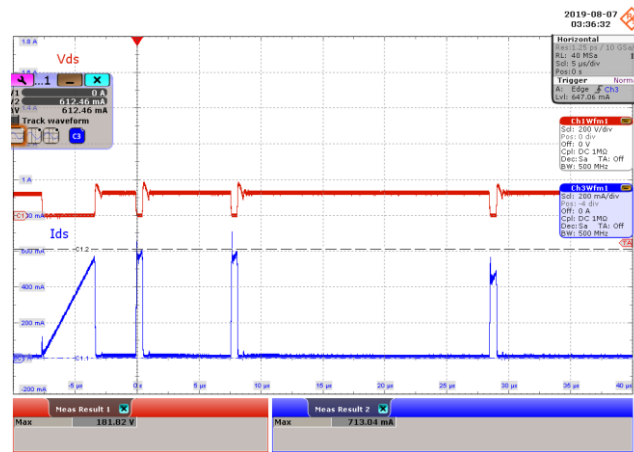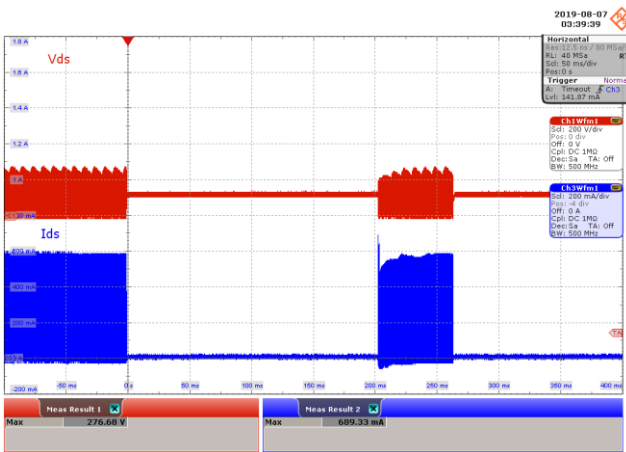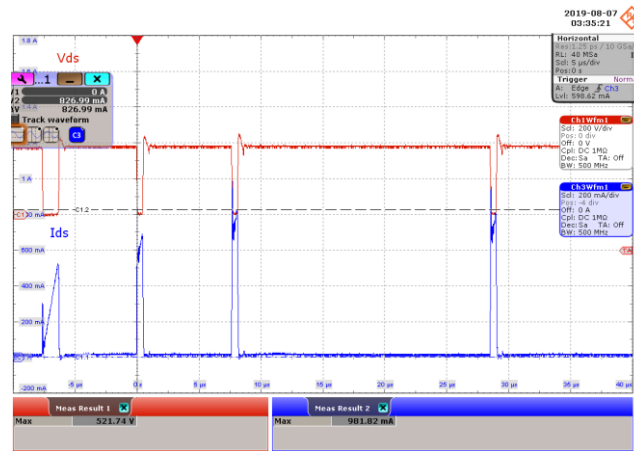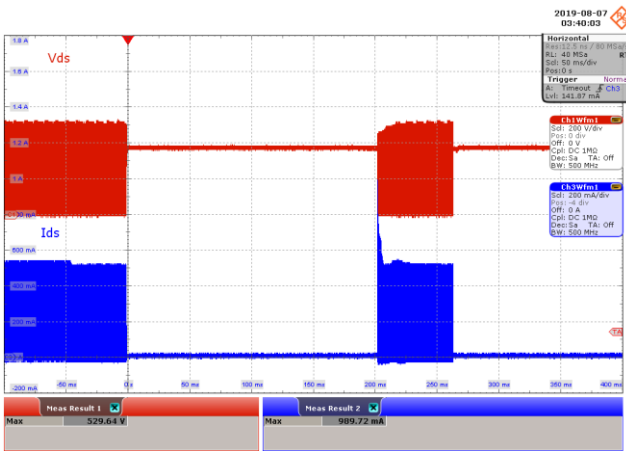$I_{LIM,MAX}$ = 713.04 mA



**Figure 97 –** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 50 ms / div.
CH3: $I_{DS}$, 200 mA / div., 50 ms / div.
$V_{DS,MAX}$ = 529.64 V.
$I_{DS,MAX}$ = 989.72 mA.



**Figure 98 –** 265 VAC 50 Hz.
CH1: $V_{DS}$, 200 V / div., 5 µs / div.
CH3: $I_{DS}$, 200 mA / div., 5 µs / div.
$I_{LIM,MAX}$ = 826.99 mA

Test Condition: Output current slowly ramped from 1A to 1.3A



**Figure 99** — 85 VAC 60 Hz.
CH2: V$_{OUT}$, 5 V / div., 5 s / div.
CH3: I$_{OUT}$, 500 mA / div., 5 s / div.
Math1: P$_{OUT}$, 5 W / div., 5 s / div.
P$_{O,MAX}$ = 14.436 W



**Figure 100** — 115 VAC 60 Hz.
CH2: V$_{OUT}$, 5 V / div., 5 s / div.
CH3: I$_{OUT}$, 500 mA / div., 5 s / div.
Math1: P$_{OUT}$, 5 W / div., 5 s / div.
P$_{O,MAX}$ = 15.588 W



**Figure 101** — 230 VAC 50 Hz.
CH2: V$_{OUT}$, 5 V / div., 5 s / div.
CH3: I$_{OUT}$, 500 mA / div., 5 s / div.
Math1: P$_{OUT}$, 5 W / div., 5 s / div.
P$_{O,MAX}$ = 15.093 W



**Figure 102** — 265 VAC 50 Hz.
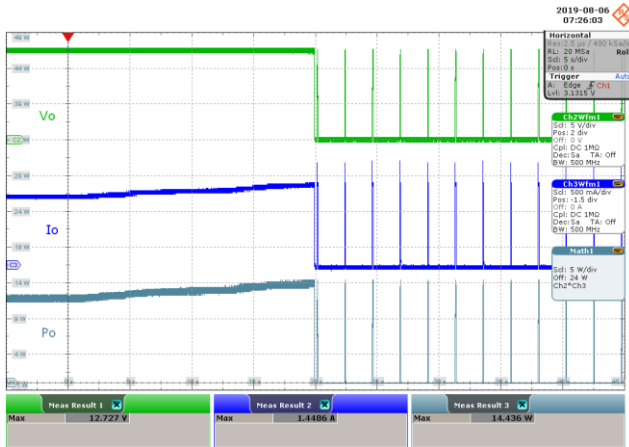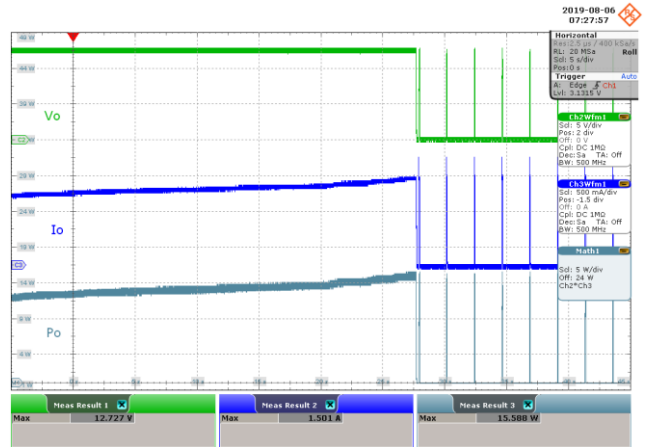CH2: V$_{OUT}$, 5 V / div., 5 s / div.
CH3: I$_{OUT}$, 500 mA / div., 5 s / div.
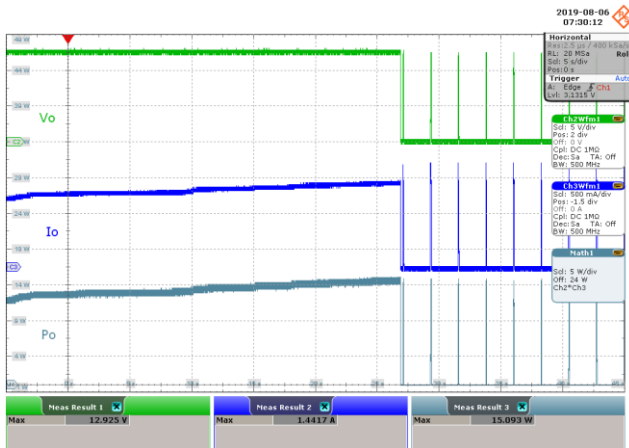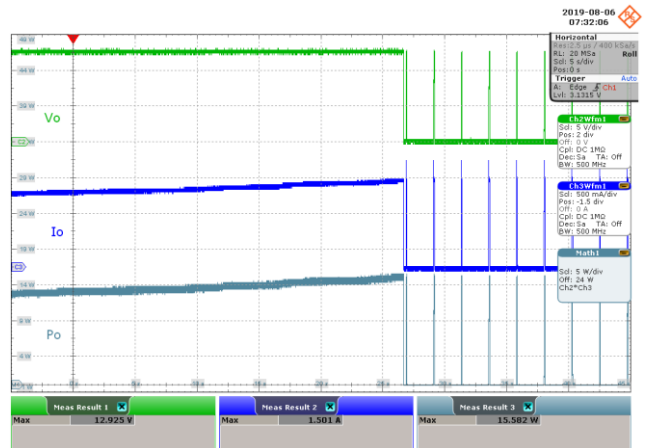Math1: P$_{OUT}$, 5 W / div., 5 s / div.
P$_{O,MAX}$ = 15.582 W

## 11.6 *Output Voltage Ripple*

### 11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu$F / 50 V ceramic type and one (1) 47 $\mu$F / 50 V aluminum electrolytic.  The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).
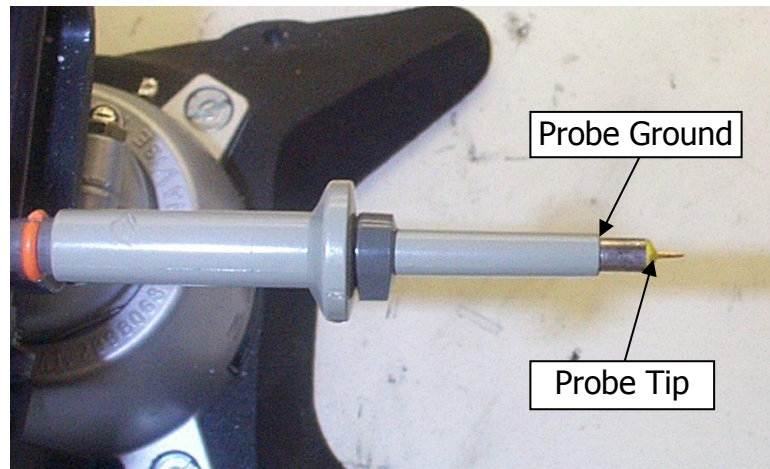


**Figure 103 –** Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)
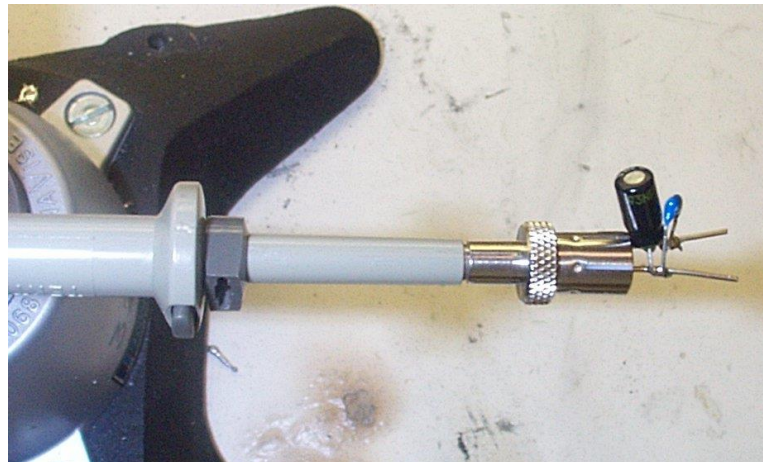


**Figure 104 –** Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

## 11.6.2    Measurement Results

## 11.6.2.1    100% Load Condition



**Figure 105 –** 85 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 75.889 mV.



**Figure 106 –** 115 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 66.403 mV.
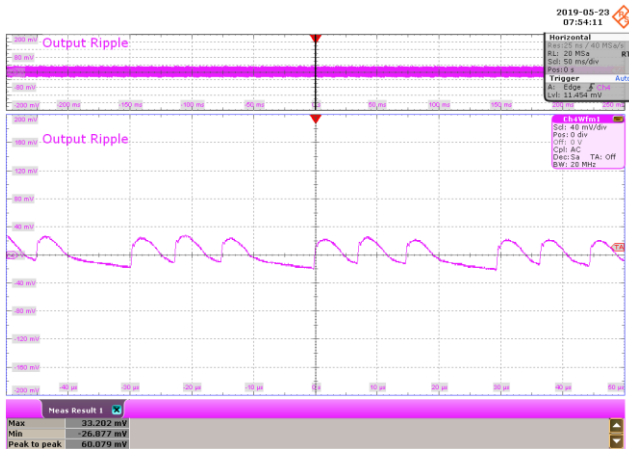


**Figure 107 –** 230 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 60.079 mV.
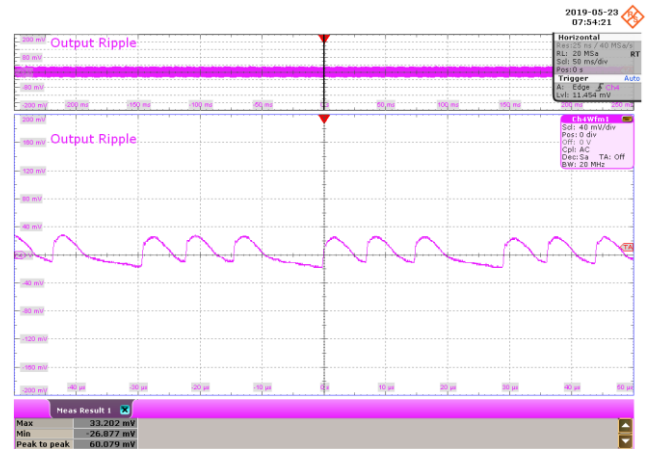


**Figure 108 –** 265 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 60.079 mV.

## 11.6.2.2    75% Load Condition

**Figure 109 –** 85 VAC 60 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 71.146 mV.
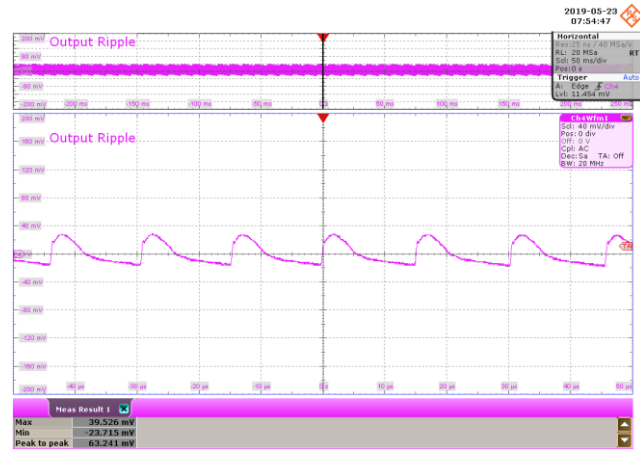
**Figure 110 –** 115 VAC 60 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 63.241 mV.
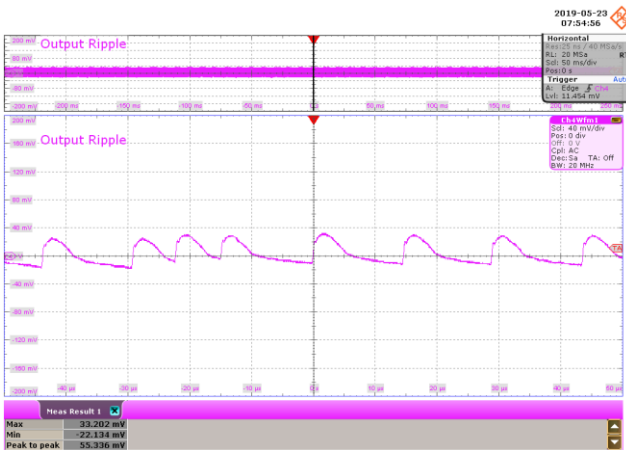
**Figure 111 –** 230 VAC 50 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 55.336 mV.

**Figure 112 –** 265 VAC 50 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 55.336 mV.
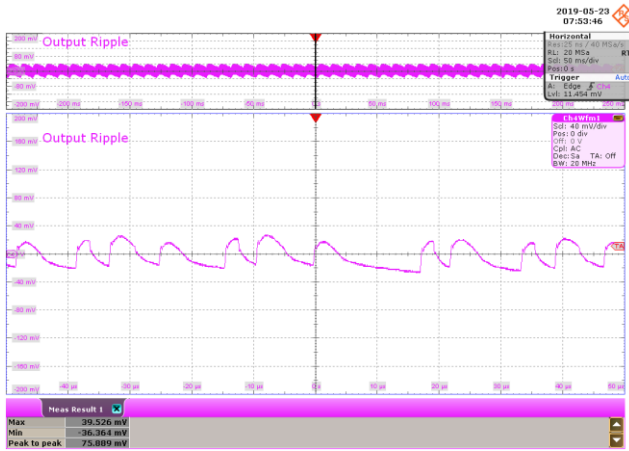
## 11.6.2.3    50% Load Condition
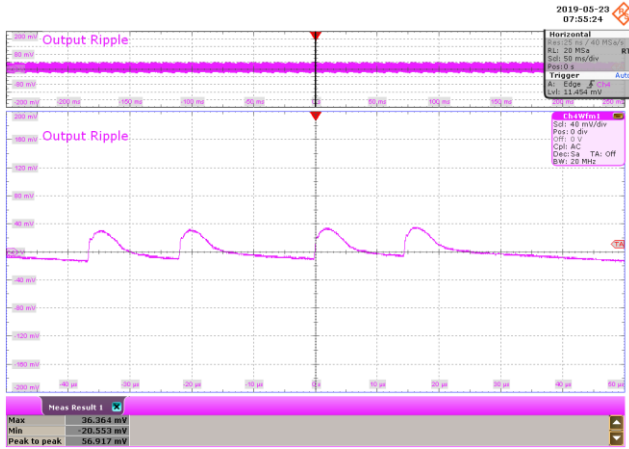


**Figure 113 –** 85 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
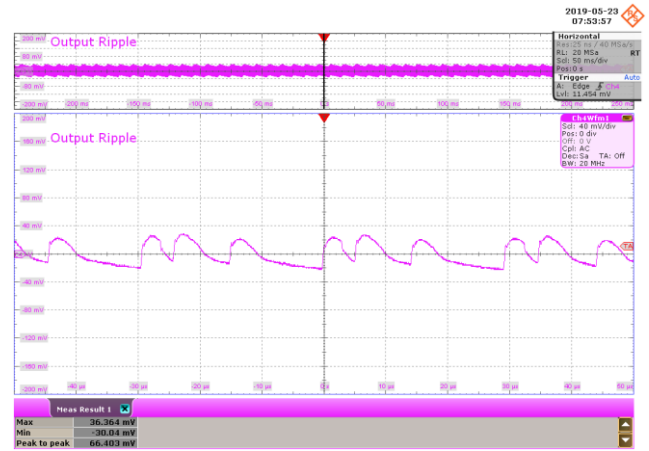Zoom: 10 μs / div.
Output Ripple = 56.917 mV.



**Figure 114 –** 115 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 56.917 mV.
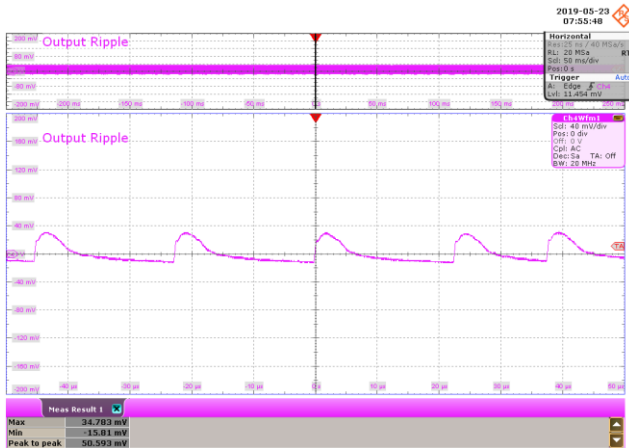


**Figure 115 –** 230 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 50.593 mV.
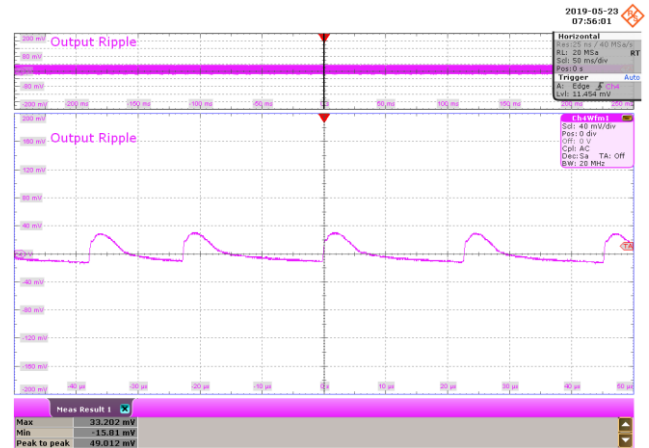


**Figure 116 –** 265 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 49.012 mV.

## 11.6.2.4    25% Load Condition
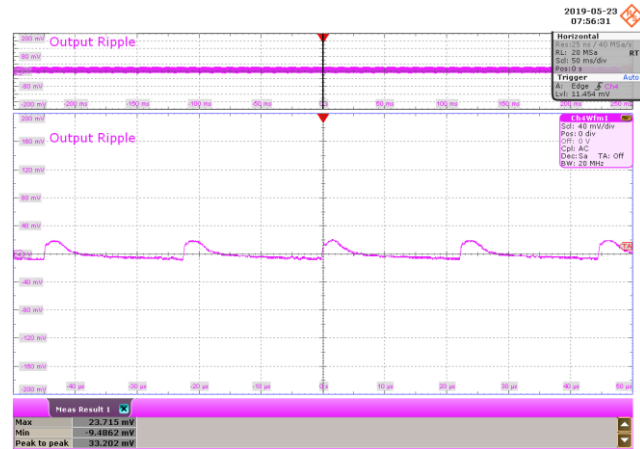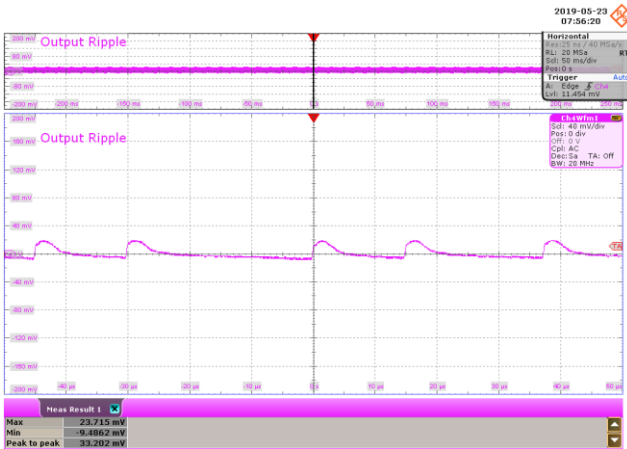


**Figure 117 –** 85 VAC 60 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 33.202 mV.



**Figure 118 –** 115 VAC 60 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 33.202 mV.
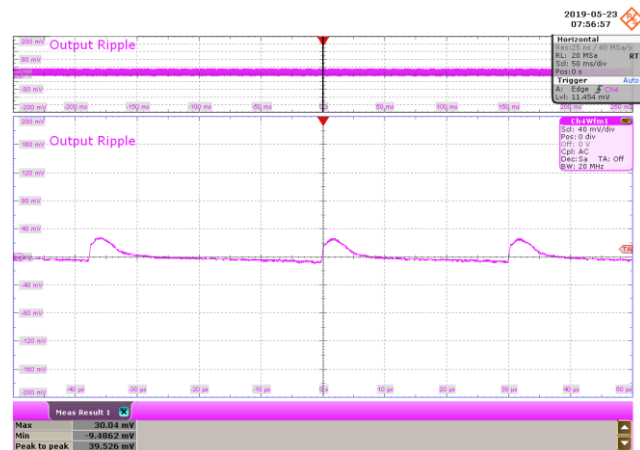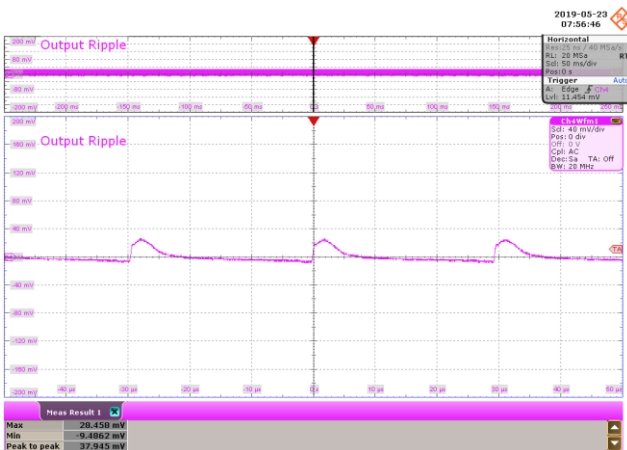


**Figure 119 –** 230 VAC 50 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 37.945 mV.



**Figure 120 –** 265 VAC 50 Hz.
CH4: V$_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 μs / div.
Output Ripple = 39.526 mV.

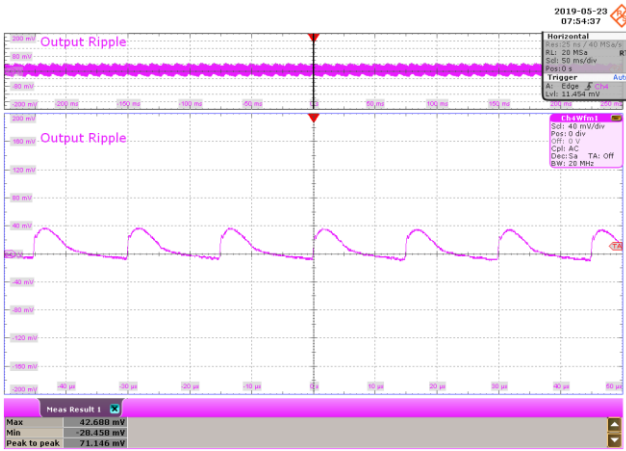## 11.6.2.5    0% Load Condition
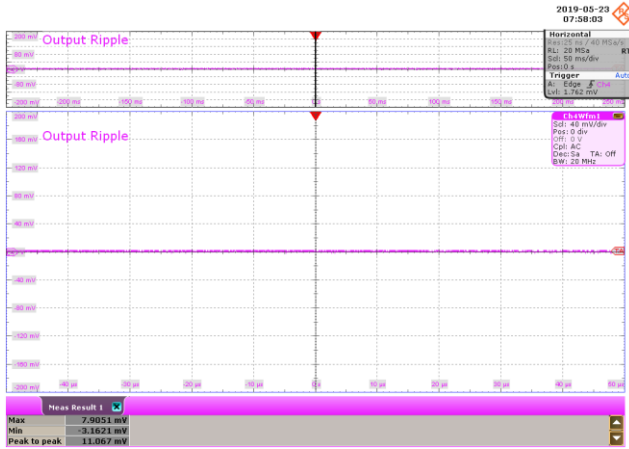


**Figure 121 –** 85 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 11.067 mV.
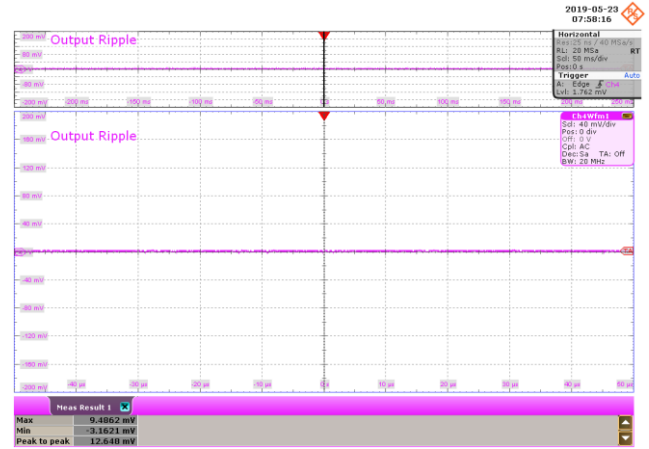


**Figure 122 –** 115 VAC 60 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 12.648 mV.
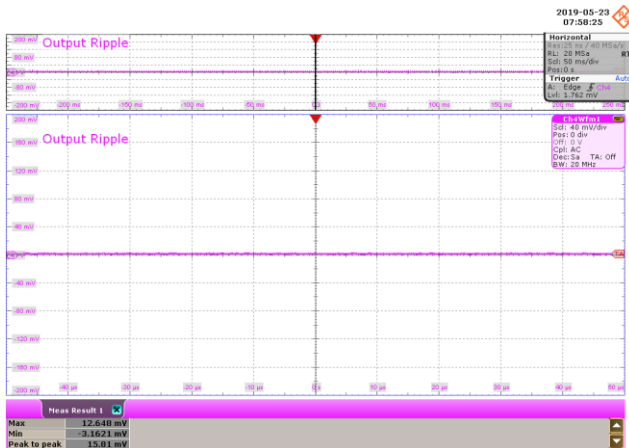


**Figure 123 –** 230 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 15.81 mV.
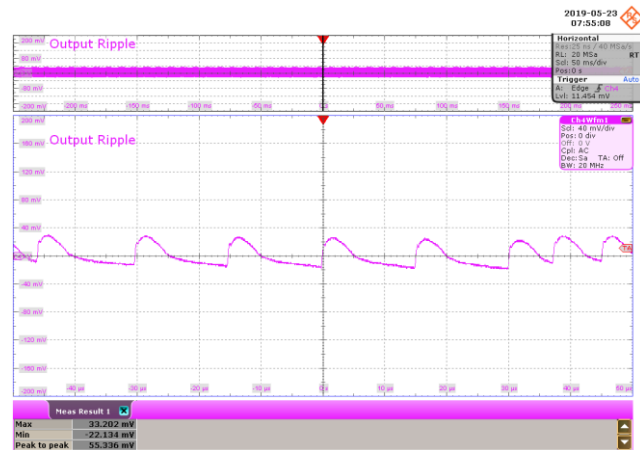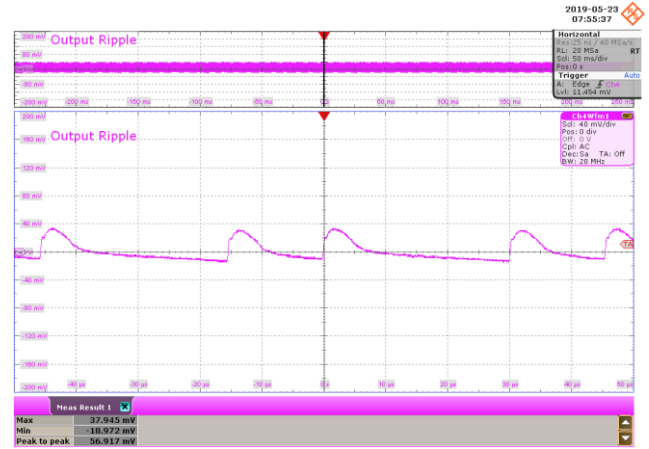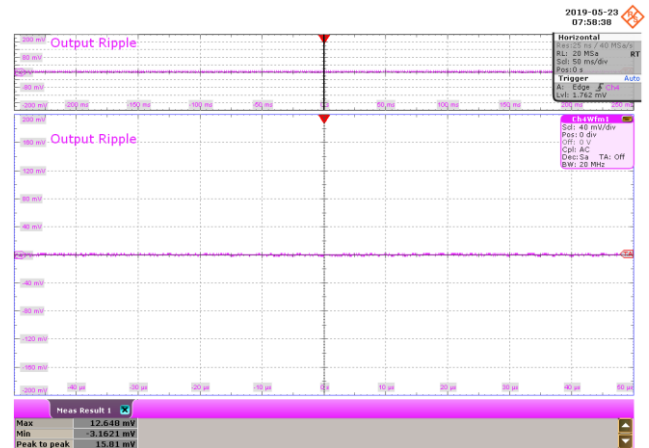


**Figure 124 –** 265 VAC 50 Hz.
CH4: $V_{OUT}$, 40 mV / div., 50 ms / div.
Zoom: 10 µs / div.
Output Ripple = 15.81 mV.

## 11.6.3    Output Ripple Voltage Graph from 0% - 100%
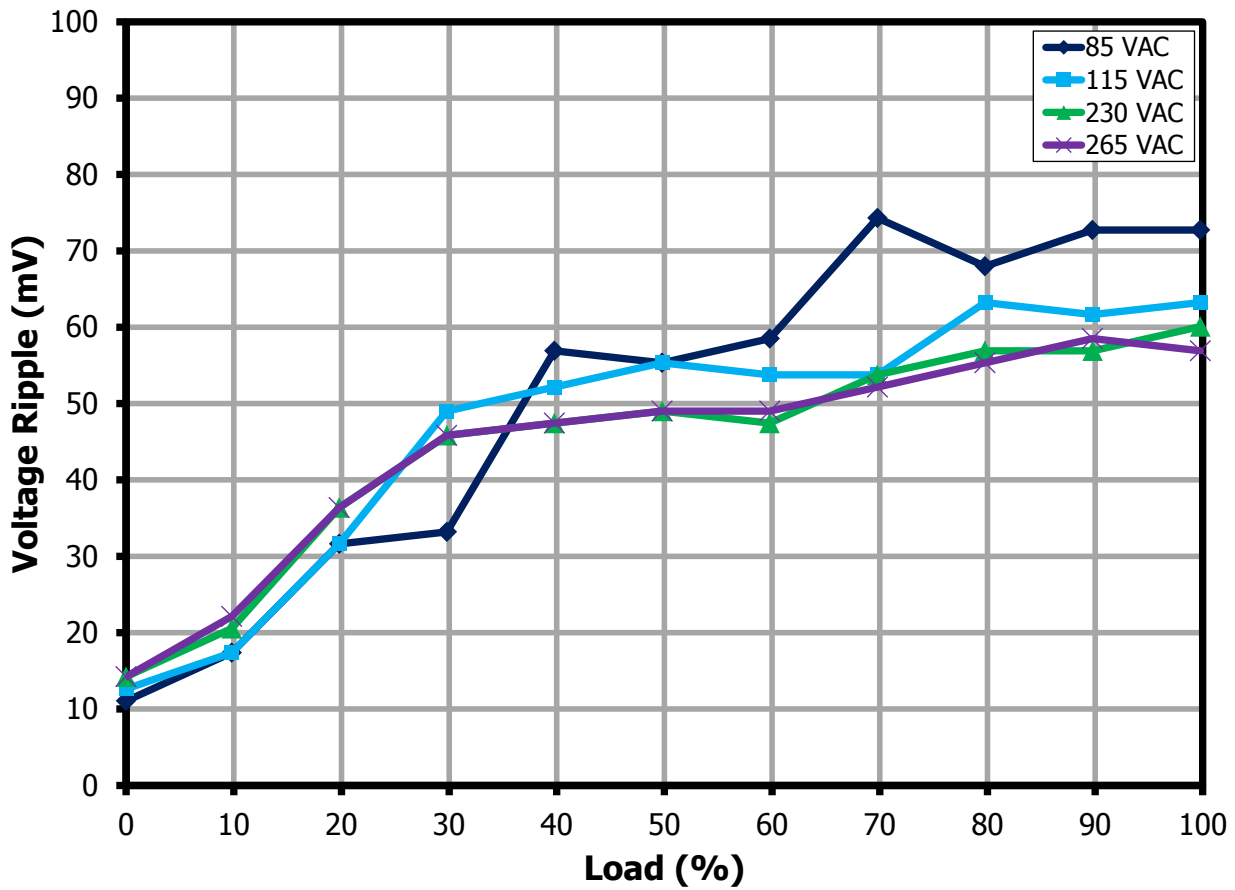


**Figure 125 –** Measured at the Board Output Terminals at Room Temperature.

## 12  **Thermal Performance**

### 12.1  *Test Set-Up*

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for two hours under full load conditions.

**Note:** In all thermal testing data, package D (SO-8C) was used instead of package P (DIP-8C).
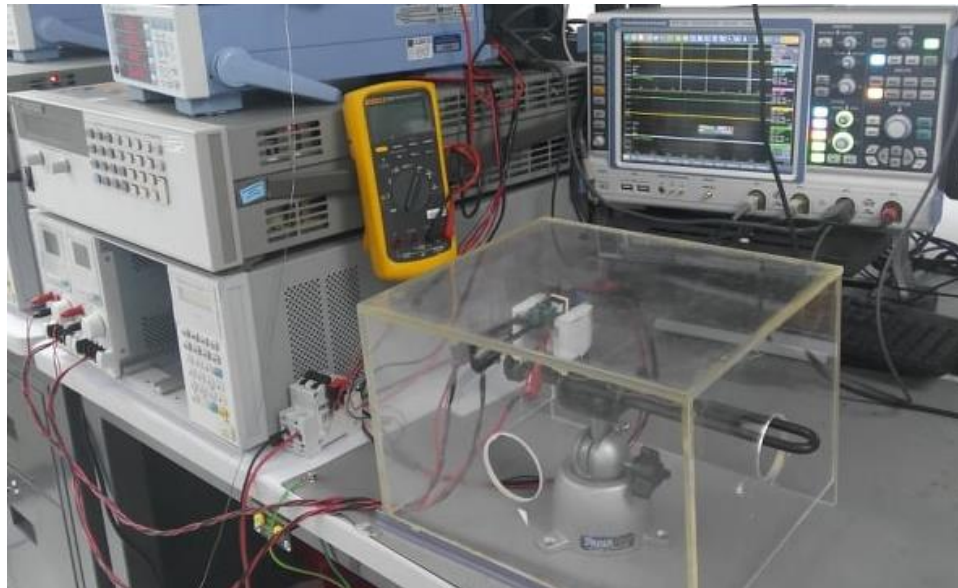


**Figure 126 –** Thermal Performance Set-up Using an Acrylic Box.



**Figure 127 –** Thermal Performance Set-up Using Thermal Chamber.

## 12.2    *Thermal Performance at Room Temperature*

### 12.2.1    85 VAC at room temperature
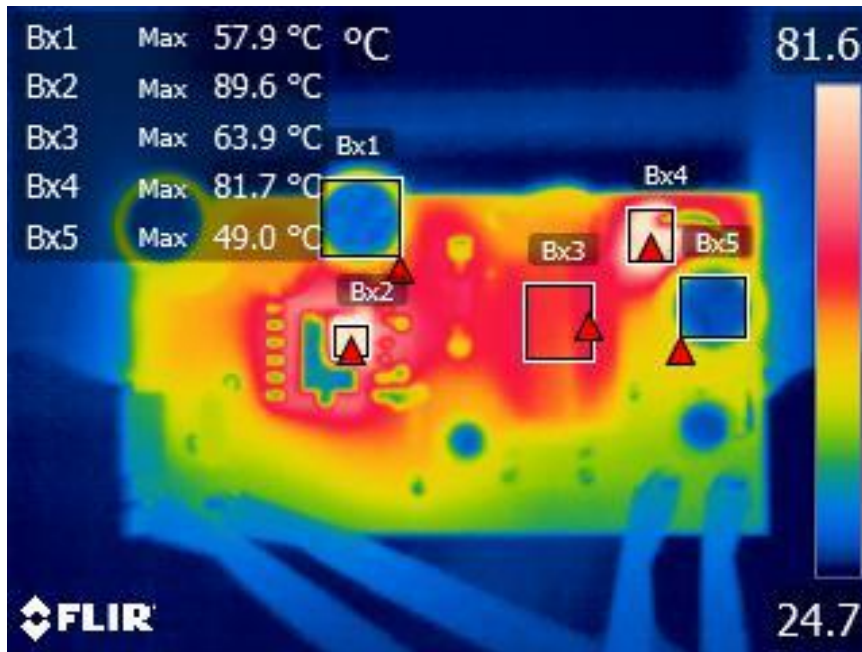


**Figure 128 –** Thermal Performance at 85 VAC, Full Load Using TNY288D.

| Component | Temperature (°C) |
|---|---|
| Input Capacitor (C2) | 57.9 |
| Transformer (T1) | 63.9 |
| TNY288 (U1) | 89.6 |
| Output Capacitor (C7) | 49.0 |
| Output Diode (D3) | 81.7 |
| Ambient | 26.0 |

## 12.2.2    265 VAC at Room Temperature
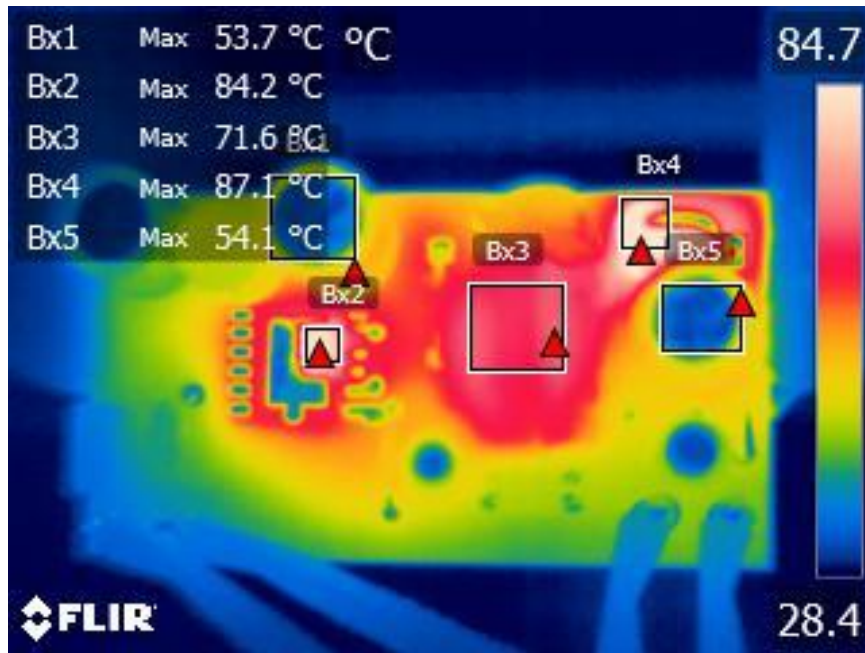


**Figure 129 –** Thermal Performance at 265 VAC, Full Load Using TNY288D.

| Component | Temperature (°C) |
|---|---|
| Input Capacitor (C2) | 53.7 |
| Transformer (T1) | 71.6 |
| TNY288 (U1) | 84.2 |
| Output Capacitor (C7) | 54.1 |
| Output Diode (D3) | 87.1 |
| Ambient | 26.5 |

## 12.3 *Thermal Performance at 50 °C*

### 12.3.1 85 VAC at 50 °C
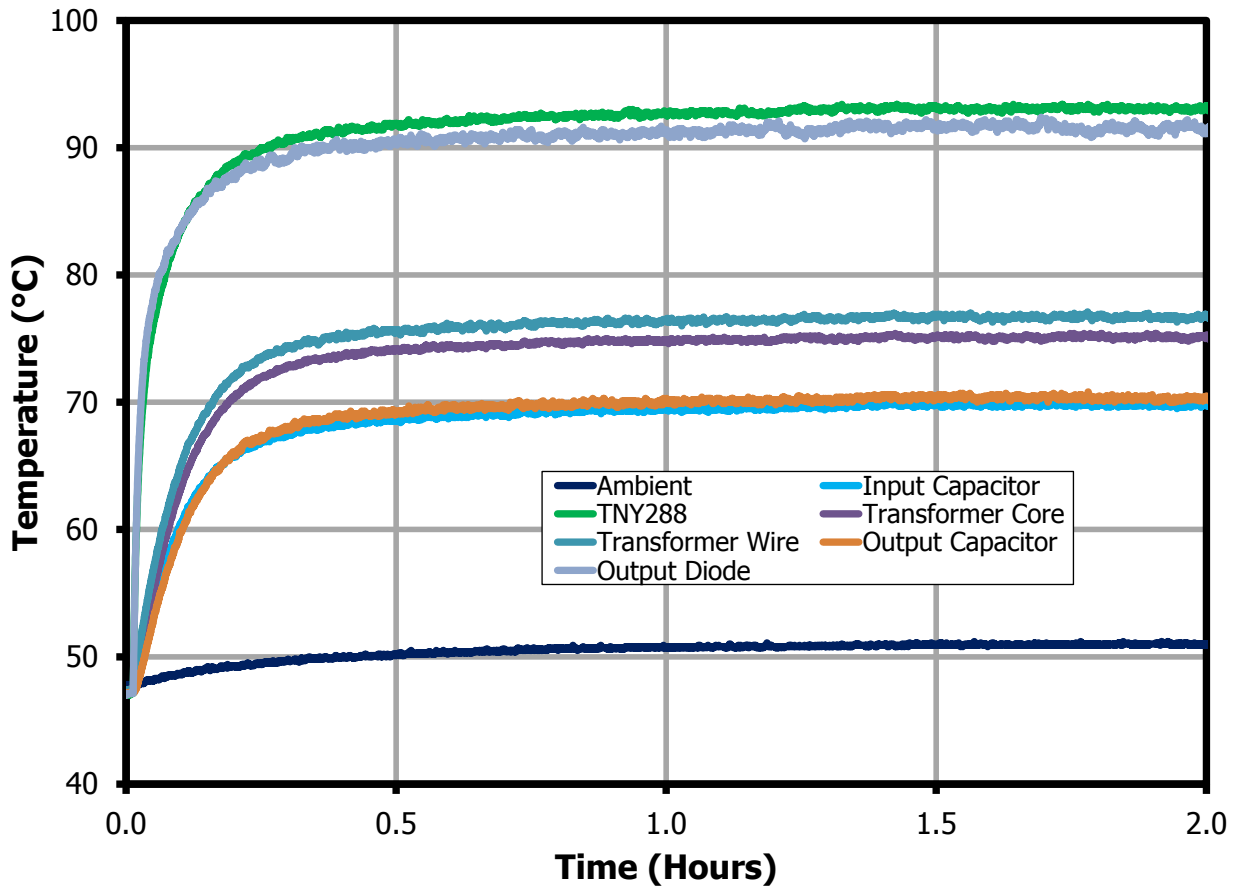


**Figure 130 –** Thermal Performance at 85 VAC, Full Load Using TNY288D.

| Component | Temperature (°C) |
|---|---|
| Ambient | 51.0 |
| Input Capacitor (C2) | 69.9 |
| TNY288 (U1) | 93.2 |
| Transformer Core (T1) | 75.2 |
| Transformer Wire (T1) | 76.6 |
| Output Capacitor (C7) | 70.3 |
| Output Diode (D3) | 91.6 |

## 12.3.2    265 VAC at 50 °C
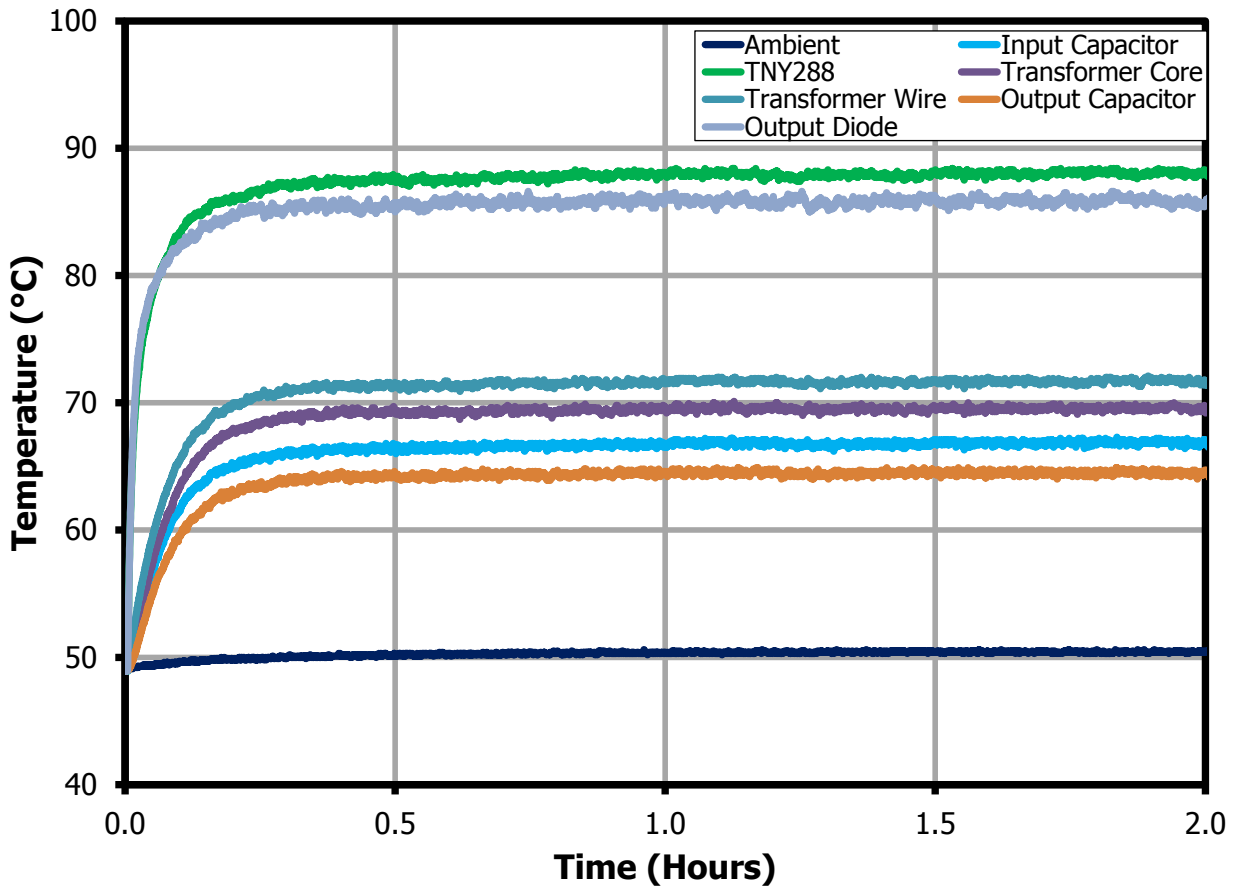


**Figure 131 –** Thermal Performance at 265 VAC, Full Load Using TNY288D.

| Component | Temperature (°C) |
|---|---|
| Ambient | 50.4 |
| Input Capacitor (C2) | 66.8 |
| TNY288 (U1) | 87.9 |
| Transformer Core (T1) | 69.5 |
| Transformer Wire (T1) | 71.5 |
| Output Capacitor (C7) | 64.2 |
| Output Diode (D3) | 85.8 |

## 12.4   *Over Temperature Protection*

### 12.4.1   OTP at 85 VAC
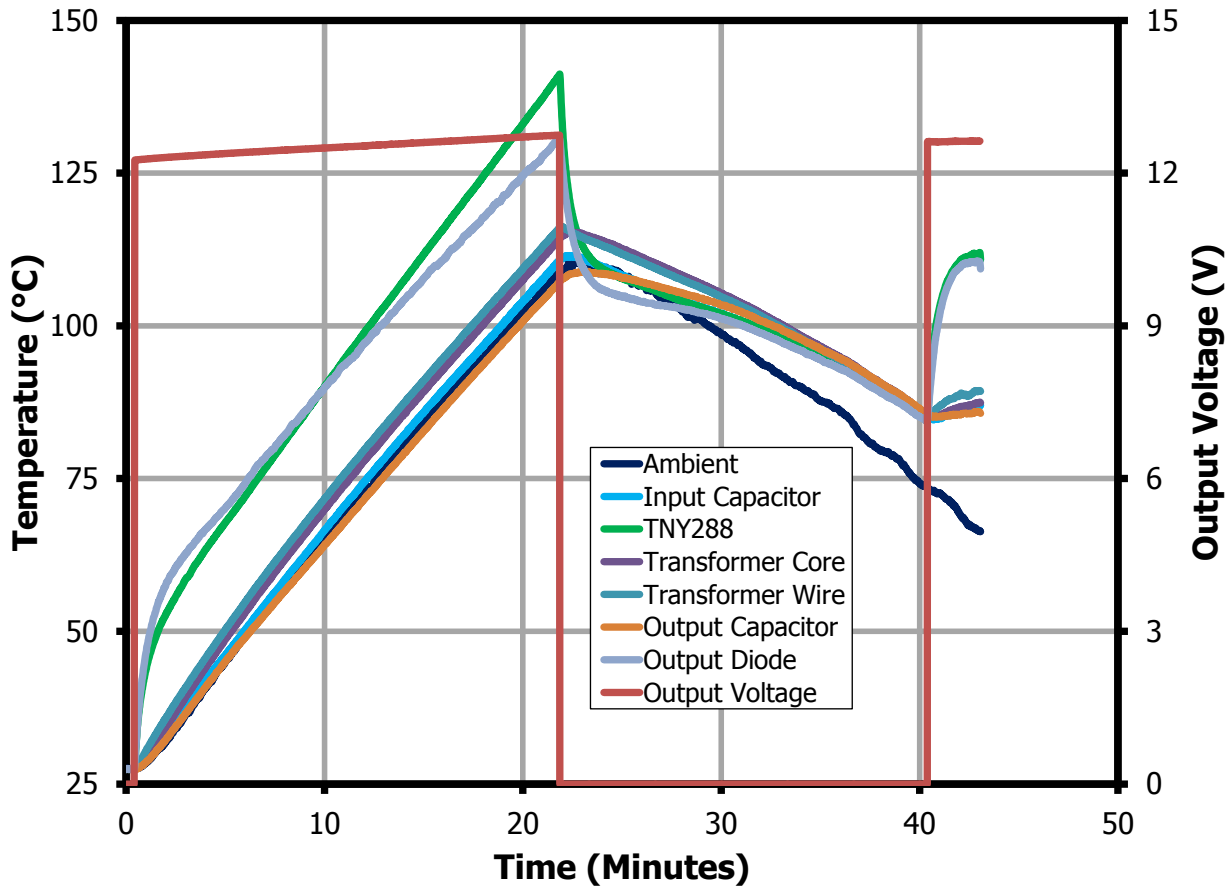


**Figure 132 –** Over Temperature Protection at 85 VAC Using TNY288D.

| Component | At OTP Trigger Temperature (°C) | At Recovery Temperature (°C) |
|---|---|---|
| Ambient | 109.2 | 73.5 |
| Input Capacitor (C2) | 110.7 | 84.9 |
| TNY288 (U1) | 141.2 | 84.6 |
| Transformer Core (T1) | 114.2 | 85.5 |
| Transformer Wire (T1) | 116.0 | 85.3 |
| Output Capacitor (C7) | 107.2 | 85.5 |
| Output Diode (D3) | 130.6 | 84.6 |

## 12.4.2    OTP at 265 VAC
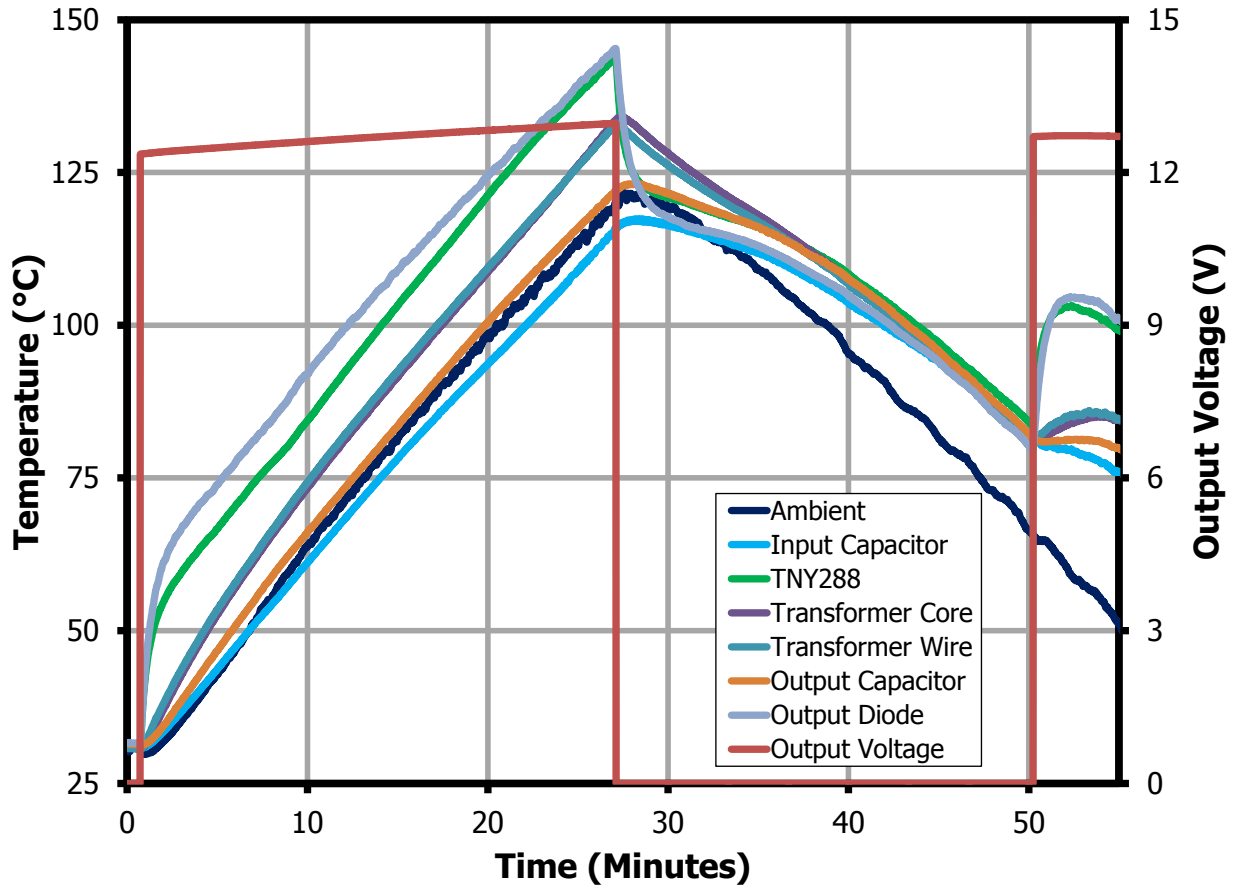


**Figure 133 –** Over Temperature Protection at 265 VAC using TNY288D.

| Component | At OTP Trigger Temperature (°C) | At Recovery Temperature (°C) |
|---|---|---|
| Ambient | 120.3 | 65.8 |
| Input Capacitor (C2) | 115.9 | 81.3 |
| TNY288 (U1) | 144.0 | 83.5 |
| Transformer Core (T1) | 133.6 | 81.4 |
| Transformer Wire (T1) | 133.0 | 81.2 |
| Output Capacitor (C7) | 122.1 | 81.7 |
| Output Diode (D3) | 145.3 | 79.5 |

## 13   Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V, 1 A). Measurements were taken with an Artificial Hand connected and a floating DC output load resistor. A DC output cable was included.

### 13.1   *Test Set-up Equipment*

#### 13.1.1   Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.

### 13.2   *Test Set-up*
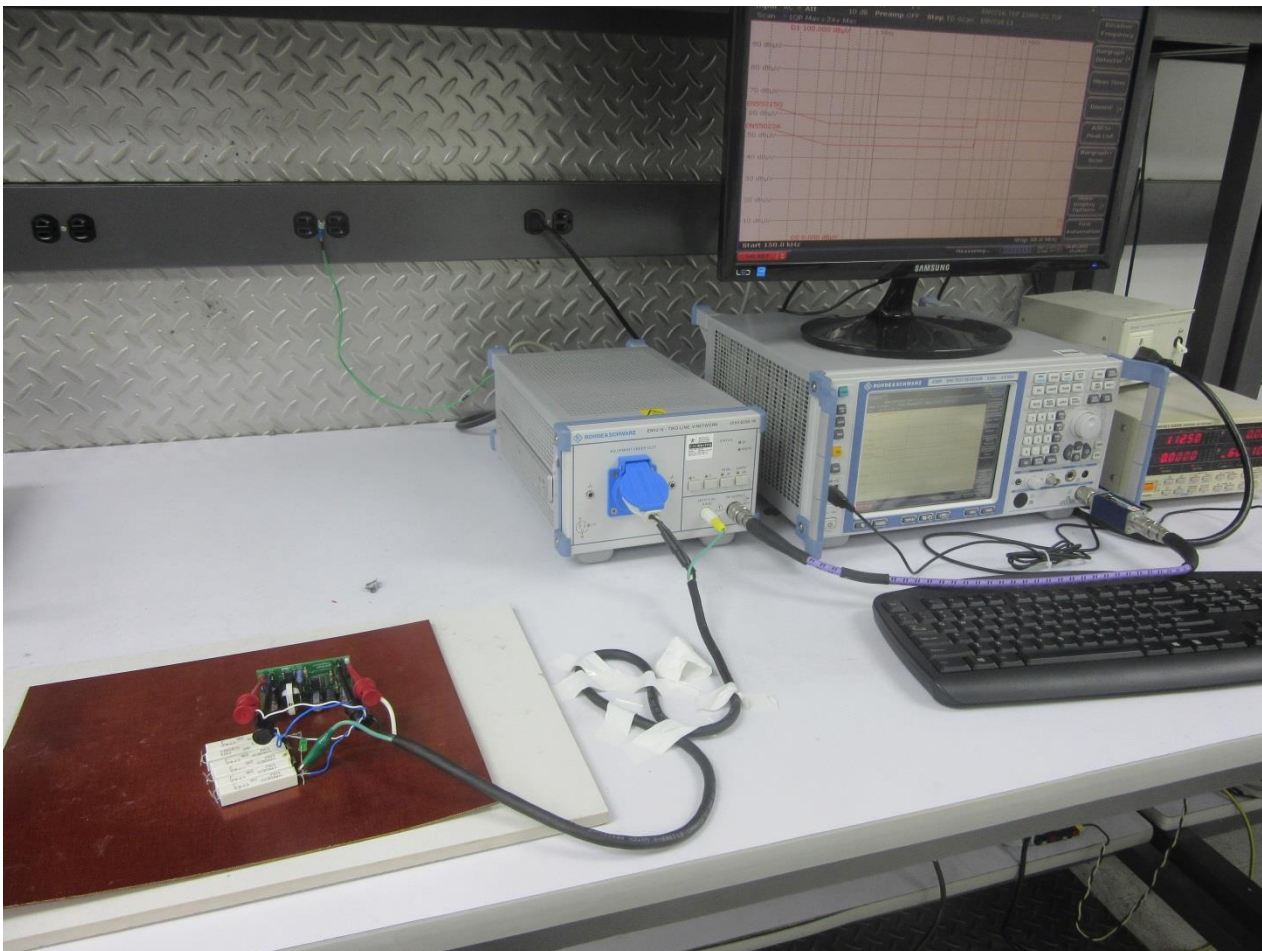


**Figure 134 –** EMI Test Set-up.

### 13.3  *Test Results*
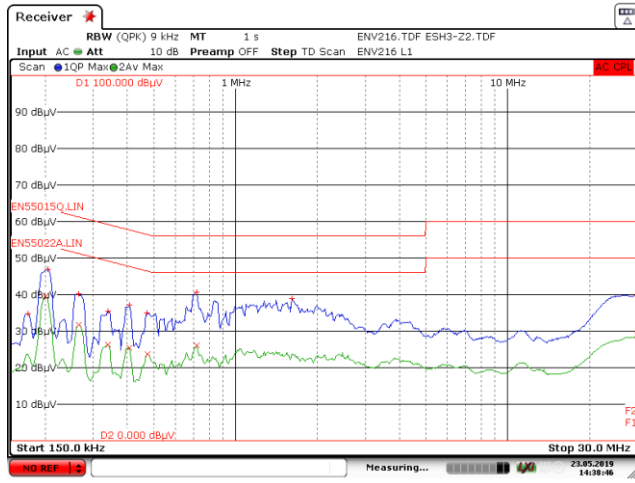


**Figure 135 –** 115 VAC 60 Hz, Line with Artificial Hand.
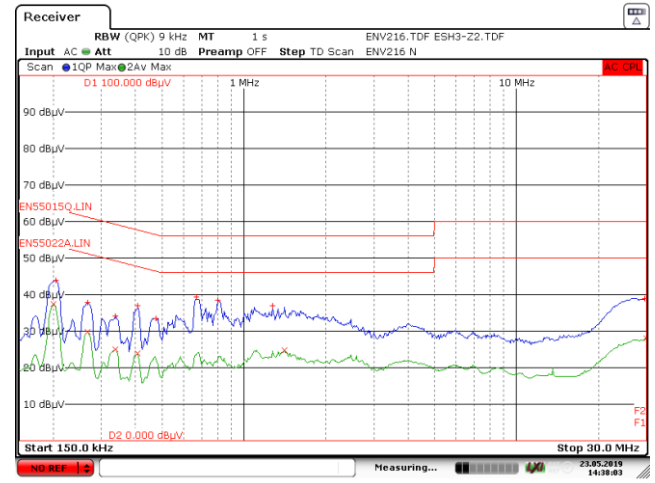


**Figure 136 –** 115 VAC 60 Hz, Neutral with Artificial Hand.
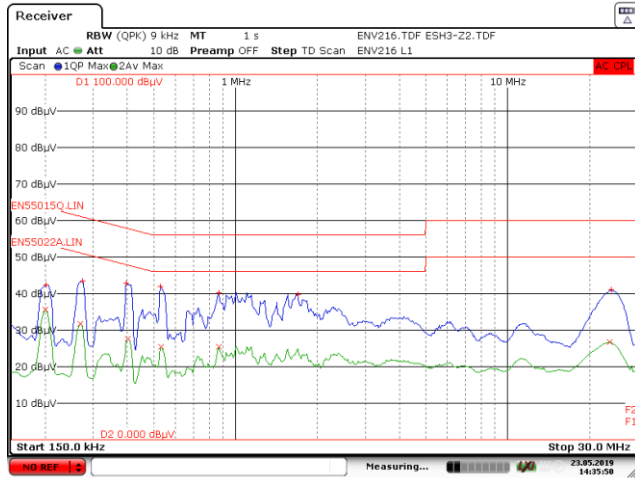


**Figure 137 –** 230 VAC 60 Hz, Line with Artificial Hand.
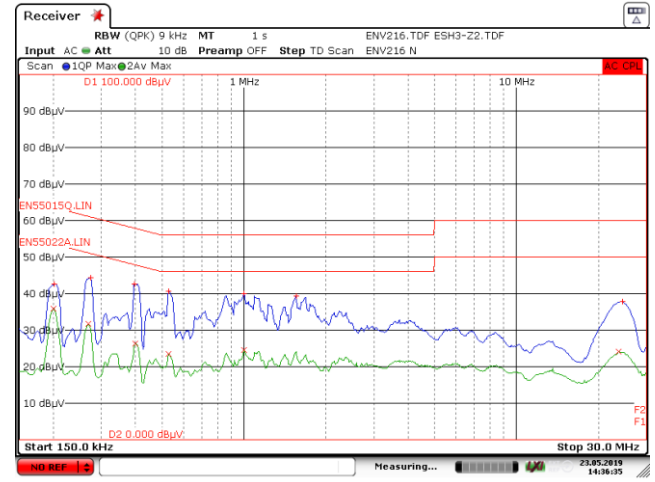


**Figure 138 –** 230 VAC 60 Hz, Neutral with Artificial Hand.

## 14   Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

### 14.1   *Differential and Common Mode Surge*

| DM Surge Level (V) | Input Voltage (VAC) | Injection Location | Injection Phase (º) | Test Result (Pass/Fail) |
|---|---|---|---|---|
| +1000 | 230 | L to N | 0 | Pass |
| -1000 | 230 | L to N | 0 | Pass |
| +1000 | 230 | L to N | 90 | Pass |
| -1000 | 230 | L to N | 90 | Pass |
| +1000 | 230 | L to N | 180 | Pass |
| -1000 | 230 | L to N | 180 | Pass |
| +1000 | 230 | L to N | 270 | Pass |
| -1000 | 230 | L to N | 270 | Pass |

| CM Surge Level (V) | Input Voltage (VAC) | Injection Location | Injection Phase (º) | Test Result (Pass/Fail) |
|---|---|---|---|---|
| +2000 | 230 | L, N to PE | 0 | Pass |
| -2000 | 230 | L, N to PE | 0 | Pass |
| +2000 | 230 | L, N to PE | 90 | Pass |
| -2000 | 230 | L, N to PE | 90 | Pass |
| +2000 | 230 | L, N to PE | 180 | Pass |
| -2000 | 230 | L, N to PE | 180 | Pass |
| +2000 | 230 | L, N to PE | 270 | Pass |
| -2000 | 230 | L, N to PE | 270 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

**Figure 139 –** DM Surge.
$V_{DS(MAX)}$ = 702 V.



**Figure 140 –** CM Surge.
$V_{DS(MAX)}$ = 613 V

## 14.2  *Ring Wave*

| Surge Level (V) | Input Voltage (VAC) | Injection Location | Injection Phase (º) | Test Result (Pass/Fail) |
|---|---|---|---|---|
| +3000 | 230 | L, N to PE | 0 | Pass |
| -3000 | 230 | L, N to PE | 0 | Pass |
| +3000 | 230 | L, N to PE | 90 | Pass |
| -3000 | 230 | L, N to PE | 90 | Pass |
| +3000 | 230 | L, N to PE | 180 | Pass |
| -3000 | 230 | L, N to PE | 180 | Pass |
| +3000 | 230 | L, N to PE | 270 | Pass |
| -3000 | 230 | L, N to PE | 270 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

### 14.3  *Electrical Fast Transient (EFT)*

| Surge Level (V) | Injection Phase (°) | Frequency | T-Burst | T-Rep | Test Duration | Injection Location | Result (PASS,FAIL,AR) |
|---|---|---|---|---|---|---|---|
| +4000 | 0 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 0 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 0 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 0 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 0 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |
| -4000 | 0 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |
| +4000 | 90 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 90 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 90 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 90 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 90 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |
| -4000 | 90 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |
| +4000 | 270 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 270 | 2.5 kHz | 30 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 270 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| -4000 | 270 | 5 kHz | 15 ms | 300 ms | 120 s | L to N | Pass |
| +4000 | 270 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |
| -4000 | 270 | 100 kHz | 750 $\mu$s | 300 ms | 120 s | L to N | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

## 15  **ESD**

Passed ±8 kV contact discharge

| Contact Voltage (kV) | Applied to | Number of Strikes | Test Result |
|---|---|---|---|
| +8 | +12 V terminal | 10 | Pass |
| | RTN terminal | 10 | Pass |
| -8 | +12 V terminal | 10 | Pass |
| | RTN terminal | 10 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

Passed ±15 KV Air discharge.

| Air Discharge Voltage (kV) | Applied to | Number of Strikes | Test Result |
|---|---|---|---|
| +15 | +12 V terminal | 10 | Pass |
| | RTN terminal | 10 | Pass |
| -15 | +12 V terminal | 10 | Pass |
| | RTN terminal | 10 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

## 16  **Revision History**

| Date | Author | Revision | Description and Changes | Reviewed |
|---|---|---|---|---|
| 16-Jul-19 | JPB | 1.0 | Initial Release. | Apps & Mktg |
| 13-Aug-19 | JPB | 1.1 | Added output short circuit (11.5.2) and overload (11.5.3) | Apps & Mktg |
| 29-Jul-20 | KM | 1.2 | Added Supplier for T1. | Apps & Mktg |
|  |  |  |  |  |

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