Display Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 240128E FGH-PW

Product Specification ***Version: 2***

26.12.2018

GENERAL SPECIFICATION

MODULE NO. :

DEM 240128E FGH-PW

CUSTOMER P/N:

Version No.	Change Description	Date
0	First Issue	30.10.2009
1.0	Change Production Line	31.10.2018
1.1	Update the module drawing/BL drawing on page4/page5/page7	01.11.2018
2	Correct the BL circuit on page 7	26.12.2018

PREPARED BY: PS **DATE:** 26.12.2018

APPROVED BY: MHI **DATE:** 26.12.2018

CONTENTS

1. FUNCTIONS & FEATURES

- DEM 240128E FGH-PW LCD Type :

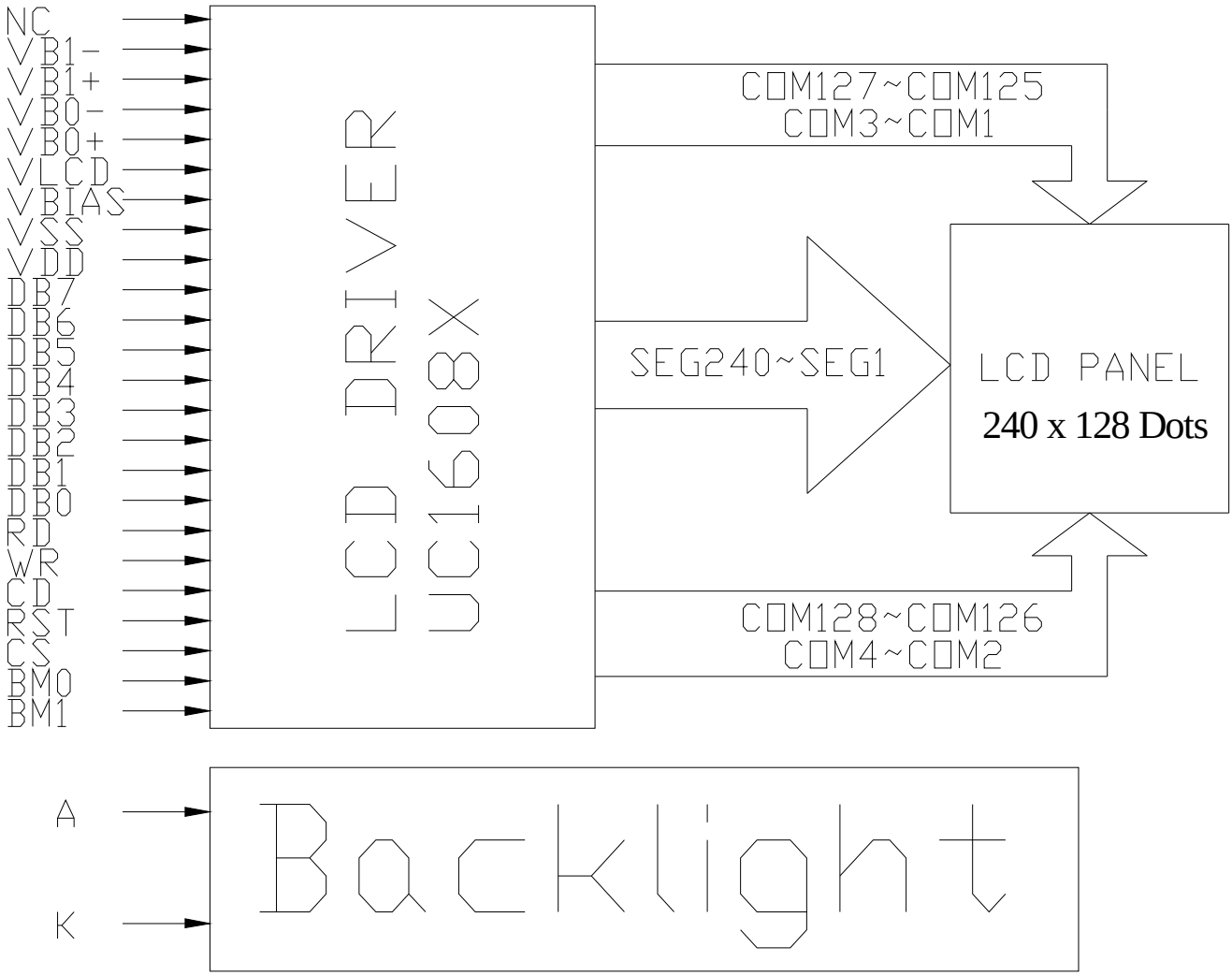
Module	LCD Type	Remark
DEM 240128E FGH-PW	FSTN Transflective Positive	---

- Viewing Direction : 6 O'clock
- Driving Scheme : 1/128 Duty Cycle, 1/12 Bias
- Power Supply Voltage : 3.3Volt (typ.)
- LCD Driving Voltage : 14.5Volt (typ.)
- Driver IC : UC1608X
- Display Contents : 240 x 128 Dots
- Lightguide: RGB

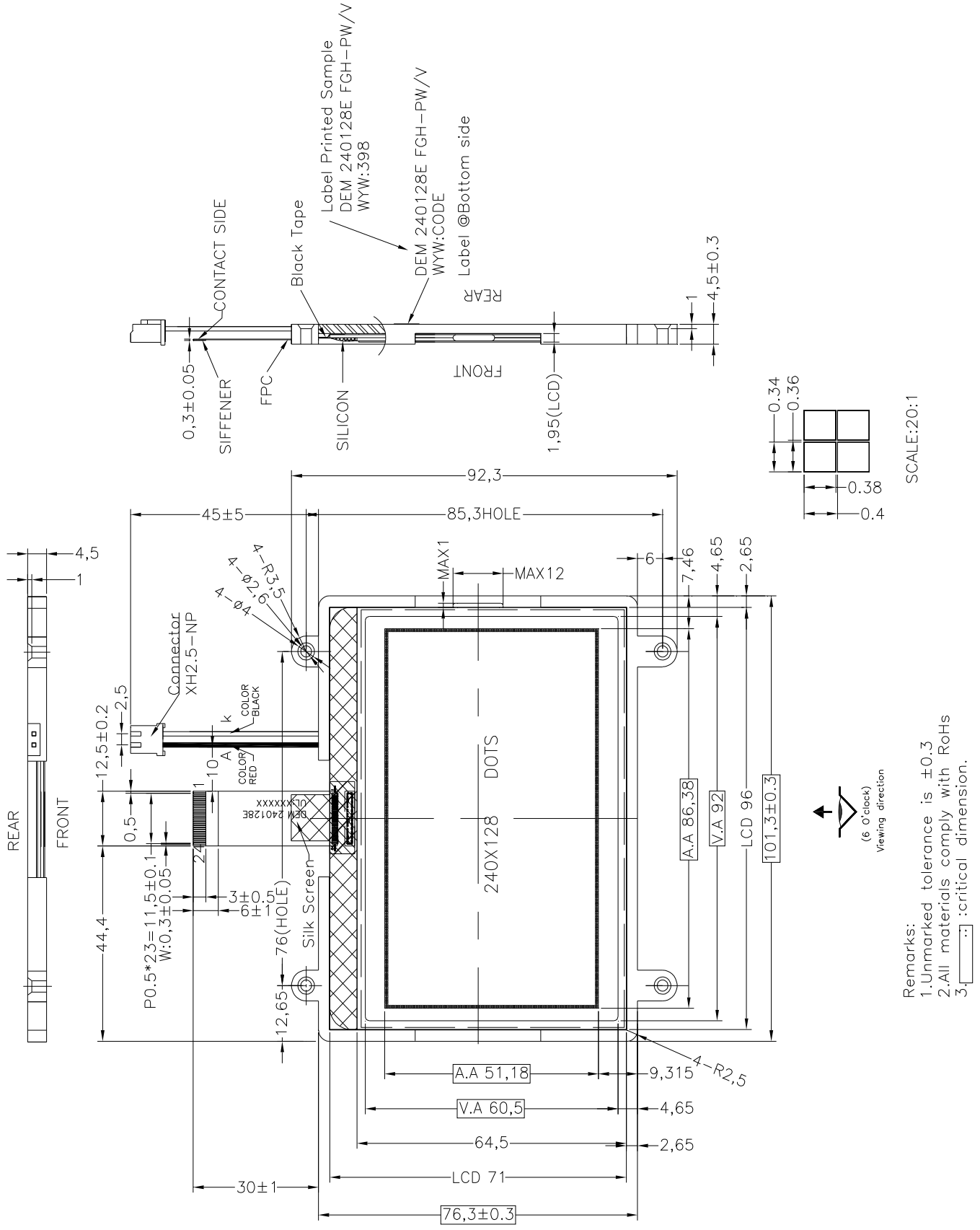
2. MECHANICAL SPECIFICATIONS

- Module Size : 101.30 x 92.30 x 4.50max. mm
- View Area Size : 92.00 x 60.50 mm
- Active Area Size : 86.38 x 51.18 mm
- Dot Size : 0.34 x 0.38 mm
- Dot Gap : 0.02mm

3. BLOCK DIAGRAM



4. EXTERNAL DIMENSIONS

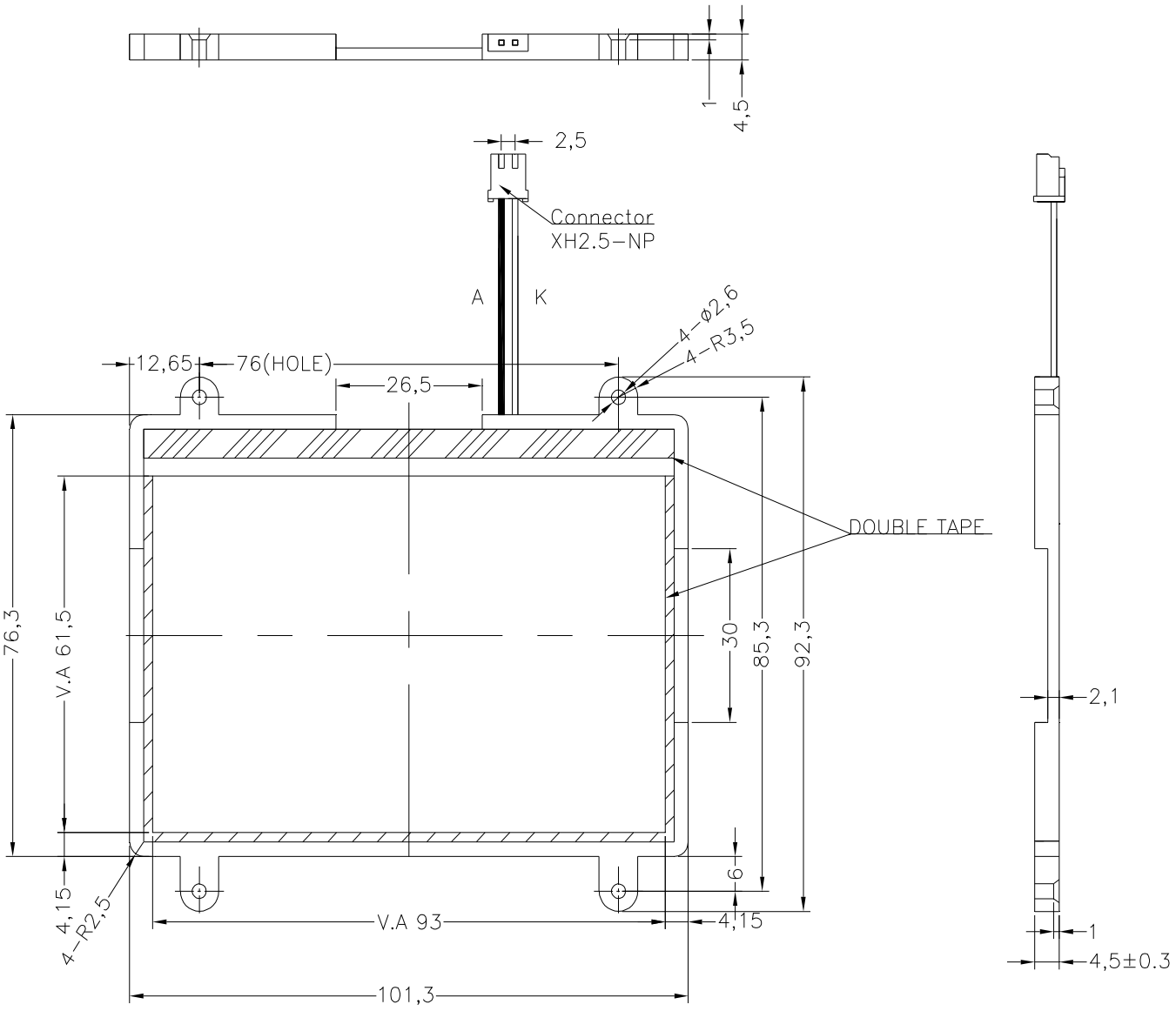


5. PIN DESCRIPTION

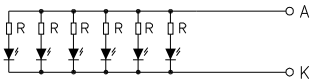
<table>
<tr><th>Pin No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>No Connect</td></tr>
<tr><td>2</td><td>VB1-</td><td rowspan="4">LCD Bias Voltages. These are the voltage source to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX between VBX+ and VBX–.</td></tr>
<tr><td>3</td><td>VB1+</td></tr>
<tr><td>4</td><td>VB0-</td></tr>
<tr><td>5</td><td>VB0+</td></tr>
<tr><td>6</td><td>VLCD</td><td>Main LCD Power Supply. Connect these pins together.</td></tr>
<tr><td>7</td><td>VBIAS</td><td>This is the reference voltage to generate the actual SEG driving</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground input</td></tr>
<tr><td>9</td><td>VDD</td><td>Power supply input.</td></tr>
<tr><td>10</td><td>DB7</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table><tr><th></th><th>BM=1x (Parallel)</th><th>BM=0x (Parallel)</th><th>BM=01 (S9)</th><th>BM=00 (S8/S8uc)</th></tr><tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr><tr><td>D1</td><td>D1</td><td>D1/D5</td><td>–</td><td>–</td></tr><tr><td>D2</td><td>D2</td><td>D2/D6</td><td>–</td><td>–</td></tr><tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr><tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr><tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr><tr><td>D6</td><td>D6</td><td>–</td><td>S9</td><td>S8/S8uc</td></tr><tr><td>D7</td><td>D7</td><td>0</td><td>1</td><td>1</td></tr></table>Connect unused pins to VDD or VSS.</td></tr>
<tr><td>11</td><td>DB6</td></tr>
<tr><td>12</td><td>DB5</td></tr>
<tr><td>13</td><td>DB4</td></tr>
<tr><td>14</td><td>DB3</td></tr>
<tr><td>15</td><td>DB2</td></tr>
<tr><td>16</td><td>DB1</td></tr>
<tr><td>17</td><td>DB0</td></tr>
<tr><td>18</td><td>RD(WR1)</td><td rowspan="2">These terminals controls the read/write operation of host interface
<table><tr><td></td><td>8080</td><td>6800</td><td>Serial</td></tr><tr><td>WR</td><td>/RW</td><td>R/W</td><td>0</td></tr><tr><td>(RD)WR1</td><td>/RD</td><td>EN</td><td>0</td></tr></table></td></tr>
<tr><td>19</td><td>WR</td></tr>
<tr><td>20</td><td>CD</td><td>Select Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect CD to VSS when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>21</td><td>RST</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1608 has built-in Power-ON-Reset and Software Reset command, RST pin is not required for proper chip operation. When RST is not used, connect the pin to VDD.</td></tr>
<tr><td>22</td><td>CS</td><td>Chip Select. The chip is selected when CS=”H”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>23</td><td>BM0</td><td rowspan="2">Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:
<table><tr><th>BM[1:0]</th><th>D[7:6]</th><th>Mode</th></tr><tr><td>11</td><td>Data</td><td>6800/8bit</td></tr><tr><td>10</td><td>Data</td><td>8080/8bit</td></tr><tr><td>01</td><td>0X</td><td>6080/4bit</td></tr><tr><td>00</td><td>0X</td><td>8080/4bit</td></tr><tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr><tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr><tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr></table></td></tr>
<tr><td>24</td><td>BM1</td></tr>
</table>

6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATION

ELECTRICAL–OPTICAL CHARACTERISTICS						
Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Curret	Vf	–	90	110	mA	If= 3.5 V
Power Dissipation	Pd	–	315	385	mW	If= 3.5 V
Luminous Uniformity	ΔLv	70			%	MIN/MAX*100%
Luminance	Lv	300	380		cd/m²	If= 3.5 V T=25°C
Color Coordinate	X	0.27		0.31		
	Y	0.26		0.30		
Lifetime			50000HOURS			



REMARKS:
1.UNMARKED TOLERANCE: ±0.30
2.COLOR: WHITE
3.THE MATERIAL COMPLY WITH RoHs



7. ABSOLUTE MAXIMUM RATINGS

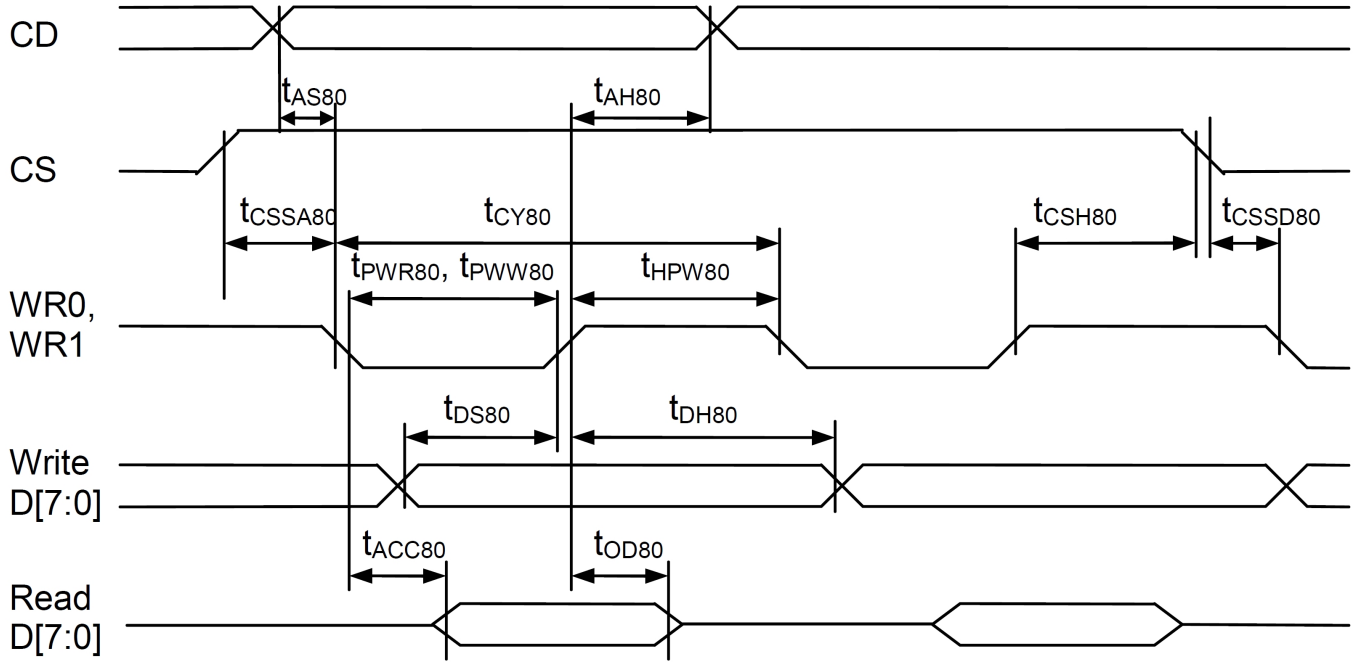
Parameter	Symbol	Conditions	Unit
Logic Supply Voltage	V_{DD}	-0.3 ~ 4.0	V
LCD Generator Supply Voltage	V_{DD2}	-0.3 ~ 4.0	V
Analog Circuit Supply Voltage	V_{DD3}	-0.3 ~ 4.0	V
Voltage Difference Between VDD and VDD2/3	$V_{DD2/3}$-V_{DD}	1.6Max	V
LCD Generated Voltage	V_{LCD}	-0.3~+17.0	V
Any Input Voltage	V_{IN}	-0.4~V_{DD}+0.5	V
Operating Temperature Range	T_{OPR}	-20~+70	℃
Storage Temperature	T_{STR}	-30~+80	℃

8. DC CHARACTERISTICS

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{DD}		3.0	3.3	3.3	V
LCD Supply Voltage	V_{OP}		14.2	14.5	14.8	V
Supply Current	I_{DD}		---	TBD	---	uA

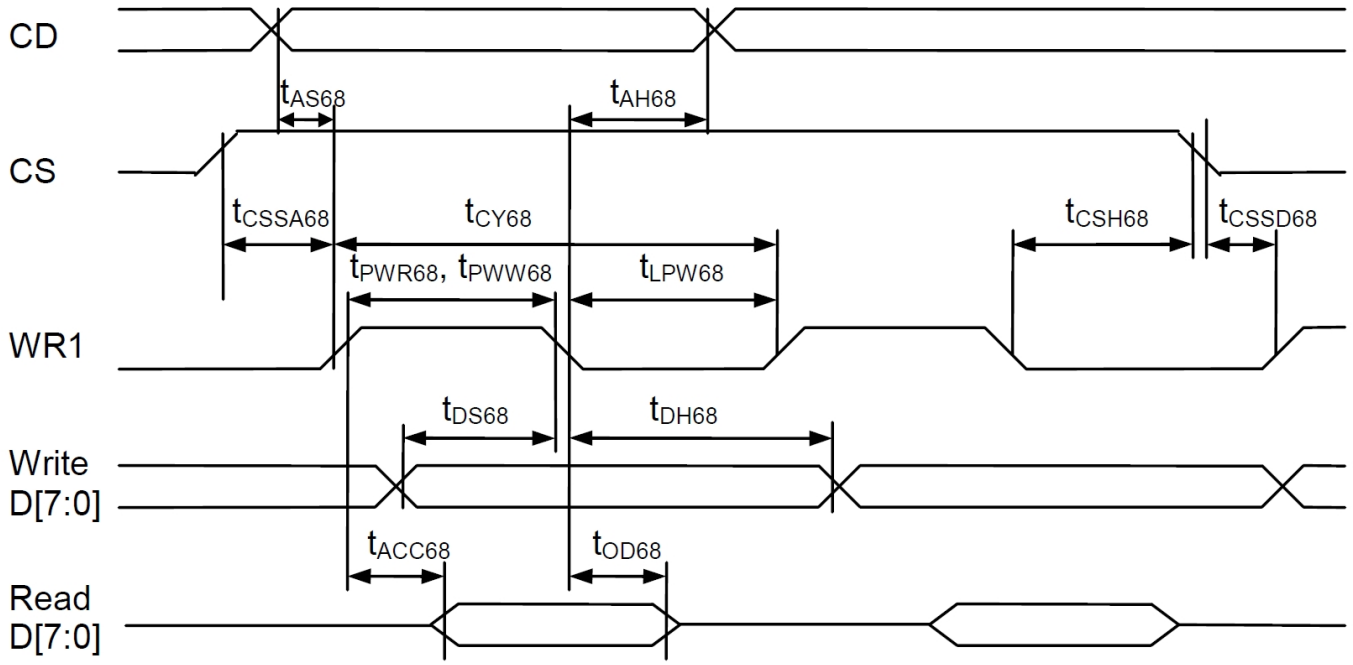
9. AC ELECTRICAL CHARACTERISTICS

Parallel Bus Timing Characteristics (for 8080 MCU)



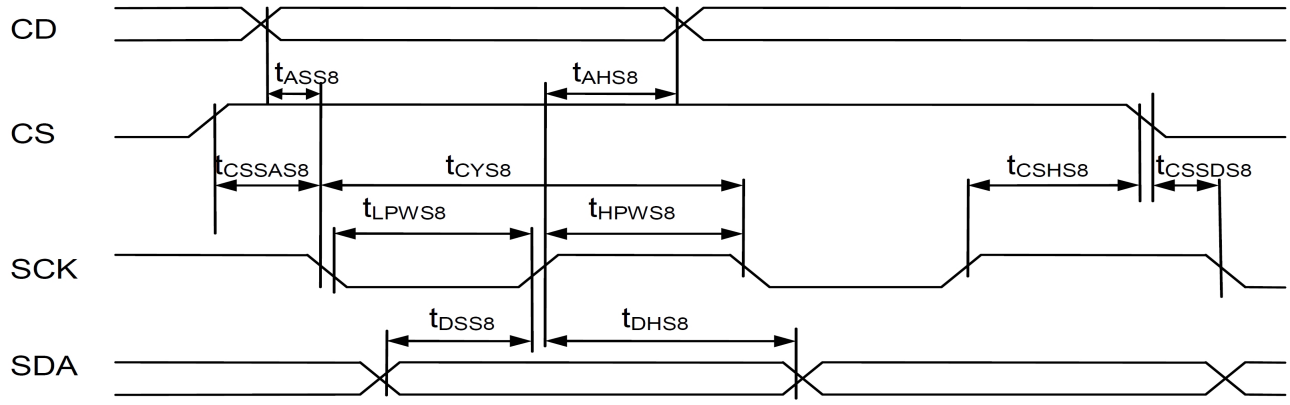
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 20	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 140 140 140	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 65	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 12	60 20	nS
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS

Parallel Bus Timing Characteristics (for 6800 MCU)



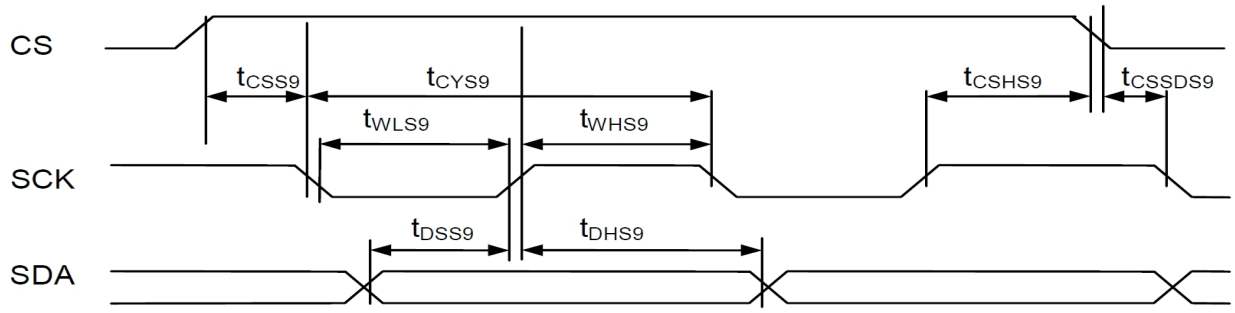
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	nS
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 140 140 140	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 65	 –	 nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 12	60 20	nS
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

Serial Bus Timing Characteristics (for S8)



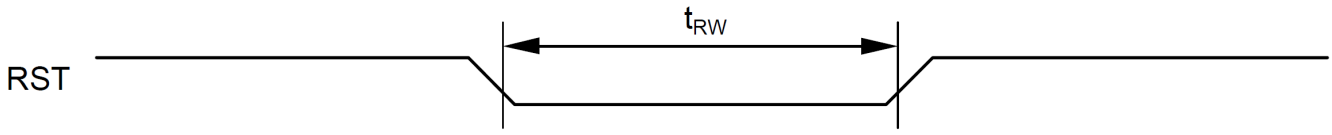
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		20	–	nS
t_{CYS8}	SCK	System cycle time		140	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS	Chip select setup time		10 20 10		nS

Serial Bus Timing Characteristics (for S9)



Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		140	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS	Chip select setup time		10 20 10		nS

Reset Characteristics



Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1000	–	nS

10. INSTRUCTION TABLE

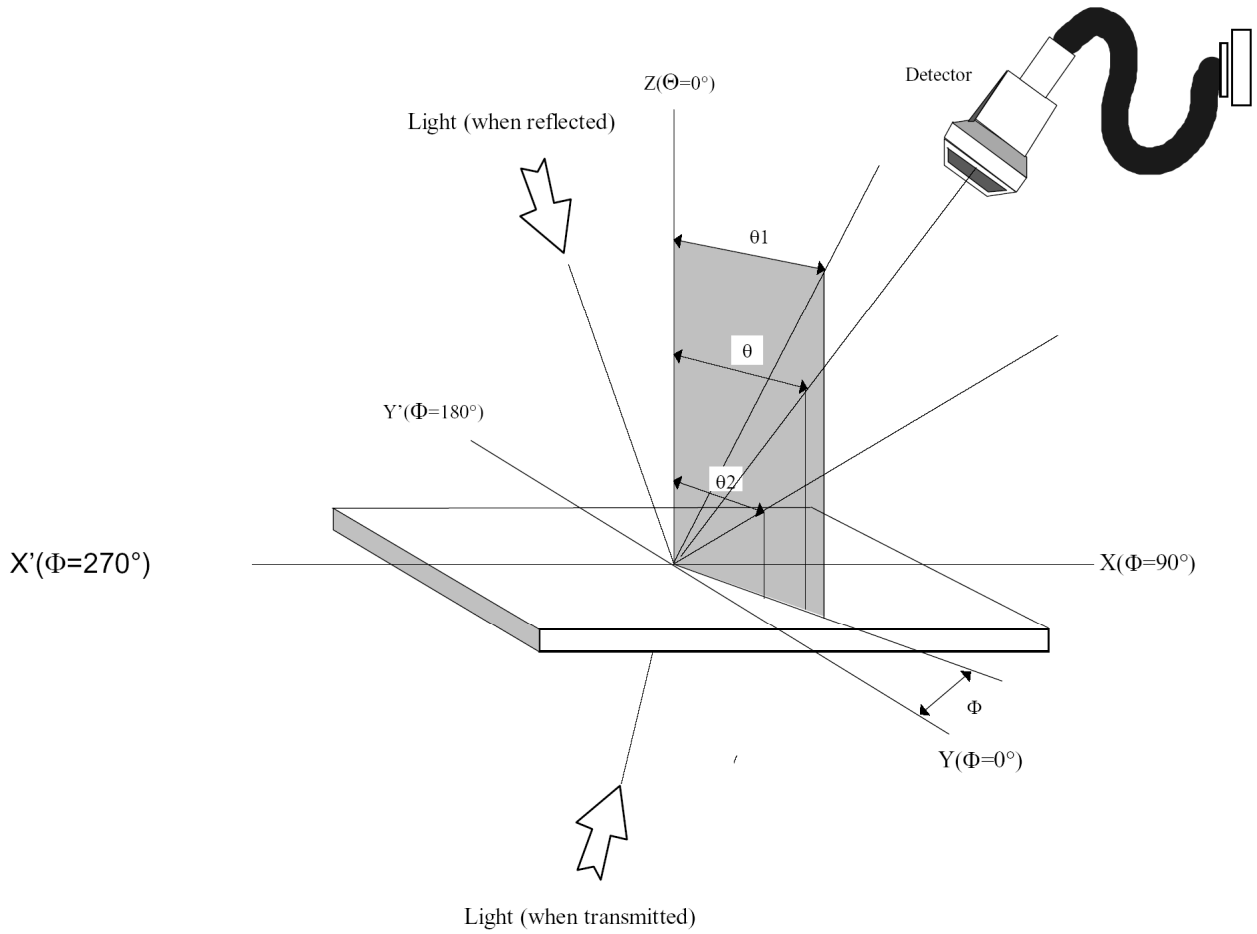
	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Mux Rate and temperature compensation.	0	0	0	0	1	0	0	#	#	#	Set {MR, TC[1:0]}	MR: 1b TC: 00b
6	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	101b
7	Set Adv. Program Control. (double byte command)	0	0	0	0	1	1	0	0	0	R	For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
8	Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9	Set Gain and Potentiometer (double-byte command)	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set {GN[1:0], PM[5:0]}	GN=3 PM=0
10	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
11	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0=disable
12	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0=disable
13	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0=disable
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
16	Set LCD Mapping Control	0	0	1	1	0	0	#	#	#	#	Set LC[3:0]	0
17	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
18	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
19	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b=12
20	Reset Cursor Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
21	Set Cursor Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
22	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		

* Other than commands listed above, all other bit patterns may result in undefined behavior.

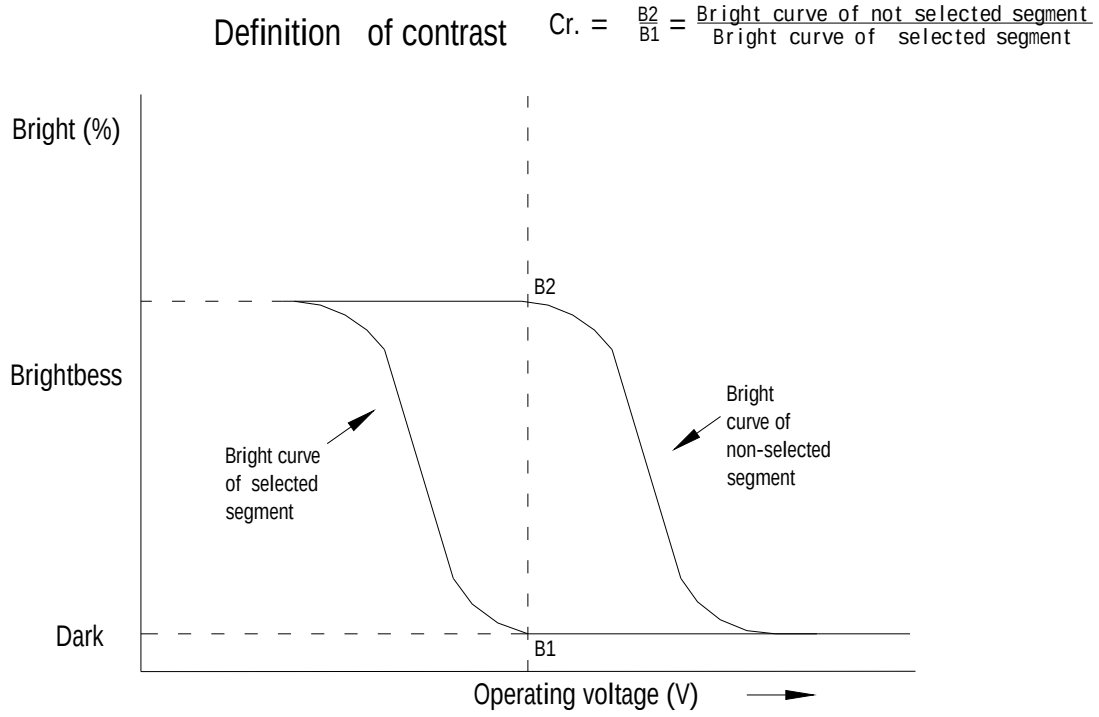
11. LCD ELECTRICAL& OPTICAL CHARACTERISTICS

Item	Symbol	Description	Condition	Temp.	Min.	Typ.	Max.	Unit
Operating Voltage	Vop		Ta=-20°C		14.7	15.0	15.3	V
			Ta=25°C		14.2	14.5	14.8	
			Ta=70°C		13.7	14.0	14.3	
Contrast	Cr		θ=10°, Φ=0° V_{DD}=3.3	25°C	2	4	---	
Viewing Angle	θ	6 o'clock axis (θ=0°)	Cr≥2.0 V_{DD}=3.3V	25°C	---	40	---	°
		12 o'clock axis (θ=180°)	V_{DD}=3.3V		---	35	---	
	θ	3 o'clock axis (θ=90°)	V_{DD}=3.3V		---	35	---	
		9 o'clock axis (θ=270°)	V_{DD}=3.3V		---	35	---	
Response Time	T_r	Rise Time	V_{DD}=3.3	25°C	---	250	500	ms
	T_d	Decay Time	V_{DD}=3.3		---	300	600	

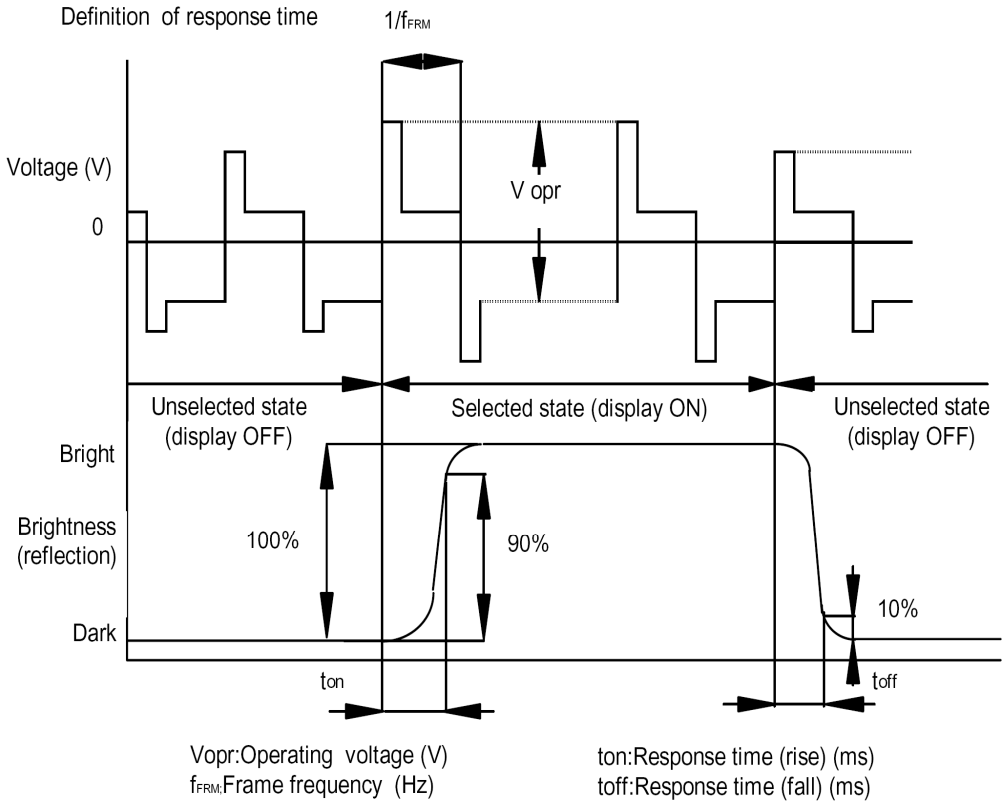
11.1 Definition of Characteristics.



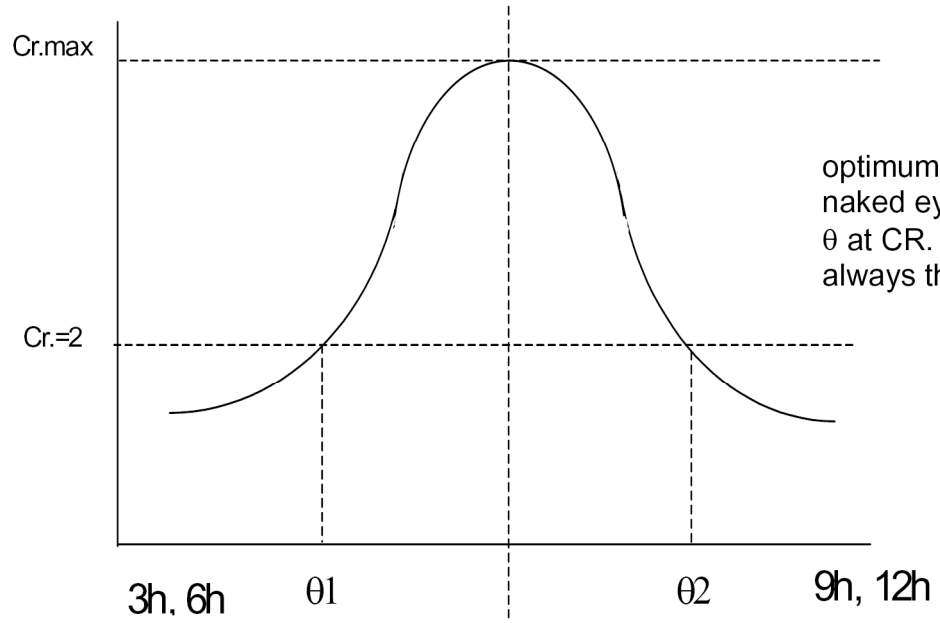
11.2. Definition of Viewing Angle



11.3 Definition of Response Time

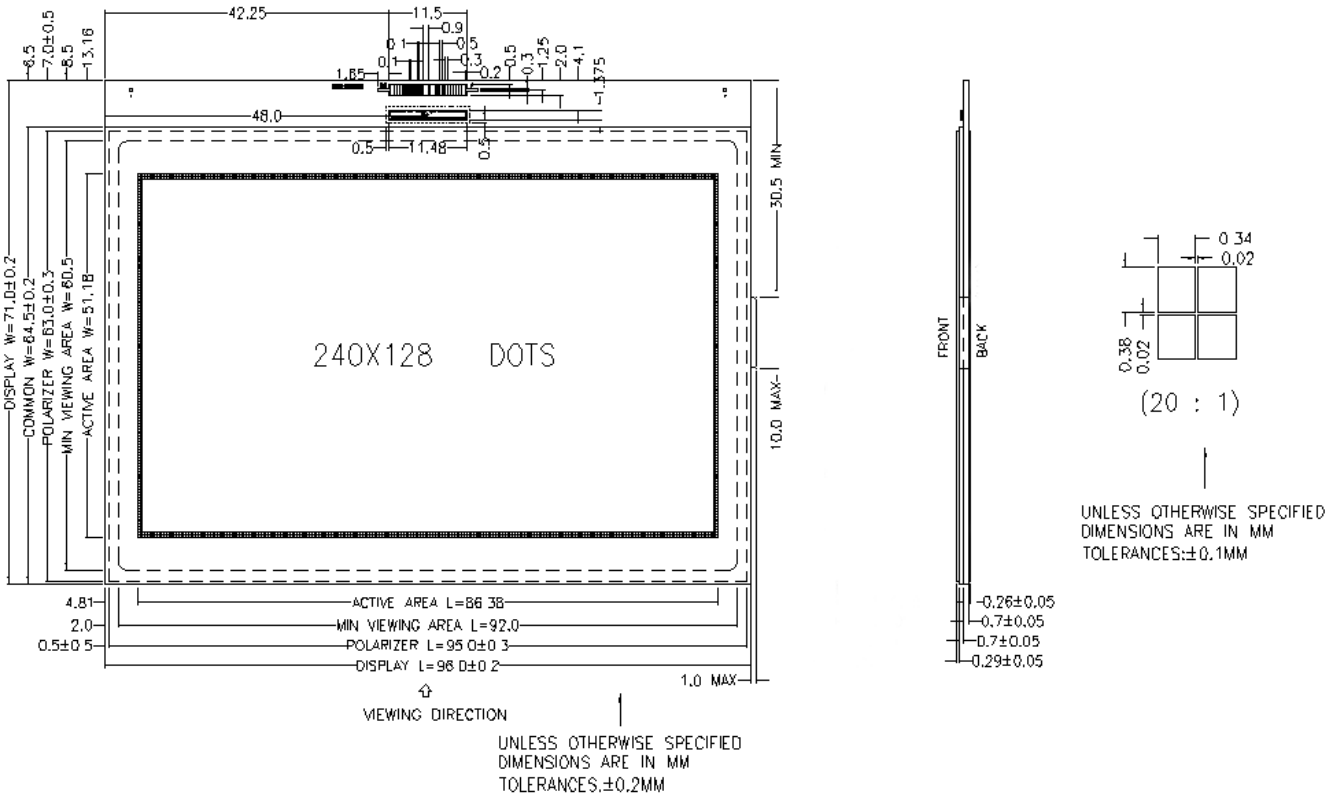


Definition of viewing angle θ1 and θ2

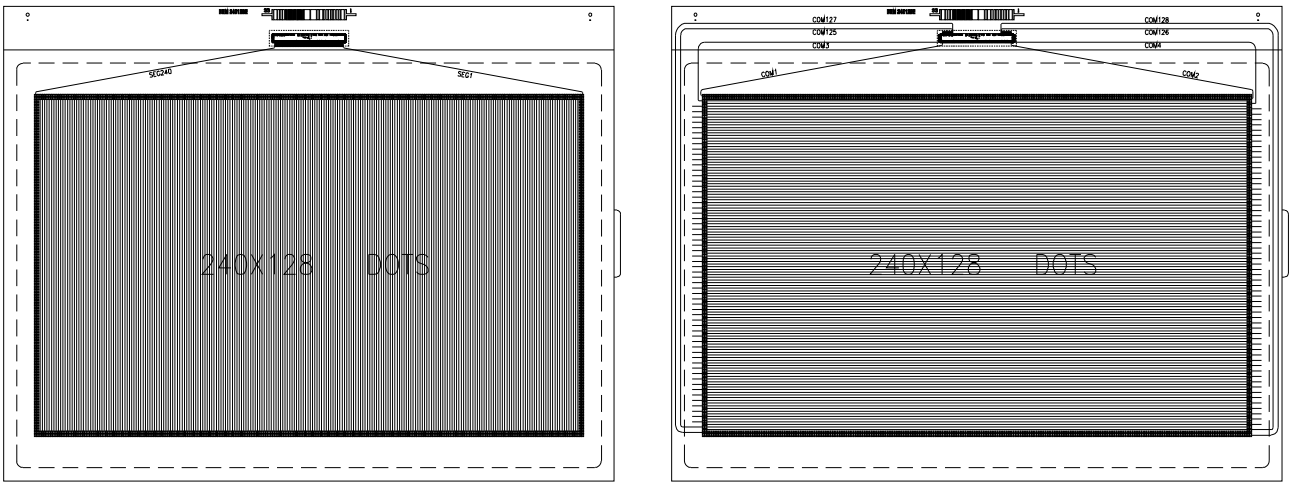


optimum vision with the naked eye and viewing angle θ at CR. max above are not always the same

12. LCD ARTWORK

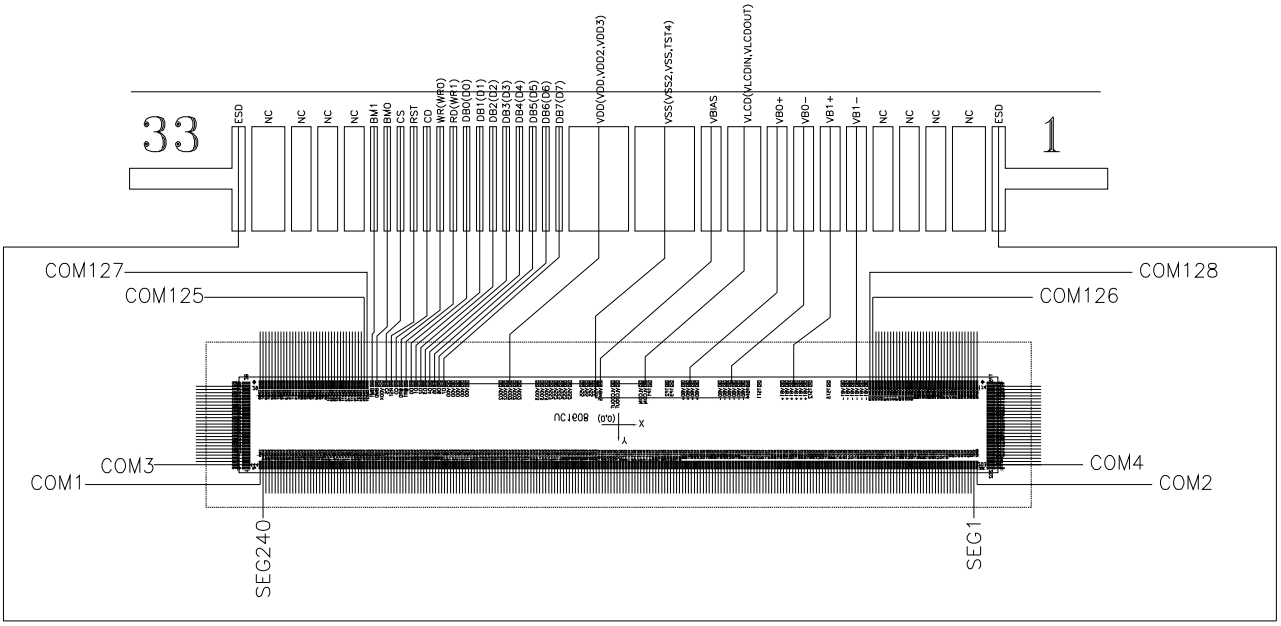


13. SEG & COM LAYOUT



SEG LAYOUT COM LAYOUT

14. IC LAYOUT



15. MODULE ACCEPT QUALITY LEVEL (AQL)

Inspection Standard: ANSI Z-1.4 Table Normal Inspection Single Sampling Level Ⅱ.

16. RELIABILITY TEST

Operating life time: 50000 Hours (at room temperature without direct irradiation of sunlight)
Reliability characteristics shall meet following requirements.

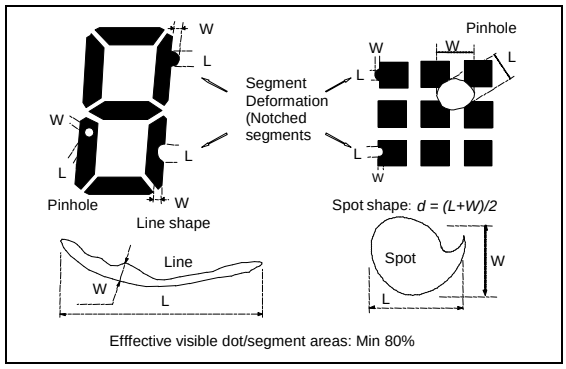
Tests Item	Condition
High Temperature Storage	+80°C x 96 hrs
Low Temperature Storage	-30°C x 96 hrs
High Temperature Operation	+70°C x 96 hrs
Low Temperature Operation	-20°C x 96 hrs
High Temperature, High Humidity	+60°C x 90%RH x 96 hrs
Thermal Shock	-20°C x 30min à 25°C x 10s à +70°C x 30 min x 5 cycles
Vibration Test	Frequency x Swing x Time 40Hz x 4mm x 4hrs
Drop Test	Height x no. of drop 1.0m x 6 drops

17. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

Specific type-related items are covered in this sheet.

a: Table for Cosmetic defects
(Note: nc = not counted).
Sizes and number of defects
(Max. Qty)

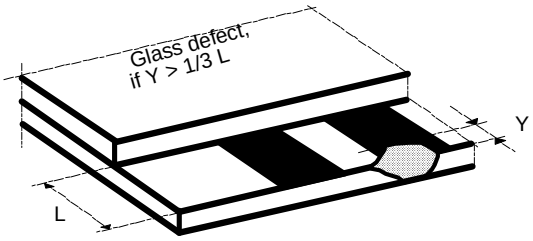


Defect Type	Max. defect size [µm] d or L	W	Max. Quantity.
Black or White Spots	d ≤ 100		nc
	100< d ≤ 200		5
Black or White Lines	--	W ≤ 10	nc
	L ≤ 5000	W ≤ 30	3
	L ≤ 2000	W ≤ 50	2
Pinhole	d ≤ 100 100< d ≤ 200		nc 1/segment
(Total defects)			(5)
Segment Deformation		W ≤ 100	nc
Bubble (e.g. under pola)	d ≤ 150		nc
	200< d ≤ 400		3
	400< d ≤ 600		1

Examples/Shapes

b: Glass defects

b1:Glass defects at contact ledge



b2:Glass chipping in other areas shall not be in conflict with the product's function.

18. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

19. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections