DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9436, 78F9456

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F9436 and 78F9456 belong to the μPD789436, 789456 Subseries (for LCD drivers) in the 78K/0S Series.

The μPD78F9436 has flash memory in place of the internal ROM of the μPD789435 and 789436, and the μPD78F9456 has flash memory in place of the internal ROM of the μPD789455 and 789456.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789426, 789436, 789446, 789456 Subseries User's Manual: U15075E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory and RAM capacities

Item / Part Number	Flash Memory	Data Memory	
		Internal High-Speed RAM	LCD Display RAM
μPD78F9436	16 KB	512 bytes	5 × 4 bits
μPD78F9456			15 × 4 bits

- Minimum instruction execution time can be changed from high-speed (0.4 μs at 5.0 MHz operation with main system clock) to ultra-low-speed (122 μs at 32.768 kHz operation with subsystem clock).
- I/O ports: 40 (μPD78F9436)
  : 30 (μPD78F9456)
- Timer: 5 channels
- A/D converter
  10-bit resolution: 6 channels
- Serial interface: 1 channel
- LCD controller/driver
  Segment signals: 5, common signals: 4 (μPD78F9436)
  Segment signals: 15, common signals: 4 (μPD78F9456)
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Portable audio systems, cameras, healthcare equipment, etc.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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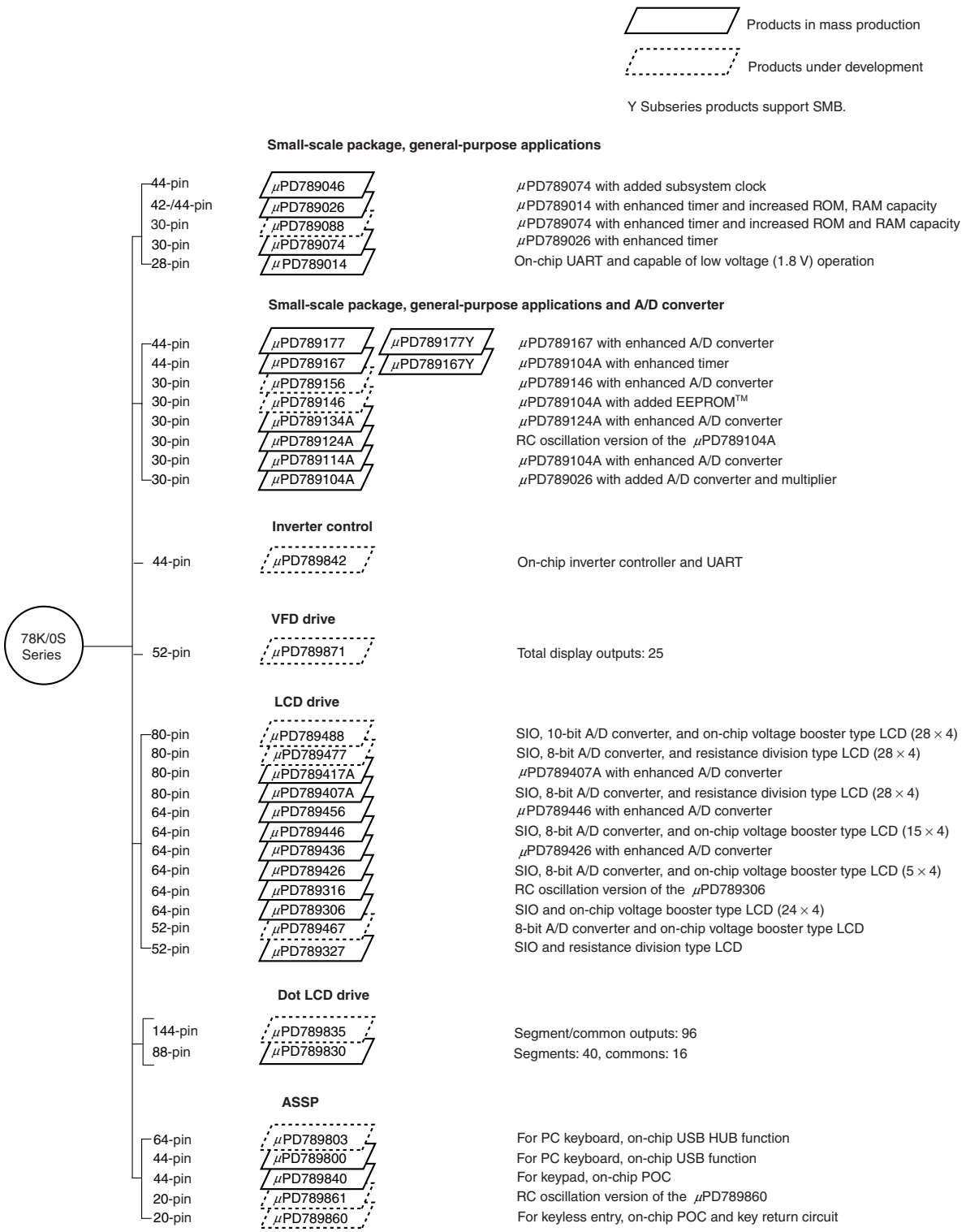
ORDERING INFORMATION

Part Number	Package
μPD78F9436GK-9ET	64-pin plastic TQFP (12 × 12)
μPD78F9456GK-9ET	64-pin plastic TQFP (12 × 12)

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as "FIP™" (fluorescent Indicator panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC-oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789477	24 K					8 ch	–				
	μPD789417A	12 K to 24 K					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC-oscillation version
	μPD789306											–
	μPD789427	4 K to 24 K		–			1 ch		–	18		
	μPD789327						–		1 ch	21		
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC-oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD78F9436	μPD78F9456
Internal memory	Flash memory	16 KB	
	High-speed RAM	512 bytes	
	LCD display RAM	5 × 4 bits	15 × 4 bits
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock) 122 μs (@ 32.768 kHz operation with subsystem clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test)	
I/O ports		Total: 40 • CMOS I/O: 30 • CMOS input: 6 • N-ch open drain: 4	Total: 30 • CMOS I/O: 20 • CMOS input: 6 • N-ch open drain: 4
Timers		• 16-bit timer: 1 channel • 8-bit timer: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
A/D converter		10-bit resolution × 6 channels	
Serial interface		• Switchable between 3-wire serial I/O mode and UART mode: 1 channel	
LCD controller/driver		• Segment signal outputs: 5 (max.) • Common signal outputs: 4 (max.)	• Segment signal outputs: 15 (max.) • Common signal outputs: 4 (max.)
Vectored interrupt sources	Maskable	Internal: 9, external: 5	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		64-pin plastic TQFP (12 × 12)	

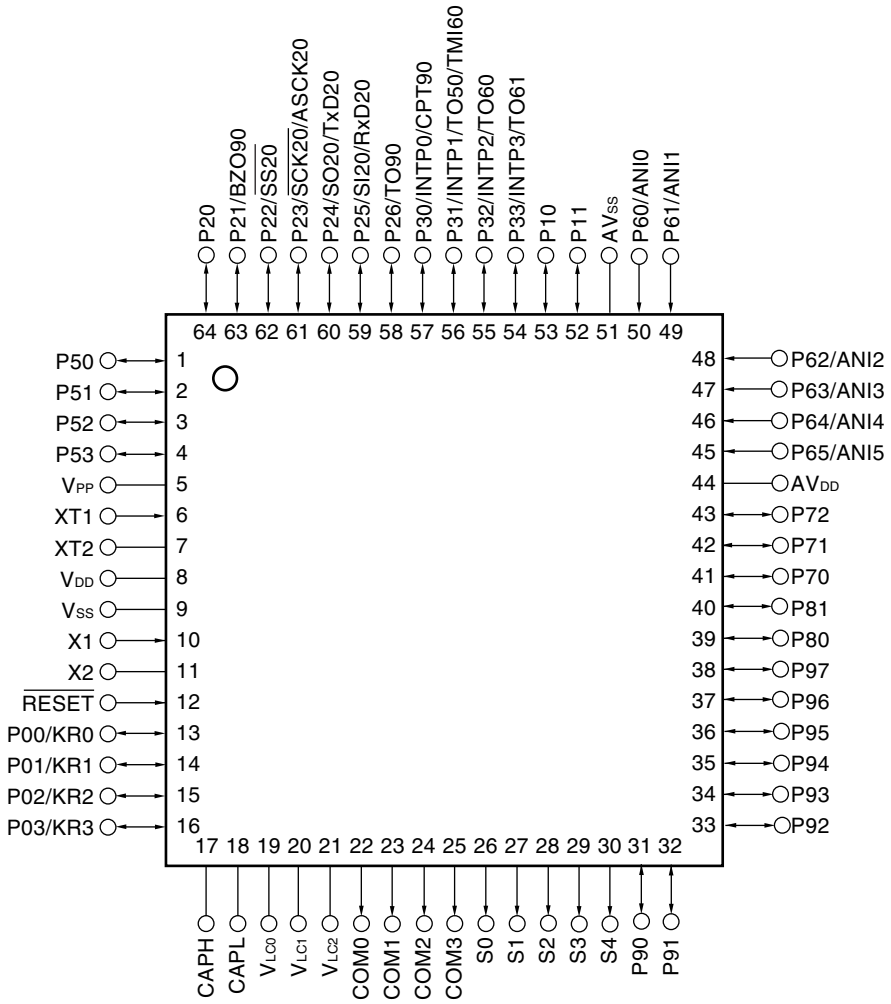
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

1.1 Pin Configuration of the μPD78F9436 (Top View)

64-pin plastic TQFP (12 × 12)

μPD78F9436GK-9ET



Cautions 1. Connect the V_{PP} pin directly to V_{SS}.

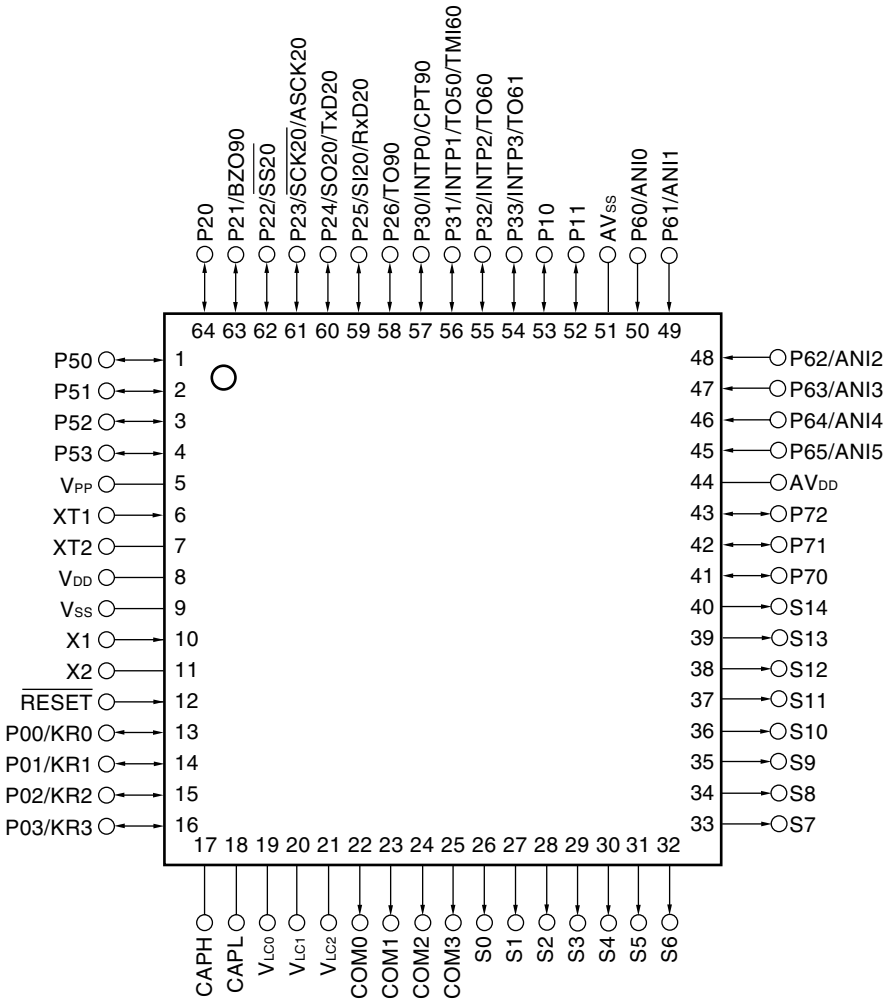
2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

1.2 Pin Configuration of the μPD78F9456 (Top View)

64-pin plastic TQFP (12 × 12)

μPD78F9456-9ET



Cautions 1. Connect the V_{PP} pin directly to V_{SS}.

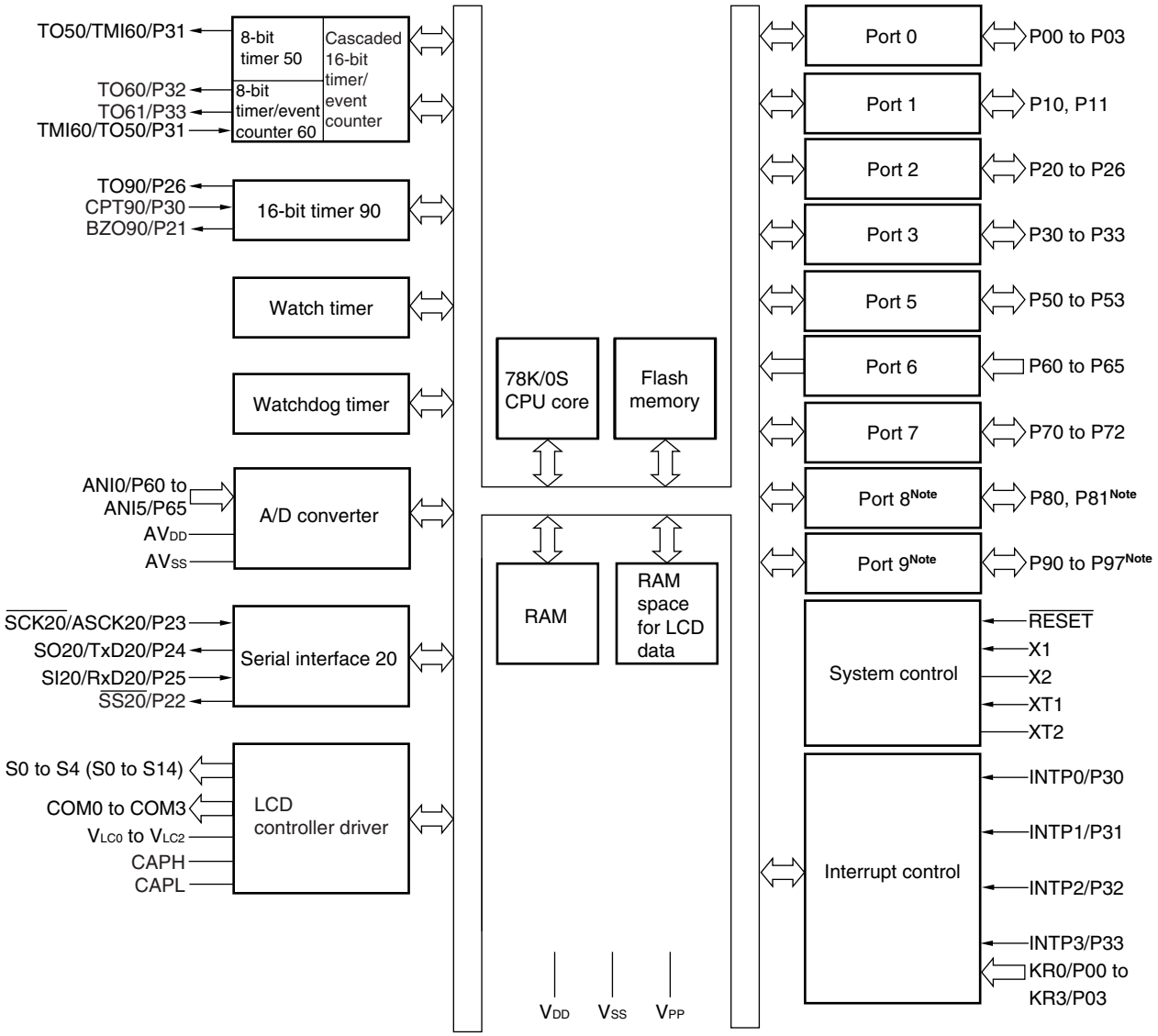
2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

ANI0 to ANI5:	Analog input	P90 to P97[Note]:	Port 9
ASCK20:	Asynchronous serial input	$\overline{\text{RESET}}$:	Reset
AV_{DD}:	Analog power supply	RxD20:	Receive data
AV_{SS}:	Analog ground	$\overline{\text{SS20}}$:	Serial chip select
BZO90:	Buzzer output	S0 to S14:	Segment output
CAPH, CAPL:	LCD power supply capacitance control	$\overline{\text{SCK20}}$:	Serial clock
COM0 to COM3:	Common output	SI20:	Serial input
CPT90:	Capture trigger input	SO20:	Serial output
INTP0 to INTP3:	External interrupt input	TMI60:	Timer input
KR0 to KR3:	Key return	TO90, TO50, TO60,	
P00 to P03:	Port 0	TO61:	Timer output
P10, P11:	Port 1	TxD20:	Transmit data
P20 to P26:	Port 2	V_{DD}:	Power supply
P30 to P33:	Port 3	V_{LC0} to V_{LC2}:	LCD power supply
P50 to P53:	Port 5	V_{PP}:	Programming power supply
P60 to P63:	Port 6	V_{SS}:	Ground
P70 to P72:	Port 7	X1, X2:	Crystal (Main system clock)
P80 to P81[Note]:	Port 8	XT1, XT2:	Crystal (Subsystem clock)

Note μPD78F9436 only

2. BLOCK DIAGRAM



Note μPD78F9436 only

Remark Descriptions in parentheses are for the μPD78F9456.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	KR0 to KR3
P10, P11	I/O	Port 1. 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	—
P20	I/O	Port 2. 7-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	—
P21				BZO90
P22				$\overline{SS20}$
P23				$\overline{SCK20}$/ASCK20
P24				SO20/TxD20
P25				SI20/RxD20
P26				TO90
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP0/CPT90
P31				INTP1/TO50/TMI60
P32				INTP2/TO60
P33				INTP3/TO61
P50 to P53	I/O	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units.	Input	—
P60 to P65	Input	Port 6. 6-bit input port.	Input	ANI0 to ANI5
P70 to P72	I/O	Port 7. 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	—
P80, P81[Note]	I/O	Port 8. 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	—
P90 to P97[Note]	I/O	Port 9. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by a software setting.	Input	—

Note μPD78F9436 only

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/CPT90
INTP1				P31/TO50/TMI60
INTP2				P32/TO60
INTP3				P33/TO61
KR0 to KR3	Input	Key return signal detection	Input	P00 to P03
$\overline{SS20}$	Input	Serial interface (SIO20) chip select	Input	P22
$\overline{SCK20}$	I/O	Serial interface (SIO20) serial clock input/output	Input	P23/ASCK20
SI20	Input	SIO20 serial interface serial data input	Input	P25/RxD20
SO20	Output	SIO20 serial interface serial data output	Input	P24/TxD20
ASCK20	I/O	Asynchronous serial interface serial clock input	Input	P23/$\overline{SCK20}$
RxD20	Input	Asynchronous serial interface serial data input	Input	P25/SI20
TxD20	Output	Asynchronous serial interface serial data output	Input	P24/SO20
TO90	Output	16-bit timer (TM90) output	Input	P26
CPT90	Input	Capture edge input	Input	P30/INTP0
TO50	Output	8-bit timer (TM50) output	Input	P31/INTP1/TMI60
TO60	Output	8-bit timer (TM60) output	Input	P32/INTP2
TO61	Output	8-bit timer (TM60) output	Input	P33/INTP3
TMI60	Input	External count clock input to 8-bit timer (TM60)	Input	P31/INTP1/TO50
ANI0 to ANI5	Input	A/D converter analog inputs	Input	P60 to P65
S0 to S4	Output	Segment signal outputs for LCD controller/driver	Output	—
S5 to S14[Note]	Output	Segment signal outputs for LCD controller/driver	Output	—
COM0 to COM3	Output	Common signal outputs for LCD controller/driver	Output	—
V_{LC0} to V_{LC2}	—	LCD drive voltage	—	—
CAPH	—	Connection pin for LCD driver's capacitor	—	—
CAPL	—		—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	—	—
XT2	—		—	—
$\overline{RESET}$	Input	System reset input	Input	—
V_{DD}	—	Positive power supply for ports	—	—
V_{SS}	—	Ground potential	—	—
AV_{DD}	—	A/D converter analog potential	—	—
AV_{SS}	—	A/D converter ground potential	—	—
V_{PP}	—	Flash memory programming mode setting. High-voltage application for program write/verify. In normal operation mode, connect directly to V_{SS}.	—	—

Note μPD78F9456 only

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

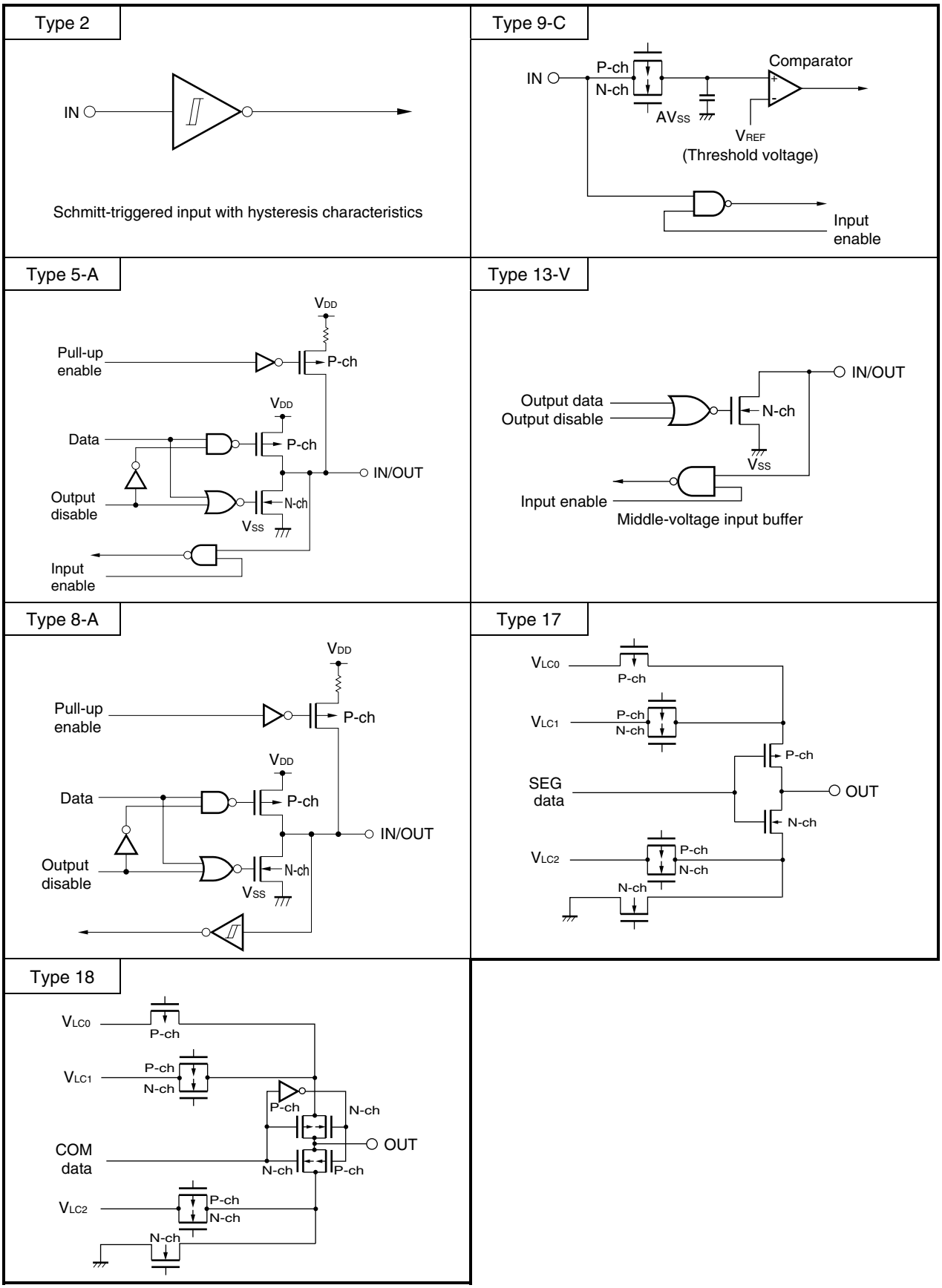
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin Input/Output Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P03	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10, P11	5-A		
P20	8-A		
P21/BZO90			
P22/$\overline{SS20}$			
P23/$\overline{SCK20}$/ASCK20			
P24/SO20/TxD20			
P25/SI20/RxD20			
P26/TO90			
P30/INTP0/CPT90			Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P31/INTP1/TO50/ TMI60			
P32/INTP2/TO60			
P33/INTP3/TO61			
P50 to P53	13-V		Input: Independently connect to V_{DD} via a resistor. Output: Leave open.
P60/ANI0 to P65/ANI5	9-C	Input	Connect directly to V_{DD} or V_{SS}.
P70 to P72	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P80, P81[Note 1]			
P90 and P97[Note 1]			
S0 to S4	17	Output	Leave open.
S5 to S14[Note 2]			
COM0 to COM3	18	—	
V_{LC0} to V_{LC2}	—		
CAPH, CAPL			
XT1		Input	Connect to V_{SS}.
XT2		—	Leave open.
AV_{SS}			Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
$\overline{RESET}$	2	Input	—
V_{PP}	—	—	Connect directly to V_{SS}.

Notes 1. μPD78F9436 only
2. μPD78F9456 only

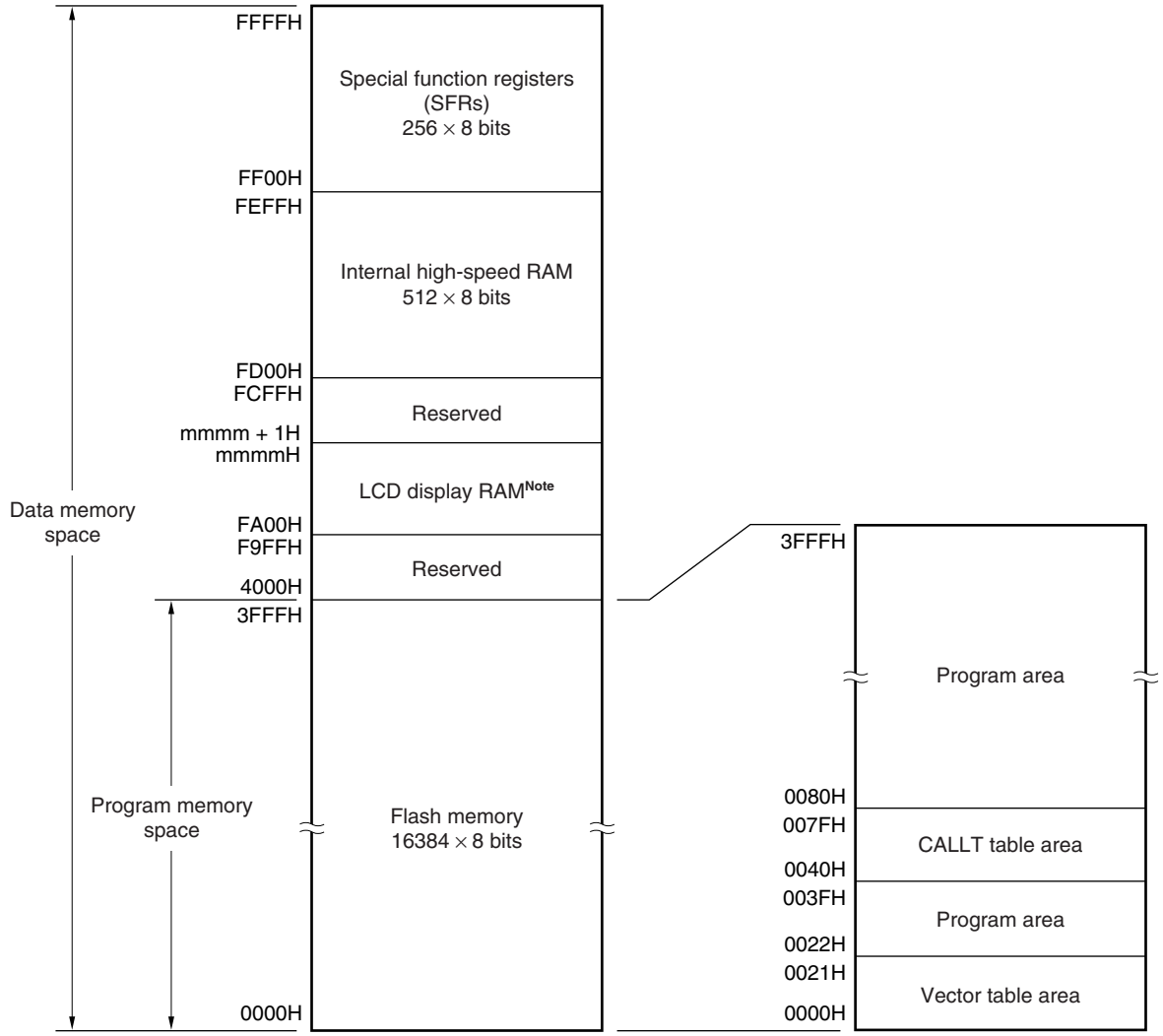
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The capacity of the LCD display RAM varies depending on the product (see following table).

Part Number	Last Address of LCD display RAM mmmmH
μPD78F9436	FA04H
μPD78F9456	FA0EH

5. FLASH MEMORY PROGRAMMING

The program memory that is incorporated in the μPD78F9436 and 78F9456 is flash memory.

With flash memory, it is possible to write programs on-board. Writing is performed by connecting a dedicated flash programmer (Flashpro III (Part No. FL-PR3, PG-FP3)) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro III in a serial communication mode. Select one of the communication modes in Table 5-1. The selection of the communication mode is made by using the format shown in Figure 5-1. Each communication mode is selected using the number of V_{PP} pulses shown in Table 5-1.

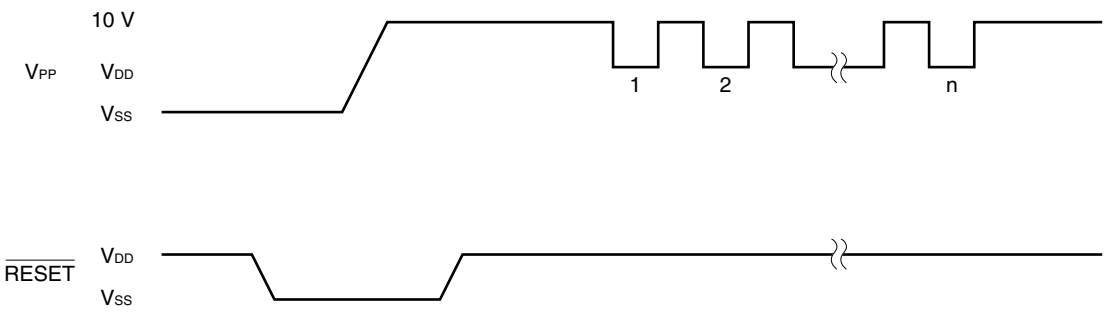
Table 5-1. List of Communication Mode

Communication Mode	Pins[Note]	V_{PP} Pulses
3-wire serial I/O	$\overline{SCK20}$/P23 SO20/P24 SI20/P25	0
	P00/KR0 (serial clock input) P01/KR1 (serial data output) P02/KR2 (serial data input)	1
UART	TxD20/P24 RxD20/P25	8

Note Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. If the external device connected to the port does not acknowledge the port state immediately after reset, handling such as connecting to V_{DD} or V_{SS} via a resistor or connecting to is required.

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Communication Mode Selection



5.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 5-2 shows the major functions of flash memory programming.

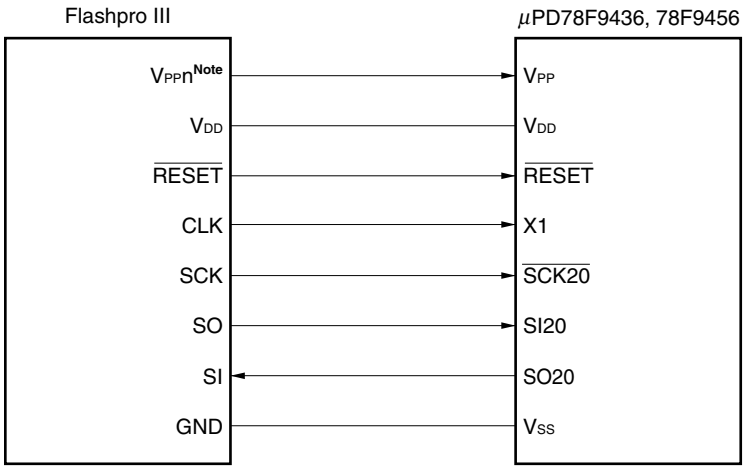
Table 5-2. Major Function of Flash Memory Programming

Function	Description
Batch erase	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
Data write	Performs a write operation to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

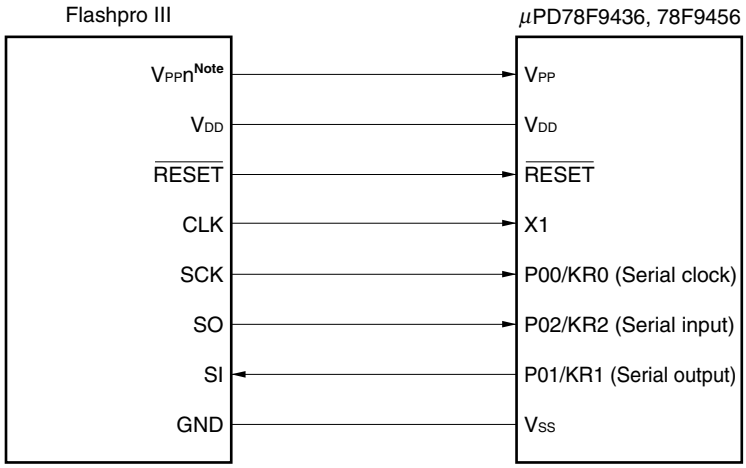
The connection of the Flashpro III and the μPD78F9436 and 78F9456 differs according to the communication mode (3-wire serial I/O or UART). The connections for each communication mode are shown in Figures 5-2 and 5-3, respectively.

Figure 5-2. Connection Example of Flashpro III When Using 3-Wire Serial I/O Mode (1/2)



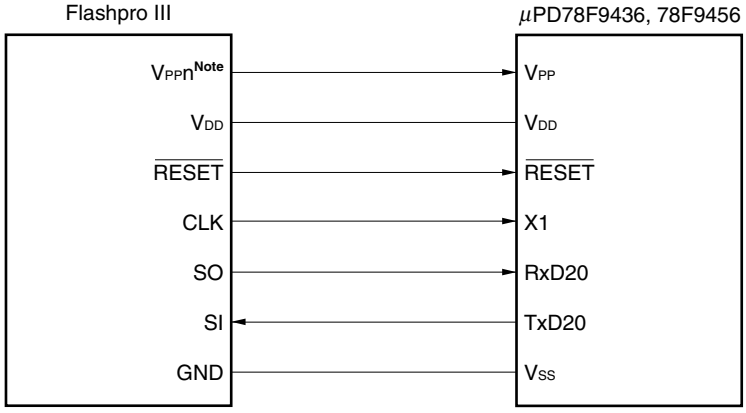
Note n = 1, 2

Figure 5-2. Connection Example of Flashpro III When Using 3-Wire Serial I/O Mode (2/2)



Note n = 1, 2

Figure 5-3. Connection Example of Flashpro III When Using UART Mode



Note n = 1, 2

5.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

<1> Load a parameter file.
<2> Select the mode of serial communication and serial clock with a type command.
<3> Make the settings according to the example of settings for PG-FP3 shown below.

Table 5-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V_{PP} Pulse Number[Note 1]
3-wire serial I/O	COMM PORT	SIO-ch0	0
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
	COMM PORT	SIO-ch1	1
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9600 bps[Note 2]	

Notes 1. This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.

2. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT: Serial port selection
SIO CLK: Serial clock frequency selection
CPU CLK: Input CPU clock source selection

6. OVERVIEW OF INSTRUCTION SET

This section lists the instruction set for the μPD78F9436 and 78F9456.

6.1 Conventions

6.1.1 Operand expressions and description methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand expression (see the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and symbols, #, !, $, and [ ] are key words and are described as they are. The meaning of each symbol is described below.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

For immediate data, enter an appropriate numeric value or a label. When using a label, be sure to enter the #, !, $ and [ ] symbols.

For operand register expressions, r and rp, either function names (X, A, C, etc.) or absolute names (names in parenthesis in the table below, R0, R1, R2, etc.) can be used for the description.

Table 6-1. Operand Expressions and Description Methods

Expression	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: immediate data or label FE20H to FF1FH: immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: immediate data or label (even addresses only for 16-bit data transfer instruction) 0040H to 007FH: immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

6.1.2 Description of "Operation" column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag indicating non-maskable interrupt servicing in progress
( ):	Memory contents indicated by address or register contents in parenthesis
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
$\overline{\vee}$:	Exclusive logical sum (exclusive OR)
$\overline{\ }$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

6.1.3 Description of "Flag" column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is restored

6.2 List of Operations

Mnemonic	Operand	Bytes	Clocks	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			
XCHW	AX, rp Note 3	1	8	AX ↔ rp			

Notes 1. Except r = A

2. Except r = A, X

3. Only when rp = BC, DE, HL

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1 time			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1 time			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1 time			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1 time			×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag
					Z AC CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1	
	sfr. bit	3	6	sfr. bit ← 1	
	A. bit	2	4	A. bit ← 1	
	PSW. bit	3	6	PSW. bit ← 1	× × ×
	[HL]. bit	2	10	(HL). bit ← 1	
CLR1	saddr. bit	3	6	(saddr. bit) ← 0	
	sfr. bit	3	6	sfr. bit ← 0	
	A. bit	2	4	A. bit ← 0	
	PSW. bit	3	6	PSW. bit ← 0	× × ×
	[HL]. bit	2	10	(HL). bit ← 0	
SET1	CY	1	2	CY ← 1	1
CLR1	CY	1	2	CY ← 0	0
NOT1	CY	1	2	CY ← $\overline{CY}$	×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2	
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2	
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2	
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R R R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1	
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2	
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R R R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2	
MOVW	SP, AX	2	8	SP ← AX	
	AX, SP	2	6	AX ← SP	
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected via the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	AV_{DD}				
	V_{PP}			–0.3 to +10.5	V
Input voltage	V_{I1}	P00 to P03, P10, P11, P20 to P26, P30 to P33, P60 to P65, P70 to P72, P80[Note 1], P81[Note 1], P90 to P97[Note 1], X1, X2, XT1, XT2, $\overline{RESET}$		–0.3 to V_{DD} + 0.3[Note 2]	V
	V_{I2}	P50 to P53	N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3[Note 2]	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for all pins		–30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

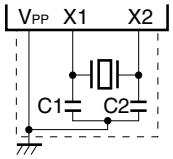
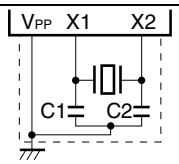
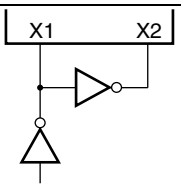
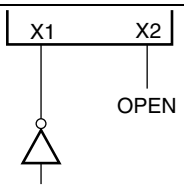
Notes 1. For μPD78F9436

2. 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency(f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

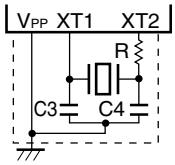
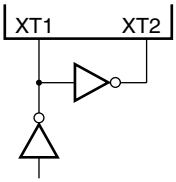
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin				10	mA
		All pins				80	mA
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Input voltage, high	V_{IH1}	P10, P11, P60 to P65, P70 to P72, P80[Note], P81[Note], P90 to P97[Note]	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53 (N-ch open drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P00 to P03, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P10, P11, P60 to P65, P70 to P72, P80[Note], P81[Note], P90 to P97[Note]	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P00 to P03, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P03, P10, P11, P20 to P26, P30 to P33, P60 to P65, P70 to P72, P80[Note], P81[Note], P90 to P97[Note], X1, X2, XT1, XT2	4.5 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 10 mA			1.0	V
			1.8 ≤ V_{DD} < 4.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	4.5 ≤ V_{DD} < 5.5 V, I_{OL} = 10 mA			1.0	V
			1.8 ≤ V_{DD} < 4.5 V, I_{OL} = 1.6 mA			0.4	V

Note μPD78F9436 only

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	P00 to P03, P10, P11, P20 to P26, P30 to P33, P60 to P65, P70 to P72, P80[Note 1], P81[Note 1], P90 to P97[Note 1], $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	P00 to P03, P10, P11, P20 to P26, P30 to P33, P60 to P65, P70 to P72, P80[Note 1], P81[Note 1], P90 to P97[Note 1], $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3[Note 2]	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V	P00 to P03, P10, P11, P20 to P26, P30 to P33, P70 to P72, P80[Note 1], P81[Note 1], P90 to P97[Note 1]	50	100	200	kΩ

Notes 1. μPD78F9436 only

2. If P50 to P53 have been set to input mode when a read instruction is executed to read from P50 to P53, a low-level input leakage current of up to –30 μA flows during only one cycle. At all other times, the maximum leakage current is –3 μA.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operation mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		4.5	9	mA
			V_{DD} = 3.0 V ±10%[Note 3]		1	2	mA
			V_{DD} = 2.0 V ±10%[Note 3]		0.65	1.5	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		1.4	2	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.4	0.8	mA
			V_{DD} = 2.0 V ±10%[Note 3]		0.19	0.42	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode[Note 4] (C3 = C4 = 22 pF, R1 = 220kΩ)	V_{DD} = 5.0 V ±10%		100	230	μA
			V_{DD} = 3.0 V ±10%		70	160	μA
			V_{DD} = 2.0 V ±10%		58	120	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4] — LCD not operating	V_{DD} = 5.0 V ±10%		25	65	μA
			V_{DD} = 3.0 V ±10%		7	29	μA
			V_{DD} = 2.0 V ±10%		4	20	μA
		LCD operating[Note 5]	V_{DD} = 5.0 V ±10%		28	70	μA
			V_{DD} = 3.0 V ±10%		9.6	34	μA
			V_{DD} = 2.0 V ±10%		6	25	μA
	I_{DD5}	STOP mode[Note 6]	V_{DD} = 5.0 V ±10%		0.1	17	μA
			V_{DD} = 3.0 V ±10%		0.05	5.5	μA
			V_{DD} = 2.0 V ±10%		0.05	3.5	μA
	I_{DD6}	5.0 MHz crystal oscillation A/D operating mode[Note 7] (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		5.2	10.8	mA
			V_{DD} = 3.0 V ±10%[Note 3]		1.4	3.8	mA
			V_{DD} = 2.0 V ±10%[Note 3]		1.0	2.9	mA

Notes 1. The port current (including the current that flows to the on-chip pull-up resistor) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock is stopped

5. This is the current when the LCD controller/driver is operating (LCDON0 = 1, VAON0 = 1, LIPS0 = 1). The power supply current when the LCD is not operating (LCDON0 = 0, VAON0 = 1, LIPS0 = 0) is included in I_{DD2} (HALT mode).

6. When the LCD voltage amplifier is stopped (LCDON0 = 0, VAON0 = 0)

7. This is the total current that flows to V_{DD} and AV_{DD}.

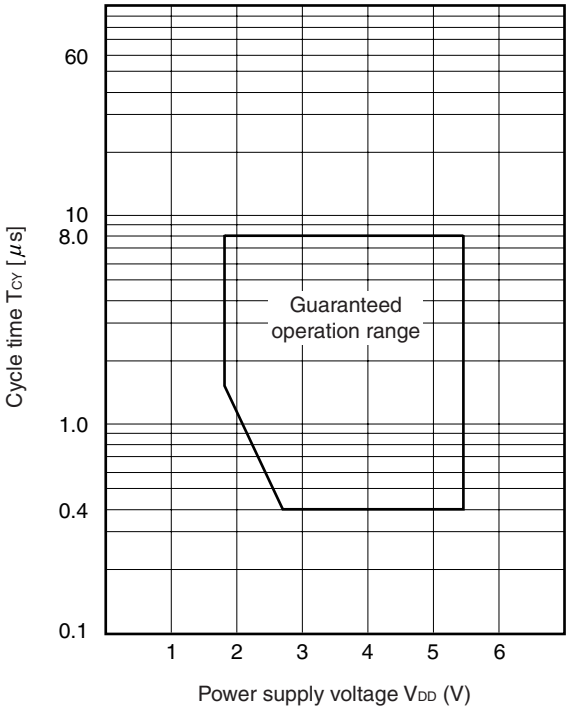
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8.0	μs
				1.6		8.0	μs
		Operating with subsystem clock		114	122	125	μs
Capture input high-/low-level width	t_{CPTH}, t_{CPTL}	CPT90		10			μs
TMI60 input frequency	f_{TMI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TMI60 input high-/low-level width	t_{TIMH}, t_{TIML}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
Key return input low-level width	t_{KRL}	KR0 to KR3		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface 20 (SIO20) (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{SI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK20}$↓ to SO20 output	t_{SO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode (external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{SI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK20}$↓ to SO20 output	t_{SO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns
SO20 setup time (with $\overline{SS20}$, to $\overline{SCK20}$↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
						400	ns
SO20 disable time (with $\overline{SS20}$, from $\overline{SCK20}$↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
						800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

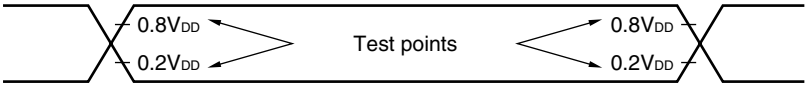
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

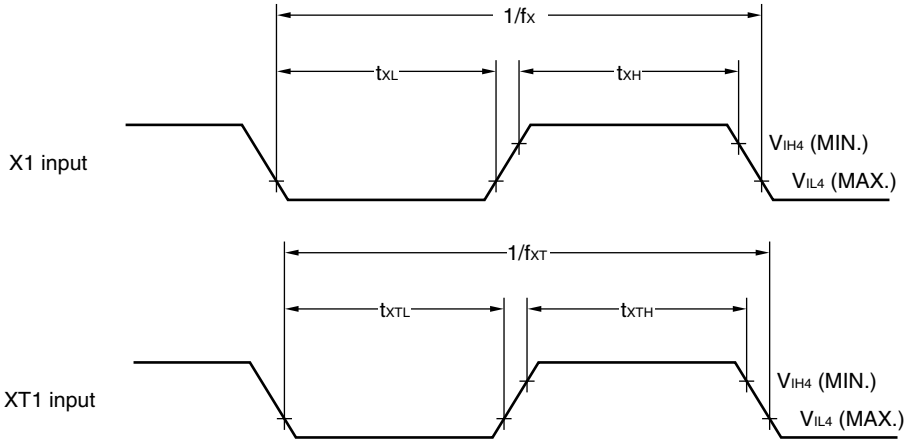
(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
			3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

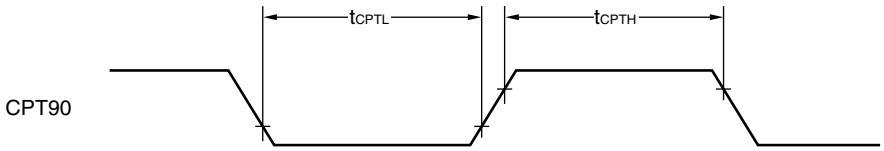
AC Timing Test Points (excluding X1 and XT1 inputs)



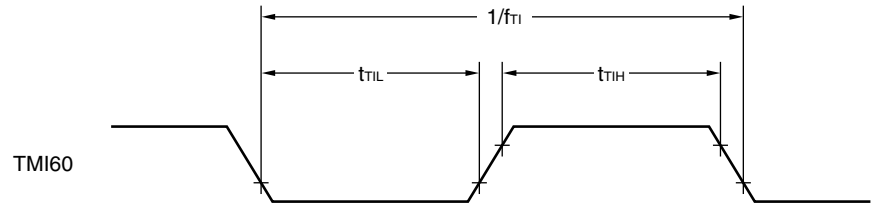
Clock Timing



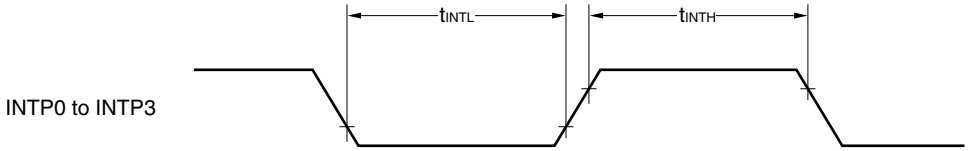
Capture Input Timing



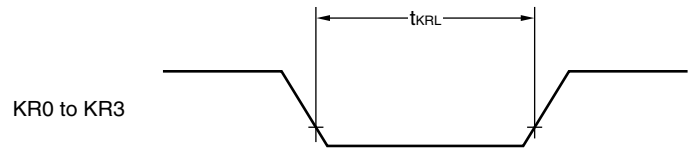
TMI Timing



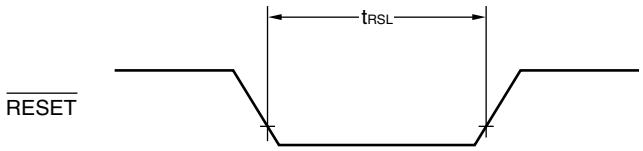
Interrupt Input Timing



Key Return Input Timing

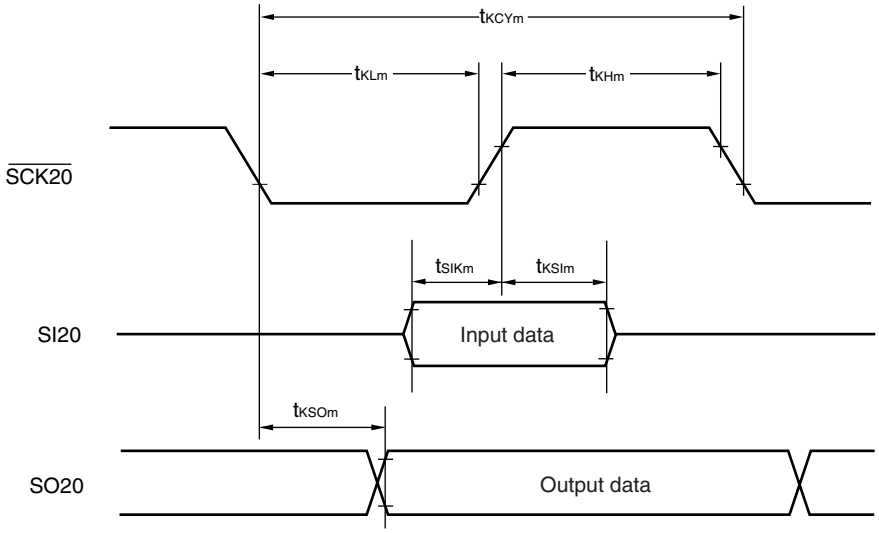


$\overline{\text{RESET}}$ Input Timing



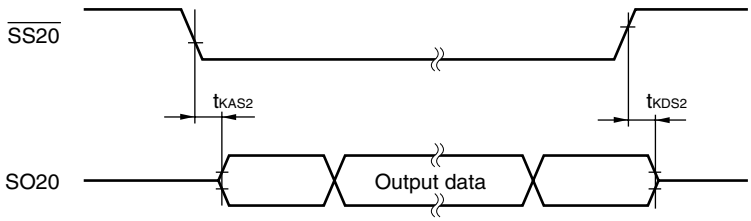
Serial Transfer Timing

3-wire serial I/O mode:

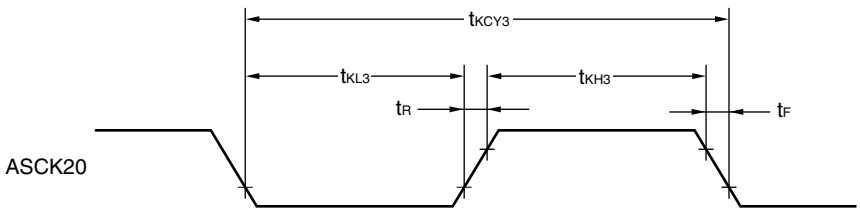


Remark m = 1, 2

3-wire serial I/O mode (when using $\overline{\text{SS20}}$):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{DD} < 4.5 V	19		100	μs
		1.8 V ≤ AV_{DD} < 2.7 V	28		100	μs
Zero-scale error[Note]	AINL	4.5 V ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ AV_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Note]	AINL	4.5 V ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ AV_{DD} < 2.7 V			±1.2	%FSR
Non-integral linearity[Note]	INL	4.5 V ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ AV_{DD} < 2.7 V			±8.5	LSB
Non-differential linearity[Note]	DNL	4.5 V ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ AV_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Note Excludes quantization error (±0.05%)

Remark FSR: Full scale range

LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{LCD2}	C1 to C4[Note 1] = 0.47 μF	GAIN = 1	0.84	1.0	1.165	V
			GAIN = 0	1.26	1.5	1.74	V
Doubler output	V_{LCD1}	C1 to C4[Note 1] = 0.47 μF		$2V_{LCD2}$ –0.1	$2.0V_{LCD2}$	$2.0V_{LCD2}$	V
Tripler output	V_{LCD0}	C1 to C4[Note 1] = 0.47 μF		$3V_{LCD2}$ –0.15	$3.0V_{LCD2}$	$3.0V_{LCD2}$	V
Voltage amplification wait time[Note 2]	t_{VAWAIT}	GAIN = 0		0.5			s
		GAIN = 1	$5.0 \le V_{DD} \le 5.5$ V	2.0			s
			$4.5 \le V_{DD} < 5.0$ V	1.0			s
			$1.8 \le V_{DD} < 4.5$ V	0.5			s
LCD output voltage differential[Note 3] (common)	V_{ODC}	I_O = ±5 μA		0		±0.2	V
LCD output voltage differential[Note 3] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{LC0} and V_{SS}
C3: A capacitor connected between V_{LC1} and V_{SS}
C4: A capacitor connected between V_{LC2} and V_{SS}

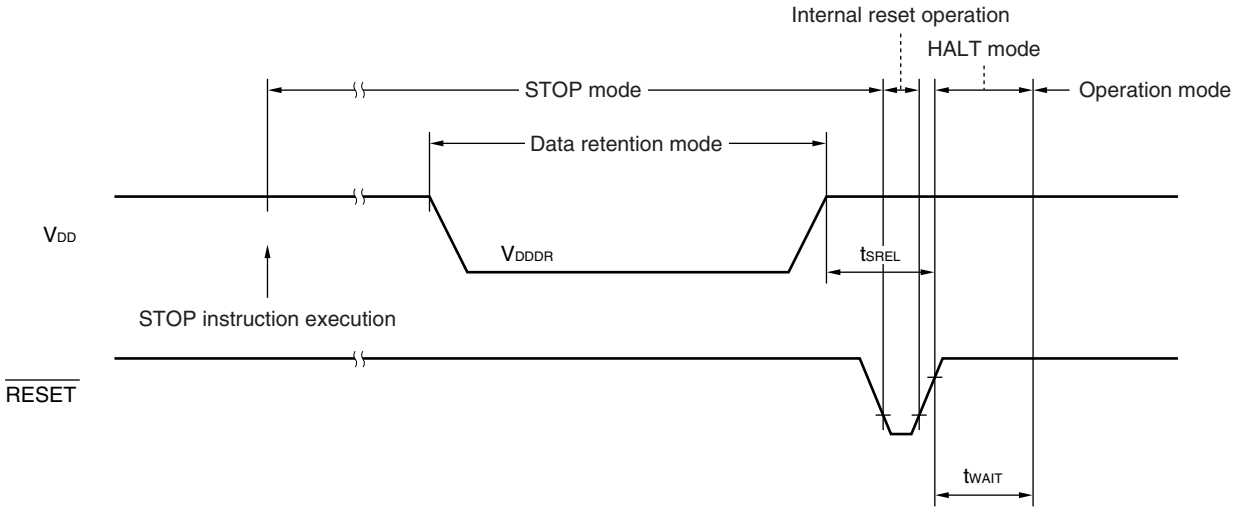
2. This is the wait time from when voltage amplification is started (VAON0 = 1) until display is enabled (LCDON0 = 0).

3. The voltage differential is the difference between the segment and common signal output's actual and ideal output voltages.

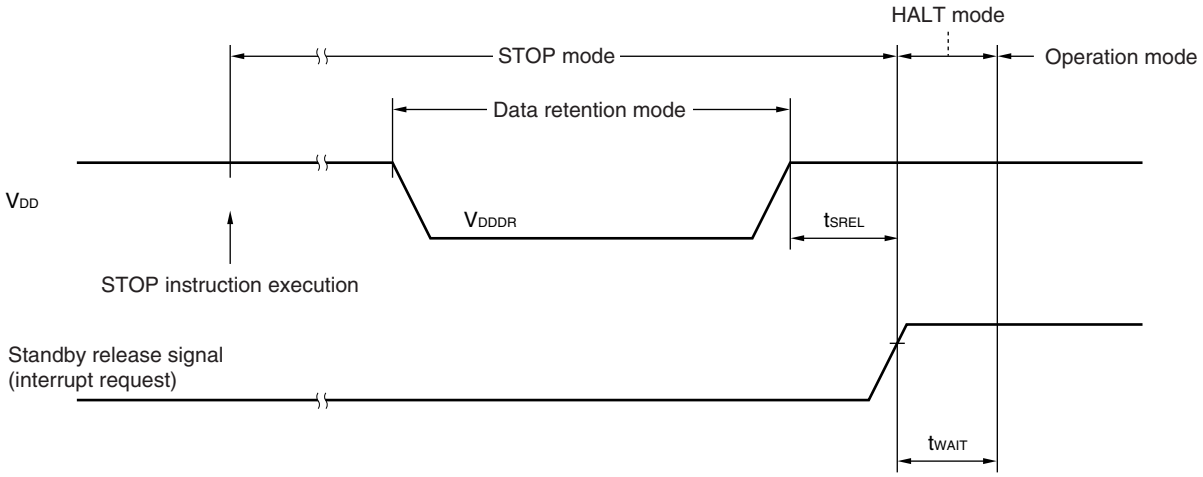
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Oscillation Stabilization Wait Time (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt		**Note 2**		s

Notes 1. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.

2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_X: Main system clock oscillation frequency

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	V_{DD} = 2.7 to 5.5 V		1.0		5	MHz
				1.0		1.25	MHz
Write current[Note] (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1}	During f_X = 5.0 MHz operation			7	mA
Write current[Note] (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}				12	mA
Erase current[Note] (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1}	During f_X = 5.0 MHz operation			7	mA
Erase current[Note] (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}				100	mA
Unit erase time	t_{er}			0.5	1	1	s
Total erase time	t_{era}					20	s
Write count		Erase/write are regarded as 1 cycle				20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation		0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming		9.7	10.0	10.3	V

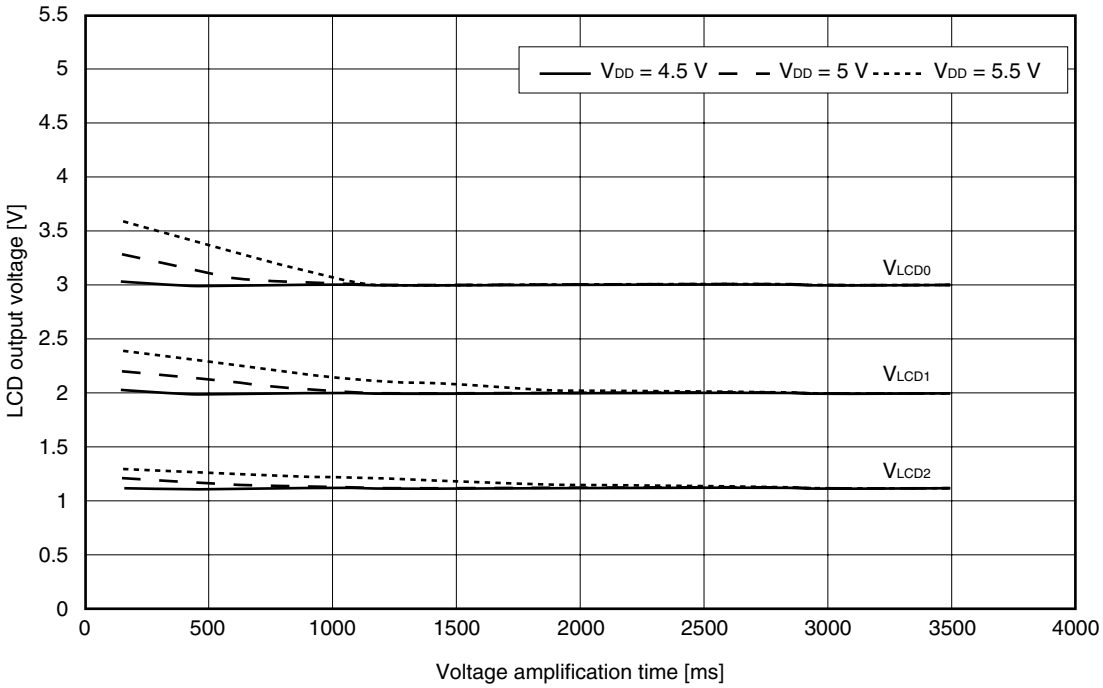
Note The port current (including the current that flows to the on-chip pull-up resistors) is not included.

8. CHARACTERISTICS CURVES OF LCD CONTROLLER/DRIVER (REFRENCE VALUES)

(1) Characteristics curves of voltage amplification stabilization time

The following shows the characteristics curves of the time from the start of voltage amplification (VAON0 = 1) and the changes in the LCD output voltage (when GAIN is set as 1 (using the 3 V display panel)).

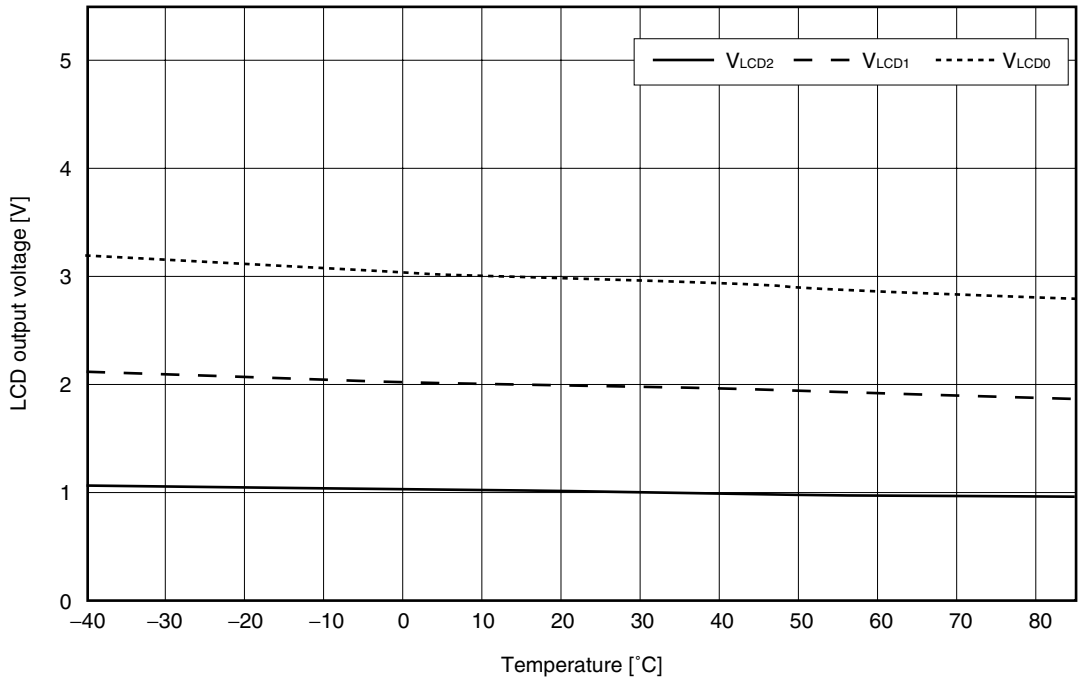
LCD output voltage/Voltage amplification time



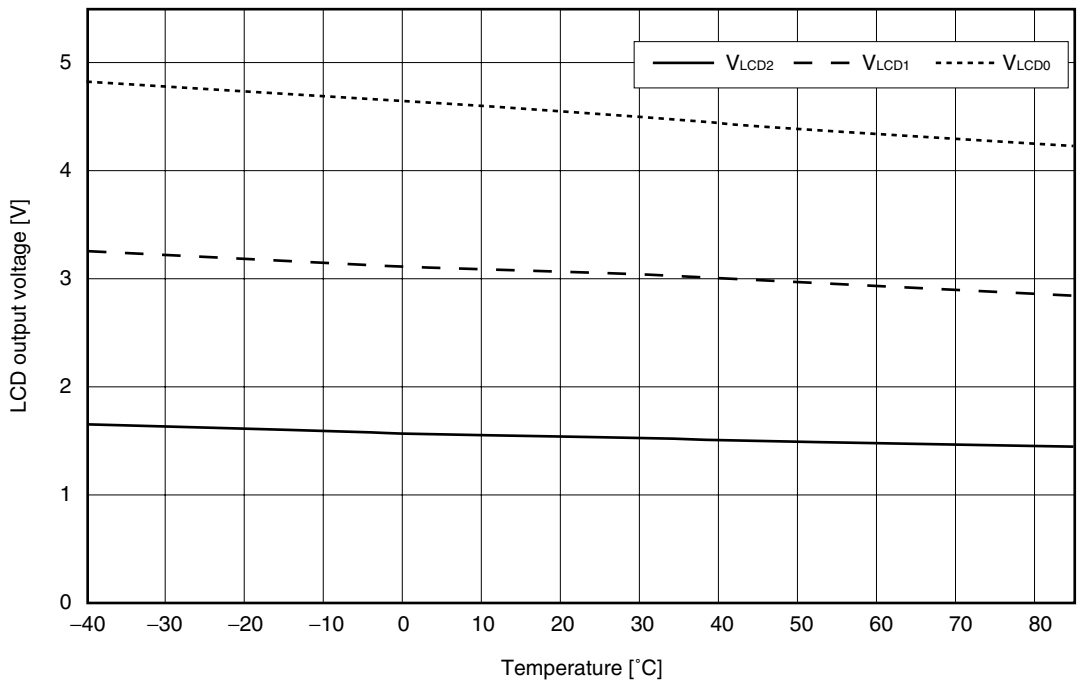
(2) Temperature characteristics of LCD output voltage

The following shows the temperature characteristics curves of LCD output voltage.

LCD output voltage/ Temperature (When GAIN = 1)

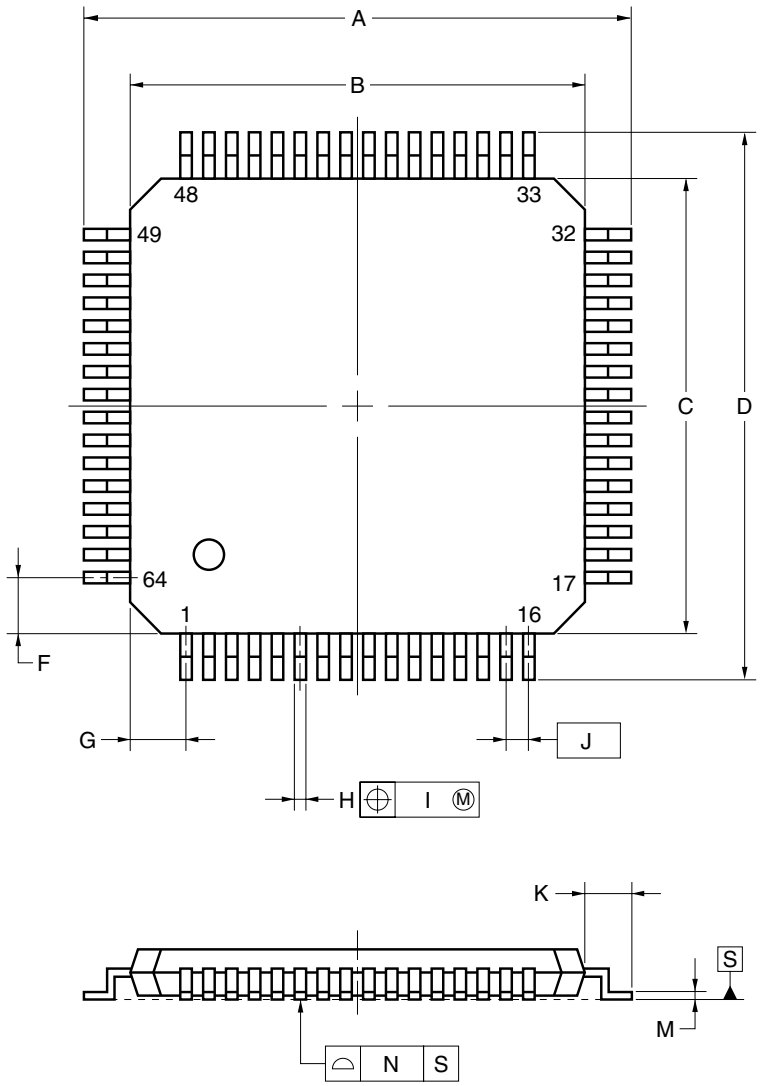


LCD output voltage/ Temperature (When GAIN = 0)

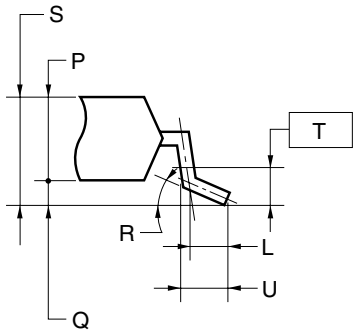


9. PACKAGE DRAWINGS

64-PIN PLASTIC TQFP (12x12)



detail of lead end



ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-3

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9436 and 78F9456 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F9436-9ET: 64-pin plastic TQFP (12 × 12)
μPD78F9456-9ET: 64-pin plastic TQFP (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Interface reflow	Package peak temperature: 235°C, Time:30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time:40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry peak, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN μPD78F9436, 78F9456 AND MASK ROM VERSIONS

The μPD78F9436 and 78F9456 have flash memory in place of the internal ROM of the mask ROM versions. Differences between the μPD78F9436 and 78F9456 and the mask ROM versions are shown in Table A-1.

Table A-1. Differences Between μPD78F9436, 78F9456 and Mask ROM Versions

Item \ Part Number		Flash Memory Versions		Mask ROM Versions			
		μPD78F9436	μPD78F9456	μPD789435	μPD789436	μPD789455	μPD789456
Internal memory	ROM	16 KB		12 KB	16 KB	12 KB	16 KB
	High-speed RAM	512 bytes					
	LCD display RAM	5 × 4 bits	15 × 4 bits	5 × 4 bits		15 × 4 bits	
IC pin		Not available		Available			
V_{PP} pin		Available		Not available			
Pull-up resistors		30 (software control: 30)	20 (software control: 20)	34 (software control: 30, mask option: 4)		24 (software control: 20, mask option: 4)	
Electrical specifications		Refer to the relevant data sheet.					

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9436 and 78F9456.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789456[Notes 1, 2, 3,]	Device file for μPD789426, 789436, 789446, 789456 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64GK-9ET[Note 4]	Flash memory writing adapter for 64-pin plastic TQFP (GK-9ET type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	This is an in-circuit emulator for debugging the hardware and software of an application system using the 78K/0S Series. It supports the integrated debugger (ID78K0S-NS). It is used with an AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator	This is a board to expand the functions of the IE-78K0S-NS. The addition of this board enhances debugging functions such as the coverage, tracer, and timer functions.
IE-70000-MC-PS-B AC adapter	This is the adapter for supplying power from an AC-100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	This adapter is needed when a PC-9800 series PC (except notebook type) is used as the host machine for an IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	This PC card and interface cable are needed when a PC-9800 series notebook-type PC is used as the host machine for an IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C Interface adapter	This adapter is needed when an IBM PC/AT™ or compatible PC is used as the host machine for an IE-78K0S-NS (supports ISA bus).
IE-70000-PCI-IF-A Interface adapter	This adapter is needed when a PC that includes a PCI bus is used as the host machine for an IE-78K0S-NS.
IE-789436-NS-EM1 Emulation board	This is an emulation board for emulating the peripheral hardware inherent to μPD789426, 789436 Subseries devices. It is used with an in-circuit emulator.
IE-789456-NS-EM1 Emulation board	This is an emulation board for emulating the peripheral hardware inherent to μPD789446, 789456 Subseries devices. It is used with an in-circuit emulator.
NP-64GK[Note 4] Emulator probe	This is a cable that is used to connect an in-circuit emulator to the target system. It is for a 64-pin plastic TQFP (GK-9ET type).
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789456[Notes 1, 2]	Device file for μPD789426, 789436, 789446, 789456 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on PC-9800 Series (Japanese Windows™)

2. Based on IBM PC/AT compatibles (Japanese/English Windows)

3. Based on HP9000 Series 700™ (HP-UX™), or SPARCstation™ (SunOS™, Solaris™)

4. This product is manufactured by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789456.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to devices

Document Name	Document No.
μPD789425, 789426, 789435, 789436, 789445, 789446, 789455, 789456 Data Sheet	U14493E
μPD78F9436, 78F9456 Data Sheet	This document
μPD789426, 789436, 789446, 789456 Subseries User's Manual	U15075E
78K/0S Series User's Manual Instructions	U11047E
78K/0, 78K/0S Series Application Note Flash Memory Write	U14458E

Documents related to development tools (user's manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0, System Simulator Ver.2.10 or later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver.2.20 or later Windows Based	Operation	U14910E
IE-78K0S-NS In-circuit Emulator		U13549E
IE-789436-NS-EM1 Emulation Board		To be prepared
IE-789456-NS-EM1 Emulation Board		To be prepared
PG-FP3 Flash Memory Programmer		U13502E

Documents related to embedded software (user's manuals)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Other documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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