

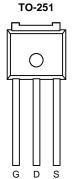
# CED630N-VB Datasheet N-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
200	0.270 at V <sub>GS</sub> = 10 V	8			

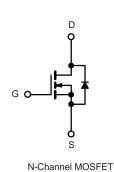
#### **FEATURES**

- Trench Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC





Top View



#### **APPLICATIONS**

· Primary Side Switch

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	200			
Gate-Source Voltage	$V_{GS}$	± 20	V			
Continuous Drain Current (T <sub>.I</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	8			
Continuous Drain Current (1 <sub>J</sub> = 175 °C) <sup>2</sup>	T <sub>C</sub> = 125 °C		5			
Pulsed Drain Current	I <sub>DM</sub>	25	Α			
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	5				
Avalanche Current	I <sub>AS</sub>	5				
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	18	mJ		
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	Pn	96 <sup>b</sup>	W		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	'D	3 <sup>a</sup>			
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
lunation to Ambiant	t ≤ 10 s	R <sub>thJA</sub>	15	18	°C/W		
Junction-to-Ambient <sup>a</sup>	Steady State		40	50			
Junction-to-Case (Drain)	•	R <sub>thJC</sub>	0.85	1.1			

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.



Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200				
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	_ V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μA	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	40			Α	
		$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.270			
- 1 - 1 - 1 - h	D	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 125 °C		0.300			
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 175 °C		0.320		Ω	
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 3 A		0.310		1	
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3 A		35		S	
Dynamic <sup>a</sup>							
Input Capacitance	C <sub>iss</sub>			800		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, F = 1 \text{ MHz}$		100			
Reverse Transfer Capacitance	C <sub>rss</sub>			50			
Total Gate Charge <sup>c</sup>	$Q_g$			34	51		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		8		nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			12			
Gate Resistance	R <sub>g</sub>		0.5		2.9	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_{L} = 5.2 \Omega$		50	75		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		30	45	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>			60	90		
Source-Drain Diode Ratings and Char	acteristics (7	<sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				5	Α	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0 V		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3 A, dI/dt = 100 A/µs		180	250	ns	

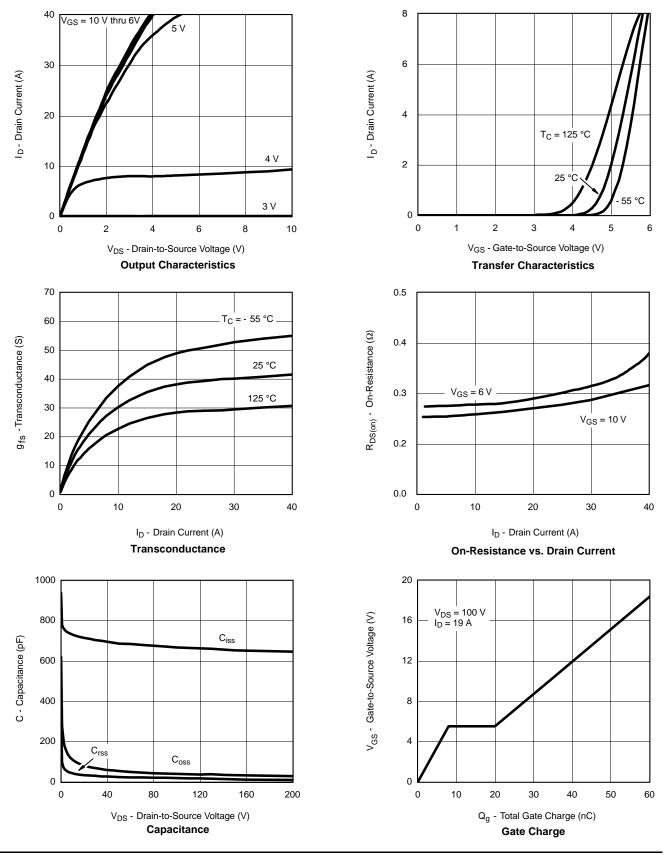
#### Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

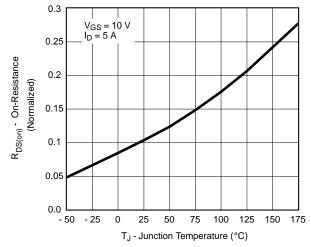


### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

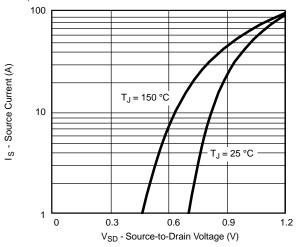




### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature

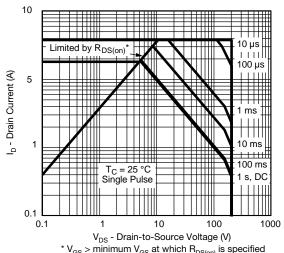


Source-Drain Diode Forward Voltage

#### THERMAL RATINGS

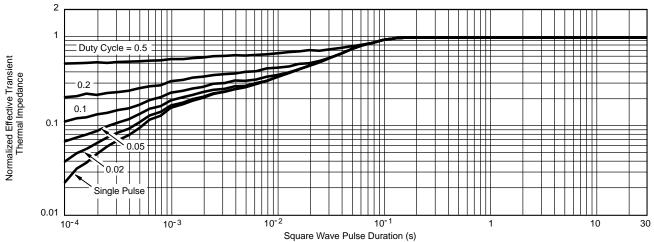


Maximum Avalanche Drain Current vs. Case Temperature



\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

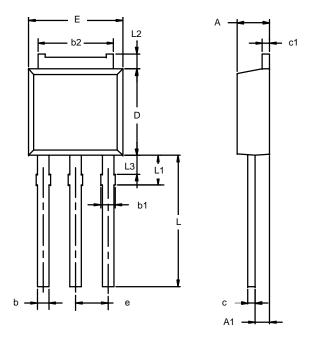
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



### **TO-251AA**



Note: Dimension L3 is for reference only.

	MILLIM	IETERS	INC	HES	
Dim	Min	Max	Min	Max	
Α	2.21	2.38	0.087	0.094	
A1	0.89	1.14	0.035	0.045	
b	0.71	0.89	0.028	0.035	
b1	0.76	1.14	0.030	0.045	
b2	5.23	5.43	0.206	0.214	
С	0.46	0.58	0.018	0.023	
с1	0.46	0.58	0.018	0.023	
D	5.97	6.22	0.235	0.245	
E	6.48	6.73	0.255	0.265	
е	2.28	BSC	0.090 BSC		
L	3.89	9.53	0.153	0.375	
L1	1.91	2.28	0.075	0.090	
L2	0.89	1.27	0.035	0.050	
L3	1.15	1.52	0.045	0.060	
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346					



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