MegaChips

KL5BPLC250WMP

Multi-Hop Powerline

Networking IC

Databrief

Rev. 0.0.5

1 Product overview

1.1 Function Overview

MegaChips KL5BPLC250WMP is a state-of-the-art single-chip broadband over power line (BPL) solution based on IEEE 1901 standard (HD-PLC). It delivers bi-directional, IP based, high-speed communication over AC/DC power lines, COAX and twisted pair wiring where wider bandwidths, robustness, long-range, support for larger number of nodes, and highly secure network is required.

The KL5BPLC250WMP combines the physical (PHY) and media access control (MAC) layers using a 32-bit ARM microcontroller, and a fully integrated Analog-Front-End (AFE) with high precision A/D, D/A data converters and programmable gain amplifiers (PGA) in a single compact package to reduce cost, size and complexity.

The KL5BPLC250WMP uses a high-performance wavelet conversion OFDM modulation and advanced forward error correction (FEC) schemes to enable robust data communication using the existing electrical lines. With 432 sub-carriers in the 2 MHz - 28 MHz operating frequency band, the KL5BPLC250WMP provides a maximum PHY rate of 240Mbps. A channel estimation technique is used to determine the optimal data rate according to the power line channel characteristics with the multi-level modulation for each sub-carrier. Optional sub-carrier masking function is adapted to meet individual country's regulations. Security is provided using an AES-128 encryption/decryption security and authentication engine.

The KL5BPLC250WMP uses ITU-T G.9905, Centralized Matrix based Source Routing (CMSR) mechanism designed specifically to improve robustness, extended range, and wider coverage, while putting minimum load on the network. The multi-hop functionality extends the communication range up to 10 times. In addition, it uses a 128-bit AES encryption engine for the highest security at every node meeting today's Internet-of-Things (IoT) requirements.

Key Features

- Support multi-hop system up to 1024 nodes
- HD-PLC/Ethernet bridge functionality
- Supports IPv4/IPv6 internet protocol
- Lowest power in the industry
- On-chip PLL multiplier and synthesizer provides a single clock source
- Network construction and optimization
- Advanced network diagnostics and management
- HD-PLC network bridge function compatible with Ethernet address system.
- Ethernet⇔Ethernet, RS485⇔RS485 bridge function
- Industrial operating temperature (-40°C to +85°C)
- Package TQFP-144 pins

1.2 Block Diagram

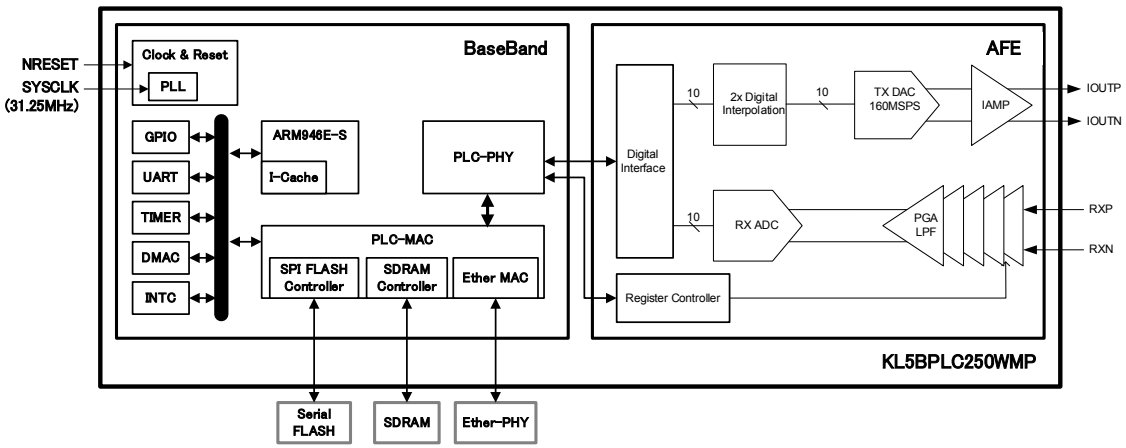

Figure 1 Block Diagram of KL5BPLC250WMP

2 Pins

2.1 Pin Assignments

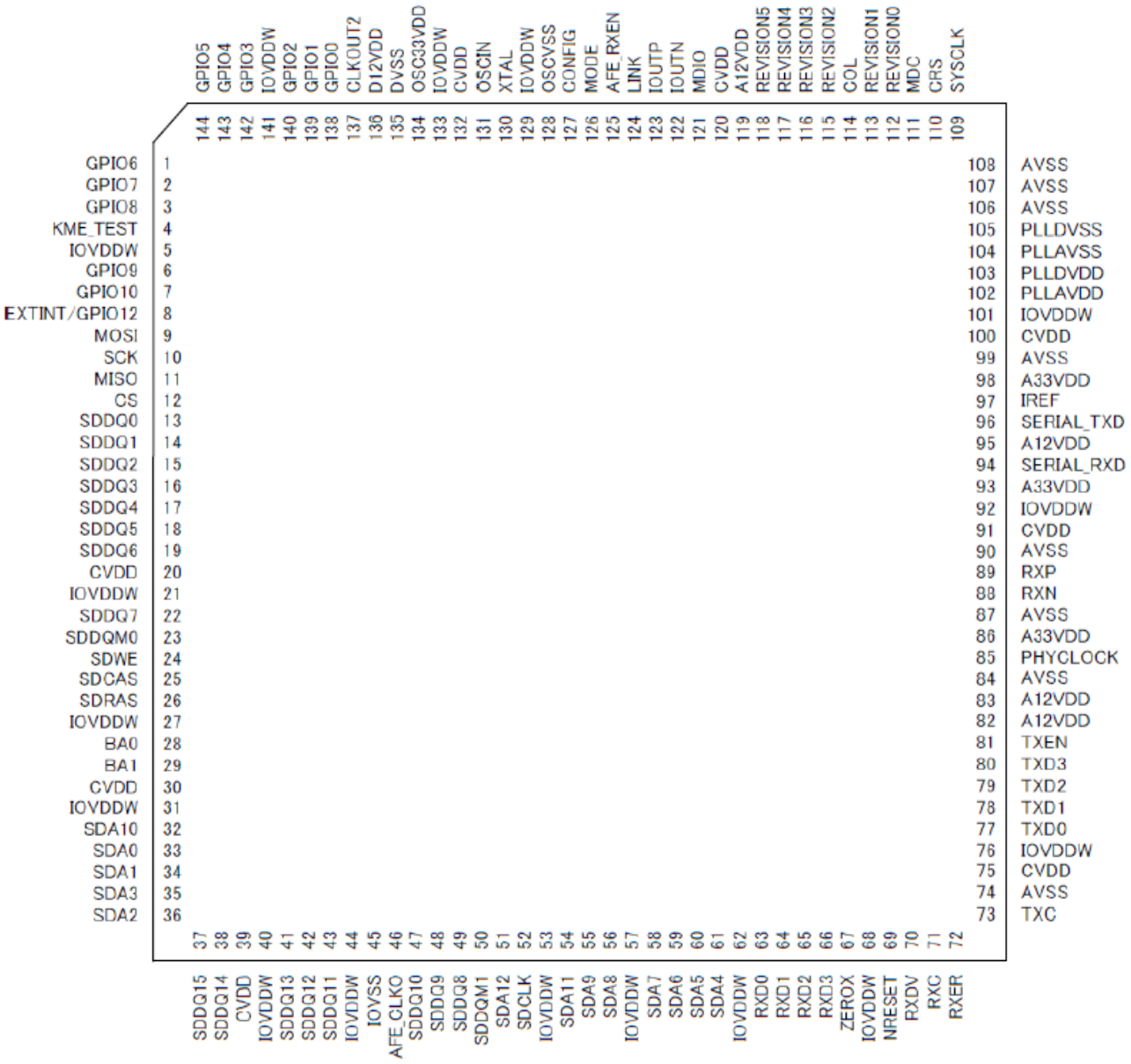

Figure 2 Pin Assignment

3 Operating Conditions

3.1 Absolute Maximum Ratings

Table- 1 shows absolute maximum ratings.

Table- 1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
External supply IO voltage	V_{IOVDDW}	-0.3 to 4.0	V
External supply Analog voltage	V_{A33VDD}	-0.3 to 4.0	V
External supply Analog voltage	$V_{OSC33VDD}$	-0.3 to 4.0	V
Internal supply voltage for BaseBand	V_{CVDD}	-0.3 to 1.32	V
Internal supply voltage for AFE (Analog Part)	V_{A12VDD}	-0.3 to 1.6	V
Internal supply voltage for AFE (Digital Part)	V_{D12VDD}	-0.3 to 1.6	V
Input pin voltage	V_I	-0.3 to V_{IOVDDW} +0.3	V
Analog Input/Output Voltage RXP,RXN,IREF IOUTP, IOUTN OSCIN, XTAL	 V_{A1} V_{A2} V_{A3}	 -0.3 to V_{A33VDD} +0.3 -0.3 to 6.0 -0.3 to $V_{OSC33VDD}$ +0.3	 V V V
Output current (2mA)	I_O	-5.2/+15.9	mA
Output current (4mA)	I_O	-10.6/+31.7	mA
Output current (8mA)	I_O	-21.2/+63.4	mA
Power dissipation	P_D	700	mW
Storage temperature	T_{stg}	-55 to 125	°C

Note:

- *The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.*
- *Directly connect all VDD pins to external power supplies and ground all VSS pins.*
- *Ensure that the junction temperature (Tj) is 125°C or less during use.*

3.2 Recommended Operating Conditions

Table- 2 shows recommended operating conditions.

Table- 2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External supply voltage	V_{IOVDDW} V_{A33VDD} $V_{OSC33VDD}$	---	3.1	3.3	3.5	V
Internal supply voltage	V_{CVDD} V_{A12VDD} V_{D12VDD}	---	1.1	1.2	1.3	V
Operating package surface temperature	T_C	Tj = 125°C	-40	---	85	°C

4 BaseBand Part

4.1 Block Diagram

Figure- 2 provides a block diagram for the KL5BPLC250WMP BaseBand part.

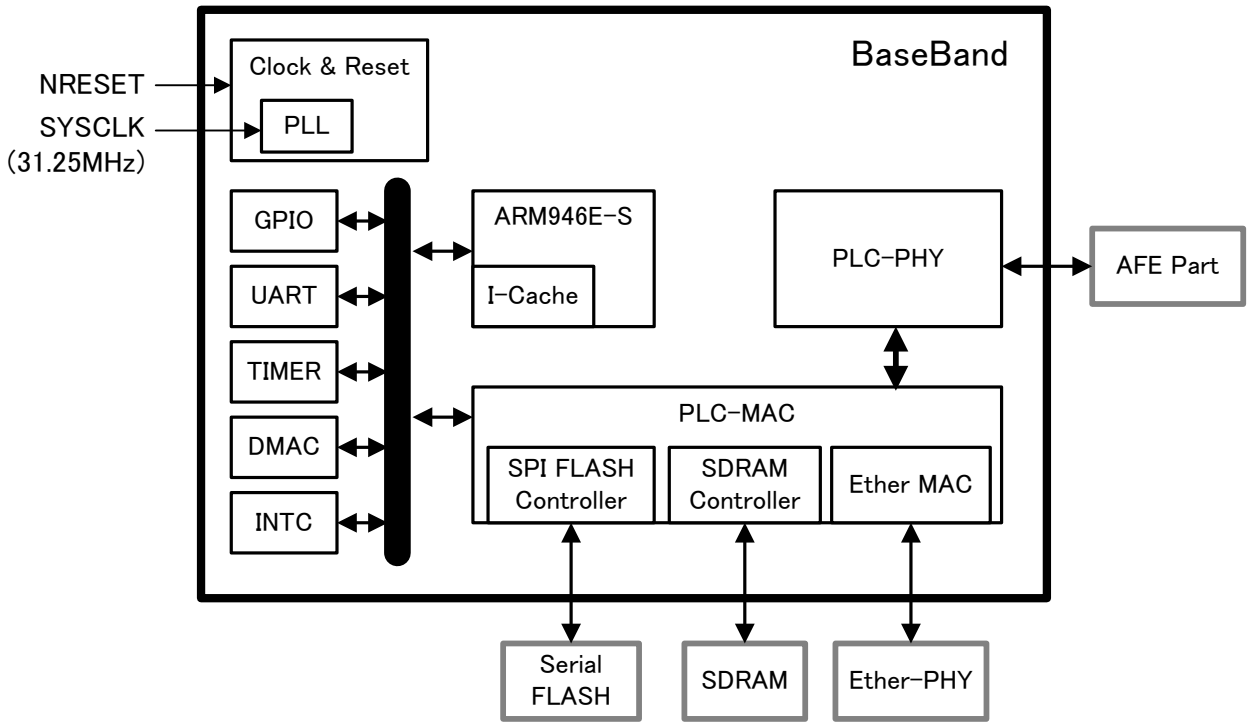

Figure 3 KL5BPLC250WMP Block Diagram

4.2 List of Functions

4.2.1 Microcontroller and Peripherals

- CPU — ARM946E-S with 16 Kbyte Instruction Cache
- System Clock — 125MHz
- Interrupt Controller
- 16bit Timer — 8Channels
- Serial Communication Controller — 1Channel
- GPIO
- DMAC
- Debug Function — Embedded ICE

4.2.2 PLC-PHY Function

- Frequency bandwidth — 2 MHz to 28 MHz
- Transmission scheme — Wavelet OFDM
- Sampling frequency — 62.5 MHz
- Sub carrier — 360 carriers (without notch filter: 432 carriers) including flexible notch function
- Primary modulation scheme — 32-PAM to 2-PAM
- Transmission speed — 240Mbps
- Error correction schemes — LDPC-CC, Reed-Solomon encoding and decoding / convolutional encoding +Viterbi decoding

4.2.3 PLC-MAC Processing Function

- Multiple access control method — CSMA/CA
- Data encryption functionality — 128bit AES
- Channel estimation control functionality
- Integrated IEEE 802.3 compliant MAC
- Integrated SDRAM controller

4.2.4 SPI FLASH Interface Function

- SPI (Serial Peripheral Interface) — Flash memory control functionality
- Clock frequency — 50MHz
- Boot RAM — 4Kbyte integrated boot RAM

4.2.5 SDRAM Interface Functions

- Clock frequency — 125MHz
- Data bus width — 16-bit
- Support Capacity — 16MByte/32MByte
- Row Address — 12-bit(16MByte Device)/13-bit(32MByte Device)
- Column Address — 8-bit/9-bit(16MByte, 32MByte Device)

  (8MBytes device is unsupported)

4.2.6 Ethernet PHY Interface Functions

- Supported interface — MII/RMII/Turbo-MII
- Clock frequency — 25MHz(MII)/50MHz(RMII, Turbo-MII)

4.2.7 Clock and Reset Control Functions

- Clock generation — 25MHz / 31.25MHz / 50MHz / 62.5MHz / 125MHz / 250MHz
- Reset control functionality
- Low-power mode control functionality — Link signal monitoring function

4.3 Example System Architectures

This section illustrates example normal mode and ICE mode system architectures for the KL5BPLC250WMP. For more information about these modes, see Section **Error! Reference source not found. Error! Reference source not found.**.

4.3.1 Normal Mode

Figure- 3 illustrates an example of normal mode system architecture.

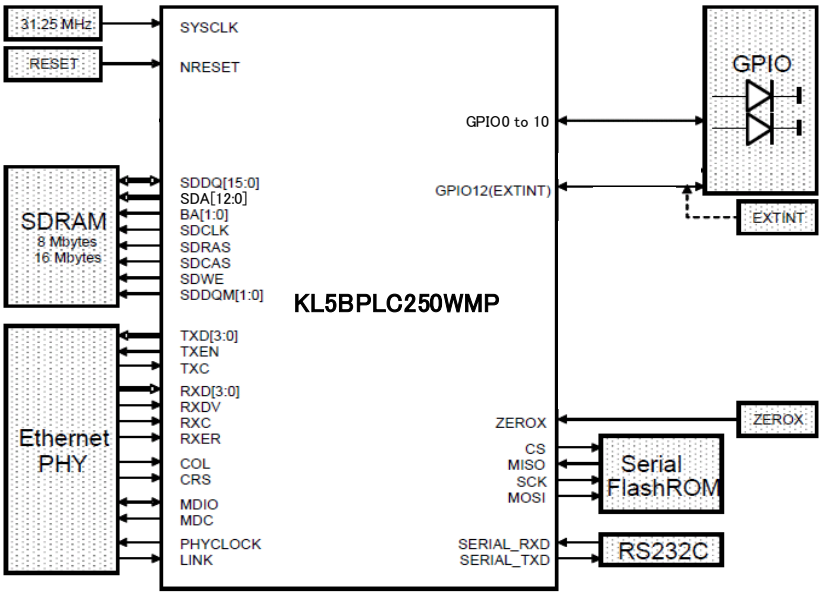

Figure 4 Normal Mode Connection Diagram

4.3.2

4.4 Electrical Characteristics

Table- 3 show electrical characteristics.

Table- 3 Electrical characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	---	2.0	---	5.5	V
Input low voltage	V_{IL}	---	-0.3	---	0.8	V
Input threshold voltage	V_T	---	1.30	1.40	1.50	V
Schmitt Trigger Input threshold voltage	V_{T+}	Low to High	1.56	1.68	1.77	V
	V_{T-}	High to Low	1.14	1.23	1.33	V
Input leakage current	I_{LI}	$V_I = V_{IOVDDW}$ or V_{SS}	---	---	±10	µA
Pull-up resistor	R_{IH}	$V_I = V_{SS}$	26	38	59	kΩ
Pull-down resistor	R_{IL}	$VI = V_{IOVDDW}$ or V_{SS}	33	47	81	kΩ
Output high voltage	V_{OH}	---	2.4	---	---	V
Output low voltage	V_{OL}	---	---	---	0.4	V
Output leakage current	O_{LI}	$V_I = V_{IOVDDW}$ or V_{SS} $V_O = V_{IOVDDW}$ or V_{SS}	---	---	±10	µA

Conditions: V_{IOVDDW} = 3.3 V ± 0.3 V, V_{CVDD} = 1.2 V ± 0.12 V, -40°C < Tj < 125°C

5 Analog Front-End(AFE) Part

5.1 General Description

The KL5BPLC250WMP has highly integrated analog front-end part for PLC. Data rate is supported up to 80 MSPS and 160 MSPS in Rx path and Tx path, respectively. Interfacing can be either binary or twos compliment, LSB or MSB first. A serial peripheral interface (SPI) allows software programmability of the front-end. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.

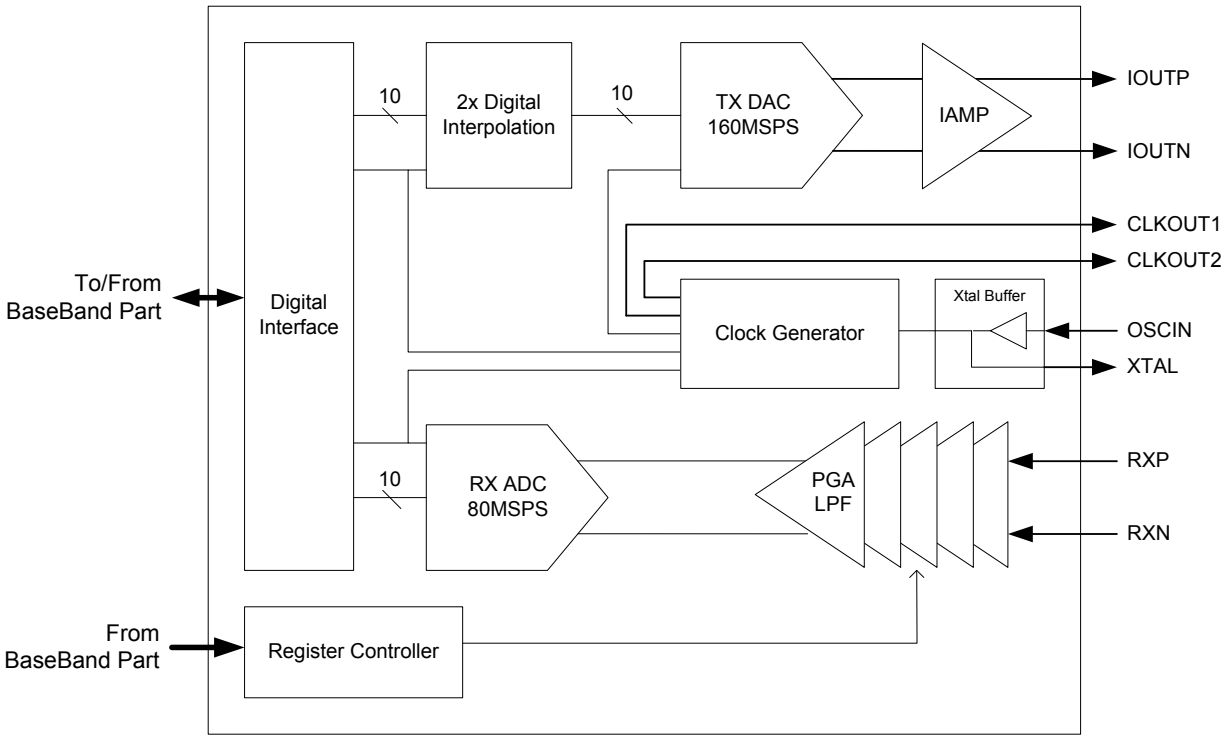

Figure 5 AFE Functional Block Diagram.

5.2.1 Power Supply Specifications

Table- 4 Power Supply Specifications

Parameter	Temp	Min	Typ	Max	Unit
SUPPLY VOLTAGES					
A12VDD, D12VDD	Full	1.1	1.2	1.3	V
A33VDD , IOVDDW, OSC33VDD	Full	3.1	3.3	3.5	V
POWER CONSUMPTION (HALF-DUPLEX) (f_{DATA} = 80 MSPS)					
Tx Mode					
I_{A12VDD} + I_{D12VDD} (1.2V Supply Current)	25°C		39		mA
I_{A33VDD} + $I_{IO33VDD}$ + $I_{OSC33VDD}$ (3.3V Supply Current)	25°C		37		mA
Rx Mode					
I_{A12VDD} + I_{D12VDD} (1.2V Supply Current)	25°C		70		mA
I_{A33VDD} + $I_{IO33VDD}$ + $I_{OSC33VDD}$ (3.3V Supply Current)	25°C		57		mA
POWER CONSUMPTION OF FUNCTIONAL BLOCKS (f_{DATA} = 80 MSPS)					
RxPGA (3.3V)	25°C		35		mA
ADC (1.2V)	25°C		39		mA
TxDAC (3.3V)	25°C		4		mA
IAMP + 28 mA output (3.3V)	25°C		30		mA
Reference (1.2V)	25°C		1		mA
CLK PLL, Synthesizer and 1.2V Logic(Rx)	25°C		30		mA
MAXIMUM ALLOWABLE POWER DISSIPATION	Full			490	mW
STANDBY POWER CONSUMPTION					
I_{VDD_TOT} (Total Supply Current)	Full		10		mA
POWER DOWN DELAY (USING PWD PIN)					
RxPGA	25°C		100		ns
ADC	25°C		20		ns
TxDAC	25°C		20		ns
IAMP	25°C		20		ns
CLK PLL and Synthesizer	25°C		20		ns
POWER UP DELAY (USING PWD PIN)					
RxPGA	25°C		7		µs
ADC	25°C		5.5		µs
TxDAC	25°C		9	13	µs
IAMP	25°C			1	µs
CLK PLL and Synthesizer	25°C			410	µs
WAKE UP TIME (FROM SLEEP)					
RxPGA & ADC	Full			1	µs
DAC & IAMP (95% OUTPUT CURRENT)	Full			1	µs

O33VDD=OSC33VDD=A33VDD=3.3V ±0.2V, D12VDD=A12VDD=1.2V ± 0.1V
UNLESS OTHERWISE NOTED

5.2.2 Digital Interface Specifications

Table- 5 Digital Interface Specifications

Parameter	Temp	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
High Level Input Voltage	Full	2.0			V
Low Level Input Voltage	Full			0.8	V
Input Leakage Current	Full			10	µA
Input Capacitance	Full		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)					
High Level Output Voltage (I_{OH} = 2 mA)	Full	2.4			V
Low Level Output Voltage (I_{OH} = 2 mA)	Full			0.4	V
Output Rise/Fall Time (C_{LOAD} = 16 pF)	Full		2.2/2.2		ns
Output Rise/Fall Time (C_{LOAD} = 5 pF)	Full		1.2/1.1		ns
RESET					
Minimum Low Pulse Width (Relative to f_{ADC})		1			Clock cycles

IO33VDD=OSC33VDD=A33VDD=3.3V ±0.2V, D12VDD=A12VDD=1.2V ± 0.1V
UNLESS OTHERWISE NOTED

6 Package

Figure- 5 shows the package outline of KL5BPLC250WMP (Exposed TQFP-144 pins).

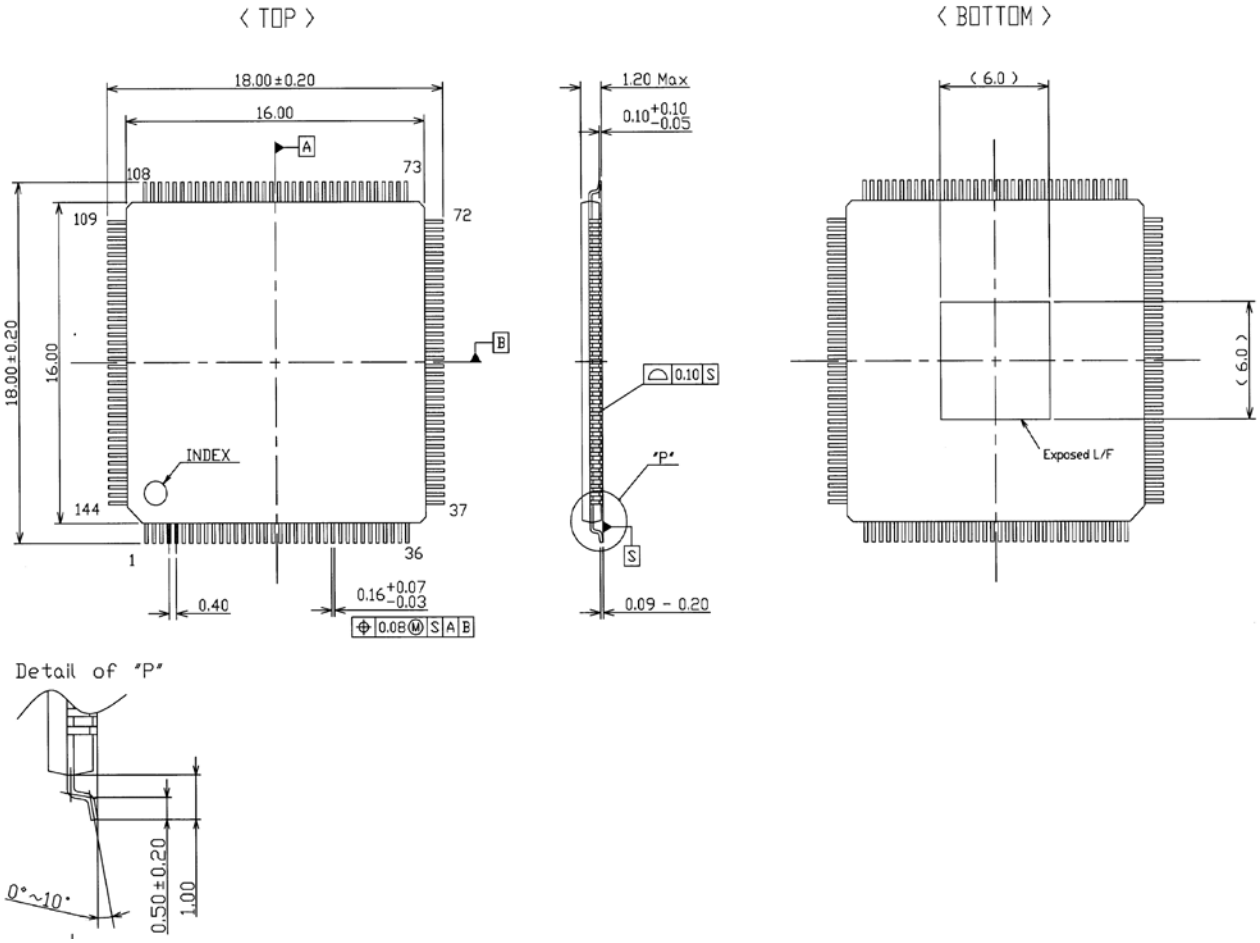

Figure 6 KL5BPLC250WMP package outline (Exposed TQFP-144 pins)

7 Ordering Information

Part Number: KL5BPLC250WMP

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