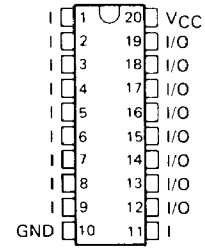
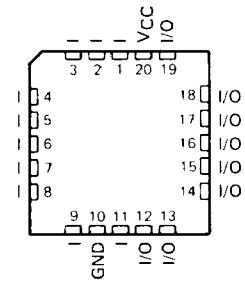
D3086, DECEMBER 1987 - REVISED AUGUST 1988

- **Very-High-Speed Address Decoder (Ideal for Use with High Speed Processors)**
- **I/O Propagation Delay: 6 ns Max**
- **Suitable for High Speed NAND-NAND Logic Implementation**
- **Field Programmable on Standard PLD Programmers**
- **Fully TTL Compatible**
- **Security Fuse Prevents Unauthorized Duplication**
- **Dependable Texas Instruments Quality and Reliability**
- **Potential Applications**
  - **Address Decoders**
  - **Random Logic (NAND-NAND)**
  - **Code Detectors**
  - **Peripheral Selectors**
  - **Fault Monitors**
  - **Machine State Decoders**

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIBPAD18N8-6C is a very-high-speed Programmable Address Decoder featuring 6-ns maximum propagation delay, the highest speed in the TTL programmable logic family. The TIBPAD18N8 uses the IMPACT-X™ process and proven titanium-tungsten fuse technology to provide reliable, high-performance substitutes for conventional TTL logic.

The TIBPAD18N8-6C contains 10 dedicated inputs and 8 product terms, each followed by an inverting buffer. Each of the eight buffers can be individually programmed so that the corresponding pin can function either as an input or output, depending on the state of the fuse controlling the output buffer, as indicated by Table 1. This allows the device to be used for functions requiring up to 17 inputs and a single output or down to 10 inputs and 8 outputs.

A high-speed feedback path, which does not go through the output buffer, is provided to offer higher performance operation in designs where feedback is required. The architectural fuse on the internal multiplexer is used for the selection of this path (see Table 2). This makes the TIBPAD18N8-6C ideal for the implementation of a very fast NAND-NAND logic. The TIBPAD18N8 is supplied with all eight output buffers disabled thus establishing all programmable input/output lines as inputs. If an I/O line is selected to be an output it must be programmed accordingly.

The TIBPAD18N8-6C is characterized for operation from 0°C to 75°C.

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functional block diagram (positive logic)

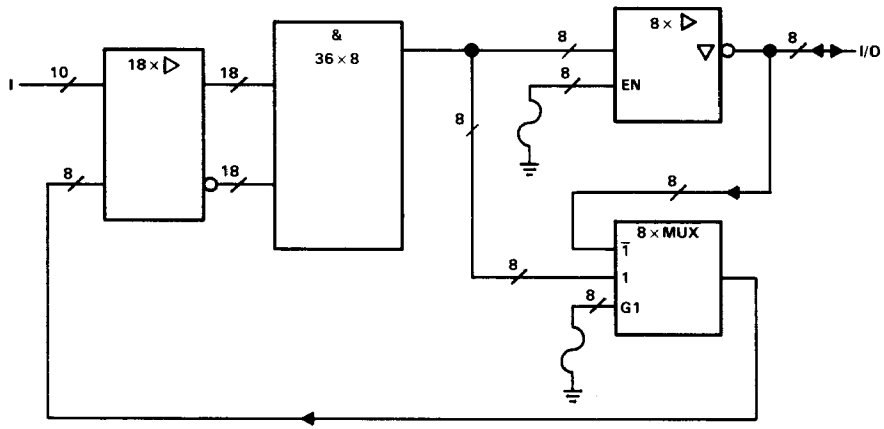

Table 1. Output Buffer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	Input (Output Buffer in 3-State)
Blown	Output

Table 2. I/O Multiplexer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	Output Buffer Feedback
Blown	Fast Feedback (pre-output buffer)

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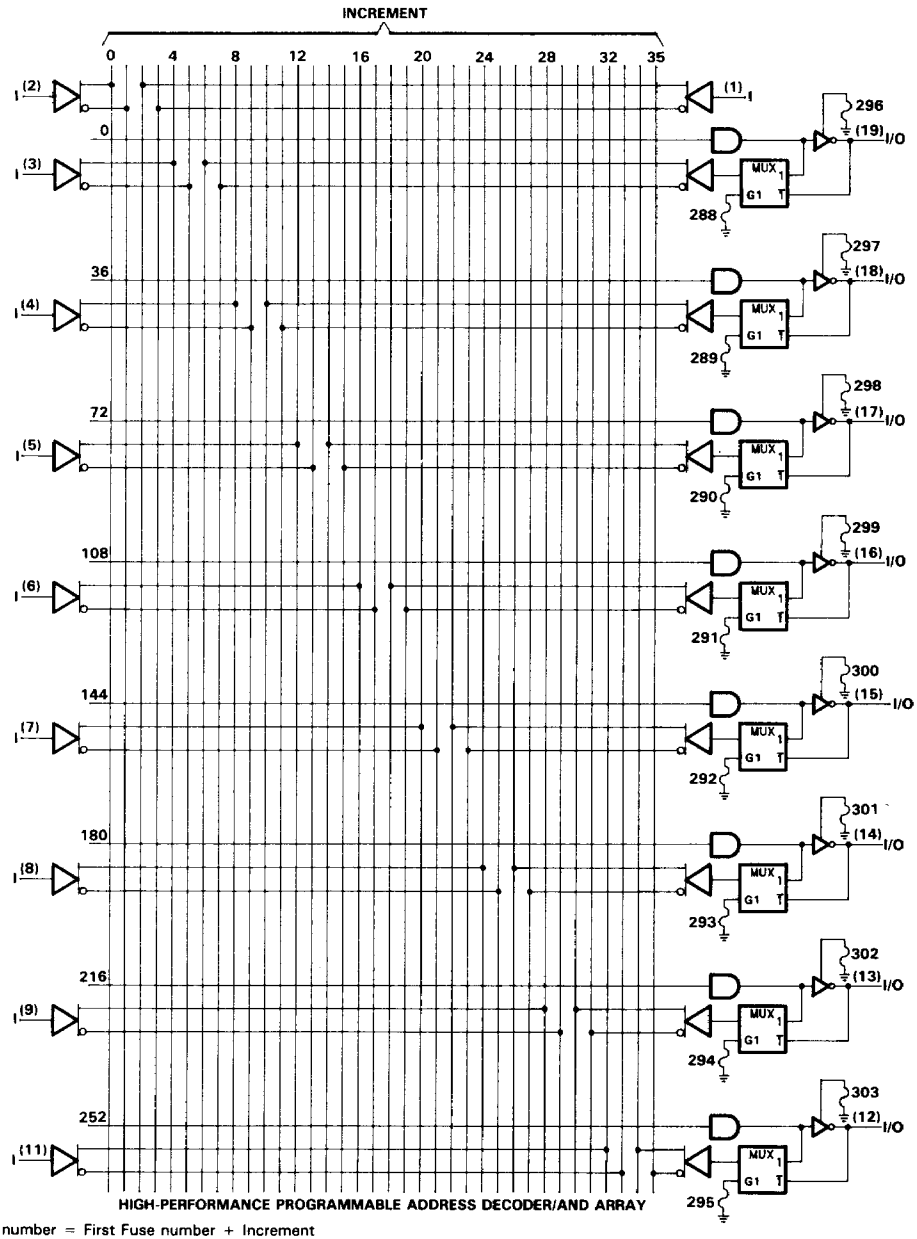
logic diagram (positive logic)



Fuse number = First Fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2			V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 24 mA		0.37	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
I_{OZL}‡	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.25 V, V_I = 5.5 V			20	μA
I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_O§	V_{CC} = 5.25 V, V_O = 0.5 V	−30	−75	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 4.5 V		145	180	mA
C_i	V_I = 2 V		5		pF
C_o	V_O = 2 V		6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	I (2 outputs switching)	O (no feedback)	R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	2	4.5	6	ns
		O (with 1 fast feedback path)		3.5	7	10	ns
		O (with 2 fast feedback paths)		5	9.5	14	ns
		O (with 3 fast feedback paths)		6.5	12	18	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worse case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}.
§ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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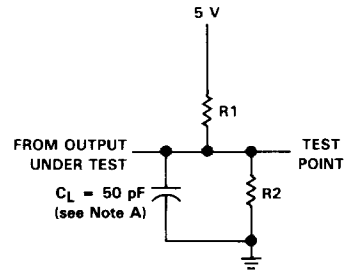
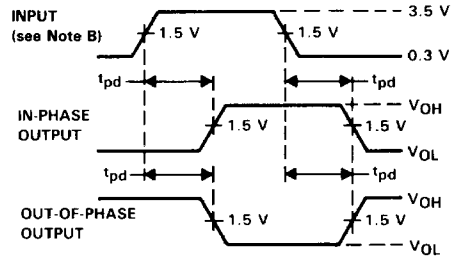
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.

FIGURE 1

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

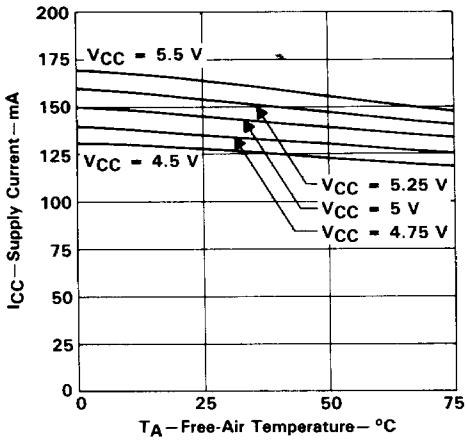


FIGURE 2

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

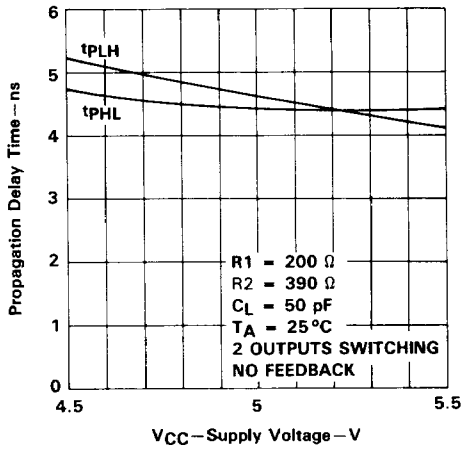


FIGURE 3

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

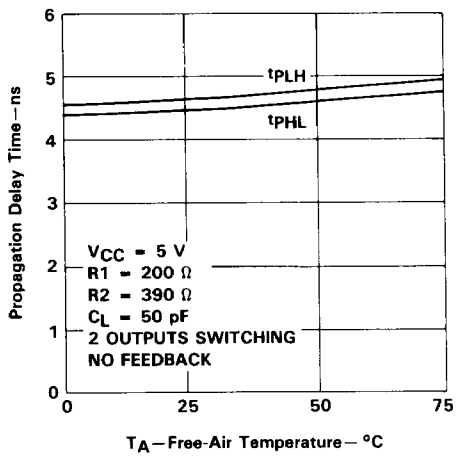


FIGURE 4

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

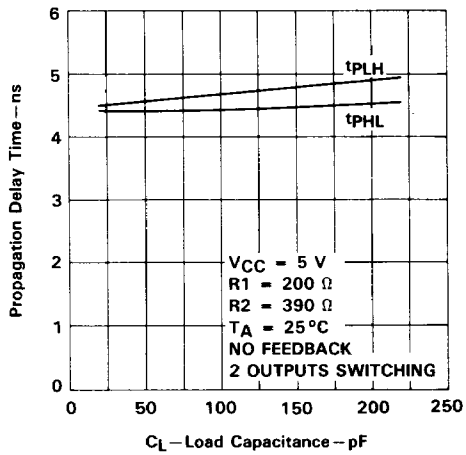


FIGURE 5

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
NUMBER OF FAST FEEDBACK PATHS

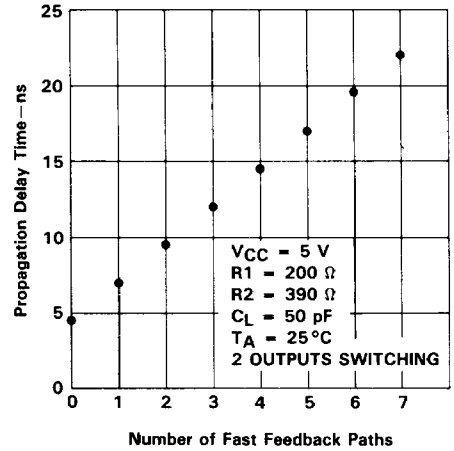

FIGURE 6

WORST-CASE PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

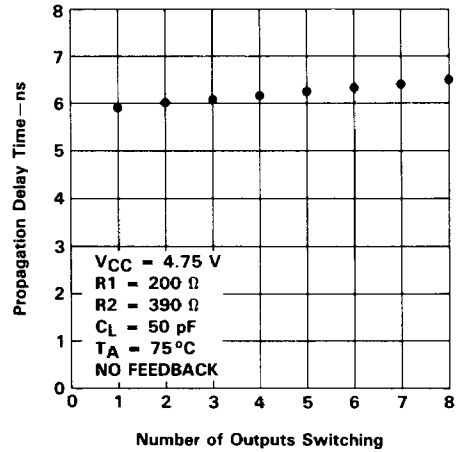

FIGURE 7