

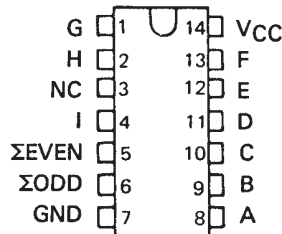
SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

SDLS152 – DECEMBER 1972 – REVISED MARCH 1988

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:
'LS280 . . . 80 mW
'S280 . . . 335 mW

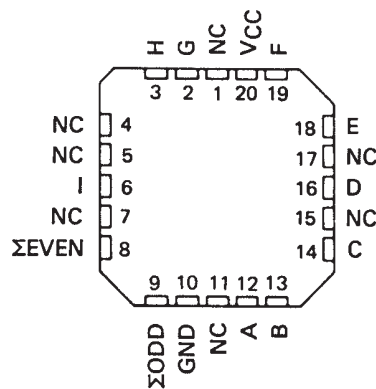
SN54LS280, SN54S280 . . . J OR W PACKAGE
SN74LS280, SN74S280 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS280, SN54S280 . . . FK PACKAGE

(TOP VIEW)



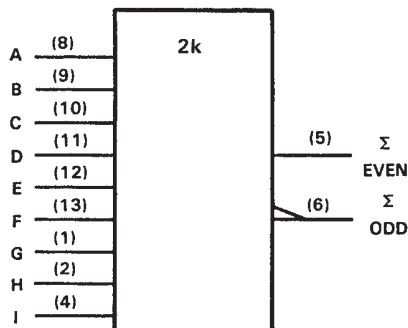
NC - No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

description

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

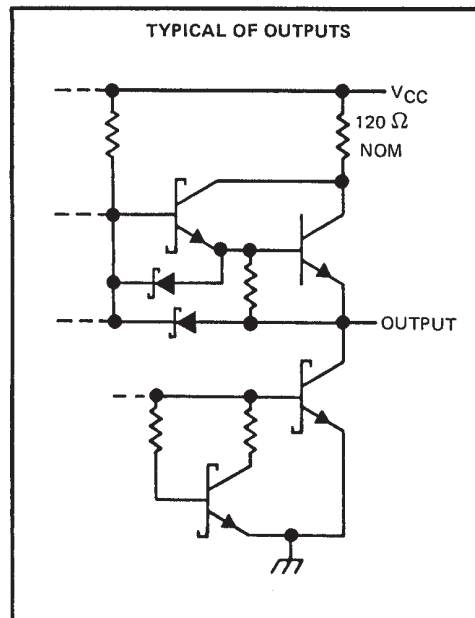
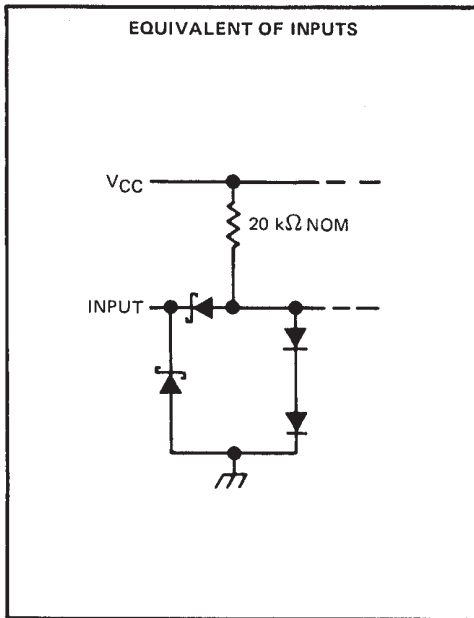
These devices are fully compatible with most other TTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

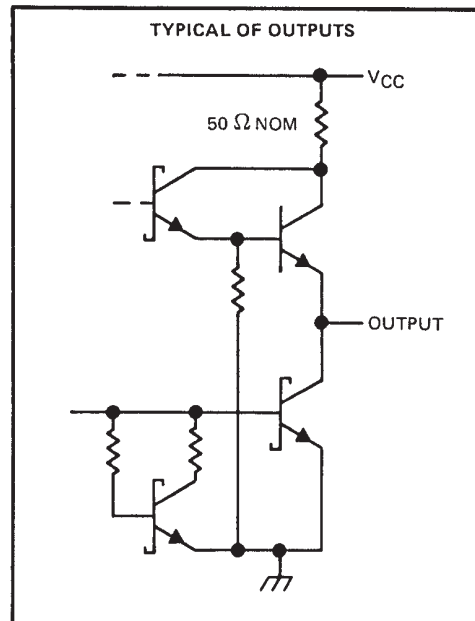
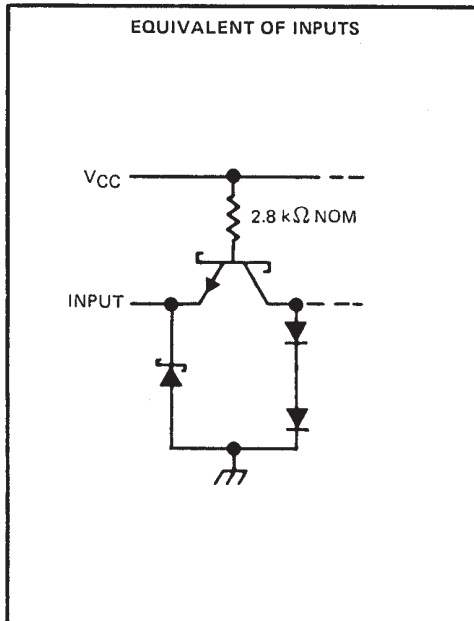
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schematics of inputs and outputs

'LS280



'S280



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: 'LS280	7 V
'S280	5.5 V
Operating free-air temperature range: SN54'	- 55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

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recommended operating conditions

	SN54LS280			SN74LS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LS280		SN74LS280		UNIT		
		MIN	TYP†	MAX	MIN		TYP‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	
		I _{OL} = 8 mA				0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20		20	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA	
I _{OS} §	V _{CC} = MAX	-20		-100	-20	-100	mA	
I _{CC}	V _{CC} = MAX, See Note 2		16	27		16	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Σ Even	C _L = 15 pF, R _L = 2 kΩ, Inputs not under test at 0 V, See Note 3		33	50	ns
t _{PHL}					29	45	
t _{PLH}	Data	Σ Odd			23	35	ns
t _{PHL}					31	50	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

SDLS152 – DECEMBER 1972 – REVISED MARCH 1988

recommended operating conditions

	SN54S280			SN74S280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
V_{IH} High-level input voltage		2			V	
V_{IL} Low-level input voltage				0.8	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S'	2.5	3.4	V	
		SN74S'	2.7	3.4		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$			-40	-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54S280	67	99	mA	
		SN74S280	67	105		
	$V_{CC} = \text{MAX}, T_A = 125^\circ \text{C},$ See Note 2	SN54S280N		94	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 3		14	21	ns
t_{PHL}					11.5	18	
t_{PLH}	Data	Σ Odd			14	21	ns
t_{PHL}					11.5	18	

¶ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

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logic diagram (positive logic)

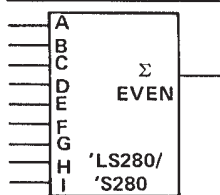
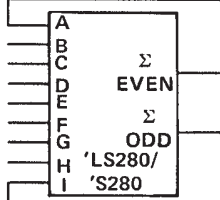


Pin numbers shown are for D, J, N, and W packages.

TYPICAL APPLICATION DATA

25-LINE PARITY/GENERATOR CHECKER

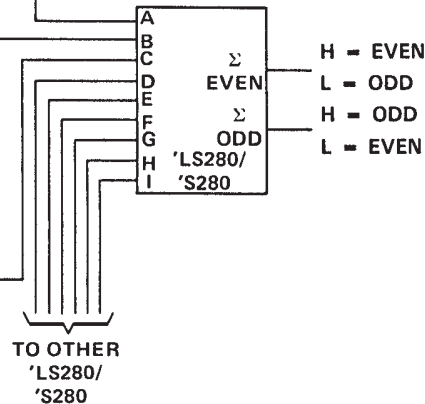
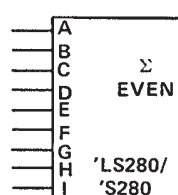
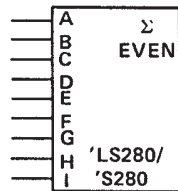
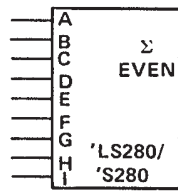
Three 'LS280's or 'S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 75 or 25 nanoseconds respectively.



As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER

Longer word lengths can be implemented by cascading 'LS280's or 'S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 75 or 25 nanoseconds respectively.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/32901B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32901B2A	
JM38510/32901BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BCA	Samples
JM38510/32901BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BCA	Samples
JM38510/32901BDA	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BDA	
JM38510/32901BDA	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BDA	
M38510/32901B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32901B2A	
M38510/32901B2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32901B2A	
M38510/32901BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BCA	Samples
M38510/32901BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BCA	Samples
M38510/32901BDA	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BDA	
M38510/32901BDA	NRND	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32901BDA	
SN54LS280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS280J	Samples
SN54LS280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS280J	Samples
SN54S280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S280J	Samples
SN54S280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S280J	Samples
SN74LS280D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS280	Samples
SN74LS280D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS280	Samples
SN74LS280J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS280J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN74LS280N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS280N	Samples
SN74LS280N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS280N	Samples
SN74LS280N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS280N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS280NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS280	Samples
SN74LS280NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS280	Samples
SN74S280D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74S280D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74S280N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	SN74S280N	
SN74S280N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	SN74S280N	
SN74S280N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74S280N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ54LS280FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS280FK	
SNJ54LS280FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS280FK	
SNJ54LS280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS280J	Samples
SNJ54LS280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS280J	Samples
SNJ54LS280W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS280W	Samples
SNJ54LS280W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS280W	Samples
SNJ54S280FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S280FK	
SNJ54S280FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S280FK	
SNJ54S280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S280J	Samples
SNJ54S280J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S280J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54S280W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S280W	Samples
SNJ54S280W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S280W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS280, SN54S280, SN74LS280, SN74S280 :

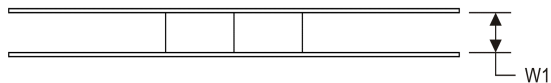
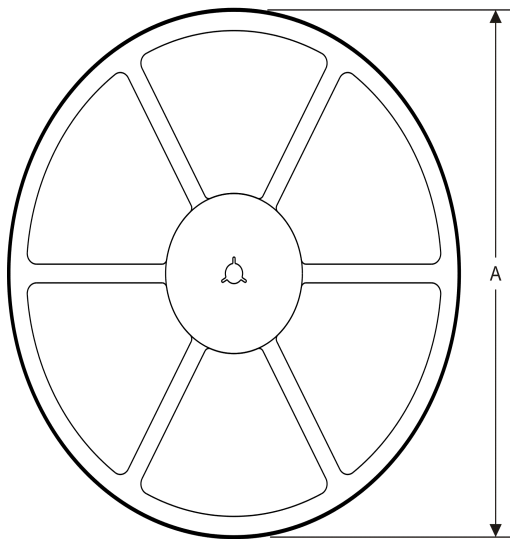
- Catalog: [SN74LS280](#), [SN74S280](#)
- Military: [SN54LS280](#), [SN54S280](#)

NOTE: Qualified Version Definitions:

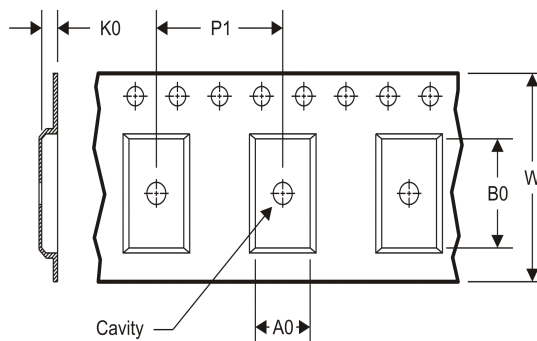
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS280NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS280NSR	SO	NS	14	2000	367.0	367.0	38.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

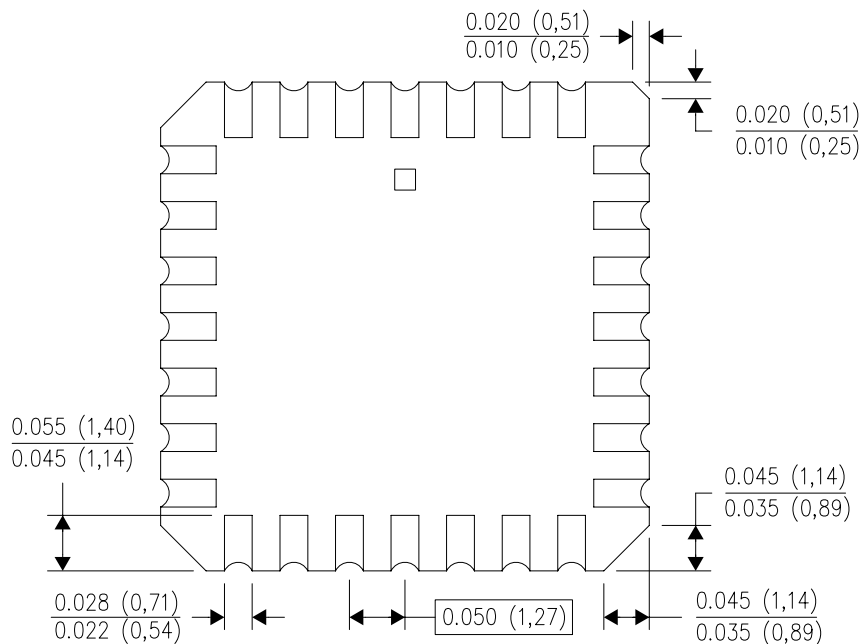
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

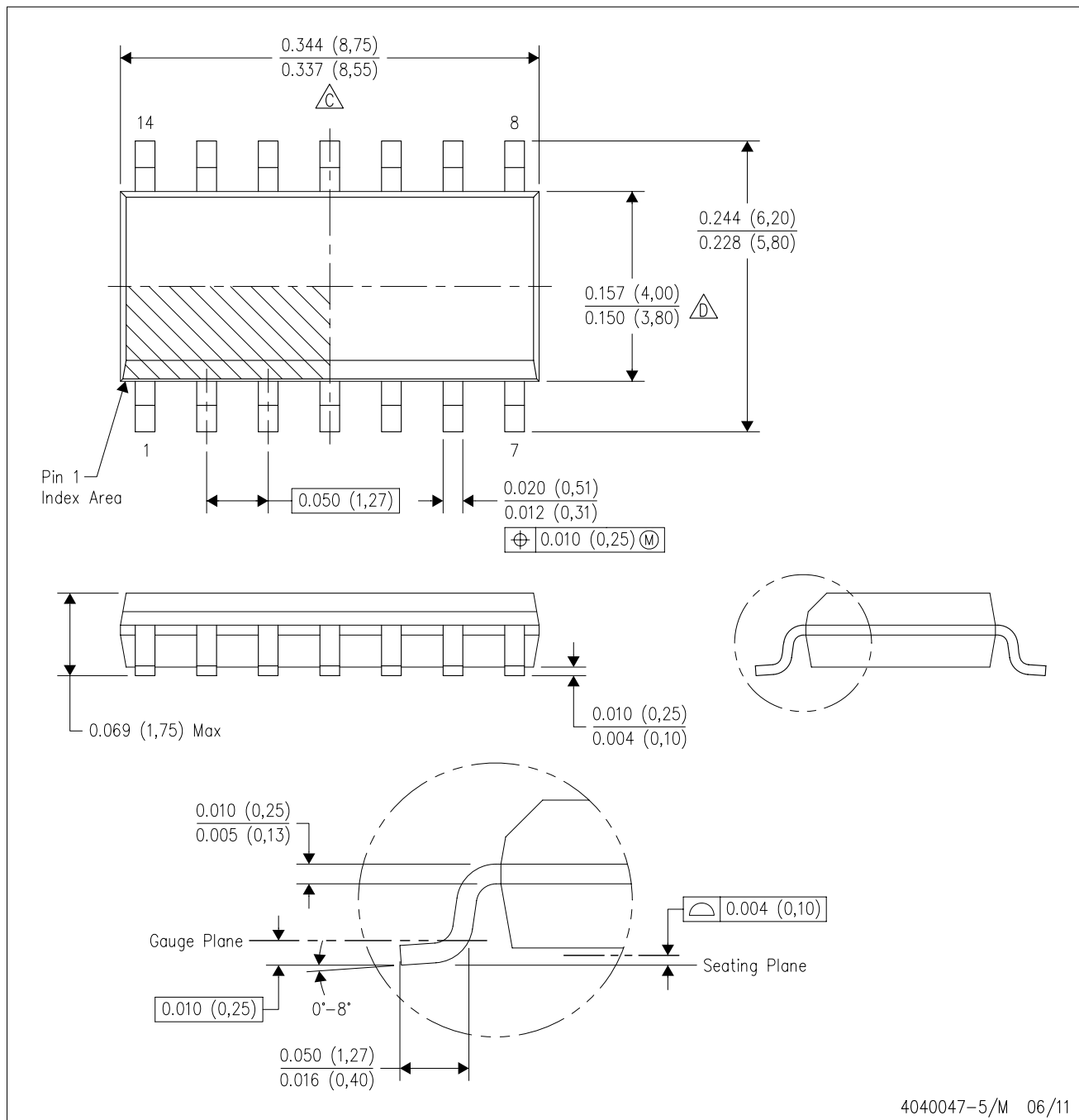
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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